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Design of VCO-based ADCs

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Abstract

Today's complex electronic systems with billions of transistors on a single die are enabled by the aggressive scaling down of the device feature size at an exponential rate as predicted by the Moore's law. Digital circuits benefit from technology scaling to become faster, more energy efficient as well as more area efficient as the feature size is scaled down. Moreover, digital design also benefits from mature CAD tools that simplify the design and cross-technology porting of complex systems, leveraging on a cell-based design methodology. On the other hand, the design of analog circuits is getting increasingly difficult as the feature size scales down into the deep nanometer regime due to a variety of reasons like shrinking voltage headroom, reducing intrinsic gain of the devices, increasing noise coupling between circuit nodes due to shorter distances etc. Furthermore, analog circuits are still largely designed with a full custom design flow that makes their design and porting tedious, slow, and expensive. In this context, it is attractive to consider realizing analog/mixed-signal circuits using standard digital components. This leads to scaling-friendly mixed-signal blocks that can be designed and ported using the existing CAD framework available for digital design. The concept is already being applied to mixed-signal components like frequency synthesizers where all-digital architectures are synthesized using standard cells as basic components. This can be extended to other mixed-signal blocks like digital-to-analog and analog-to-digital converters as well, where the latter is of particular interest in this thesis.

A voltage-controlled oscillator (VCO)-based analog-to-digital converter (ADC) is an attractive architecture to achieve all-digital analog-to-digital conversion due to favorable properties like shaping of the quantization error, inherent anti-alias filtering etc. Here a VCO operates as a signal integrator as well as a quantizer. A converter employing a ring oscillator as the VCO lends itself to an all-digital implementation.

In this dissertation, we explore the design of VCO-based ADCs synthesized using digital standard cells with the long-term goal of achieving high performance data converters built from low accuracy switch components. In a first step, an ADC is designed using vendor supplied standard cells and fabricated in a 65 nm CMOS process. The converter delivers an 8-bit ENOB over a 25 MHz bandwidth while consuming 3.3 mW of power resulting in an energy efficiency of 235 fJ/step (Walden FoM). Then we utilize standard digital CAD tools to synthesize converter designs that are fully described using a hardware description language. A polynomial-based digital post-processing scheme is proposed to correct for the VCO nonlinearity. In addition, pulse modulation schemes like delta modulation and asynchronous sigma-delta modulation are used as a signal pre-coding scheme, in an attempt to reduce the impact of VCO nonlinearity on converter performance. In order to investigate the scaling benefits of all-digital data conversion, a VCO-based converter is designed in a 28 nm CMOS process. The design delivers a 13.4-bit ENOB over a 5 MHz bandwidth achieving an energy efficiency of 4.3 fJ/step according to post-synthesis schematic simulation, indicating that such converters have the potential of achieving good performance in deeply scaled processes by exploiting scaling benefits. Furthermore, large conversion errors caused by non-ideal sampling of the oscillator phase are studied. An encoding scheme employing ones counters is proposed to code the sampled ring oscillator output into a number, which is resilient to a class of sampling induced errors modeled by temporal reordering of the transitions in the ring. The proposed encoding reduces the largest error caused by random reordering of up to six subsequent bits in the sampled signal from 31 to 2 LSBs. Finally, the impact of process, voltage, and temperature (PVT) variations on the performance while operating the converter from a subthreshold supply is investigated. PVT-adaptive solutions are suggested as a means to achieve energy-efficient operation over a wide range of PVT conditions.

Populärvetenskaplig sammanfattning

Analog-till-digitalomvandlare omvandlar analoga signaler till digital form som enkelt kan bearbetas med exempelvis en dator. Konventionella dataomvandlare konstrueras oftast med analoga kretsar och ett specialanpassat konstruktionsflöde som gör processen besvärlig, långsam och dyr. Det blir också allt svårare att nå bra prestanda med analoga konstruktioner när de integrerade elektroniska kretsarna skalas ner till allt finare dimensioner, vilket är önskvärt för att förbättra yt- och energi-effektivitet. Å andra sidan så gynnar krympningen istället de digitala kretsarna som blir bättre och snabbare. Det digitala konstruktionsflödet är dessutom standardiserat och effektivt och erbjuder omfattande datorstöd. På grund av detta så är vi intresserade av att konstruera dataomvandlare med hjälp av digital teknik i så stor utsträckning som möjligt. Detta angreppssätt resulterar förhoppningvis i bättre och billigare dataomvandlare.

Denna avhandling undersöker speciellt hur spänningsstyrda oscillatorer kan användas för att översätta mellan analog och digital form. Idéen bygger på att en digital oscillator genererar svängningar med en frekvens som beror av ett analogt spänningsvärde. Svängingens frekvens mäts sedan med hjälp av digitala kretsar som översätter den till ett numeriskt tal. Oscillatorn implementerar också delar av signalbehandlingen om man mäter fasen, vilken matematiskt sett är integralen av dess frekvens. Denna egenskap kan användas för att förbättra dataomvandlarens noggrannhet inom ett visst frekvensband.

I arbetet så har en oscillatorbaserad analog-till-digitalomvandlare konstruerats och tillverkats med hjälp av vanliga digitala automatiseringsverktyg och komponentbibliotek. Konstruktionen ger en god energieffektivitet med 235 fJ per omvandlingssteg (Walden FOM)

vid 250 MHz samplingstakt samtidigt som noggrannheten motsvarar mer än åtta korrekta databitar (ENOB) för 25 MHz signalbandbredd. Vidare så har fel som uppstår i modern nanometerteknik undersökts. En metod för att undertrycka samplingsfel föreslås som bygger på en speciell kodning av multifasutgången på en vanlig digital oscillatortyp. Olika pulsmoduleringsscheman som deltamodulering och asynkron sigma-delta-modulering undersöks för att linjärisera funktionen. Vi undersöker också hur metoderna kan anpassas till lågeffekttillämpningar och föreslår lösningar för att uppnå god energieffektivitet även när vi har stora variationer i tillverkning, spänning och temperatur.

Preface

This dissertation presents the result of the research work performed by the author at the Department of Electrical Engineering, Linköping University, Sweden. The dissertation is divided into two parts. The first part provides a brief introduction to the research. The second part is a compilation of nine research papers produced during the course of the work. The papers are listed below.

1. V. Unnikrishnan and M. Vesterbacka, "Time-mode analog-to-digital conversion using standard cells," *IEEE Trans. Circuits Syst. I*, vol. 61, no. 12, 2014, pp. 3348-3357.

2. V. Unnikrishnan, S. R. Pathapati, and M. Vesterbacka, "A fully synthesized all-digital VCO-based analog-to-digital converter," in *Proc. IEEE Nordic Circuits and Systems Conference (NORCAS)*, Oslo, Norway, 2015, pp. 1-4.

3. V. Unnikrishnan and M. Vesterbacka, "A NAND gate based standard cell VCO for use in synthesizable ADCs," in *Proc. IEEE Nordic Circuits and Systems Conference (NORCAS)*, Oslo, Norway, 2015, pp. 1-4.

4. V. Unnikrishnan and M. Vesterbacka, "Linearization of synthesizable VCO-based ADCs using delta modulation," in *Proc. European Conference on Circuit Theory and Design (ECCTD)*, Trondheim, Norway, 2015, pp. 1-4.

5. V. Unnikrishnan and M. Vesterbacka, "Mixed-signal design using digital CAD," in *Proc. IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, Pittsburgh, USA, 2016, pp. 6-11.

6. V. Unnikrishnan and M. Vesterbacka, "Linearization of VCO-based ADCs using asynchronous sigma-delta modulation," in *Proc. IEEE 59th Midwest Symposium on Circuits and Systems (MWSCAS)*, Abu Dhabi, UAE, 2016.

7. V. Unnikrishnan and M. Vesterbacka, "Design of a VCO-based ADC in 28 nm CMOS," in *Proc. IEEE Nordic Circuits and Systems Conference (NORCAS)*, Copenhagen, Denmark, 2016.

8. V. Unnikrishnan and M. Vesterbacka, "Mitigation of sampling errors in VCO-based ADCs," submitted to *IEEE Trans. Circuits Syst. I.*

9. V. Unnikrishnan, M. Vesterbacka, and A. Alvandpour, "VCO-based ADCs for IoT applications," accepted for publication in *Proc. International Symposium on Integrated Circuits (ISIC)*, Singapore, 2016.

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Linköping, November 2016
Vishnu Unnikrishnan

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Part I

Background

Chapter 1

Introduction

Integrated electronics has evolved steadily since the invention of the first solid-state transistor in late 1940s. The progress has shown an exponential increase in the number of devices on integrated circuit chip, as predicted by Gordon Moore in the mid-1960s. The trend, the well known Moore's law, has continued for many decades but is now projected to gradually slow down. The increase in the number of devices is mainly achieved by a reduction in the device dimension, which generally leads to an increase in the circuit speed, the area efficiency of the integrated functions, and the energy efficiency of the circuit. With the invention of three-dimensional devices like the FinFET, as opposed to the conventional planar transistor design, the downscaling of the device feature size is expected to continue at least for some more years.

The relentless miniaturization of electronics is marked by persistent research and numerous break-through technological innovations. This has resulted in a steadily growing complexity of integrated circuits, enabling today's advanced signal processing and computational electronic systems. Two notable advancements are the invention of microprocessors (CPU) and the advent of digital signal processing (DSP) hardware. The two technologies dominate a majority of the integrated electronic systems produced today. Further, the two technologies favor processing of information and signals in a digital (time-discrete and amplitude-discrete) fashion as opposed to analog (time-continuous and amplitude-continuous) processing. Meanwhile, complementary metal-oxide-semiconductor (CMOS) technology emerged as the favored device

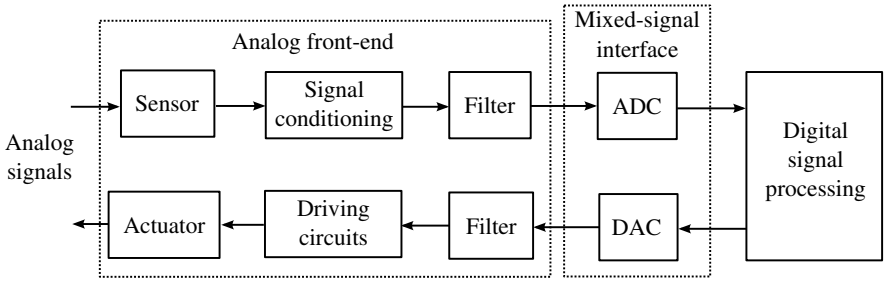

Figure 1.1: A signal processing system with a DSP core and analog signal interfaces.

fabrication technology to implement integrated circuits due to low fabrication cost, good energy efficiency, and high integration density. Another notable progress is the development of advanced computer aided design (CAD) tools that simplify and automate the design of complex digital systems.

It is convenient to implement complex signal processing tasks in digital technology due to the well-developed knowledge of DSP and due to the design automation support available to digital systems. Further, digital technology is more robust to noise as well as to variations in fabrication parameters, temperature, and the supply voltage than analog circuits and systems. However, most of the real life signals that need to be processed/generated are analog. This necessitates mixed-signal interface circuits that convert analog signals to digital and vice-versa. A typical signal processing system with a DSP core and analog signal interfaces is shown in Fig. 1.1. An analog-to-digital converter (ADC) converts time-continuous and amplitude-continuous (analog) signals to their time-discrete and amplitude-discrete (digital) approximation. A digital-to-analog converter (DAC) performs the reverse mapping.

The remaining part of Chapter 1 provides a motivation for considering digital implementation of mixed-signal blocks like ADCs and DACs.

1.1 Technology scaling and analog design

Technology scaling road-maps and the associated priorities are often set by the goal of improving the properties of digital circuits. In general,

digital circuits become faster, more energy efficient, and more area efficient as the feature size is scaled down. This is typically achieved by reducing the device dimension and the supply voltage. On the other hand, analog design becomes increasingly difficult as the technology is scaled down deep into the nanoscale regime (< 100 nm) due to a variety of reasons like the shrinking voltage headroom available for the designer, the reducing intrinsic gain of the devices, and the increasing noise coupling due to shorter distances between the circuit nodes [1–3]. Hence, it is beneficial to implement conventional analog functions with digital techniques in deeply scaled processes.

1.2 Design automation and analog design

The design of today's complex digital ICs packing billions of devices is supported by a set of mature design automation tools. Technology independent designs described using hardware description languages (HDLs) are mapped to a technology specific cell library, enabled by a cell-based design approach. The layout can then be generated automatically by assembling the cell layouts from the library. This makes design and porting of digital circuits easy, inexpensive and fast. On the other hand, analog circuits are still largely designed with a full custom design that is tedious, slow, and expensive [4, 5]. Further, the resulting designs are not easy to be ported to a finer technology. Attempts to synthesize analog circuits have had limited success [6–15]. Hence, it is desired to improve the design automation support for analog/mixed-signal blocks.

1.3 Digital implementation of analog/mixed-signal functions

An attractive alternative approach to design analog/mixed-signal blocks in nanoscale processes is to implement them using digital circuits. This results in circuits that are more scaling-friendly than their analog counterparts. Furthermore, this enables the possibility of automated design and porting of mixed-signal blocks using existing digital CAD framework thereby reducing design cost and time. A long-term goal is hence to develop robust and adaptive switch-based systems that interact directly with analog signals.

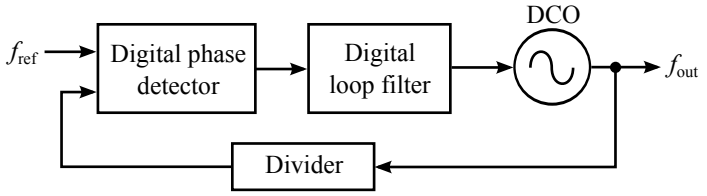

Figure 1.2: An all-digital frequency synthesizer.

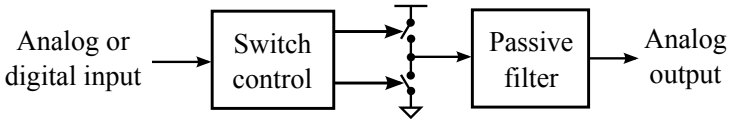

Figure 1.3: Basic topology of a class-D amplifier where high efficiency analog signal amplification is realized with switching functions.

The interest in digital implementation of analog/mixed-signal circuits is steadily increasing. Some examples are given below. Phase locked loops (PLLs) and frequency synthesizers are now being designed with digital components as well as being synthesized using standard cells [16,17]. An all-digital frequency synthesizer architecture is shown in Fig. 1.2 where a digitally controlled oscillator (DCO) is regulated using a digital phase detector and a digital loop filter. Class-D amplifiers constitute another example where analog signal amplification is achieved with switch-based circuits leading to good power efficiency [18–21]. The basic topology of a class-D amplifier is shown in Fig. 1.3. An ingenious attempt is made in [22] to build an operational amplifier from standard digital gates as shown in Fig. 1.4. A digital-to-analog interface can be realized using a digital sigma-delta modulator generating a one-bit stream and an on-chip or off-chip passive reconstruction filter, as shown in Fig. 1.5.

The concept of all-digital implementation can be extended to ADCs as well. A brief introduction to all-digital analog-to-digital conversion is provided in the next section.

1.4 Introduction to all-digital ADCs

All-digital analog-to-digital conversion is relatively less explored in the literature and is the focus of this dissertation. It is possible to realize ADCs with digital components. Some examples of all-digital ADCs are discussed below.

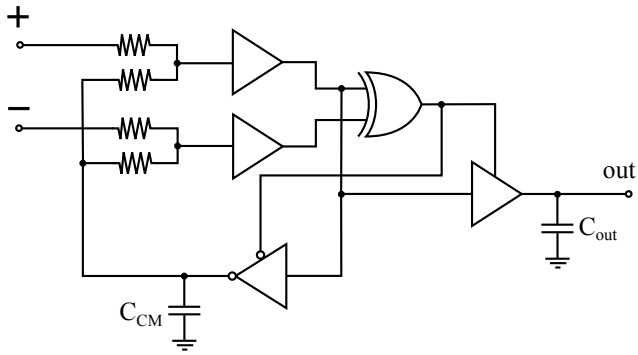

Figure 1.4: A digital circuit approximating an operational amplifier [22].

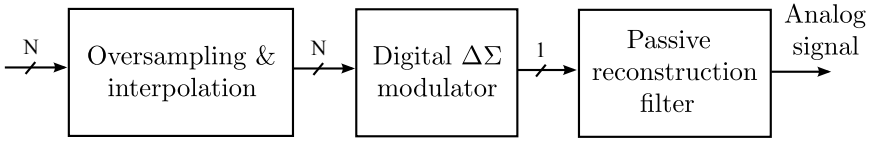

Figure 1.5: A digital-to-analog interface consisting of a digital sigma-delta modulator generating a one-bit stream and a passive reconstruction filter.

1.4.1 Stochastic converters

One approach to all-digital analog-to-digital conversion in deeply scaled processes utilizes circuit non-idealities like the variability of circuit parameters across a large number of components to realize a quantizer. Such converters are referred to as stochastic converters since the non-ideal variation of the circuit parameters is often modeled by stochastic processes. A stochastic all-digital ADC synthesized with standard cells is reported in [23]. The concept is illustrated in Fig. 1.6(a) where the Gaussian distributed voltage thresholds provided by circuit variability are utilized to build a flash-like quantizer. The analog input is applied to the positive terminals of a large number of comparators and the negative terminals are connected to a common reference. The random variation in the comparator offset provides a Gaussian distributed set of references. The output of the comparator array is sampled and added together. An inverse Gaussian function is applied to the result to generate the converter output. The clocked analog comparator built with digital gates is shown in Fig. 1.6(b). Even though such architectures may be useful in realizing low to medium resolution converters with a low design cost, it can be difficult to achieve high resolution and/or

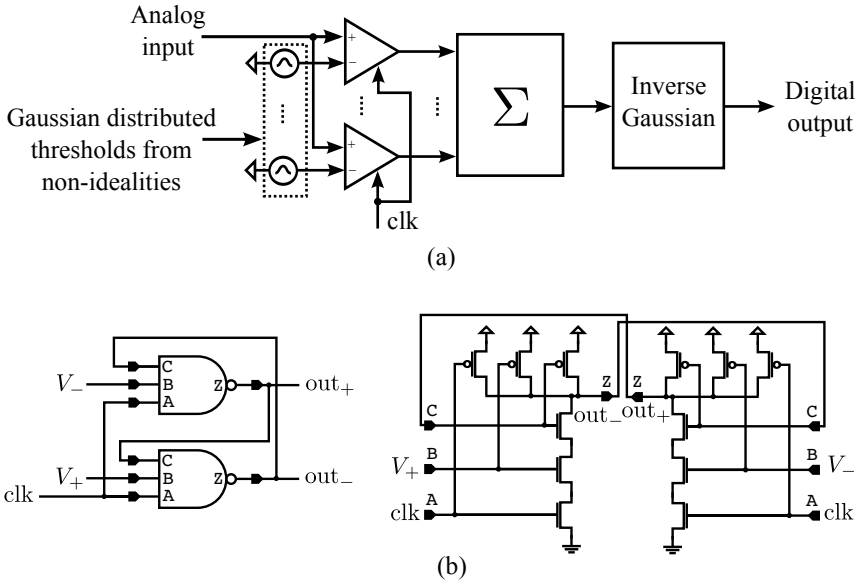

Figure 1.6: Stochastic all-digital ADC (a) and the analog comparator built with digital gates (b).

good energy efficiency with the approach.

1.4.2 Time-domain converters

Another approach to all-digital analog-to-digital conversion involves converting the input voltage/current into a time-domain parameter, which is then measured using digital circuits as shown in Fig. 1.7. Here, time-domain parameter refers to a signal parameter defined by the timing of transitions, including delay, position, frequency, and phase of digital pulses. The sampling is not shown in Fig. 1.7 since it can be placed before or after voltage-time conversion depending on the implementation.

An example is shown in Fig. 1.8 where a time-domain ADC is built from a voltage-controlled delay (voltage-time converter) and a Vernier time-to-digital converter (TDC). The voltage-controlled delay generates a delayed version of the converter clock signal and this delay is then measured using the TDC. A Vernier TDC helps obtain a high resolution which is not limited by the minimum inverter delay in the given technology.

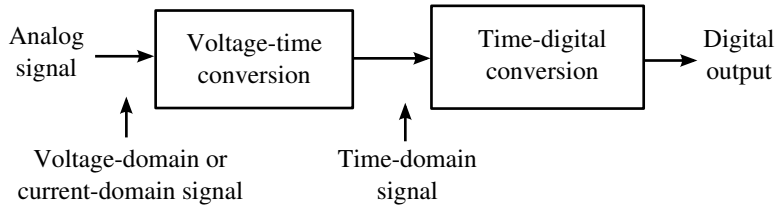

Figure 1.7: Time-domain analog-to-digital conversion.

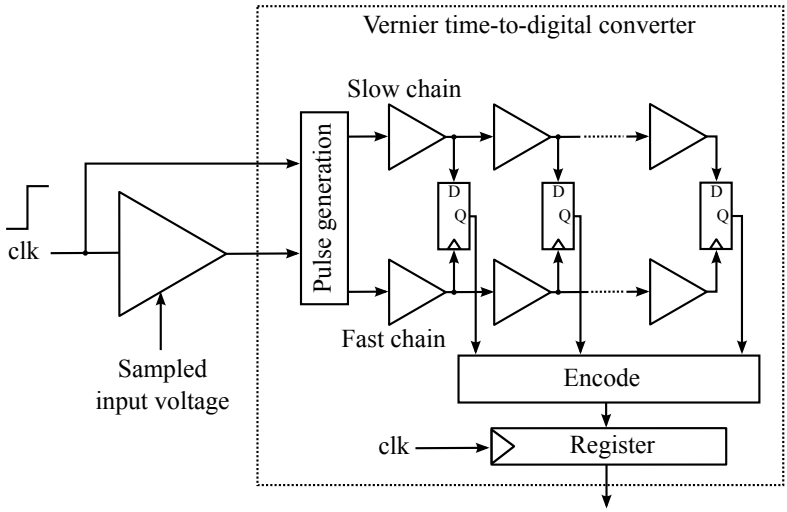

Figure 1.8: A time-domain ADC built from a voltage-controlled delay and a Vernier TDC.

Another interesting time-domain ADC architecture is a voltage-controlled oscillator (VCO)-based ADC where a VCO is used as both a voltage-time converter as well as a time-domain quantizer. It has several attractive signal processing properties that can be used to obtain a high performance. This dissertation explores the design of VCO-based ADCs with an emphasis on all-digital realizations. An overview of VCO-based ADCs is given in the next chapter.

1.5 Automatic design and porting with digital CAD

Even though digital implementation of data converters and other mixed-signal functions has received increased attention recently, most of the

designs discussed in the literature still use custom circuits for improved performance. This limits the possibility of automated design and porting of all-digital mixed-signal blocks using digital CAD tools. If such blocks are implemented entirely using standard cells, they can be synthesized, placed, and routed like other digital blocks thereby reducing design time and cost. Further, the technology independent HDL described mixed-signal blocks are relatively easier to port to a finer technology compared to their analog counterparts designed with a custom design flow.

It is indeed challenging to realize high performance mixed-signal blocks using generic low accuracy building blocks like standard cells. A key strategy is to employ as many architectural features and circuit techniques as possible to reduce the dependency of performance on component accuracy and layout irregularities. In this dissertation, we make an effort to design ADCs with digital CAD tools and standard cells, and to devise some circuit techniques that are useful in realizing robust all-digital ADCs.

The remaining part of the dissertation is organized as follows. Chapter 2 gives an overview of voltage-controlled oscillator based analog-to-digital converters. Chapter 3 presents a brief summary of the contributions of the dissertation. Chapter 4 discusses the research outcomes and suggests some opportunities for future research. Part II of the dissertation consists of a compilation of the research papers and manuscripts produced during the course of this work.

Chapter 2

VCO-based ADCs

VCO-based ADC refers to a class of ADCs that employ a VCO as a signal integrator as well as a phase-domain quantizer. A VCO operates as a signal integrator since the phase of the oscillator is a scaled integral of its frequency. Further, if the output of the VCO is processed such that the phase progression is detected only at discrete phase steps, the VCO also serves as a phase-domain quantizer. A brief introduction to VCO-based ADCs is given in the following sections.

2.1 Open-loop sigma-delta modulation

One of the earliest VCO-based ADCs is described in [24] where a VCO is used in an open-loop configuration to realize a frequency-domain first order sigma-delta converter. It is shown that a sigma-delta modulator [25] can be realized without an explicit feedback loop in the topology. This is extended to digital-to-analog conversion and to multi-order modulators in [26, 27] and is discussed in general in [28]. The concept is illustrated in Fig. 2.1 with the example of a first-order modulator, where the sigma, delta, and the quantizer functions in a sigma-delta modulator are implemented as cascaded blocks without a signal feedback between the input and the output. The sigma and the delta functions can be realized as modulo-integrator and modulo-differentiator respectively thereby avoiding the need for unlimited signal accumulation. The modulator is demonstrated for a time-discrete case in [28], where ADCs with first and second order shaping of quantization error are simulated.

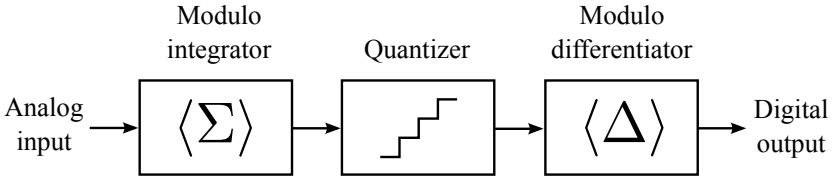

Figure 2.1: Open-loop implementation of a first order sigma-delta modulator.

2.2 VCO in open-loop sigma-delta ADC

A basic VCO-based converter where a VCO is used in a first-order open-loop sigma-delta ADC is shown in Fig. 2.2. The analog input signal is applied as the control voltage of the VCO. Assuming a linear VCO, the output of the oscillator is a frequency-domain signal approximating the input signal as illustrated in Fig. 2.3. A VCO with square wave output is assumed. The counter connected to the VCO output tracks the phase progression of the oscillator. Since the counter detects only integer increments of the VCO phase, quantization error is introduced in the phase tracking. The counter output is sampled with a register triggered by the converter clock. The resulting sample sequence is differentiated in the digital domain to retrieve the frequency information from the sampled phase, thereby generating the converter output. The two's complement arithmetic in the counter and the subtractor allows wrap around (modulo) operation of the counter as long as the counter does not progress more than a full cycle within a sampling interval even at the maximum VCO frequency. A behavioral simulation of the circuit is performed with a sinusoid input signal. Signals at different circuit nodes in Fig. 2.2 are shown in Fig. 2.4. It can be seen that the output at node Z provides a digital approximation of the input signal.

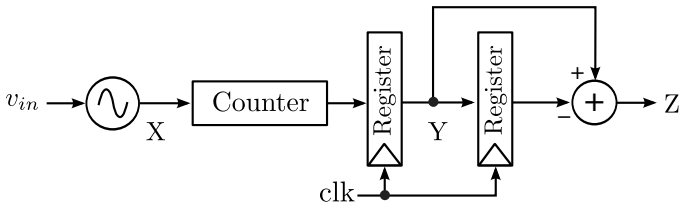

Figure 2.2: A basic VCO-based ADC realizing an open-loop first-order sigma-delta converter.

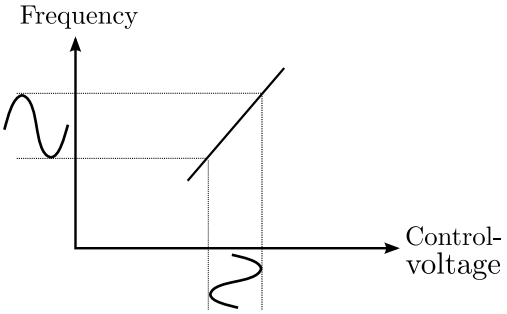

Figure 2.3: Transfer characteristics of the VCO.

2.2.1 Quantization error shaping

A model of the circuit is illustrated in Fig. 2.5. The input signal $v(t)$ is linearly mapped to the frequency signal $\psi(t)$ with a scaling factor K_{VCO}, where K_{VCO} is the VCO gain. The quantized phase output of the square wave VCO, $\phi_q(t)$, is modeled using a quantizer operating on the continuous phase, $\phi(t)$, of the oscillator. $\phi_q(t)$ is sampled at a rate F_s $(=1/T_s)$ yielding $\phi_q(kT_s)$, where k is the sample index. Discrete-time first-order differentiation on $\phi_q(kT_s)$ yields the output $y(k)$.

Assuming an ideal VCO with instantaneous frequency $\psi(v(t)) = 2\pi(f_0 + K_{osc}v(t))$ and instantaneous phase $\phi(t) = \int_0^t \psi(v(\tau))\,\mathrm{d}\tau$, the phase quantization error at the end of the k^{th} sampling interval is $\phi_\epsilon(kT_s) = \phi(kT_s) - \phi_q(kT_s)$. The output of the ADC can be expressed as

$$\begin{aligned} y(k) &= \frac{1}{2\pi}\left[\phi_q(kT_s) - \phi_q((k-1)T_s)\right] \\ &= \frac{1}{2\pi}\left[\Delta\phi(kT_s) - \Delta\phi_\epsilon(kT_s)\right] \end{aligned} \tag{2.1}$$

where Δ is the discrete-time backward difference operation defined as $\Delta x(n) = x(n) - x(n-1)$. Taking the Laplace transform, Equation (2.1) becomes

$$Y(s) = \frac{1}{2\pi}(1 - z^{-1})\left[\frac{\Psi(s)}{s} - \Phi_\epsilon(s)\right] \tag{2.2}$$

where $z = e^{sT_s}$, $\Psi(s) = \mathcal{L}\{\psi(v(t))\}$ and $\Phi_\epsilon(s) = \mathcal{L}\{\phi_\epsilon(t)\}$. Further, the noise transfer function (NTF) and the signal transfer function (STF) can be obtained as

$$NTF = \left.\frac{Y(s)}{\Phi_\epsilon(s)}\right|_{\Psi(s)=0} = -\frac{1}{2\pi}(1 - z^{-1}) \tag{2.3}$$

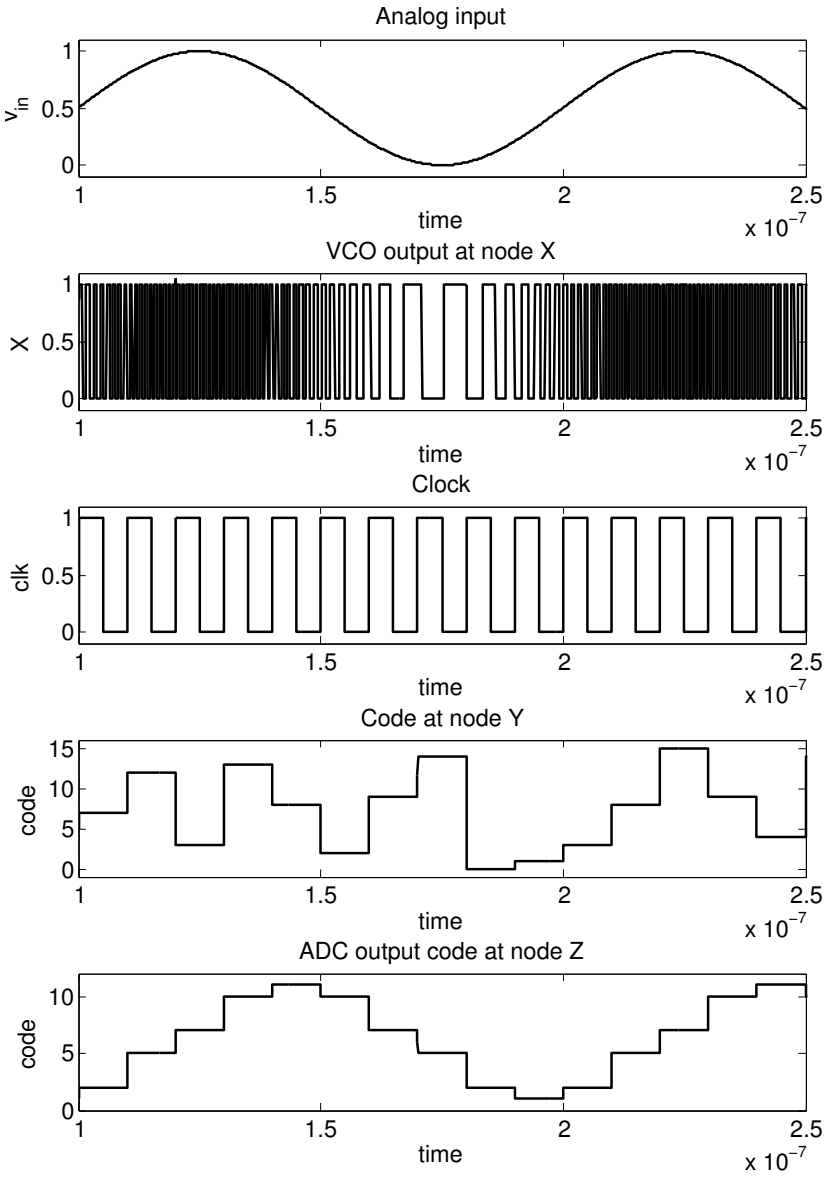

Figure 2.4: Signals at different circuit nodes in Fig. 2.2.

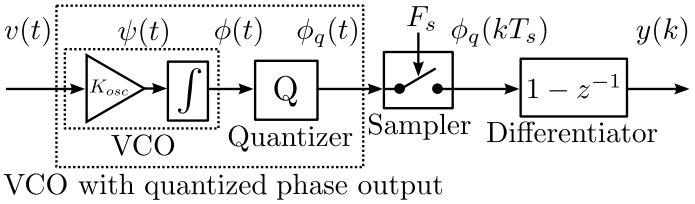

Figure 2.5: Model of the circuit in Fig. 2.2.

$$STF = \frac{Y(s)}{\Psi(s)}\bigg|_{\Phi_\epsilon(s)=0} = \frac{1}{2\pi}(1-z^{-1})\frac{1}{s} \tag{2.4}$$

indicating first-order shaping of the phase quantization error [29]. Noise shaping results from the memory of the oscillator, which keeps the phase quantization error of a sampling interval and subtracts it from the next.

2.2.2 Continuous-time sampling and inherent anti-alias filter

The model performs a post-quantization continuous-time sampling involving signal integration within sampling intervals as hinted by (2.4) implying a low pass filtering of the input, which relaxes the anti-alias filter design for the ADC. As shown in [30], substituting for $\phi(kT_s)$ and setting the input signal $v(t)$ to a sinusoid $A_{\text{in}}\cos(\omega_{\text{in}}t)$ where $\omega_{\text{in}} = 2\pi f_{\text{in}}$, Equation (2.1) can be reduced to

$$y(k) = C + K_{\text{ADC}}A_{\text{in}}cos\left(\frac{\omega_{\text{in}}T_s}{2}(2k-1)\right) - E_q \tag{2.5}$$

where $C = f_0T_s$ represents the DC component at the output, and

$$K_{\text{ADC}} = K_{\text{osc}}T_s\text{sinc}(T_sf_{\text{in}}) \tag{2.6}$$

represents the ADC gain component where $\text{sinc}(x) = \sin(\pi x)/(\pi x)$, $A_{\text{in}}\cos\left((\omega_{\text{in}}T_s/2)(k-1)\right)$ term represents the signal component, and $E_q = \frac{1}{2\pi}\Delta\phi_\epsilon(kT_s)$ represents the first-order shaped quantization noise. Equation (2.6) indicates sinc filtering with zeros at integral multiples of F_s.

2.2.3 Examples from the literature

VCO-based converters realizing open-loop sigma-delta modulators are demonstrated in a number of works, one of the earliest being [24] where

a converter is implemented in 1.2 μm CMOS. Digital intensive designs are demonstrated in [29, 31–34]. The impact of circuit non-idealities on VCO-based open-loop converters is analyzed in [30].

2.3 VCO-based quantizer in conventional sigma-delta ADC

In addition to the possibility of using a VCO in open-loop converter configuration, it is proposed to employ a VCO to realize the final integration stage and the quantizer in a conventional sigma-delta converter as shown in Fig. 2.6. The main benefit of this approach is that the feedback suppresses the impact of VCO nonlinearity by limiting the range of the VCO tuning curve that is used. The idea of using VCO as a quantizer in a closed-loop sigma-delta converter is proposed already in 2000 [35]. The data-weighted cycling of the delay cells in the ring VCO is utilized to implement an inherent dynamic matching of the DAC unit elements in [36]. In order to further reduce the impact of VCO nonlinearity, phase is used as the output quantity of the VCO instead of frequency in [37]. A fourth order modulator with a VCO-based quantizer is realized in [38] achieving 78 dB SNDR.

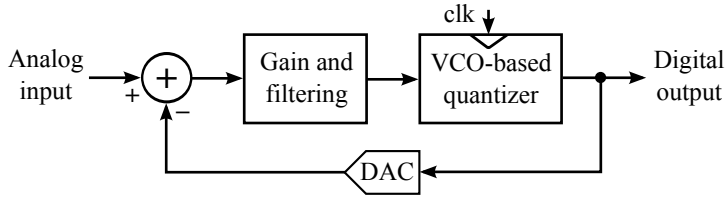

Figure 2.6: VCO-based quantizer in a conventional closed-loop sigma-delta converter.

2.4 VCO nonlinearity

A circuit non-ideality that needs to be compensated for to obtain good performance from VCO-based converters is the tuning non-linearity of the VCO. In the closed-loop converters discussed above, the feedback partly addresses VCO nonlinearity. Most of the solutions proposed to reduce the impact of VCO nonlinearity on the performance of open-loop

converters are of two types. The first involves digital post-processing where the correction is implemented as a look-up table [29,30,34,39] or using arithmetic circuits [40]. The second approach is to pre-code the input signal into a pulse waveform before measuring it with a VCO-based converter [41, 42]. This forces the VCO to operate between two fixed frequencies thereby removing the tuning nonlinearity from the transfer function.

2.5 All-digital implementation using standard cells

While VCO-based ADCs employing ring oscillators lend themselves to full digital implementation, most of the solutions described above use analog or custom circuits henceforth limiting the possibility of design automation using digital CAD tools. The focus of this dissertation is to explore the design of all-digital VCO-based converters implemented exclusively using standard cells in order to enable automated circuit and layout synthesis with digital CAD. This results in scaling-friendly architectures that benefit from technology scaling to become faster as well as more area and energy efficient as the feature size reduces. Moreover, design automation with digital CAD tools reduces design cost and time as well as the porting cost.

In a first step, a VCO-based converter employing a supply controlled ring VCO is designed with standard cells and fabricated in a 65 nm CMOS process achieving an 8-bit ENOB over 25 MHz bandwidth, demonstrating that a good performance is feasible while building converters with standard cells [40]. We then synthesized a few HDL described converter designs using digital CAD tools for synthesis and place-and-route [43, 44]. Further, a converter design in 28 nm CMOS delivers a 13.4-bit ENOB over a 5 MHz bandwidth according to post-synthesis schematic simulation with the Spectre simulator, indicating that standard cell implemented converters can achieve a good performance in deeply scaled processes exploiting scaling benefits [45].

Chapter 3

Contributions of the Dissertation

The contribution of the dissertation is provided as a compilation of papers and manuscripts in Part II of the dissertation. A brief summary of the papers is given below.

3.1 Summary of papers

The following list provides a summary of nine research papers produced during the course of this work. For each paper, the contribution of the paper as well as the specific contribution of the author in the work are provided.

- Paper A: Time-Mode Analog-to-Digital Conversion Using Standard Cells

  Authors: Vishnu Unnikrishna and Mark Vesterbacka

  Published in IEEE Transactions on Circuits and Systems I, 2014.

  In this work, a time-domain ADC is designed exclusively using standard cells and fabricated in a 65 nm CMOS process to investigate the performance that can be achieved while designing converters with low accuracy building blocks. The paper presents the design as well as the measurement results of the converter.

The proposed design is a VCO-based ADC employing a supply-controlled ring VCO. A quantizer design with a Gray-counter array is proposed to mitigate the problem of partial sampling of counter outputs in multi-bit VCO-based quantizers, thereby limiting the maximum sampling induced error to one LSB. Further, a digital post-processing scheme employing polynomial-fit non-linearity estimation is proposed to correct for VCO non-linearity. The design occupies 0.026 mm^2 and delivers an ENOB of 8.1 bits over a signal bandwidth of 25.6 MHz, while sampling at 205 MHz. It consumes a relatively low average power of 3.3 mW achieving a Walden FoM of 235 fJ/step.

I have designed and simulated the converter under the guidance of the second author. The fast Gray-counter design is provided by the second author. I have created the layout of the converter, verified the design, and taped it out. I have also performed the post-fabrication evaluation of the converter. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper B: A Fully Synthesized All-Digital VCO-Based Analog-to-Digital Converter

  Authors: Vishnu Unnikrishnan, Srinivasa Rao Pathapati, and Mark Vesterbacka

  Published in the proceedings of IEEE Nordic Circuits and Systems Conference (NORCAS), Oslo, Norway, 2015.

  In this work, a VCO-based ADC that is fully described using a digital HDL is synthesized, placed, and routed using standard digital design tools. A standard cell library in a 65 nm CMOS process is used. Post synthesis and post place-and-route performances are provided. The converter delivers a resolution of 9 ENOB over 10 MHz bandwidth according to post layout parasitic extracted simulations using the Spectre simulator.

  I have designed, synthesized, and simulated the converter with some help from the second author. I have set up the tool flow and have written the necessary scripts. I have written the manuscript of the paper and refined it based on the feedback from the third author.

- Paper C: A NAND Gate Based Standard Cell VCO for Use in Synthesizable ADCs

Authors: Vishnu Unnikrishnan and Mark Vesterbacka

Published in the proceedings of IEEE Nordic Circuits and Systems Conference (NORCAS), Oslo, Norway, 2015.

This paper proposes a VCO circuit built from NAND gates for use in synthesizable VCO-based converters, which mitigates the problem of low input impedance in supply-controlled ring VCOs. The circuit is demonstrated by employing it in an all-digital VCO-based converter. Transistor level simulation of the resulting netlist using the Spectre simulator shows that a performance of 10 bit ENOB over a 10 MHz bandwidth can be achieved after digital correction, while using the proposed VCO.

I have designed, synthesized, and simulated the circuits. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper D: Linearization of Synthesizable VCO-Based ADCs Using Delta Modulation

  Authors: Vishnu Unnikrishnan and Mark Vesterbacka

  Published in the proceedings of European Conference on Circuit Theory and Design (ECCTD), Trondheim, Norway, 2015.

  This work explores an alternate linearization scheme for VCO-based converters instead of digital post-processing. The signal is pre-coded into a delta-modulated pulse stream before being used to drive a VCO-based converter. This causes the oscillator to operate at two distinct frequencies thereby eliminating the VCO non-linearity from the converter transfer function. A circuit is proposed that consists of a synthesized digital block realizing all the active parts of the circuit and a passive RC net used as an integrator. Spectre simulation of the netlist synthesized using a 65 nm standard cell library shows a performance of 8.2 bit ENOB over a 3 MHz bandwidth without using any digital post-processing.

  I have designed, synthesized, and simulated the converter. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper E: Mixed-Signal Design Using Digital CAD

  Authors: Vishnu Unnikrishnan and Mark Vesterbacka

  Published in the proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Pittsburgh, USA, 2016.

The paper investigates the use of the existing CAD framework for digital circuit synthesis to design and synthesize a selected set of mixed-signal functions like analog-to-digital and digital-to-analog conversions. Some circuit examples for implementation of data conversion using digital circuits are discussed, leveraging on time-domain signal processing. Some of the signal corruption mechanisms in time-domain signal processing systems are considered in order to suggest adaptations to the conventional digital design flow for the synthesis of mixed-signal circuits. As an example, a VCO-based ADC is designed and synthesized with the vendor supplied standard cell library in a 65 nm CMOS process. Spectre simulation results show the feasibility of employing a digital CAD framework to synthesize high performance mixed-signal circuits by applying time-domain signal processing.

I have done the literature survey, and have designed, synthesized, and simulated the converter. I have also set up the tool flow required for the synthesis of the converter. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper F: Linearization of VCO-Based ADCs Using Asynchronous Sigma-Delta Modulation

  Authors: Vishnu Unnikrishnan and Mark Vesterbacka

  Published in the proceedings of IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, UAE, 2016.

  Asynchronous sigma-delta modulation is investigated as an alternative linearization scheme for all-digital VCO-based ADCs instead of digital post-processing. The modulator output, when used to drive a VCO-based converter, causes the oscillator to operate at two fixed frequencies thereby removing the VCO nonlinearity from the transfer function. A circuit is designed, consisting of a digital block and a passive RC circuit operating as an integrator. Spectre simulation of the design synthesized using a 65 nm standard cell library indicate that a harmonic suppression up to -60 dB is feasible.

  I have designed, synthesized, and simulated the converter. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper G: Design of a VCO-based ADC in 28 nm CMOS

Authors: Vishnu Unnikrishnan and Mark Vesterbacka

Published in the proceedings of IEEE Nordic Circuits and Systems Conference (NORCAS), Copenhagen, Denmark, 2016.

In this work, a VCO-based converter is designed and synthesized in a 28 nm FDSOI CMOS process to investigate the scaling benefits of all-digital analog-to-digital conversion. A coarse-fine quantizer is used to obtain high energy efficiency. Common patterns of sample errors at the multi-phase VCO output are identified and mitigated. Final design indicates an ENOB of 13.4 and a Walden FoM of 4.3 fJ/step over a 5 MHz bandwidth while sampling at 150 MHz, according to schematic simulation of the synthesized netlist.

I have designed, synthesized, and simulated the converter. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper H: Mitigation of Sampling Errors in VCO-Based ADCs

  Authors: Vishnu Unnikrishnan and Mark Vesterbacka

  Submitted to IEEE Transactions on Circuits and Systems I.

  During the work that constitutes Paper G, it is observed that complex sampling induced errors are possible while designing VCO-based converters in deeply scaled technologies, causing large conversion errors. The solution proposed in Paper G is a static mapping of the identified error patterns in the sampled ring oscillator output to the nearest valid pattern. This work reviews sampling induced errors in VCO-based converters and investigates errors resulting from non-ideal sampling of a fast switching multi-phase ring oscillator output. A scheme employing ones-counters is proposed to encode the sampled ring oscillator code into a binary representation, which is resilient to a class of sampling induced errors modeled by temporal reordering of the transitions in the ring. In addition to correcting errors caused by deterministic reordering, proposed encoding suppresses conversion errors in the presence of arbitrary reordering patterns that may result from heuristic place-and-route algorithms in wire delay dominated processes. The error suppression capability of the encoding is demonstrated using MATLAB simulation. The proposed encoder reduces the largest error caused by random reordering of six subsequent bits in the sampled signal from 31 to 2 LSBs.

I have investigated the problem of sampling induced conversion errors and have developed the proposed solution with some guidance and hints from the second author. I have designed, synthesized, and simulated the converter used in the experiments. I have written the MATLAB routines to simulate and validate that proposed solution. I have written the manuscript of the paper and refined it based on the feedback from the second author.

- Paper I: VCO-Based ADCs for IoT Applications

  Authors: Vishnu Unnikrishnan, Mark Vesterbacka, and Atila Alvandpour

  Accepted for publication in the proceedings of The $15^{\mathbf{th}}$ International Symposium on Integrated Circuits (ISIC), Singapore, 2016.

  Internet-of-things (IoT) benefits from fast and low cost development of technology portable re-configurable hardware. Low power consumption is desired for applications operating from harvested or limited energy. Subthreshold operation of VCO-based ADCs is investigated in this work in order to meet these challenges. A ring VCO built using NAND gates is used for reliable operation in the subthreshold region. The impact of supply scaling and PVT variations on the VCO characteristics as well as on the converter performance is studied using transistor level simulations. Some solutions are suggested towards energy-efficient operation over a wide range of PVT conditions.

  I have investigated the performance of VCO-based converters in subthreshold operation with some guidance from the second and the third authors. I have designed, synthesized, and simulated the converter and the circuits used in the experiments. I have written the manuscript of the paper and refined it based on the feedback from the second and the third authors.

Chapter 4

Discussion and Future Work

The work in this dissertation is a step towards a long-term goal of digital implementation of mixed-signal functions like analog-to-digital and digital-to-analog conversions. This leads to scaling-friendly data converter architectures that exploit the benefits of technology scaling to become faster, more energy efficient, and more area efficient as the feature size is scaled down. Moreover, the approach enables design and porting of mixed-signal blocks using the mature design automation framework available for digital design. This results in significant reduction of design and porting costs associated with mixed-signal blocks, leading to fast development of technology-portable system-on-chip solutions. The challenge, however, is to develop robust architectures and circuit techniques such that the dependency of performance on component accuracy is reduced.

VCO-based ADC is an attractive architecture to implement all-digital analog-to-digital conversion due to favorable properties like the first-order shaping of the quantization error and the sinc anti-alias filtering. It is shown that VCO-based converters can achieve a high energy efficiency [33, 46]. Even though closed-loop converters achieve good resolution [36, 37, 47], they use analog components limiting the possibility of a full digital implementation. The achievable accuracy of open-loop converters is often limited by the VCO nonlinearity and/or VCO phase noise. Several calibration schemes are proposed to correct for the VCO nonlinearity thereby achieving good nonlinearity suppression [39,48,49].

We explore converter designs that are exclusively built using standard cells enabling the possibility of automated circuit and layout synthesis. The measured results in Paper A shows that designs built with generic low accuracy components like standard cells can deliver reasonable performance and good energy efficiency. It is also shown that a polynomial-based digital post-processing for nonlinearity correction achieves good harmonic suppression with reasonable hardware cost. The design in Paper G, implemented with standard cells in a 28 nm process, delivers a resolution of 13.4-bit ENOB over 5 MHz and an energy efficiency of 4.3 fJ/step. Even though the results are from simulation without layout parasitics, the performance indicates that all-digital converters benefit significantly from technology scaling and have the potential to deliver a good performance in deeply scaled processes. The work in Paper I illustrates yet another challenge associated with the design of VCO-based converters. The variability of the VCO tuning curve as a function of PVT variations needs to be dealt with, especially for subthreshold operation aimed at low-energy conversion.

4.1 Future work

Even though the interest in VCO-based converters has increased recently, the research is still in its early stage. Some research opportunities are discussed below with an aim of moving towards the long-term goal of robust and adaptive all-digital ADCs. Digital post-processing for background nonlinearity correction with blind nonlinearity estimation is an interesting problem to pursue. All-digital modulators with higher order quantization error shaping are also of interest since they help improve the SNR and reduce limit cycle oscillations at the output. In order to implement PVT-adaptive converters like those suggested in Paper I, VCOs with digitally configurable gain are desired. Hence, standard cell implemented VCOs with high input impedance and digitally configurable gain are useful.

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Part II

Publications

Publications