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Energy-Efficient Data Converters for Low-Power Sensors

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Abstract

Wireless sensor networks (WSNs) are employed in many applications, such as for monitoring bio-potential signals and environmental information. These applications require high-resolution (> 12 -bit) analog-to-digital converters (ADCs) at low-sampling rates (several kS/s). Such sensor nodes are usually powered by batteries or energy-harvesting sources hence low power consumption is primary for such ADCs. Normally, tens or hundreds of autonomously powered sensor nodes are utilized to capture and transmit data to the central processor. Hence it is profitable to fabricate the relevant electronics, such as the ADCs, in a low-cost standard complementary metal-oxide-semiconductor (CMOS) process. The two-stage pipelined successive approximation register (SAR) ADC has shown to be an energy-efficient architecture for high resolution. This thesis further studies and explores the design limitations of the pipelined SAR ADC for high-resolution and low-speed applications.

The first work is a 15-bit, 1 kS/s two-stage pipelined SAR ADC that has been implemented in $0.35\text{-}\mu\text{m}$ CMOS process. The use of aggressive gain reduction in the residue amplifier combined with a suitable capacitive array digital-to-analog converter (DAC) topology in the second-stage simplifies the design of the operational transconductance amplifier (OTA) while eliminating excessive capacitive load and consequent power consumption. A comprehensive power consumption analysis of the entire ADC is performed to determine the number of bits in each stage of the pipeline. Choice of a segmented capacitive array DAC and attenuation capacitor-based DAC for the first and second stages respectively enable significant reduction in power consumption and area. Fabricated in a low-cost $0.35\text{-}\mu\text{m}$ CMOS process, the prototype ADC achieves a peak signal-to-noise-and-distortion ratio (SNDR) of 78.9 dB corresponding to an effective number of bits (ENOB) of 12.8-bit at a sampling frequency of 1 kS/s and provides a Schreier figure-of-merit (FoM) of 157.6 dB. Without any form of calibration, the ADC maintains an ENOB > 12.1 -bit up to the Nyquist bandwidth of 500 Hz while consuming $6.7\text{ }\mu\text{W}$. Core area of the ADC is 0.679 mm^2 .

The second work is a 14-bit, tunable bandwidth two-stage pipelined SAR ADC which is suitable for low-power, cost-effective sensor readout circuits. To overcome the high open-loop DC gain requirement of the OTA in the gain-stage, a 3-stage

capacitive charge pump (CCP) is utilized to achieve the gain-stage instead of using the switch capacitor (SC) amplifier. Unity-gain OTAs have been used as the analog buffers to prevent the charge sharing between the CCP stages. The detailed design considerations are given in this work. The prototype ADC, designed and fabricated in a low-cost 0.35- μm CMOS process, achieves a peak SNDR of 75.6 dB at a sampling rate of 20 kS/s and 76.1 dB at 200 kS/s while consuming 7.68 μW and 96 μW , respectively. The corresponding Schreier FoM are 166.7 dB and 166.3 dB. Since the bandwidth of CCP is tunable, the ADC maintains a SNDR > 75 dB up to 260 kHz. The core area occupied by the ADC is 0.589 mm².

As the low-power sensors might be active only for very short time triggered by an external pulse to acquire the data, the third work is a 14-bit asynchronous two-stage pipelined SAR ADC which has been designed and simulated in 0.18- μm CMOS process. A self-synchronous loop based on an edge detector is utilized to generate an internal clock with variable phase. A tunable delay element enables to allocate the available time for the switch capacitor DACs and the gain-stage. Three separate asynchronous clock generators are implemented to create the control signals for two sub-ADCs and the gain-stage between. Aiming to reduce the power consumption of the gain-stage, simple source followers as the analog buffers are implemented in the 3-stage CCP gain-stage. Post-layout simulation results show that the ADC achieves a SNDR of 83.5 dB while consuming 2.39 μW with a sampling rate of 10 kS/s. The corresponding Schreier FoM is 176.7 dB.

Populärvetenskaplig sammanfattning

Trådlösa sensor nätverk (Wireless sensor networks, WSNs) används i många olika applikationer, t.ex. övervakning av biopotential signaler och miljöinformation. Dessa applikationer behöver hög upplösta (> 12 -bitars) analog-till-digital omvandlare (AD-omvandlare) vid låga samplingfrekvenser (några kS/s). Sådana sensor noder är vanligtvis drivna av batterier eller med hjälp av energiskördning vilket gör att en låg energiförbrukning är väsentligt för sådana AD omvandlare. Vanligtvis används tiotals eller hundratals autonoma sensor noder för att fånga och skicka data till en central processor. Därför är det fördelaktigt om all elektronik, inklusive AD-omvandlaren, tillverkas i en lågkostnads standard CMOS process. En tvåstegs pipelined successiv approximation register (SAR) AD-omvandlare har visat sig vara en energieffektiv arkitektur för höga upplösningar. Denna avhandling undersöker och utforskar designgränserna för pipelineade SAR AD-omvandlare för applikationer med hög upplösning och låg samplingfrekvens.

Det första bidraget är en 15-bitars, 1 kS/s tvåstegs pipelined SAR AD-omvandlare implementerad i en $0.35\text{-}\mu\text{m}$ CMOS process. Den använder aggressiv förstärkningsreducering i restförstärkaren kombinerat med en lämplig kapacitiv digital-till-analog omvandlare (DA-omvandlare) topologi i det andra steget förenklar designen av operations transkonduktans förstärkaren (OTA) samtidigt som den kapacitiva lasten och effektförbrukningen minimeras. En detaljerad effektförbrukningsanalys av hela AD-omvandlaren är utförd för att bestämma antalet bitar i de olika stegen. Valet av en segmenterad kapacitiv DA-omvandlare och dämpnings kapacitans DA-omvandlare för det första respektive andra steget möjliggör en signifikant reduktion av både effektförbrukningen och arean. Tillverkad i en lågkostnads $0.35\text{-}\mu\text{m}$ CMOS process når en prototyp AD-omvandlare en maximal signal-till-brus-och-distortions förhållande (SNDR) av 78.9 dB motsvarande 12.8 effektivt antal bitars (ENOB) vid en samplingfrekvens på 1 kS/s och ger ett Schreier mätetal på 157.6 dB. Utan någon typ av kalibrering så har AD-omvandlaren en $\text{ENOB} > 12.1$ -bitars upptill Nyquist bandbredden på 500 Hz med en effektförbrukning av $6.7\text{ }\mu\text{W}$. Kärnarean av AD-omvandlaren är 0.679 mm^2 .

Det andra bidraget är en 14-bitars tvåstegs pipelined SAR AD-omvandlare med justerbar bandbredd för lågeffekts, kostnadseffektiva sensor avläsningskretsar. För att överkomma problemet med hög råförstärkning i restförstärkaren används en flerstegs kapacitiv laddningspump (CCP) istället för en switchad kapacitans (SC) förstärkaren. Förstärkare med ett i förstärkning används som analoga buffrar för att undvika laddningsdelning mellan CCP stegen. En detaljerad beskrivning av designvalen är presenterade i denna avhandling. Prototyp AD-omvandlaren, designad och tillverkad i en lågkostnads $0.35\text{-}\mu\text{m}$ CMOS process, når en maximal SNDR på 75.6 dB vid en samplingfrekvens av 20 kS/s och 76.1 dB vid 200 kS/s med en effektförbrukning av $7.68\text{ }\mu\text{W}$ respektive $96\text{ }\mu\text{W}$. Det motsvarande Schreier mätetalet är 166.7 dB respektive 166.3 dB. Eftersom bandbredden av CCPn är justerbar så har AD-omvandlaren en SNDR > 75 dB upptill 260 kHz. Kärnarean av AD-omvandlaren är 0.589 mm^2 .

Eftersom vissa lågeffekts sensornoder enbart är aktiva en väldigt kort tid och startas av en extern aktiverings signal, så är det tredje bidraget en 14-bitars asynkron tvåstegs pipelined SAR AD-omvandlare designad och simulerad i en $0.18\text{-}\mu\text{m}$ CMOS process. En självsynkroniserande loop bestående av en flankdetektor används för att generera en intern klocka med adaptiv fas. Ett justerbart fördröjningselement möjliggör allokering av den tillgängliga tiden för DA-omvandlaren och förstärkarsteget. Därefter implementerades tre separata asynkrona klockgeneratorer för att generera kontrollsignalerna till de två AD-omvandlar stegen och förstärkningssteget mellan dem. För att ytterligare reducera effektförbrukningen av förstärkarsteget används enkla sourceföljare som analog buffrar i trestegs CCP steget. Post-layout simuleringar visar att AD-omvandlaren når en SNDR av 83.5 dB med en effektförbrukning på $2.39\text{ }\mu\text{W}$ och en samplingfrekvenser av 10 kS/s. Det motsvarande Schreier mätetalet är 176.7 dB.

Preface

This dissertation presents the research work performed during the period October 2012 – November 2016 at the Division of Integrated Circuits and Systems, Department of Electrical Engineering, Linköping University, Sweden. The contents of this dissertation are based on the following publications:

- **Paper I** – **K. Chen**, P. Harikumar, and A. Alvandpour, “Design of a 12.8 ENOB, 1 kS/s pipelined SAR ADC in 0.35- μm CMOS”, *Journal of Analog Integrated Circuits and Signal Processing*, vol. 86, no. 1, pp. 87-98, Jan 2016.
- **Paper II** – **K. Chen**, A. Alvandpour, “A Pipelined SAR ADC with Gain-stage Based on Capacitive Charge Pump”, *Journal of Analog Integrated Circuits and Signal Processing* (2016), DOI: 10.1007/s10470-016-0872-4.
- **Paper III** – **K. Chen**, M. N. Lönn and A. Alvandpour, “A 14-bit Asynchronous Two-stage Pipelined SAR ADC in 0.18- μm CMOS”. (Manuscript to be submitted).
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- **Paper VI** – **K. Chen**, A. Alvandpour, “Capacitive Charge Pump Gain-stage with Source Follower Buffers for Pipelined SAR ADCs”, *15th International Symposium on Integrated Circuits*, Singapore, Dec. 2016. (Accepted)
- **Paper VII** – **K. Chen**, M. N. Lönn and A. Alvandpour, “Asynchronous Clock Generator for a 14-bit Two-stage Pipelined SAR ADC in 0.18- μm CMOS”, *34th Nordic Circuits and Systems*, Denmark, Copenhagen, Nov. 2016. (Accepted)

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List of Abbreviations

ADCs	Analog-to-Digital Converters
CMOS	Complementary Metal-Oxide-Semiconductor
CCP	Capacitive Charge Pump
CMFB	Common Mode Feedback
DAC	Digital-to-Analog Converter
DNL	Differential Nonlinearity
DDNR	Data-Driven Noise-Reduction
DFF	D-type Flip Flop
DLL	Delay-Locked Loop
ENOB	Effective Number of Bit
EOG	Electrooculogram
EEG	Electroencephalogram
FoM	Figure of Merit
FFT	Fast Fourier Transform
HD₂	Second-order Harmonic Distortion
INL	Integral Nonlinearity
ISSCC	International Solid-State Circuits Conference
JLCC	J-Leaded Chip Carrier
LSB	Least Significant Bit

MSB	Most Significant Bit
MOS	Metal-Oxide-Semiconductor
MIM	Metal-Insulator-Metal
OTA	Operational Transconductance Amplifier
OSR	Over Sampling Ratio
PVT	Process, Voltage, and Temperature
PIP	Poly-Insulator-Poly
SAR	Successive Approximation Register
SNDR	Signal-to-Noise-and-Distortion Ratio
SC	Switch Capacitor
S/H	Sample-and-Hold
WSNs	Wireless Sensor Networks

Chapter 1

Introduction

1.1 Background

The emerging infrastructure systems such as smart home [1] and wireless health monitoring [2] have remarkably improved the quality of people's life in recent years. The wireless sensor networks (WSNs) play an important role in these applications. Fig. 1-1 shows a typical WSN system [3]. The WSN is composed of a few tens to thousands

Figure 1-1: Wireless sensor network system [3].

of sensor nodes working together to monitor a region to obtain data about the targets [4, 5]. Each sensor node consists of a sensor, an analog-to-digital converter (ADC), a microprocessor and a storage as well as a wireless transceiver to transmit the collected data to the sink node. The ADC as one of the crucial blocks forms the interface between the analog world and the digital domain. In general, as these sensor nodes are powered by the batteries or the energy-harvesting sources [6–8], energy efficiency is a major design issue in order to increase the lifespan of the network [5].

In addition, the cost of building a WSN becomes critical when a large number sensor nodes are used. Hence, low-power consumption and low-cost are the two major challenges to develop the relevant electronic blocks [9], such as the ADCs. To capture the environmental information such as the temperature, pressure and humidity [10] and the bio-potential signals such as EEG and EOG [11], high resolution (> 12 -bit) ADCs with low-sampling rates (several kS/s) are required [12, 13].

1.2 Review of ADC Architectures

The successive approximation register (SAR) ADC, pipelined ADC, $\Sigma\Delta$ ADC and flash ADC are the four common ADC architectures. Fig. 1-2 shows the performance survey of the ADCs which have been published in ISSCC (1997-2016) [14]. As shown in Fig. 1-2(a), the SAR ADCs are suitable for low-speed and moderate-resolution design. The sigma-delta ($\Sigma\Delta$) ADCs are typically used for low-speed but medium-to-high resolution applications. The pipelined ADCs dominate the medium-speed and medium-resolution domain. The high-speed, low-resolution applications are dominated by the flash ADCs. Hence, to achieve an ADC with the desired resolution (> 12 -bit) and speed (several kS/s), the $\Sigma\Delta$ ADC is the primary candidate. However, achieving a $\Sigma\Delta$ ADC with a signal-to-noise-and-distortion ratio (SNDR) larger than 74 dB (12-bit) requires either a high order modulator or a high over sampling ratio (OSR) [15–18], or a combination of both [19]. No matter which solution is implemented, substantial power is consumed by the $\Sigma\Delta$ ADC [15–19]. From Fig. 1-2(b), the SAR ADCs show an excellent power efficiency at moderate resolutions. This is due to the fact that minimal analog circuits are utilized. But achieving a SAR ADC with an effective number of bits (ENOB) larger than 12-bit is a challenge due to the influence from comparator noise and capacitor mismatch [20–24]. To suppress the comparator noise, data-driven noise-reduction (DDNR) method is proposed in [12]. A nonbinary-weighted array capacitance and a preamplification stage are implemented in [24] to enhance the linearity and decrease the noise, respectively. All these techniques introduce additional design complexity.

A pipelined SAR ADC also known as the SAR-assisted pipeline ADC as an emerging architecture has been successfully implemented to achieve both high-resolution [25] and also low-power [26–28]. Such an architecture consists of two independent sub-SAR ADCs coupled by a gain-stage. The need for a high-accuracy comparator can be obviated by incorporating a SAR ADC as the sub-ADC in the pipeline stage. For a given resolution, the pipelined SAR ADC requires less number of stages compared to a conventional pipelined ADC which translates into substantial power savings. Therefore, this thesis further focuses on the design of energy-efficient pipelined SAR ADC.

(a) Nyquist sampling frequency versus SNDR

(b) Power versus SNDR

Figure 1-2: ADC performance survey. The source data are collected from ISSCC [14].

1.3 Challenges and Previous Work

For the pipelined SAR ADC, although the high-accuracy comparator is avoided, an additional gain-stage is inevitable to amplify the residue signal. Normally, the switch capacitor (SC) amplifier is the primary choice to realize the gain-stage, but a high-gain operational transconductance amplifier (OTA) is necessary to amplify the residue with sufficient accuracy [26,27,29]. Since the open-loop DC gain requirement

of the OTA grows exponentially with the resolution of the ADC [26], the design of high-gain OTA is a major challenge for implementing high-resolution pipelined SAR ADC, especially in the advanced complementary metal-oxide-semiconductor (CMOS) process technology. As shown in [26, 27], the conventional telescopic-cascode OTA is used to achieve high gain requirement. But it consumes substantial power. Thus, finding alternative gain-stage solutions to reduce the high open-loop DC gain requirement and the power consumption has gained large attention.

In [30], an open-loop amplifier as the gain-stage is proposed. Although the inter-stage gain can be provided by the open-loop solution, this voltage gain will be significantly influenced by the process variations. Thus, an extra calibration technique is inevitable. The dynamic amplifier [28, 31, 32] which allows to switch off the OTA during the reset phase, provides a power-efficient solution. Since there is no static current flowing in the OTA, the power consumption of the OTA is significantly reduced. Nevertheless, a high open-loop DC gain is still required to reduce the inter-stage gain error. Otherwise, digital calibration such as a background calibration is necessary to achieve accurate residue gain. Another alternative is the ring amplifier [33, 34] which essentially is a 3-stage inverter amplifier. Such amplifier results in a good energy efficiency and the required high open-loop DC gain can be easily achieved from three gain stages. But the stability becomes an issue. To solve this problem, a self-biased ring amplifier is reported in [35].

1.4 Objectives

Aiming to reduce high open-loop DC gain requirement of the OTA and the power consumption, this thesis further focuses on finding alternative gain-stage solutions for the pipelined SAR ADC design. The main contributions of this dissertation are as follows:

- Design and implementation of a 12.8 ENOB, 1 kS/s pipelined SAR ADC in 0.35- μm CMOS. The power analysis of the two-stage pipelined SAR ADC is provided to determine the stage resolution. Gain-reduction method is used to mitigate the high open-loop gain requirement of the OTA.
- Design and implementation of a 12.3 ENOB, 1 kS/s-260 kS/s pipelined SAR ADC in 0.35- μm CMOS where a 3-stage capacitive charge pump (CCP) is utilized to achieve the gain-stage. The unity-gain OTAs as the analog buffers are implemented in the 3-stage CCP gain-stage.
- Design of a 14-bit asynchronous two-stage pipelined SAR ADC in 0.18- μm CMOS. The proposed asynchronous clock generator provides a flexible clocking scheme which can dynamically and efficiently allocate the available time for the digital-to-analog converters (DACs), the comparators and the gain-stage.

To reduce the power consumption of the gain-stage, the source followers as the analog buffers are utilized in the 3-stage CCP gain-stage.

1.5 Thesis Organization

Chapter 2 provides the design considerations for the two-stage pipelined SAR ADC blocks. **Chapter 3** presents the design and implementation of a 12.8-bit ENOB, 1 kS/s pipelined SAR ADC. A detailed power analysis of two-stage pipelined SAR ADC and the gain-reduction method are performed to optimize the design. To reduce the high open-loop DC gain requirement of the OTA, **Chapter 4** describes the design and implementation of a two-stage pipelined SAR ADC with gain-stage which is based on the capacitive charge pump. **Chapter 5** presents the design of a 14-bit two-stage asynchronous pipelined SAR ADC in 0.18- μm CMOS. The conclusion and the future work are described in **Chapter 6**. Finally, **Appendix A** provides a copy of the published papers for a quick reference.

Chapter 2

Two-stage Pipelined SAR ADC Design Considerations

This chapter describes the basic two-stage pipelined SAR ADC and identifies the different limitations that affect the entire ADC performance. Design considerations for such ADC are discussed as well as the performance requirements of the crucial blocks.

2.1 Basic Two-stage Pipelined SAR ADC Architecture

The basic architecture of the two-stage pipelined SAR ADC is shown in Fig. 2-1 [26]. To simplify the description, a single-ended version is presented. It consists of two sub-SAR ADCs coupled by a gain-stage with a voltage gain of 2^{N_1-1} . The resolution of the first-stage and the second-stage sub-ADCs are N_1 -bit and N_2 -bit, respectively. As the first-stage has one bit redundancy [36], the total resolution of the ADC is given by $N = N_1 + N_2 - 1$. First, the input signal (V_{in}) is sampled by the switch S_0 and then the conversion starts from an approximation of the most-significant-bit (MSB). Based on the binary-search algorithm, the residue signal ($V_{res,in}$) is generated after N_1+1 steps conversion which can be expressed as

$$V_{res,in} = V_{in} - \left(\frac{V_{REF}}{2} D_{N_1-1} + \frac{V_{REF}}{2^2} D_{N_1-2} + \cdots + \frac{V_{REF}}{2^{N_1}} D_0 \right), \quad (2.1)$$

Figure 2-1: Diagram of basic two-stage pipelined SAR ADC architecture.

where V_{REF} represents the reference voltage of the capacitor array DAC. The maximum $V_{res,in}$ is one least-significant-bit (LSB) of N_1 -bit ADC which is

$$V_{res,in,max} = \frac{V_{REF}}{2^{N_1}}. \quad (2.2)$$

When the switch S_1 turns on, the residue signal is amplified by the gain-stage with a voltage gain of 2^{N_1-1} . Hence, the maximum output signal ($V_{res,out,max}$) is

$$V_{res,out,max} = \frac{V_{REF}}{2}. \quad (2.3)$$

This output signal from the gain-stage is sampled by the switch S_2 then the second SAR ADC starts the following conversion. The final digital codes can be achieved by combining two sub-ADCs' digital outputs. For the asynchronous ADC, the clock signals (clk_1, clk_2) for the sub-ADCs are generated by the on-chip clock generator. For the synchronous ADC, the clock signal is provided from an external functional generator.

From the above analysis, the entire ADC performance highly depends on the accuracy of the residue signal and the voltage gain of the gain-stage. To obtain the amplified output signal in Eq. (2.3), it is inevitable to minimize the error sources, such as mismatch error from the DAC and gain error from the gain-stage. The following sections provide the performance requirements of the key blocks in the two-stage pipelined SAR ADC and also the associated design challenges.

2.2 Capacitive DAC

2.2.1 Conventional Binary-weighted Capacitive DAC

The capacitive DAC in the first SAR ADC is used to generate the weighted reference voltages. Fig. 2-2 shows an N_1 -bit conventional binary-weighted capacitive array DAC. For the pipelined SAR ADC, although the resolution of the first-stage is N_1 -bit,

Figure 2-2: Conventional binary-weighted capacitive DAC.

the accuracy of the first DAC should satisfy N -bit resolution. In order to reduce the power consumption, the unit capacitor, denoted as C_{u1} , should be kept as small as possible. In practice, the choice of C_{u1} is usually determined by the thermal

Figure 2-3: Mismatch-limited C_{u1} versus N_1 .

noise and the capacitor mismatch. The mismatch-limited C_{u1} for the conventional binary-weighted array DAC is given by

$$C_{u1} > 4.5K_{\sigma}^2 K_c 2^{2(N-N_1)} (2^{N_1} - 1), \quad (2.4)$$

where K_σ is the mismatch parameter and K_c is the capacitor density. The detailed derivation of Eq. (2.4) is provided in Chapter 3. Fig. 2-3 shows the C_{u1} versus the first-stage resolution (N_1) under the assumption that $N=15$ -bit, $K_\sigma = 0.45\% \mu\text{m}$ and $K_c = 0.86 \text{ fF}/\mu\text{m}^2$. As shown in Fig. 2-3, a much larger unit capacitance is necessary for a smaller first-stage resolution to maintain the 15-bit linearity. For example, the minimum mismatch-limited unit capacitor is 652 fF with $N_1=7$ -bit whereas a 4.93 pF unit capacitor is needed for $N_1=4$.

2.2.2 Segmented Binary-weighted Capacitive DAC

The segmented binary-weighted capacitive DAC [37] aims to reduce the unit capacitor value without compromising linearity performance. Fig. 2-4 shows an N_1 -bit segmented array DAC. It is composed of a k -bit unary-weighted array and an $(N_1 - k)$ -bit

Figure 2-4: Segmented binary-weighted capacitive DAC.

binary-weighted array where k represents the segmented degree. As the number of capacitors to be switched during conversions is reduced in a segmented DAC, less voltage variation is caused by the capacitor mismatch. Hence, it reduces the unit capacitor value. The mismatch-limited C_{u1} for the segmented DAC can be expressed as

$$C_{u1} > 4.5K_\sigma^2 K_c 2^{2(N-N_1)} (2^{N_1-k+1} - 1). \quad (2.5)$$

The detailed derivation of Eq. (2.5) is provided in Chapter 3 as well. The ratio of the mismatch-limited unit capacitor for conventional binary-weighted DAC ($C_{u1,bw}$) and segmented DAC ($C_{u1,seg}$) can be written in terms of k as

$$\frac{C_{u1,bw}}{C_{u1,seg}} = 2^{k-1}. \quad (2.6)$$

It indicates that the C_{u1} is reduced 2^{k-1} times by using the segmented capacitive DAC. Assuming $k=3$, $N=15$ -bit, $N_1=7$ -bit, $K_\sigma = 0.45\% \mu\text{m}$ and $K_c = 0.86 \text{ fF}/\mu\text{m}^2$, the unit capacitor is 163 fF.

2.2.3 Split Binary-weighted Capacitive DAC

Eq. (2.4) also indicates that the capacitance increases exponentially with the resolution of the ADC. Therefore, it entails increased power consumption and chip area. A split binary-weighted capacitive DAC (Fig. 2-5) is used to reduce the total number of unit capacitors. It consists of a M -bit main-DAC and a S -bit sub-DAC, where

Figure 2-5: Split binary-weighted capacitive DAC.

$M + S = N_1$. The bridge capacitor C_B is given by

$$C_B = \frac{2^S}{2^{M-1}} C_{u1}, \quad (2.7)$$

which results in a total capacitance of $2^M C_{u1}$. Therefore, with the same C_{u1} , the number of the total capacitors is decreased by a factor of 2^S in comparison to the convention architecture. The mismatch-limited C_{u1} for this split-array DAC is expressed as

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N_1-M)} (2^M - 1). \quad (2.8)$$

Based on Eq. (2.8), the total capacitance of split-array DAC is written as

$$C_{tot,sp} > 4.5 K_\sigma^2 K_c 2^{2N_1-M} (2^M - 1). \quad (2.9)$$

Assuming $M = N_1$ in Eq. (2.9), then the $C_{tot,sp}$ represents the total capacitance of conventional binary-weighted DAC. Also, from Eq. (2.9), the $C_{tot,sp}$ is inversely proportional to M . Comparing with the conventional binary-weighted DAC, the split-array DAC requires a larger unit capacitance to satisfy the same linearity. However, the minimum value of the capacitor in the design-kit ($C_{u,proc}$) is another limitation. If the $C_{u,proc}$ is larger than the mismatch limited C_{u1} computed from Eq. (2.8), then $C_{u,proc}$ is chosen as the unit capacitor. In this case, the split-array DAC provides more benefits than conventional binary-weighted DAC.

2.3 Stage Resolution

Although the design of the first-stage DAC needs to satisfy N -bit resolution, the combination of the stage resolution (N_1, N_2) still affects the accuracy of the second-stage DAC and the noise requirement of the comparators in both sub-ADCs [38]. The unit capacitance of the second-stage DAC and the load of the comparator vary with the choice of stage resolution which in turn change the power consumption. Therefore, choosing a suitable combination of N_1 and N_2 can significantly optimize the ADC design.

For the basic two-stage pipelined SAR ADC as shown in Fig. 2-1, it consists of two-sub DACs, two comparators, two SAR logics and one OTA. Hence, the total power consumption can be written as

$$P_{total} = \sum_{i=1}^2 (P_{DAC.i} + P_{sar.i} + P_{com.i}) + P_{OTA}, \quad (2.10)$$

where $i=1,2$ represent the first and second sub-ADC. Referring the power analysis in [37] [39] [40], the power consumption of each part can be expressed as

$$P_{DAC.i} \approx 0.66 \cdot 2^{N_i} f_s C_{u.i} v_{ref}^2, \quad (2.11)$$

$$P_{sar.i} = 16 N_i \alpha f_{clk} C_{min} V_{dd}^2, \quad (2.12)$$

$$P_{com.i} = 2 \ln 2 \cdot N_i f_{clk} C_{LC.i} V_{FS} V_{eff} + 2 f_{clk} V_{FS}^2 C_{LC.i}, \quad (2.13)$$

$$P_{OTA} = 2 V_{FS}^2 f_s C_{LA} \left(1 + (1 + |G|) N \ln 2 \cdot \frac{V_{eff}}{V_{FS}} \right). \quad (2.14)$$

All the parameters utilized in the above equations are listed as follows.

N_i : The resolution of 1^{st} stage ADC and 2^{nd} stage ADC

f_s : Sampling frequency

f_{clk} : Clock frequency of the entire ADC

v_{ref} : Reference voltage of the DAC

v_{dd} : Supply voltage of the ADC

V_{eff} : Effective voltage of a transistor

V_{FS} : Full-scale range of the ADC

G : The close-loop voltage gain

α : Switching activity of the SAR logic

$C_{u,i}$: Unit capacitance of two-sub DACs, $i=1,2$

C_{min} : Input capacitance of a minimum-sized inverter

$C_{LC,i}$: Capacitive load of the two comparators, $i=1,2$

C_{LA} : Capacitive load of the OTA

In order to predict the power consumption bounds of the two-stage pipelined SAR ADC, the following typical CMOS parameters are used. In $0.35\text{-}\mu\text{m}$ CMOS process, the V_{eff} is 300 mV and $C_{min} = C_{pro} \approx 3$ fF [40]. For the first-stage, the mismatch-limited unit capacitor computed from Eq. (2.4) is chosen for the analysis

Figure 2-6: Predicted power bounds of 15-bit two-stage pipelined SAR ADC in $0.35\text{-}\mu\text{m}$ CMOS. (a) Mismatch-limited in stage 1 and stage 2. (b) Mismatch-limited in stage 1 and process-limited in stage 2 ($C_{pro} = 3$ fF).

because this value is always larger than the process-limited one for a 15-bit ADC design. For the second-stage, the mismatch-limited and process-limited $C_{u,2}$ are analyzed, respectively. With $T = 300\text{K}$ and $\alpha = 0.4$, we sweep the resolution of the first-stage N_1 in Eq. (2.10) to achieve the power bounds. Fig. 2-6 plots the predicted energy bounds of a 15-bit two-stage pipelined SAR ADC together with its individual

blocks. From Fig. 2-6, it is observed that choosing a large N_1 or N_2 will result in a large power consumption. An optimal stage resolution range can be found where less power is consumed. The total power is mainly dominated by the OTA if the C_{u2} is limited by the process, whereas the first-stage dominates the total power.

2.4 Gain-stage

2.4.1 DC Gain Requirement

The gain-stage is commonly used to amplify the residue signal with sufficient accuracy. Normally, the SC amplifier is the primary choice to realize the gain-stage and a high DC gain OTA is inevitable to provide a precise close-loop gain. Fig. 2-7 shows the

Figure 2-7: Switch capacitor amplifier and timing.

block diagram of the single-end switch capacitor amplifier [41] and its timing diagram. It consists of two capacitors (C_1 , C_f), one OTA and several switches. The finite DC gain of the OTA is A . Each switch is controlled by one of the two clock phases ϕ_1 and ϕ_2 . At phase ϕ_1 , the input signal $V_{res,in}$ is sampled onto the capacitor C_1 and the charge is

$$Q_1 = -V_{res,in}C_1 \quad (2.15)$$

At phase ϕ_2 , the switches (S_1 , S_4) are closed which result in the charge

$$Q_2 = -\frac{V_{res,out}}{A}C_1 + \left(-\frac{V_{res,out}}{A} - V_{res,out}\right)C_f \quad (2.16)$$

According to the charge conservation, the closed-loop gain is achieved by setting Q_2 in Eq. (2.16) equal to Q_1 in Eq. (2.15) which is

$$\frac{V_{res,out}}{V_{res,in}} = \frac{C_1}{C_f} \left(\frac{1}{1 + \frac{C_1+C_f}{AC_f}} \right) \quad (2.17)$$

Assuming $C_1 \gg C_f$, the Eq. (2.17) can be written as

$$\frac{V_{res,out}}{V_{res,in}} \approx \frac{C_1}{C_f} \left(1 - \frac{1}{A\beta} \right), \quad (2.18)$$

where the $\frac{1}{A\beta}$ represents the gain-error and feedback factor $\beta = \frac{C_f}{C_1}$. For an N -bit pipeline SAR ADC, the output voltage error of the gain-stage is required to be less than 1 LSB which is

$$\frac{V_{res,in}}{A\beta} < \frac{V_{REF}}{2^N}. \quad (2.19)$$

Substituting Eq. (2.2) into Eq. (2.19), the requirement of A is obtained as

$$A > \frac{2^{N-N_1}}{\beta}. \quad (2.20)$$

Without any form of inter-stage gain reduction, the $\beta = 2^{1-N_1}$ which results in

$$A > 2^{N-1}. \quad (2.21)$$

For a 15-bit ADC, the requirement of A is larger than 84.3 dB. Hence, a high-gain OTA is inevitable. Also, the maximum amplitude of the $V_{res,out}$ is $V_{REF}/2$ (Eq. (2.3)) which demands rail-to-rail output swing for the OTA. The design of an OTA with such specifications constitutes a formidable challenge. To alleviate the requirement of the OTA, Chapter 3 describes a gain reduction solution to reduce the high DC gain and the output swing for a 15-bit pipelined SAR ADC. Chapter 4 implements a 3-stage capacitive charge pump gain-stage for a 14-bit pipelined SAR ADC design.

2.4.2 Bandwidth Requirement

In Section 2.4.1, the DC gain requirement of the OTA shown in Fig. 2-7 is derived under the assumption that the OTA has sufficient bandwidth such that the gain error is limited only by the finite DC-gain. However, the settling time for the OTA is not infinite. In this section, the bandwidth requirement of the OTA is derived.

Assuming a first-order response of the OTA is

$$A(s) = \frac{A}{1 + \frac{s}{\omega_{3dB}}}, \quad (2.22)$$

where ω_{3dB} is the 3 dB bandwidth of the open-loop. Near the unity gain frequency (ω_u), the $A(s) \approx \frac{A\omega_{3dB}}{s}$ and $\omega_u = A\omega_{3dB}$ [42], thus the close-loop transfer function of Fig. 2-7 at the phase ϕ_2 is approximately written as

$$\frac{V_{res,out}}{V_{res,in}}(s) \approx \frac{C_1}{C_f} \left(\frac{1}{1 + \frac{s}{\omega_u\beta}} \right). \quad (2.23)$$

Hence the bandwidth of the close-loop, $\omega_{3dB,cl} = \omega_u\beta$. As the step response in the time domain of Fig. 2-7 can be expressed as

$$\frac{V_{res,out}}{V_{res,in}}(t) = \frac{C_1}{C_f} \left(1 - e^{-\frac{t}{\tau}} \right). \quad (2.24)$$

The relative error (Δ_{BW}) at the output of the gain-stage caused by the finite bandwidth is given by

$$\Delta_{BW} = e^{-\frac{t}{\tau}}, \quad (2.25)$$

where t is the settling time and the time-constant τ can be expressed as

$$\tau = \frac{1}{\omega_{3dB,cl}} = \frac{1}{2\pi f_u\beta}. \quad (2.26)$$

Here, we assume that a half clock cycle period of sampling frequency (f_s) is used for settling. For a two-stage pipelined SAR ADC with N_2 -bit second-stage, to achieve sufficient performance, we require

$$e^{-\frac{t_s}{2\tau}} < \frac{1}{2^{N_2}}. \quad (2.27)$$

Substituting Eq. (2.26) into Eq. (2.27) results in

$$f_u > \frac{N_2 \ln 2}{\pi \beta t_s}, \quad (2.28)$$

where the t_s is the period of f_s .

2.5 Sample-and-Hold Circuit

The sample-and-hold (S/H) circuit plays an important role in determining the performance of the pipelined SAR ADC. Fig. 2-8 shows the basic S/H circuit. It consists of a switch and a capacitor (C_s). During the tracking phase, the input voltage is connected to the top-plate of the capacitor. When the switch is off at the holding phase, the capacitor holds the sampled voltage. Ideally, the switch provides a constant on-resistance (R_{on}) during the tracking phase and a complete isolation during the holding phase. Thus, the S/H circuit will not degrade the entire ADC performance.

Figure 2-8: Basic sampling circuit.

However, in practice, the nonlinear variation of the R_{on} , charge injection and leakage generated by the switch directly affect the performance of the ADC.

2.5.1 Thermal Noise

The thermal noise, generated by the on-resistance of the switch, can be expressed as [43]

$$P_{n,out} = \frac{kT}{C_s}, \quad (2.29)$$

where k is the Boltzmann constant, T is the absolute temperature and C_s is the sampling capacitor. For an N -bit ADC, the quantization noise power is

$$P_Q = \frac{V_{FS}^2}{12 \cdot 2^{2N}}. \quad (2.30)$$

Normally, the C_s should be large enough so that the thermal noise is less than the quantization noise power of an N -bit ADC. Based on Eq. (2.29) and Eq. (2.30), the minimum value of C_s can be derived as

$$C_s = 12kT \frac{2^{2N}}{V_{FS}^2}. \quad (2.31)$$

2.5.2 Tracking Bandwidth

During the tracing phase, the switch is turned on and the S/H circuit forms a simple low-pass RC filter. For an N -bit ADC, the settling error at the output of the S/H circuit should be less than 1/2 LSB which can be expressed as

$$e^{\frac{-t_s}{\tau}} < \frac{1}{2^{N+1}}. \quad (2.32)$$

The time-constant τ is

$$\tau = \frac{1}{2\pi f_{3dB}}, \quad (2.33)$$

where f_{3dB} is the -3 dB bandwidth of the RC filter formed by the S/H circuit. A half period of sampling frequency (f_s) is assumed for settling. Substituting Eq. (2.33) into Eq. (2.32), the track bandwidth of the S/H circuit should satisfy

$$f_{3dB} > \frac{(N+1)\ln 2}{\pi} f_s. \quad (2.34)$$

Substituting Eq. (2.34) into Eq. (2.33), the upper-bound of R_{on} can be written as

$$R_{on} < \frac{1}{2\ln 2(N+1)f_s C_s}. \quad (2.35)$$

For a given value of C_s , a maximum R_{on} can be obtained to satisfy the targeted ADC performance.

2.5.3 Charge Injection and Clock Feedthrough

The channel charge injection and clock feedthrough are the errors generated by a metal-oxide-semiconductor (MOS) transistor sampling switch. Both errors are shown in Fig. 2-9. When the switch turns off, the total charge in the conduction channel (Q_{ch})

Figure 2-9: Charge injection and clock feedthrough errors of NMOS sampling switch.

exits through the source and drain terminals. The charge injected to the output node is stored on the C_s , introducing a voltage error. In addition to the charge injection error, the transistor couples the clock transitions to the C_s through the overlap capacitance of the gate-drain which introduces an error in the output voltage. The overall error voltages introduced to the output node for both NMOS and PMOS can be written

as [44]

$$\Delta V_{out,n} = -\frac{k(WL)_n C_{ox}(V_{DD} - V_{th,n} - V_{in})}{C_s} - \frac{C_{GD,n}}{C_s + C_{GD,n}} V_{DD}, \quad (2.36)$$

$$\Delta V_{out,p} = \frac{k(WL)_p C_{ox}(V_{in} - |V_{th,p}|)}{C_s} + \frac{C_{GD,p}}{C_s + C_{GD,p}} V_{DD}, \quad (2.37)$$

where k is the fraction of charge injected on the output node, C_{ox} is the gate-oxide capacitor, $V_{th,n}$, $V_{th,p}$ are the threshold voltages and $C_{GD,n}$, $C_{GD,p}$ are the gate-drain overlap capacitance of the NMOS and PMOS, respectively. In Eq. (2.36) and Eq. (2.37), the first part represents the charge injection error. As the $V_{th,n}$ and $V_{th,p}$ are a nonlinear function of the input signal, the charge injection introduces nonlinearity. The second part represents the clock feedthrough error which is independent of the input signal, manifesting itself as a constant offset error.

2.5.4 Impact of Leakage

Although the sampling switch turns off during the bit conversion cycles in the sub-SAR ADC, the subthreshold leakage current of the transistor causes the sampled voltage to droop. The subthreshold current can be expressed as [45]

$$I_{DS} = \mu_0 C_{ox} \frac{W}{L} (m-1) V_T^2 e^{\frac{V_{GS}-V_{th}}{m V_T}} (1 - e^{-\frac{V_{DS}}{V_T}}), \quad (2.38)$$

where m is the subthreshold swing coefficient, V_{th} is the threshold voltage, $V_T = kT/q$ is the thermal voltage, C_{ox} is the gate oxide capacitance and μ_0 is the zero bias mobility. Eq. (2.38) indicates that the sub-threshold leakage current depends on the voltage across the switch (V_{DS}) and further introduces harmonic distortion at the output of the ADC [46]. Leakage reduction can be achieved by using a stack of series-connected transistors [44], implementation of high- V_{th} transistors [47], negative body bias [48], negative gate bias [49] or a combination of these solutions.

2.6 Clock Generator

The clock generator shown in Fig. 2-1 is used to generate the clock signal for the asynchronous ADC. It is triggered by an external low-speed pulse and further creates the system clock frequency. Such clock generator is usually a delay-line based circuit and the period of the clock signal depends on the delay. Normally, the delay is generated by an inverter chain [50]. Fig. 2-10 shows a single CMOS inverter. Here, all the parasitic capacitances are lumped together in one single capacitor C_L . The

propagation delay can be express as [51]

$$t_p \approx \frac{C_L}{2V_{DD}} \left(\frac{1}{k_p} + \frac{1}{k_n} \right), \quad (2.39)$$

where $k_p = k'_p \frac{W_p}{L_p}$ and $k_n = k'_n \frac{W_n}{L_n}$ represent the gain factor of PMOS and NMOS, respectively. The k'_p and k'_n are the process transconductance parameter. In 0.35- μm CMOS, the $k'_p = 58 \mu\text{A}/\text{V}^2$ and $k'_n = 170 \mu\text{A}/\text{V}^2$ [52]. In order to find the propagation delay of a single inverter, we assume that the $V_{DD} = 3.3 \text{ V}$, $C_L = 10 \text{ fF}$ and the transistors M1 and M2 shown in Fig. 2-10 are sized with $1 \mu/0.35 \mu$ and $0.4 \mu/0.35 \mu$, respectively. The propagation delay computed from Eq. (2.39) is 35 ps.

Figure 2-10: CMOS inverter.

For the high-speed application, the propagation delay is required to be as low as possible. However, when it comes to low-speed design, a longer delay is needed. From Eq. (2.39), the longer delay can be achieved by increasing C_L , reducing k_p , k_n or equivalently reducing the W/L ratio of the transistors. Furthermore, a chain of inverters can significantly increase the delay. In [26, 53–55], targeted 50 MS/s ADC design, several hundred picoseconds delay is achieved by using the delay buffer chain. However, such delay is still not long enough for an ADC targeting at several kS/s. Definitely, a longer chain can be implemented to achieve several microseconds, but this is at the cost of consuming substantial power and area. Moreover, the process corners, voltage and temperature variations have great impacts on the delay [50] which makes it difficult for the DAC to settle. Aiming to generate several microseconds delay, the RC delay element is described in Chapter 6.

2.7 Summary

This chapter describes the design considerations of the two-stage pipelined SAR ADC. In order to achieve the desired resolution of the ADC, the performance requirements of the key blocks were elaborated upon. The characteristics of three different capacitive array DAC topologies were discussed. Stage resolution was analyzed in terms of power consumption. The DC gain and bandwidth requirements of the OTA were explained. Additionally, the design challenge of the clock generator for the low-speed asynchronous ADC was also presented.

Chapter 3

A 12.8 ENOB, 1 kS/s Pipelined SAR ADC in 0.35- μ m CMOS

In this chapter, a 15-bit, two-stage pipelined SAR ADC is presented. The use of aggressive gain reduction in the residue amplifier combined with a suitable capacitive array DAC topology in the second-stage simplifies the design of the OTA while eliminating excessive capacitive load and consequent power consumption. A comprehensive power consumption analysis of the entire ADC is performed to determine the number of bits in each stage of the pipeline. By choosing a segmented capacitive array DAC and attenuation capacitor-based DAC for the first and second stages, the power consumption and area are significantly reduced.

3.1 Introduction

To achieve a two-stage pipelined SAR ADC, a SC amplifier as the gain-stage is inevitable to amplify the residue signal with desired accuracy [56]. Since the open-loop DC gain requirement of the OTA increases exponentially with the total resolution of the ADC, it is hard to design an OTA for implementing high-resolution pipelined SAR ADC. Several works have employed inter-stage gain reduction in the pipelined SAR ADC to relax the requirements on the DC gain and output swing of the residue amplifier. Gain reduction also increases the feedback factor of the amplifier and thus improves the closed-loop bandwidth [26]. In [26], a gain reduction factor of 1/2 has been used. Higher gain reduction factors will require increased resolution/sampling capacitance for the second-stage sub-ADC to compensate for the reduced signal swing [27]. In this work, a gain reduction factor of 1/8 has been used for the residue amplifier. The increased capacitance requirement in the second-stage has been alleviated by choosing a binary-weighted capacitive DAC with attenuation capacitor. In

high-resolution SAR ADCs, matching constraints necessitate large unit capacitor in the capacitive array [57] which entails substantial power consumption and chip area. A segmented capacitive array DAC [58, 59] has been used in the first-stage which meets the targeted static linearity with a lower unit capacitance compared to a conventional binary-weighted capacitive DAC. By choosing the proper number of bits for segmentation, the power consumption due to the binary-to-thermometer decoder has been kept low. Based on an exhaustive analysis of the power consumption of the different sub-blocks of a 15-bit pipelined SAR ADC, 7-bit and 9-bit are allocated to the first and second pipeline stages respectively which provide a good trade-off between implementation complexity and power saving. The prototype ADC achieves a peak ENOB of 12.8-bit while consuming $6.7 \mu\text{W}$ at a sampling frequency of 1 kS/s.

This chapter is organized as follows. Section 3.2 provides an overview of the two-stage pipelined SAR ADC architecture. Section 3.3 describes the important features of the proposed ADC architecture. Section 3.4 discussed the implementation details of the ADC while Section 3.5 presents the measurement results. Finally, the conclusions are drawn in Section 3.6.

3.2 Overview of the Two-stage Pipelined SAR ADC

The general single-ended architecture of the two-stage pipelined SAR ADC is shown in Fig. 3-1 [26]. The resolutions for the first-stage and second-stage sub-ADCs are N_1 -bit and N_2 -bit respectively. An OTA with capacitive feedback implements the

Figure 3-1: Two-stage pipelined SAR ADC architecture.

residue amplification between the pipeline stages. Because the first-stage has one bit redundancy [36], the total resolution of the ADC is given by $N = N_1 + N_2 - 1$. Since the open-loop DC gain of the OTA grows exponentially with N , a very large DC gain is required for high-resolution pipelined ADCs [27, 60, 61].

Fig. 3-2 shows the time sequence of the two-stage pipelined SAR ADC, where f_s is the sampling frequency of the first-stage and f_r is the sampling frequency of the

second-stage. The input signal V_{in} is sampled by switch S_0 during phase f_s . During phase f_r , the switches S_1 and S_2 are turned on and the residue voltage from the first-stage is amplified and sampled by the second-stage sub-ADC. To increase the settling time available for input sampling and residue generation, the duration t_p for the phases f_s and f_r is set to $2/f_{clk}$ where f_{clk} is the system clock frequency of the pipelined SAR ADC [36]. The time interval for determining each output bit is $1/f_{clk}$. For odd N , the clock frequency can be derived as

Figure 3-2: Time sequence of the two-stage pipelined SAR ADC.

$$f_{clk} = \begin{cases} (N_1 + 2t_p + 1)f_s & N_1 \geq N_2 \\ (N_2 + t_p + 1)f_s & N_1 = N_2 - 2 \\ (N_2 + t_p)f_s & N_1 < N_2 \end{cases} \quad (3.1)$$

If the total resolution N is even, then the clock frequency can be derived as

$$f_{clk} = \begin{cases} (N_1 + 2t_p + 1)f_s & N_1 > N_2 \\ (N_2 + t_p + 2)f_s & N_1 = N_2 - 1 \\ (N_2 + t_p)f_s & N_1 < N_2 \end{cases} \quad (3.2)$$

It should be mentioned that the first-stage sub-ADC requires $N_1 + 1$ clock cycles to convert the N_1 -bit and form the residue.

3.3 Features of the Proposed ADC

Fig. 3-3 shows the circuit details of the proposed ADC architecture. A single-ended version is shown for clarity while the actual implementation is fully differential. This section motivates the important design choices for the ADC implementation along with the relevant analyses. Selection of DAC topologies for the SAR stages, gain reduction in the residue amplifier and allocation of stage resolution are described.

3.3.1 First-stage DAC Topology

The static linearity of the first-stage SAR ADC shown in Fig. 3-3 is dominated by capacitor mismatch in the corresponding capacitive array DAC. For the conventional binary-weighted capacitive DAC, the maximum error caused by mismatch of capacitors occurs during the most significant bit (MSB) code transition from ‘011...1’ to ‘100...0’ where all the capacitors switch states [62]. The worst-case standard deviation of the differential nonlinearity (DNL) for the N_1 bit first-stage DAC is given by [62]

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1}-1}}{2^{N_1}} \frac{\sigma_{C_{u1}}}{C_{u1}} V_{REF}, \quad (3.3)$$

where $\sigma_{C_{u1}}$ is the standard deviation and C_{u1} is the mismatch-limited unit capacitor of the sub-DAC. For the pipelined SAR ADC, although the resolution of the first-stage is N_1 , the accuracy for the first-stage must meet the total resolution N which requires

$$3\sigma_{DNL,max} < \frac{V_{REF}}{2^N}, \quad (3.4)$$

where $V_{REF}/2^N$ is the least significant bit (LSB) of the N -bit ADC. Combining Eq. (3.3) and Eq. (3.4), we get

$$\frac{\sigma_{C_{u1}}}{C_{u1}} < \frac{1}{3 \cdot 2^{N-N_1} \cdot \sqrt{2^{N_1}-1}}. \quad (3.5)$$

Following the derivation in [63], the $\sigma_{C_{u1}}/C_{u1}$ can be expressed as

$$\frac{\sigma_{C_{u1}}}{C_{u1}} = \frac{K_\sigma}{\sqrt{2A}}, \quad C_{u1} = K_c \cdot A, \quad (3.6)$$

where A is the capacitor area, K_σ is the mismatch parameter and K_c is the capacitor density. Substituting Eq. (3.6) into Eq. (3.5), the mismatch-limited unit capacitor of the first-stage DAC can be derived as

$$C_{u1} > 4.5 K_\sigma^2 K_c 2^{2(N-N_1)} (2^{N_1} - 1). \quad (3.7)$$

Utilizing Eq. (3.3) and Eq. (3.6), $\sigma_{DNL,max}$ for the conventional binary-weighted capacitive DAC can be formulated as

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1}-1}}{2^{N_1}} \frac{K_\sigma \sqrt{K_c}}{\sqrt{2C_{u1}}} V_{REF}. \quad (3.8)$$

For the poly-insulator-poly (PIP) capacitor in 0.35- μm CMOS process, $K_\sigma = 0.45\%$ and $K_c = 0.86 \text{ fF}/\mu\text{m}^2$. For a 15-bit two-stage pipelined SAR ADC, if a conventional binary-weighted DAC with $N_1=7$ -bit was implemented into the

first-stage, the minimum mismatch-limited unit PIP capacitor computed from Eq. (3.7) is 652 fF which results in a total capacitance of 83.4 pF. The reason for choosing $N_1 = 7$ -bit will be explained in Section 3.3.3.4.

It is desirable to lower the total capacitance of the DAC array to avail power and area savings. The required value of the mismatch-limited unit capacitor can be lowered without compromising linearity performance by using a segmented capacitive array DAC in the first-stage. Since the number of capacitors to be switched during conversions is reduced in a segmented DAC, less voltage variation is caused by capacitor mismatch. The segmented first-stage DAC is composed of a k -bit unary-weighted array and an $(N_1 - k)$ -bit binary-weighted array where the k -bit correspond to the MSBs of the array. The value of each capacitor in the unary-weighted array is $2^{N_1-k}C_{u1}$. The worst-case standard deviation of the DNL can be found as [62]

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1-k+1} - 1}}{2^{N_1}} \frac{\sigma_{C_{u1}}}{C_{u1}} V_{REF}. \quad (3.9)$$

Substituting Eq. (3.6) into Eq. (3.9), $\sigma_{DNL,max}$ for the segmented binary-weighted

Figure 3-4: $3\sigma_{DNL,max}$ versus C_{u1} .

capacitive DAC can be formulated as

$$\sigma_{DNL,max} \approx \frac{\sqrt{2^{N_1-k+1} - 1}}{2^{N_1}} \frac{K_\sigma \sqrt{K_c}}{\sqrt{2C_{u1}}} V_{REF}. \quad (3.10)$$

Comparing Eq. (3.8) and Eq. (3.10), it is seen that the $\sigma_{DNL,max}$ for the segmented

DAC is $\sqrt{2^{k-1}}$ times lower than that of the conventional binary-weighted DAC. Using the same derivation procedure as for Eq. (3.7), the mismatch-limited unit capacitor for the first-stage segmented DAC can be obtained as

$$C_{u1} > 4.5K_{\sigma}^2 K_c 2^{2(N-N_1)} (2^{N_1-k+1} - 1), \quad (3.11)$$

which is 2^{k-1} times lower than the C_{u1} for the conventional binary-weighted DAC. It should be mentioned that the segmented DAC requires a binary-to-thermometer decoder and additional switches which lead to extra power consumption and chip area. Therefore, an excessive degree of segmentation will outweigh the benefits of reduced DAC capacitance. In this work, a segmentation degree of $k = 3$ was chosen for the first-stage DAC as a trade-off between lower unit capacitance value and increased complexity/power consumption in the digital logic. Fig. 3-4 plots $3\sigma_{DNL,max}$ versus C_{u1} from Eq. (3.8) and Eq. (3.10) with $V_{REF} = 3.3$ V together with Monte Carlo simulations for the segmented DAC using PIP capacitors. Monte Carlo simulations involved 100 runs simulating the worst-case DAC switching scenario for each C_{u1} value. For the 15-bit ADC with $V_{REF} = 3.3$ V, $LSB = 100.7 \mu V$. It is seen from Fig. 3-4 that the segmented DAC requires only $C_{u1} = 159$ fF compared to $C_{u1} = 652$ fF for the conventional DAC to satisfy the condition in Eq. (3.4). The corresponding total capacitance of the segmented first-stage DAC is 20.35 pF.

Since the DAC array capacitance of the first-stage is used for sampling the inputs of the ADC, the kT/C noise of the sampling switches also imposes a restriction on the minimum value of the unit capacitance. For the first-stage of the pipelined SAR ADC, the thermal noise from the sampling switches should be below the quantization noise of the 15-bit ADC. From [39], the thermal-noise limited unit capacitance is computed as

$$C_{u1,n} = 12kT \frac{2^{2N-N_1}}{V_{FS}^2} \quad (3.12)$$

where k is the Boltzmann constant, T is the absolute temperature and V_{FS} is the full-scale range of the ADC. For $N = 15$, $N_1 = 7$, $T = 300$ K and $V_{FS} = 3.3$ V, $C_{u1,n} = 38$ fF which is significantly lower than the mismatch-limited C_{u1} . Apart from mismatch and noise, the technology process also sets a lower limit on the unit capacitance through minimum feature sizes. The final value of unit capacitance is chosen as $\max(C_{u1}, C_{u1,n}, C_{pro})$, where C_{pro} is the process-limited unit capacitor. In this work, the mismatch-limited C_{u1} sets the unit capacitance in the first-stage DAC.

3.3.2 Gain Reduction and Second-stage DAC Topology

An OTA with capacitive feedback implements the residue amplifier as shown in Fig. 3-3. The error in the amplified residue due to the finite DC gain of the OTA must be less than 1 LSB of the N -bit pipeline ADC. The requirement of the open-loop DC

gain (A) has been derived in Section 2.4.1. For ease of reference, we copy Eq. 2.20 to here which is

$$A > \frac{2^{N-N_1}}{\beta}. \quad (3.13)$$

Without any form of inter-stage gain reduction, the feedback factor (β) is 2^{1-N_1} which results in $A > 2^{N-1}$. Thus, the 15-bit ADC without gain reduction will require $A > 84.3$ dB. Allocating a 6 dB margin to maintain performance over process, supply voltage, and temperature (PVT) variations leads to $A > 90$ dB. Also the maximum amplitude of the amplified residue will be $V_{REF}/2$ which demands rail-to-rail output swing for the OTA. Since the design of an OTA with such specifications constitutes a formidable challenge, gain reduction has been employed in the residue amplifier to relax the OTA specifications.

Figure 3-5: Open-loop DC gain of OTA versus N with different reduction factor (r).

To effect gain reduction, the C_f shown in Fig. 3-3 was chosen of $2^r C_{u1}$, where r represents the reduction factor. As the $\beta \approx \frac{C_f}{C_{tot}}$ where the C_{tot} is the total capacitance of the first-stage DAC ($2^{N_1} C_{u1}$), the feedback factor $\beta \approx 2^{r-N_1}$. Consequently

$$A > 2^{N-r}. \quad (3.14)$$

Thus, the DC gain requirement for the OTA is reduced by 2^{r-1} times. Fig. 3-5 shows the estimation results of A with different N and r . It is clear to see that a larger r results in a lower DC gain. However, the signal swing at the input of the second-stage SAR ADC in Fig. 3-3 is proportionately reduced. Maintaining the same SNR for the second-stage ADC requires sufficient lowering of the noise floor.

The output voltage of a two-stage pipelined ADC (V_{pip}) with 1-bit redundancy in

the first-stage is given by

$$\begin{aligned}
 V_{pip} &= \frac{V_{REF}}{2^{N_1} C_{u1}} \sum_{i=0}^{N_1-1} 2^i C_{u1} D_i + \frac{1}{G} \left(\frac{V_{REF}}{2^{N_2} C_{u2}} \sum_{i=0}^{N_2-2} 2^i C_{u2} D_i \right) \\
 &= \frac{V_{REF}}{2} D_{N_1-1} + \dots + \frac{V_{REF}}{2^{N_1}} D_0 + \frac{1}{2^{N_1-1}} \\
 &\quad \left(\frac{V_{REF}}{2^2} D_{N_2-2} + \dots + \frac{V_{REF}}{2^{N_2}} D_0 \right), \tag{3.15}
 \end{aligned}$$

where the inter-stage gain $G = 2^{N_1-1}$ and C_{u2} is the unit capacitance of the second-stage DAC. When gain reduction with $C_f = 2^r C_{u1}$ is applied, the output voltage becomes

$$\begin{aligned}
 V_{pip} &= \frac{V_{REF}}{2^{N_1} C_{u1}} \sum_{i=0}^{N_1-1} 2^i C_{u1} D_i + \frac{1}{G} \left(\frac{V_{REF}}{2^{N_2} C_{u2}} \sum_{i=0}^{N_2-2} 2^i C_{u2} D_i \right) \\
 &= \frac{V_{REF}}{2} D_{N_1-1} + \dots + \frac{V_{REF}}{2^{N_1}} D_0 + \frac{1}{2^{N_1-r}} \\
 &\quad \left(\frac{V_{REF}}{2^2} D_{N_2-2} + \dots + \frac{V_{REF}}{2^{N_2}} D_0 \right), \tag{3.16}
 \end{aligned}$$

where the inter-stage gain $G = 2^{N_1-r}$. By comparing Eq. (3.16) and Eq. (3.15), it is evident that the total capacitance of the second-stage SAR ADC has to be increased 2^{r-1} times in order to obtain the same output voltage. The resulting total capacitance required in the second-stage is

$$C_{total} = 2^{r-1} \cdot 2^{N_2} C_{u2}. \tag{3.17}$$

where the $2^{N_2} C_{u2}$ is the original total capacitance of the conventional binary-weighted DAC. An extra capacitor C_x has been added as shown in Fig. 3-3 to satisfy the total capacitance requirement. Hence inter-stage gain reduction involves a trade-off between relaxed OTA specifications and increased capacitance in the second-stage. In this work, $r = 3$ has been chosen which provides a lower DC gain requirement $A > 72.2$ dB for the OTA and reduces output swing to $V_{REF}/8$ which corresponds to a differential output swing of 0.825 V pp. The design of the OTA is thus considerably simplified.

The choice of $r = 3$ entails a four-fold increase in the second-stage input capacitance as seen from Eq. (3.17). The N_2 -bit second-stage sub-ADC requires $3\sigma_{DNL,max} < V_{REF}/2^{N_2}$ to satisfy the linearity requirement. Utilizing a procedure similar to the derivation of Eq. (3.7), C_{u2} for a conventional binary-weighted DAC is obtained as

$$C_{u2} > 4.5 K_\sigma^2 K_c (2^{N_2} - 1). \tag{3.18}$$

A binary-weighted DAC with attenuation capacitor consisting of an M -bit main-DAC and S -bit sub-DAC as shown in Fig. 3-3 where $M + S = N_2$ has been implemented in this work to mitigate the total capacitance requirement in the DAC. For the second-stage DAC, $N_2 = 9$, $M = 5$ and $S = 4$ results in a total effective capacitance of

$$C_{total} = 2^{r-1} \cdot 2^M C_{u2}. \quad (3.19)$$

The mismatch-limited unit capacitance for the attenuation capacitor based DAC is given by [64]

$$C_{u2} > 4.5 K_\sigma^2 K_e 2^{2(N_2-M)} (2^M - 1). \quad (3.20)$$

It can be clearly seen from Eq. (3.18) and Eq. (3.20) that the attenuation-based DAC imposes a large C_{u2} value. However the C_{u2} values from Eq. (3.18) and Eq. (3.20) are much lower than the process-limited minimum PIP capacitor. Hence a C_{u2} value which is adequately larger than the process-limited capacitor has to be used in both the DACs. Comparing Eq. (3.17) and Eq. (3.19) and using the same C_{u2} value, it is found that the attenuation-based DAC reduces the total capacitance of the second-stage DAC by a factor of 1/16. Finally the extra capacitor used is given by

$$C_x = (2^{r-1} - 1) \cdot 2^M C_{u2}. \quad (3.21)$$

3.3.3 Analysis of the ADC Power Consumption

For the low sampling rate SAR ADCs, a substantial portion of the total power is consumed by the capacitive DAC [63, 65]. Proper choice of unit capacitance and DAC topology is crucial for minimizing the power consumption in SAR ADCs. For the 15-bit pipelined SAR ADC, the resolutions N_1 and N_2 for the first and second stage sub-ADCs have been determined with the aid of power consumption analysis for the entire ADC. The choice of the segmentation degree k in the second-stage ADC is also elaborated upon in this section.

3.3.3.1 DACs in the Pipeline Stages

The DAC power consumption is proportional to the total capacitance. The first-stage ADC utilizes a segmented DAC which achieves the targeted DNL performance using a lower unit capacitance as discussed in Section 3.3.1. The average power consumption of the segmented N_1 -bit DAC with a unary-weighted segment of k MSBs and N_1-k binary-weighted LSBs is given by [37] as

$$P_{DAC_seg} \approx 0.66 \cdot 2^{N_1} f_s C_{u1} V_{REF}^2 \cdot (0.6 + 0.4(\frac{1}{2})^{k-1}), \quad (3.22)$$

where C_{u1} is the unit capacitor of the first-stage. In the second-stage, a binary-weighted capacitive DAC with attenuation capacitor has been employed to mitigate the increased capacitance requirement due to gain reduction as shown in Section 3.3.2.

The power consumption of the attenuation capacitor based DAC is computed as the sum of the power consumption of the M -bit main DAC and S -bit sub-DAC. Following the analysis in [66], the power consumption of the attenuation capacitor based DAC is given by

$$P_{DAC_att} = P_{1,main_DAC} + P_{sub_DAC}, \quad (3.23)$$

where

$$P_{1,main_DAC} \approx 2^M f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{M-1} \frac{D_i}{2^i} \right)^2 \right) \quad (3.24)$$

$$P_{sub_DAC} \approx 2^S f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{S-1} \frac{D_{M+i}}{2^i} \right)^2 \right). \quad (3.25)$$

Since an additional capacitor C_x given by Eq. (3.21) is required to maintain the same SNR, the power consumption of the DAC needs to be modified accordingly. The charge on the DAC capacitors varies according to the DAC output voltage V_{DAC_i} where V_{DAC_i} is given by

$$V_{DAC_i} = \frac{\sum_{i=1}^{M-1} 2^i C_{u2} D_i}{C_{total}} V_{REF}. \quad (3.26)$$

For the M -bit main-DAC, the total capacitance is increased to $C_{M_total} = 2^{M+r-1} C_{u2}$ which means that V_{DAC_i} of the main DAC is reduced by 2^{r-1} times. Hence the power consumption for the main DAC is

$$P_{2,main_DAC} \approx 2^M f_s C_{u2} V_{REF}^2 \cdot \left(\frac{5}{6} - \frac{1}{2} \left(\sum_{i=1}^{M-1} \frac{D_i}{2^i} \right)^2 \right) \frac{1}{2^{r-1}}. \quad (3.27)$$

It should be pointed out that the additional power introduced by the C_x has been included in Eq. (3.27). When it comes to the sub-DAC, the total capacitance is given by

$$C_{S_total} = 2^S C_{u2} + C_{S0}, \quad (3.28)$$

where C_{S0} represents the total capacitance from the main-DAC which is expressed as

$$C_{S0} = C_a || (2^{M+r-1} - 1) C_{u2}. \quad (3.29)$$

where the $C_a = \frac{2^S}{2^{M-1}} C_{u2}$ is the attenuation capacitor. With larger capacitance in the main DAC, C_{S0} is more close to C_a which indicates that the total capacitance of the sub-DAC is not affected due to the addition of C_x . However, the output voltage

of the sub-DAC is reduced by 2^{r-1} times which results in the $(2^{r-1})^2$ times power reduction of the sub-DAC. Thus, the total power consumption of the attenuation DAC with C_x is given by

$$P_{DAC.att} = P_{2,main.DAC} + P_{sub.DAC} \frac{1}{(2^{r-1})^2}. \quad (3.30)$$

According to the analysis in [66], a simplified expression of Eq. (3.30) can be written as

$$P_{DAC.att} \approx 0.66 \cdot f_s C_{u2} V_{REF}^2 \frac{1}{2^{r-1}} (2^M + \frac{2^S}{2^{r-1}}). \quad (3.31)$$

3.3.3.2 OTA and Dynamic Comparator

The OTA amplifies the residue signal for conversion in the second pipeline stage. Following the analysis in [40], the power consumption of the OTA can be expressed as

$$P_{ota} = 2V_{FS}^2 f_s C_{LA} (1 + (1 + |G|) N \ln 2 \cdot \frac{V_{eff}}{V_{FS}}), \quad (3.32)$$

where C_{LA} is the capacitive load of the OTA, V_{FS} is the full-scale range of the ADC and $G = 2^{N_1-r}$ is the closed-loop voltage gain. For a classical MOS transistor in strong inversion, the parameter $V_{eff} = (V_{gs} - V_T)/2$, where V_{gs} and V_T are the gate-to-source and threshold voltages respectively [40]. Because the amplifier operates only during the sampling phase of the second-stage, the OTA load capacitance can be approximated to the total capacitance of the second-stage DAC which means that the additional C_x will increase the power consumption of the OTA.

The dynamic latch comparator is used in the first and second stage SAR ADCs. It only consumes dynamic power during the reset and regeneration phases. Normally, the duty cycle of the clock signal is 50%. So, the reset and regeneration time are the same ideally. As shown in [40], the power consumption for the regeneration phase can be derived as

$$P_{c,reg.i} = 2 \ln 2 \cdot N_i f_{clk} C_{LC.i} V_{FS} V_{eff} \quad i = 1, 2, \quad (3.33)$$

where i is the stage number and $C_{LC.i}$ is the capacitive load of the comparator which is determined by the thermal noise. For the reset phase, it is a process of discharge. We assume that the voltage drops from V_{FS} to 0. The power consumption for the reset phase can be derived as

$$P_{c,rst.i} = 2 f_{clk} V_{FS}^2 C_{LC.i} \quad i = 1, 2. \quad (3.34)$$

So the total power consumption for the dynamic latch comparator is

$$\begin{aligned}
 P_{c,tot,i} &= P_{c,reg,i} + P_{c,rst,i} \\
 &= 2 \ln 2 \cdot N_i f_{clk} C_{LC,i} V_{FS} V_{eff} + 2 f_{clk} V_{FS}^2 C_{LC,i} \\
 &\quad i = 1, 2 \quad . \quad (3.35)
 \end{aligned}$$

3.3.3.3 Digital Blocks

The conventional method to build the SAR logic is to use D-type Flip Flops (DFF). Based on the analysis provided in [39], the power consumption of the synchronous SAR logic in each pipeline stage can be expressed as

$$P_{sar,i} = 16 N_i \alpha f_{clk} C_{min} V_{DD}^2 \quad i = 1, 2, \quad (3.36)$$

where C_{min} is the input parasitic capacitor of a minimum-sized inverter, V_{DD} is the supply voltage, and α represents the total switching activity of the SAR logic.

A binary-to-thermometer decoder is required for implementing the segmented DAC. The power consumption for a k -bit decoder is given by [37]

$$P_{dec} \approx 6 \alpha 2^k f_{clk} C_{min} V_{DD}^2. \quad (3.37)$$

3.3.3.4 Power Consumption of the Pipelined SAR ADC

Figure 3-6: Predicted power bounds for the 15-bit pipelined SAR ADC.

Ignoring the power consumption of the switches and the leakage currents, the total power consumption is found using Eq. (3.22), Eq. (3.31), Eq. (3.32), Eq. (3.35),

Eq. (3.36), and Eq. (3.37) as

$$P_{total} = P_{DAC_{seg}} + P_{DAC_{att}} + P_{ota} + P_{dec} + \sum_{i=1}^2 (P_{sar,i} + P_{c,tot,i}). \quad (3.38)$$

In order to predict the power consumption bound for the two-stage pipelined SAR ADC, the following typical CMOS parameters are used. For 0.35- μm CMOS, $V_{eff} = 300$ mV and $C_{min} = C_{pro} = 3$ fF [40]. For the first-stage, the mismatch-limited PIP capacitor given by (3.11) is used for the analysis. With $T=300$ K, $k=3$, $m=3$, $\alpha=0.4$ and $V_{DD} = V_{REF} = V_{FS} = 3.3$ V, Fig. 3-6 plots the total ADC power given by (3.38) as a function of the first-stage resolution N_1 for three different scenarios of the second-stage unit capacitor C_{u2} . The mismatch-limited power bound in Fig. 3-6 is of little use when $N_1 > 6$ -bit because the mismatch-limited C_{u2} is smaller than the process-limited capacitor as illustrated in Section 3.3.2. In contrast, the mismatch-limited C_{u2} dominates the power consumption for $N_1 < 6$ -bit. In this work, the ADC is pipelined with $N_1 = 7$ -bit and $N_2 = 9$ -bit as a compromise between lower power consumption and increased complexity in the second-stage sub-ADC.

Figure 3-7: OTA energy consumption versus inter-stage gain reduction factor.

As per the discussion in Section 3.3.2, it is necessary to make a trade-off between the inter-stage gain reduction factor m and the increased capacitance in the second-stage sub-ADC. Fig. 3-7 shows the OTA power consumption according to (3.32) as a function of r . The value of C_{LA} is given by (3.19) where $C_{u2} = 3$ fF, the process-limited unit capacitance and $M = 5$. Based on Fig. 3-7, $r = 3$ has been

chosen which considerably relaxes the OTA specifications without entailing excessive power consumption due to the increased capacitive load.

In order to find the optimal degree of segmentation k for the first-stage DAC, the power consumption of the segmented DAC, associated decoder and first-stage SAR logic was analyzed as a function of k . For this purpose, expressions in (3.22), (3.37) and (3.36) were used with the aforementioned values for the constituent parameters and $N_1 = 7$. The results are shown in Fig. 3-8. The total power in Fig. 3-8 is computed as the sum of Eq. (3.22), Eq. (3.36) and Eq. (3.37). It is seen that choosing $k \leq 2$ or $k > 5$ increases the total power consumption of the sub-ADC. As a compromise $k = 3$ was chosen.

Figure 3-8: Energy consumption of segmented SAR ADC versus k .

3.4 Implementation Details

3.4.1 First-stage sub-ADC

Based on the analysis in Section 3.3.3.4, the first pipeline stage has a resolution of 7-bit and utilizes a segmented DAC [58] with $k = 3$. Incorporating some design margin for the unit capacitor $C_{u1} = 159$ computed using Fig. 3-4, a PIP capacitor with the value of 212 fF was used to design the segmented DAC resulting in a total capacitance of 27 pF for the first-stage.

The block diagram of the SAR control logic [67] for the first-stage sub-ADC consisting of two separate shift registers is illustrated in Fig. 3-9. The upper DFF chain is triggered by a “set” signal which subsequently generates the switch control

signals (D14 $\cdots$ D8) for the DAC. Seven DFFs in the upper row generate the bit approximation pulses while the DFFs in the lower row store the output C_{out} of the comparator. The additional four DFFs on the far right side of Fig. 3-9 generate the sampling signals f_s and f_r , as shown in Fig. 3-2 for the first-stage and second-stage respectively. Fig. 3-10 shows the schematic of the 3-to-7 binary-to-thermometer

Figure 3-9: SAR control logic.

decoder required for the unary-weighted 3-bit DAC segment which consists of basic logic gates.

Figure 3-10: 3-to-7 binary to unary thermometer decoder.

For the input sampling switch S_0 in Fig. 3-3, the bootstrapping technique [68] shown in Figure. 3-11 is used for improving the linearity. In Sec. 2.5.2, Eq. (2.35) derives the maximum on-resistance (R_{on}) of the sampling switch. For this 15-bit ADC design, the sampling time is determined by the clock frequency, which is $12f_s$ in this work. Hence the Eq. (2.35) can be modified as

$$R_{on} < \frac{1}{2\ln 2(N+1)12f_s C_s}. \quad (3.39)$$

Figure 3-11: Bootstrapped switch.

For a $N=15$ -bit ADC with $C_s=27$ pF, $f_s=1$ kHz, the maximum R_{on} is 139.1 k Ω in terms of Eq. (3.39). The M1 and M2 shown in Figure. 3-11 are set with the same size ($1.3 \mu/0.35 \mu$). Simulations show that the sampling switch has a worst case (slow process corner, 85°C) R_{on} of 6.12 k Ω and the corresponding ENOB of 16.7-bit. Here,

Figure 3-12: Dynamic latch comparator.

the M1 and M2 are connected in series to reduce the sub-threshold leakage. Simple inverters have been used to implement the DAC switches in both pipeline stages. The conventional dynamic latch comparator [69, 70] shown in Fig. 3-12 is used to generate the digital output bits (D8 $\cdots$ D14).

3.4.2 OTA

According to the analysis in Section 3.3.2, the inter-stage gain reduction factor $r = 3$ lowers the open-loop DC gain of the OTA to 72.25 dB while the maximum differential output swing is relaxed to 0.825 V pp. A simple two-stage OTA with

Figure 3-13: Two-stage OTA with Miller compensation.

Miller compensation [43] as shown in Fig. 3-13 is implemented in this work. With $V_{DD} = 3.3$ V, the simulated open-loop DC gain of the OTA is 89.7 dB which affords > 10 dB design margin. The unity-gain frequency and phase margin are 298 kHz and

Figure 3-14: Open-loop gain and phase of OTA.

72° respectively with a load capacitance of 2 pF which corresponds to the second-stage DAC capacitance. The power consumption is $5.05 \mu\text{W}$. The positive power supply rejection ratio (PSRR) is 54 dB. Fig. 3-14 shows the simulated open-loop gain

and phase of the OTA. Switched capacitor common-mode feedback (CMFB) circuits are used in the input-stage and output-stage of the OTA. Simulated result shows that the worst case open-loop DC gain is 77.9 dB under 85°C at the fast process corner.

In this work, the switch capacitor amplifier as the gain-stage provides a voltage gain of 16. By setting the feedback factor (β) is $\frac{1}{16}$, the simulated close-loop gain is 15.9. The 3rd order harmonic distortion (HD3) is -69.09 dB with a differential output swing of 0.825 V pp. The total output noise is 691.8 μ V which is lower than $\frac{1}{2}$ LSB of the second sub-ADC (11-bit accuracy).

3.4.3 Second-stage sub-ADC

A 9-bit SAR ADC with attenuation capacitor DAC forms the second-stage sub-ADC. The DAC consists of a 5-bit main-DAC and 4-bit sub-DAC. Owing to the use of gain reduction, the total capacitance is given by (3.19) where $r = 3$ and $M = 5$. A unit PIP capacitor $C_{u2} = 15$ fF was chosen yielding a total capacitance of 1.94 pF. The SAR logic for the second-stage is similar to that shown in Fig. 3-9. However, the four DFFs in Fig. 3-9 that generate the sampling signals f_s and f_r are omitted in the second-stage. Since the resolution of this stage is 9-bit, a transmission gate is used to design the sampling switch S_2 shown in Fig. 3-3. The same dynamic latch comparator topology as in the first-stage is used to generate the digital output bits.

3.5 Measurement Results

Figure 3-15: Chip micrograph of the ADC.

The fully differential 15-bit ADC with a core area of 900 μ m $\times$ 754 μ m was fabricated in a one-poly-four-metal (1P4M) 0.35- μ m CMOS process. The core is packaged in a J-Leaded Chip Carrier (JLCC) package. The chip micrograph is shown

in Fig. 3-15. The unmarked area in Fig. 3-15 includes decoupling capacitors and I/O buffers. Fig. 3-16 and Fig. 3-17 show the measured Fast Fourier Transform (FFT)

Figure 3-16: Measured 4096-point FFT spectrums with near-DC input at 1 kS/s.

Figure 3-17: Measured 4096-point FFT spectrums with near-Nyquist input at 1 kS/s.

spectrum of the ADC operating at a sampling rate of 1 kS/s with near-DC (10 Hz) and near-Nyquist (490.97 Hz) input tones. The amplitude of the input signal is set to -0.066 dBFS. A clock frequency of $f_{clk} = 12$ kHz is used. The SNDR, SFDR and ENOB are 78.86 dB, 91.66 dB and 12.8-bit respectively with the near-DC input tone. For the near-Nyquist input tone SNDR, SFDR and ENOB are 74.84 dB, 92.87 dB and

12.1-bit respectively. The SNDR and SFDR over the range of input signal frequencies up to the Nyquist bandwidth for 1 kS/s are shown in Fig. 3-18. An SNDR > 74 dB is

Figure 3-18: Measured SNDR and SFDR at 1 kS/s vs input frequency.

Figure 3-19: Measured DNL and INL at 1 kS/s.

maintained up to the Nyquist bandwidth. Histogram test is used to measure the static linearity of the ADC. A 5.127 Hz fully differential sinusoidal input tone is applied to the ADC. The measured differential nonlinearity (DNL) and integral nonlinearity

(INL) of the ADC are shown in Fig. 3-19. The peak DNL and INL are 1.24/-0.93 LSB and 3.31/-2.94 LSB, respectively.

With $V_{DD} = 3.15$ V for the OTA and $V_{DD} = 3$ V for the rest of the circuits, the total power consumption of the ADC is $6.7 \mu\text{W}$. The OTA consumes $6.19 \mu\text{W}$ while the sub-ADCs consume $0.522 \mu\text{W}$. The OTA consumes $\approx 92\%$ of the total ADC power which is due to the static currents that always flow in the OTA. Switching on the OTA only during the residue amplification phase and disabling it during the rest of the clock cycles can significantly reduce power consumption. Table 3-1 compares the proposed ADC with other high-resolution pipelined SAR, pipelined and $\Delta\Sigma$ ADCs. The Schreier FoM defined as

$$\text{FoM} = \text{SNDR} + 10 \log\left(\frac{BW}{P}\right) \quad (3.40)$$

has been used to compare the performance of the ADCs. The proposed ADC achieves a peak FoM of 157.6 dB. Compared to the implementations in 0.35- μ m CMOS reported in [61], [71] and [72] this work achieves a superior FoM. The achieved FoM is very competitive in comparison to that of the $\Delta\Sigma$ ADCs in [73], [74] and [18] which have signal bandwidth similar to this work. Featuring an ENOB > 12 -bit and power consumption of $6.7 \mu\text{W}$ in a low-cost CMOS process, the proposed ADC offers an attractive choice for energy-constrained applications such as wireless sensor networks.

3.6 Summary

In this chapter, a high-resolution pipelined SAR ADC for low-power, low sampling rate applications was presented. A detailed analysis of the power consumption of the various sub-blocks facilitated the choice of suitable sub-ADC resolutions for the two pipeline stages. By employing substantial inter-stage gain reduction, the specifications of the OTA used in the residue amplifier were relaxed. Appropriate choice of DAC topologies in the sub-ADCs yielded considerable area and power saving by reducing the total capacitance requirement. Prototyped in a 0.35- μ m CMOS process, the ADC achieves a competitive FoM among related works while maintaining an ENOB > 12.1 -bit up to the Nyquist bandwidth.

Table 3-1: Comparison of the ADC with other high-resolution ADCs

Specification	[61]	[75]	[71]	[27]	This work
CMOS	0.35- μm	0.18- μm	0.35- μm	0.13- μm	0.35- μm
Architecture	Pipelined	Pipelined	Pipelined	Pipelined SAR	Pipelined SAR
Resolution (bits)	14	16	14	14	15
SNDR (dB)	74	78.6	74	70.4	78.86
SFDR (dB)	94	96	100	79.6	91.66
BW (Hz)	37.5E+06	6.25E+06	40E+06	15E+06	0.5E+03
Power (W)	318E-03	385E-03	1200E-03	2.54E-03	6.71E-06
Calibration	No	Yes	No	No	No
DC gain (dB)	100	-	-	86	>72.3
Area (mm ²)	7.8	15	-	0.24	0.679
FoM (dB)	154.7	160.7	149.2	168.1	157.6
Specification	[72]	[73]	[74]	[18]	This work
CMOS	0.35- μm	0.35- μm	0.18- μm	65 nm	0.35- μm
Architecture	Pipelined	$\Delta\Sigma$ Order (3)	$\Delta\Sigma$ Order (2)	$\Delta\Sigma$ Order (2)	Pipelined SAR
Resolution (bits)	12	-	-	-	15
SNDR (dB)	72.5	65	72	76	78.86
SFDR (dB)	84.4	-	-	-	91.66
BW (Hz)	10E+06	0.12E+03	0.256E+03	0.5E+03	0.5E+03
Power (W)	56.3E-03	0.73E-06	13.3E-06	2.1E-06	6.71E-06
Calibration	Yes	No	No	No	No
DC gain (dB)	90	-	-	-	>72.3
Area (mm ²)	20.6	0.35	0.51	0.033	0.679
FoM (dB)	155	147.2	144.8	159.8	157.6

Chapter 4

A Pipelined SAR ADC with Gain-stage Based on Capacitive Charge Pump

In this chapter, a 14-bit, tunable bandwidth two-stage pipelined SAR ADC is presented. To overcome the high open-loop DC gain requirement of the OTA in the gain-stage, the multi-stage capacitive charge pump (CCP) is utilized to achieve the gain-stage instead of using the SC integrator. The detailed design considerations are given in this work. To verify the proposed solution, the 14-bit ADC was designed and fabricated in a low-cost 0.35- μm CMOS process.

4.1 Introduction

One of the limiting factors for the pipelined SAR ADC to achieve a high resolution is the design of a high DC gain OTA. In Chapter 3, a two-stage OTA with a 89.7 dB open-loop DC gain is utilized to achieve a 15-bit ADC in 0.35- μm CMOS. For a higher resolution ADC, the folded-cascode with gain boosting OTA or the three-stage OTA can significantly improve the open-loop DC gain, but the cascode architecture limits the output swing and the stability is another issue in the three-stage architecture. Furthermore, the design of the OTA with such architecture to obtain a DC gain above 90 dB in the advanced CMOS technologies presents a formidable challenge due to a lower intrinsic gain of the transistor. In [30, 56], an open-loop amplifier as the gain-stage is offered. But the process variations significantly affect the voltage gain. Hence, an extra calibration technique is required. To overcome the high DC gain requirement, in this chapter, we employ the design, analysis and implementation of a 14-bit, tunable bandwidth two-stage pipelined SAR ADC in 0.35- μm CMOS process

which uses a 3-stage CCP as the gain-stage instead of using the SC amplifier. Since the basic CCP cell can provide a gain of 2 [76], m -stage CCP can be connected in series to achieve a gain of 2^m . Combining the gain reduction solution as shown in Chapter 3, 3-stage CCP is utilized to achieve a stage gain of 8. As the gain reduction solution requires increased sampling capacitance for the second-stage sub-ADC to compensate for the reduced signal swing [27], the attenuation DAC [77] is chosen to alleviate the increased capacitance requirement in the second-stage. The segmented capacitive array DAC [37] is implemented in the first-stage which meets the targeted static linearity with a lower unit capacitance. The prototype ADC achieves a peak SNDR of 75.6 dB at a sampling rate of 20 kS/s and 76.1 dB at a sampling rate of 200 kS/s while consuming 7.68 μ W and 96 μ W, respectively.

This chapter is organized as follows. Section 4.2 introduces the proposed pipelined SAR ADC architecture and the operating sequence. Section 4.3 describes the details of circuit implementation. The measurement results are presented in Section 4.4, followed by the conclusions in Section 4.5.

4.2 Proposed Two-stage Pipelined SAR ADC

4.2.1 Architecture

Fig. 4-1 shows the proposed two-stage pipelined SAR ADC architecture. It consists of N_1 -bit SAR ADC with segmented binary-weighted capacitive DAC, a multi-stage CCP and a N_2 -bit SAR ADC with split binary-weighted capacitive DAC. For the pipelined SAR ADC, although the resolution of the first-stage is N_1 , the accuracy for the first-stage must meet the total resolution N and also the matching constraints necessitate large unit capacitor in the capacitive array which entails large power consumption and chip area. For the segmented DAC with a segmentation degree k , the unit capacitor value is 2^{k-1} times lower than the unit capacitor for the conventional binary-weighted DAC in order to meet the same targeted static linearity [62]. Hence the SAR ADC with segmented binary-weighted capacitive DAC serves as the first-stage in order to relax the unit capacitor value and the active chip area. The multi-stage CCP works as the gain-stage to amplify the residue signal with a inter-stage gain of 2^m where the $m = N_1 - r$ and r is the gain reduction factor. Since the basic CCP cell applies an ideal gain of 2 [76], $N_1 - r$ stages are necessary to achieve a gain of 2^{N_1-r} . The inter-stage gain is reduced by 2^r times, which means an extra capacitor $C_x = (2^{r-1} - 1)C_{tot2}$ is required for the second-stage DAC to compensate for the reduced signal swing where the C_{tot2} represents the total capacitance of second DAC. So the SAR ADC with split binary-weight capacitive DAC is chosen to alleviate the increased capacitance requirement in the second-stage.

4.2.2 Timing

Fig. 4-2 is the timing diagram of the proposed architecture with 3-stage CCP. The input signal V_{in} is sampled through the switch S_1 at the phase f_{s1} and then the first-stage starts the conversion. The residue signal is generated after $N_1 + 1$ steps conversions. Thereafter, the residue signal is amplified by the 3-stage CCP gain-stage with a voltage gain of 8. The final output signal from the gain-stage is then sampled by the switch S_2 at the rising edge of f_{s2} and the second SAR ADC starts the following conversion. From Fig. 4-2, the clock frequency can be derived as

$$f_{clk} = (N_1 + 2t_p + m + 1)f_s, \quad (4.1)$$

where $m = N_1 - r$ is the stage number of gain-stage and t_p is the duration of sampling frequency which is set to $2/f_{clk}$.

Figure 4-2: Timing diagram for proposed pipelined SAR ADC architecture with $m=3$.

4.3 Proposed Pipelined SAR ADC Architecture Implementation

4.3.1 Multi-stage CCP Analysis and Implementation

The multi-stage CCP architecture is shown in Fig. 4-1, consisting of several basic charge pump cell [76]. For each cell, it supplies a gain of 2. Thus, the multi-stage CCP could achieve a gain of 2^m ideally. In this architecture, the only active circuitry is the unity gain buffer with a capacitive load of C_m . Proper choice of the C_m is crucial for

keeping the noise level below the corresponding quantization noise. Meanwhile, the choice of the stage number m is also elaborated upon in this section.

4.3.1.1 Basic CCP

Charge pump is the circuit that generates an output voltage which is larger than the input voltage. The basic CCP cell [76] is shown in Fig. 4-3. The capacitor is charged

Figure 4-3: Capacitive charge pump cell.

to $\pm v_{in}$ during phase ϕ_{1-s} . At phase ϕ_{1-a} , the v_{in} is connected to the bottom plate of the capacitor, while the capacitor maintains its charge from previous phase which is $v_{in}C$. According to the charge conservation, we have

$$(V_{out} - (V_{cm} \pm v_{in}))C = \pm v_{in}C, \quad (4.2)$$

So,

$$V_{out} = V_{cm} \pm 2v_{in}. \quad (4.3)$$

Eq. (4.3) shows that one CCP cell has a gain of 2. To achieve a 2^m stage gain available for pipelined SAR ADC, m charge pump cells can be connected in series as shown in Fig. 4-1.

4.3.1.2 Noise Analysis

The thermal noise, introduced by the on-resistance of the sampling switch, is the main noise source for the first CCP stage. This noise is sampled by C_1 during ϕ_{1-s} which is given by

$$\overline{v_{n,\phi_{1-s}}^2} = \frac{kT}{C_1}, \quad (4.4)$$

where k is the Boltzmann constant and T is the absolute temperature.

For the second CCP stage, the noise is determined by three noise sources which are the noise from the switch in the stage itself, the noise from the previous sampling switch and also the noise from unity gain buffer respectively. The OTA in unity gain configuration as shown in Fig. 4-4 is employed in this work. Because the unity gain

Figure 4-4: OTA in unity gain configuration.

frequency of the buffer is $\frac{g_{m1}}{C_2}$, where the g_{m1} is the transconductance of M1 in Fig. 4-4, the total noise of the resistor is shaped by the low-pass characteristic. Hence, the total noise power of the resistors is given by

$$\overline{v_{n_{R_{on}, \phi_{2.s}}}^2} = \frac{16kTR_{on}}{4\tau}. \quad (4.5)$$

By using $\tau = \frac{C_2}{g_{m1}}$, where τ is the time constant, the total noise power from resistor is

$$\overline{v_{n_{R_{on}, \phi_{2.s}}}^2} = \frac{kT}{C_2} 4g_{m1}R_{on}. \quad (4.6)$$

For the unity gain buffer, the output noise power is

$$\overline{v_{n_{OTA, \phi_{1.a}}}^2} = \frac{4kT}{3C_2} \left(1 + \frac{g_{m3}}{g_{m1}}\right), \quad (4.7)$$

where g_{m3} is the transconductance of M3 in Fig. 4-4. Hence, the total noise power sampled by C_2 at phase $\phi_{2.s}$ is given by the sum of Eq. (4.6) and Eq. (4.7) which is

$$\overline{v_{n_{tot, \phi_{2.s}}}^2} = \frac{kT}{C_2} 4g_{m1}R_{on} + \frac{4kT}{3C_2} \left(1 + \frac{g_{m3}}{g_{m1}}\right), \quad (4.8)$$

with $g_{m1}=27.2 \mu\text{A/V}$, $g_{m3}=10.9 \mu\text{A/V}$, $R_{on}=8.8 \text{ k}\Omega$ and $C_2=2 \text{ pF}$, the total noise power $\overline{v_{n_{tot, \phi_{2.s}}}^2} = 5.85 \times 10^{-9} \text{ V}^2$ at phase $\phi_{2.s}$. To verify the noise estimation, the test bench with the first-stage was built and simulated in $0.35\text{-}\mu\text{m}$ CMOS process. Fig. 4-5 shows the simulation result that is very close to the calculation. Hence, the

Figure 4-5: The total noise in C_2 at phase $\phi_{2,s}$.

total input referred noise for the first CCP stage is:

$$\overline{v_{n,tot,in-c}^2} = \frac{kT}{C_1} + \frac{1}{(G_s)^2} \left(\frac{kT}{C_2} 4g_{m1}R_{on} + \frac{4kT}{3C_2} \left(1 + \frac{g_{m3}}{g_{m1}} \right) \right), \quad (4.9)$$

where G_s is the stage gain which is 2 ideally for single stage.

The above noise analysis just focus on one CCP stage. If this single stage is followed by another stage, the noise of the following stage will contribute to the total noise of the previous stage. Eq. (4.8) could stand for the total output noise for each CCP stage. Hence, for the multi-stage charge pump, the total input referred noise can be derived as

$$\overline{v_{n,tot,input}^2} = \frac{kT}{C_1} + \frac{\overline{v_{n,tot,\phi_{2,s}}^2}}{(G_s)^2} + \frac{\overline{v_{n,tot,\phi_{3,s}}^2}}{(G_s)^4} + \dots + \frac{\overline{v_{n,tot,\phi_{m,s}}^2}}{(G_s)^{2^{m-1}}}. \quad (4.10)$$

It can be seen from Eq. (4.10) that more stages will contribute more noise to the total input referred noise. Thus, a large C_1 is inevitable. For the 3-stage CCP, in order to maintain the input referred noise is below the quantization noise of a 14-bit ADC, the minimum $C_1=2.7$ pF which is calculated from Eq. (4.10). This is under the assumption that the $C_2=C_3=2$ pF and the same parameters from Eq. (4.8) are used. Meanwhile more stages also indicate more power consumption. Hence, proper choice of stage number is important. Since the gain bandwidth of unity gain buffer can be changed by tuning the V_{bias} in Fig. 4-4, the bandwidth of CCP is tunable.

4.3.1.3 Gain Requirement and Power Analysis

The voltage gain of SC integrator can be shown as

$$G = \frac{1}{\beta} \left(1 - \frac{1}{\beta A} \right), \quad (4.11)$$

where $\beta = 2^{r-N_1}$ is the feedback factor with the gain reduction factor r and $\Delta e = \frac{1}{\beta A} = \frac{1}{2^{N-N_1}}$ is the gain error caused by the finite open-loop DC gain of the OTA. In order to obtain the same voltage gain by using the CCP architecture, m charge pump stages should be connected in series. The gain of one CCP stage is

$$G_s = 2G_{buf}, \quad (4.12)$$

thus

$$(2G_{buf})^m = \frac{1}{\beta}(1 - \Delta e), \quad (4.13)$$

where the G_{buf} is unity gain of the buffer which can be expressed as

$$G_{buf} = 1 - \frac{1}{A_{buf}}. \quad (4.14)$$

Substituting Eq. (4.14) into Eq. (4.13) and replacing β , Δe with 2^{r-N_1} and 2^{N_1-N}

Figure 4-6: DC gain requirement of OTA in CCP and SC architecture versus voltage gain (2^m).

respectively. The DC gain A_{buf} of the OTA in unity gain configuration can be formulated as

$$A_{buf} = \frac{1}{1 - \frac{1}{2^{N_1-r}} \sqrt[2^{N-N_1}]{1 - \frac{1}{2^{N-N_1}}}}. \quad (4.15)$$

By using $A = 2^{N-r}$ and Eq. (4.15), Fig. 4-6 plots the DC gain requirement of OTA in SC and CCP for a 14-bit ADC with $N_1 = 7$. It is clear to note that the DC

gain for SC grows exponentially whereas it increases linearly for CCP's DC gain. For instance, to achieve a voltage gain of 8, the open-loop DC gain of the OTA in unity gain configuration is $A_{buf} = 383$ (51.7 dB). However, this DC gain value for OTA in SC amplifier is 1024 (60.2 dB). Although the DC gain is reduced, m -stage CCP is needed to achieve a voltage of 2^m . Hence it is worth analyzing the power consumption of CCP.

Following the analysis in [40], the power consumption for a single-stage transconductance amplifier with capacitive feedback is

$$P_{OTA.G} = 2V_{FS}^2 f_s C_{LA} \left(1 + (1 + |G|) N \ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right), \quad (4.16)$$

where C_{LA} is the capacitive load of OTA, N is total resolution of ADC, V_{FS} is the full-scale range of the ADC and G is the voltage gain. For a MOS transistor in strong inversion, the parameter $V_{eff} = (V_{gs} - V_T)/2$, where V_{gs} and V_T are the gate-to-source and threshold voltages respectively [40]. By replacing G with Eq. (4.11), the Eq. (4.16) can be expressed as

$$P_{OTA.G} = 2V_{FS}^2 f_s C_{LA} \left(1 + (1 + |2^m(1 - \frac{2^m}{A})|) \cdot N \ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right). \quad (4.17)$$

For the CCP, the only active circuitry is the unity gain buffer which dominates the total power consumption of CCP. For such OTA, the power consumption is

$$P_{OTA.1} = 2V_{FS}^2 f_s C_{LA} \left(1 + (1 + |1 - \frac{1}{A_{buf}}|) N \ln 2 \cdot \frac{V_{eff}}{V_{FS}}\right). \quad (4.18)$$

To achieve a gain of 2^m , m unity gain buffers are needed. To simplify the analysis, we assume that the power consumption of each buffer is equal to the first one's and also ignore the power consumption from switches. Normally, the implementation is fully differential. Hence the total power for m -stage CCP is

$$P_{OTA.m} = 2m \cdot P_{OTA.1}. \quad (4.19)$$

With $V_{FS} = 3.3$ V, $V_{eff} = 0.3$ V, Fig. 4-7 plots the OTA energy consumption in CCP and SC architecture according to Eq. (4.17) and Eq. (4.19) as a function of m . To find the influence from larger m , $N = 14$ and $N = 16$ are chosen respectively but with the same load capacitance of 3 pF. In practice, the load capacitance increases along with the growth of resolution. From Fig. 4-7, the OTA power in SC grows exponentially but linearly in CCP. The CCP consumes more power than SC with lower voltage gain due to more unity gain buffers are used. However, the CCP is more power efficient than SC with high voltage gain which shows a power saving potential for designing higher resolution ADC.

To verify the analysis, the gain-stage utilized the CCP and SC amplifier were

simulated in 0.35- μm CMOS. In order to find the impacts from the stage number, the voltage gain of 8 and 64 are chosen for the simulation. To achieve the high gain requirement of the OTA in the SC amplifier, the two-stage OTA with Miller compensation is utilized. The simulation results show that the DC gain requirement in the CCP architecture is 51.8 dB to obtain a voltage gain of 7.94 and the corresponding power is $1.17 \mu\text{W}$ at 1 kS/s with $C_1=3 \text{ pF}$, $C_2=C_3=2 \text{ pF}$. For the SC amplifier, the power is $0.87 \mu\text{W}$ at 1 kS/s with $C_{LA}=3 \text{ pF}$ but the DC gain is 61.7 dB to achieve the same voltage gain. The CCP's power is higher than SC's due to more unity gain buffers are used. When it comes to the voltage gain of 64, the power of CCP is $5.53 \mu\text{W}$ at 1 kS/s with $C_1=3 \text{ pF}$, $C_2=C_3=C_4=C_5=C_6=2 \text{ pF}$ whereas the power of SC is $8.67 \mu\text{W}$ with $C_{LA}=3 \text{ pF}$ at the same sampling rate and the corresponding DC gain requirements are 58 dB for unity gain buffer and 78.5 dB for the OTA in SC to get a voltage gain of 63.4. The four simulation results are added into Fig. 4-7 as well and the above relevant capacitors values are obtained from Eq. (4.10). In Fig. 4-7, the simulated results are higher than the predicted results. This is due to the design margin has been taken into the OTA design.

Figure 4-7: OTA energy consumption in CCP and SC architecture versus voltage gain (2^m) with $N=14$, $N_1=7$ and $N=16$, $N_1=9$ together with the simulation results (Δ : CCP; $\square$: SC; ∇ : CCP; $\diamond$: SC).

In this work, the solution of $m = 3$ has been applied to our 14-bit two-stage pipelined SAR ADC project. It should be pointed out that the main purpose of this work is to verify the overall functionality of the proposed multi-stage capacitive charge pump. Compared to the conventional SC integrator, the CCP gain-stage with a voltage gain of 8 is not power-efficient choice for design of a 14-bit ADC. It remains

as a future work to find a low-power analog buffer instead of using the unity-gain OTA. However, Fig. 4-7 suggests that the presented gain-stage would result in higher power efficiency for higher resolutions, for example for 16-bit ADC with 9-bit in the first-stage.

The implementation of unity-gain buffer is shown in Fig. 4-4 which has a DC gain of 51.8 dB. To determine the impact of process variations and device mismatch on the unity-gain, 200 Monte Carlo simulations were performed. With an external V_{bias} of 0.48 V, Table 4-1 summarizes the simulated unity-gain of the OTA across process corners, device mismatch and at a temperature range of -40°C to 85°C .

Table 4-1: Unity-gain OTA performance

$V_{dd}=3.3\text{ V}$	Unity-gain		
Temperature	Min.	Max.	3σ
-40°C	0.9963	0.9978	740.7e-6
0°C	0.9968	0.9978	563.7e-6
27°C	0.9968	0.9977	542.1e-6
85°C	0.9967	0.9977	655.8e-6

As the table 4-1 shows the unity-gain OTA maintains its gain sufficiently constant. To meet the noise requirement of 14-bit ADC, the $C_1=3\text{ pF}$, $C_2=C_3=2\text{ pF}$ are chosen. Since the input signal of gain-stage is discrete time, the NMOS transistors are used to achieve the switches. It should be mentioned that one more unity gain buffer is needed between the first-stage DAC and the input of gain-stage. The gain error caused by this buffer will be compensated by tuning the reference voltage of the second DAC.

4.3.2 First-stage SAR ADC Implementation

For the 14-bit two-stage pipelined SAR ADC, the $N_1 = 7$ was allocated to the first-stage. Aiming to reduce the power consumption and active area of the first-stage, the segmented binary-weighted capacitive DAC was implemented in the first SAR ADC. Following the detailed analysis in section 3.3.1, the mismatch-limited unit capacitor for the segmented binary-weighted capacitive DAC is

$$C_{u1} > 4.5K_{\sigma}^2 K_c 2^{2(N-N_1)} (2^{N_1-k+1} - 1), \quad (4.20)$$

where K_{σ} is the mismatch parameter, K_c is the capacitor density and k is the segmented degree. For the poly-insulator-poly capacitor in $0.35\text{-}\mu\text{m}$ CMOS process, $K_{\sigma} = 0.45\% \mu\text{m}$ and $K_c = 0.86\text{ fF}/\mu\text{m}^2$. The segmented DAC requires $C_{u1} = 40.8\text{ fF}$ with a segmented degree $k = 3$. Here, the minimum mismatch-limited unit capacitance (40.8 fF) is calculated under the assumption that the sampling switch is ideal. In practice, the sampling switch introduces the charge injection and clock feed-through errors which further cause the harmonic distortions. Hence a large unit

capacitor of 117.7 fF is required by simulations to achieve the targeted 14-bit ADC performance.

It should be noted that the segmented DAC requires a binary-to-thermometer decoder which leads to extra power consumption and chip area. Larger segmentation degree indicates that the circuit complexity, area occupation and power increase. In Chapter 3, the optimal segmentation degree range is $3 \leq k \leq 5$. In this work, a segmentation degree of $k = 3$ is chosen for the first-stage DAC as a trade-off among lower unit capacitor value, increased circuit complexity and power consumption in the digital logic. The same 3-to-7 binary-to-thermometer decoder shown in Chapter 3 (Fig. 3-10) is required for the 3-bit unary-weighted DAC.

Figure 4-8: Control logic. (a) SAR control logic of first-stage. (b) Control logic of three-stage CCP.

Fig. 4-8 shows the control logic circuits which are used to generate the time sequence as shown in Fig. 4-2. The block diagram of the SAR control logic for the first-stage consisting of two separate DFF registers is shown in Fig. 4-8a which is similar to the Fig. 3-9. The upper DFFs chain generate the bit approximation pulses

while the DFFs in lower row store the output C_{out} of the comparator. Finally, the switch control signals (D13...D7) for the DAC are generated which will be involved in the ADC conversion. The control logic of the three-stage CCP is illustrated in Fig. 4-8b. The first four DFFs are connected in series condition which are used to generate the sampling phase ($\phi_{1,s}... \phi_{3,a}$). By choosing the $\phi_{2,s}$, $\phi_{3,s}$ and $\phi_{3,a}$ as the input signals of an OR gate, the amplifying phase $\phi_{1,a}$ can be obtained from the output of OR gate. The $\phi_{2,a}$ can be implemented through the same way. An AND gate is utilized to create the reset signal by connecting the reverse of four sampling phases. The additional two DFFs with an OR gate are triggered by a “set” signal which subsequently create the sampling signal f_{s1} for the first-stage and also the f_{s1} as the start signal is connected to the relevant position as shown in Fig. 4-8a.

For the input sampling switch S_1 in Fig. 4-1, the conventional bootstrapped switch [68] is used for improved linearity. Simulation results indicate a linearity corresponding to 17.6-bit for S_1 with a sampling capacitance of 20 pF at 20 kS/s sampling frequency which is sufficient for the 14-bit resolution. The conventional dynamic latch comparator as shown in Chapter 3 (Fig. 3-12) is used to generate the digital output bits. Simple inverters have been used to implement the DAC switches.

4.3.3 Second-stage SAR ADC Implementation

A 8-bit SAR ADC with attenuation capacitor based DAC forms the second-stage sub-ADC. The DAC consists of a 4-bit main-DAC and 4-bit sub-DAC. Since $m = 3$, the extra capacitor $C_x = 112C_{u2}$ is added into the DAC. As the total capacitance of the second sub-ADC (C_{tot2}) is also the load capacitance of the gain-stage, a unit PIP capacitor C_{u2} is chosen as 15.8 fF yielding a $C_{tot2} = 2.0$ pF to maintain the total input-referred noise of the gain-stage (equation (4.10)) below the quantization noise of 14-bit ADC. Such choice also satisfies the thermal noise and mismatch requirements of the second-stage ADC’s accuracy (11-bit). The SAR logic for the second-stage is similar to that shown in Fig. 4-8a except the reset signal should be connected to $\phi_{3,a}$ generated by control logic as shown in Fig. 4-8b. Since the accuracy of this stage is 11-bit, a transmission gate is used to design the sampling switch S_2 as shown in Fig. 4-1. The same dynamic latch comparator topology as in the first-stage is used to generate the digital output bits.

4.4 Measurement Results

The fully differential 14-bit ADC with a core area of $860 \mu m \times 685 \mu m$ was fabricated in a one-poly-four-metal (1P4M) 0.35- μm CMOS process. The core is packaged in a JLCC44 package. Fig. 4-9 shows the chip micrograph. The unmarked area in Fig. 4-9 includes decoupling capacitors and I/O buffers. At $V_{bias} = 0.48$ V as shown in Fig. 4-4, the measured FFT spectrum of the ADC operating at a sampling rate of 20 kS/s with near-DC (0.5127 kHz) and near-Nyquist (9.526 kHz) input tones are

Figure 4-9: Die micrograph.

shown in Fig. 4-10 and Fig. 4-11 respectively. The amplitude of the input signal is set

Figure 4-10: Measured 4096-point FFT spectrums with near-DC ($f_{in} = \frac{105}{4096} f_s$) input at 20 kS/s.

to -0.052 dBFS. A clock frequency of $f_{clk} = 300$ kHz is used. The SNDR, SFDR and ENOB are 75.6 dB, 90.9 dB and 12.27-bit respectively with the near-DC input tone. For the near-Nyquist input tone, the SNDR, SFDR and ENOB are 74.63 dB, 90.79 dB and 12.1-bit, respectively.

Figure 4-11: Measured 4096-point FFT spectrums with near-Nyquist ($f_{in} = \frac{1951}{4096} f_s$) input at 20 kS/s.

Figure 4-12: Measured 4096-point FFT spectrums with near-DC ($f_{in} = \frac{105}{4096} f_s$) input at 200 kS/s.

By increasing the V_{bias} to 0.63 V, the ADC can work at a sampling frequency of 200 kHz. Fig. 4-12 and Fig. 4-13 show the measured FFT spectrum with near-DC and near-Nyquist input tones but under a sampling rate of 200 kS/s. With the same amplitude of the input signal, the measured SNDR is 76.11 dB, providing a 12.35-bit

Figure 4-13: Measured 4096-point FFT spectrums with near-Nyquist ($f_{in} = \frac{1951}{4096} f_s$) input at 200 kS/s.

ENOB with near-DC input. For the near-Nyquist input, the ADC also achieves a 74.47 dB SNDR and 12.08-bit ENOB. The SNDR and SFDR over the range of input signal frequencies up to the Nyquist bandwidth for 20 kS/s, 200 kS/s are shown in Fig. 4-14. The SNDR > 74 dB is maintained up to the Nyquist bandwidth for the two sampling rates.

Since the bandwidth of CCP is tunable, Fig. 4-15 shows the measured SNDR versus the sampling rate under the different V_{bias} setting. By increasing the bandwidth of CCP, the proposed ADC achieves a SNDR > 75 dB up to 260 kS/s. Due to the speed limitation of comparator and sampling switch, the ADC performance drops fast after $f_s = 260$ kHz.

Histogram test is used to measure the static linearity of the ADC. A full swing, differential sinusoidal input tones ($f_{in}=14.64$ Hz at $f_s=20$ kHz, $f_{in}=146.48$ Hz at $f_s=200$ kHz) are applied to the ADC. The measured DNL and INL for 20 kS/s and 200 kS/s are shown in Fig. 4-16 and Fig. 4-17. The peak DNL and INL are 1.06/-0.83 LSB and 2.37/-2.58 LSB for 20 kS/s. For the 200 kS/s sampling rate, the peak DNL and INL are 0.97/-0.82 LSB and 2.42/-2.06 LSB, respectively.

With a supply voltage of 3.3 V for the analog and 3 V for the digital, the total power consumption of the ADC is $7.68 \mu\text{W}$ at $f_s = 20$ kS/s and $96 \mu\text{W}$ at $f_s = 200$ kS/s. For 20 kS/s sampling rate, about 40.6% of the total power is consumed by the digital, 26.9% by the CCP, 20% by the DAC and 12.5% by the comparator. For 200 kS/s, the corresponding percentages are 32.7%, 41.8%, 15.5% and 10%, respectively. Due to the increased V_{bias} , the CCP occupies more power with the sampling rate of

Figure 4-14: Measured SNDR and SFDR at 20 kS/s ($V_{bias} = 0.48$ V), 200 kS/s ($V_{bias} = 0.63$ V) versus input frequency.

Figure 4-15: Measured SNDR versus f_s with near-DC input ($f_{in} = \frac{105}{4096} f_s$).

200 kS/s. Table 4-2 compares the performance of proposed ADC with other high-resolution pipelined SAR, pipelined and nyquist ADC. The proposed ADC achieves a peak Schreier FoM of 166.7 dB at 20 kS/s and 166.3 dB at 200 kS/s. Compared

Figure 4-16: Measured DNL and INL at 20 kS/s.

Figure 4-17: Measured DNL and INL at 200 kS/s.

to the implementations in $0.35\text{-}\mu\text{m}$ CMOS reported in [61], [71] and [72] this work achieves a best FoM. The achieved FoM is also comparable to the reported result from [27]. Hence, the proposed solution offers an attractive choice for designing the

Table 4-2: Comparison of the ADC with other high-resolution ADCs

Specification	[71]	[72]	[27]	This work	
CMOS	0.35- μm	0.35- μm	0.13- μm	0.35- μm	
Architecture	Pipelined with SC	Pipelined with SC	Pipelined SAR with SC	Pipelined SAR with CCP	
Resolution (bits)	14	12	14	14	
Calibration	No	Yes	No	No	
DC gain (dB)	-	60	86	51.8	
Area(mm^2)	-	20.6	0.24	0.589	
f_s (Hz)	80E+06	20E+06	30E+06	20E+03	200E+03
SNDR (dB)	74	72.5	70.8	75.6	76.1
SFDR (dB)	100	84.4	87.8	90.9	92.7
Power (W)	1200E-03	56.3E-03	2.54E-03	7.68E-06	96E-06
FoM (dB)	149.2	155	168.5	166.7	166.3
Specification	[29]	[28]	[24]	This work	
CMOS	65 nm	28 nm	65 nm	0.35- μm	
Architecture	Pipelined SAR with ring amplifier	Pipelined SAR with dynamic SC	Nyquist SAR	Pipelined SAR with CCP	
Resolution (bits)	13	14	14	14	
Calibration	No	Yes	No	No	
DC gain (dB)	>80	-	-	51.8	
Area(mm^2)	0.054	0.137	0.28	0.589	
f_s (Hz)	50E+06	80E+06	10E+03	20E+03	200E+03
SNDR (dB)	71.5	68.0	78.1	75.6	76.1
SFDR (dB)	87.0	80.7	88.5	90.9	92.7
Power (W)	1.0E-03	1.5E-03	2.48E-06	7.68E-06	96E-06
FoM (dB)	175.5	172.3	171.1	166.7	166.3

high resolution pipelined SAR ADC without designing a high DC gain OTA.

4.5 Summary

The three-stage capacitive charge pump as the gain-stage for a 14-bit two-stage pipelined SAR ADC was presented in this chapter. Due to the tunable bandwidth of CCP, The proposed ADC achieves a SNDR > 75 dB up to 260 kHz. Meanwhile the ADC also provides a competitive FoM among related works. By employing the CCP as the gain-stage, the high DC gain OTA in the SC integrator was avoided while also reducing the design complexity. Hence, we concluded that the multi-stage capacitive charge pump shows another solution to achieve the function of the gain-

stage instead of using the SC integrator for the low-speed, two-stage pipelined SAR ADC application.

Chapter 5

A 14-bit Asynchronous Two-stage Pipelined SAR ADC

This chapter describes the design and implementation of an asynchronous clock generator which is used in a 14-bit two-stage pipelined SAR ADC for low-power sensor applications. Aiming to reduce the power consumption of unity-gain buffers utilized in the multi-stage CCP gain-stage, simple source followers as the analog buffers are used in this work.

5.1 Introduction

Low-power sensors might be active only for very short time triggered, for example, by an external pulse to acquire the data. Hence, an asynchronous clock generator for a 14-bit pipelined SAR ADC is described in this chapter. The overall goal has been achieved a flexible clocking scheme which can dynamically and efficiently allocate the available time for the DAC charge redistribution, the comparator and the gain-stage. Such clock generators are often based on delay elements. In [26] [55], the delay buffer provides a propagation delay of several hundred picoseconds which is not suitable for low-speed ADCs. In [78] [79], a delay buffer chain has been implemented to apply a fixed delay of 10 ns. However, several missing codes are observed due to the fixed delay which is not long enough for the DAC to settle all the digital codes. In order to provide variable redistribution time for the switched capacitor DAC, a tunable delay element has been utilized to create a controllable delay. Furthermore, a comparator with variable regeneration time has been achieved by using a self-synchronization loop utilizing edge detector. Such variable duration allows longer time for the comparator to act on smaller input signals.

The 3-stage CCP [80] with a voltage gain of 8 as another solution for the gain-stage has been successfully implemented in a 14-bit ADC as shown in Chapter 4 and the unity-gain OTAs are used as the analog buffers to prevent the charge sharing between the CCP stages. As the power consumption of the CCP gain-stage is dominated by the unity-gain OTAs, in this chapter, we propose the source follower amplifiers as the analog buffers to further reduce the power consumption. Open-loop amplifier has been also proposed earlier (e.g. in [30]). However, in this work the source follower amplifier aims to serve as an open-loop buffer with unity gain. Finally, a 14-bit two-stage pipelined SAR ADC with proposed asynchronous clock generator has been designed and simulated in $0.18\text{-}\mu\text{m}$ CMOS. A 3-stage CCP with four source follower buffers is used to achieve the gain-stage. The post layout simulation results show that the ADC achieves an ENOB of 13.58-bit at 10 kS/s sampling rate while consuming $2.39\text{ }\mu\text{W}$.

This chapter is organized as follows. Section 5.2 describes the overview of asynchronous two-stage pipelined SAR ADC. Section 5.3 provides the detailed circuit implementation of the proposed asynchronous clock generator. Section 5.4 and Section 5.5 present the implementation of 3-stage CCP gain-stage with source follower buffers and DACs in both sub-ADCs. Section 5.6 presents the simulation results. Finally, conclusions are drawn in Section 5.7.

5.2 Proposed Asynchronous Two-stage Pipelined SAR ADC Architecture

Fig. 5-1 shows the architecture and timing of the proposed 14-bit asynchronous two-stage pipelined SAR ADC. The 7-bit SAR ADC with segmented binary-weighted capacitive DAC [58] [59] serves as the first-stage in order to reduce the unit capacitor value and the chip area. The 3-stage CCP, described in Chapter 4, is used as the gain-stage to amplify the residue signal with a inter-stage gain of 8. As the inter-stage gain is reduced from 64 to 8, an extra capacitor with value of $7C_{tot2}$ is required for the second-stage DAC to compensate the reduced signal swing, where the C_{tot2} represents the total capacitance of the capacitor array in the second DAC. An 8-bit SAR ADC with split binary-weighted capacitive DAC [65] is chosen in order to alleviate the increased capacitance requirement in the second-stage DAC.

Three asynchronous clock generators are utilized in the ADC to generate the internal control signals for two sub-ADCs and the gain-stage, respectively. The 1st asynchronous clock generator is triggered by an external pulse (f_{s1}) which subsequently creates an internal clock signal (clk_{in1}) for the first sub-ADC. Once the data conversion of the first-stage is completed, the start signal (f_{res}) for the 2nd asynchronous clock generator is generated by the SAR1 logic and further triggers the 2nd asynchronous clock generator to create the control signal (ϕ_a) for the gain-stage. It should be mentioned that the ϕ_a represents a group of signals including three

Figure 5-1: Architecture and timing of the proposed asynchronous two-stage Pipelined SAR ADC.

phases for sampling and three phases for amplifying as shown in Fig. 5-7. The clk_{in2} can be generated by the 3rd generator with the trigger pulse f_{s2} . The t_c , t_{d1} and t_{d2} represent the comparator's regeneration time, charge redistribution time of DAC and the amplifying time for the gain-stage, respectively. Since the comparator's input signals vary with the proceeding of conversion, the t_c is variable. A tunable RC element is used to create a controllable delay.

5.3 Asynchronous Clock Generator Implementation

5.3.1 Internal Clock Generator

The internal clock generator, which is based on self-synchronization, serves as the key part of the asynchronous clock generator. Fig. 5-2 shows the block diagram of the internal clock generator and its timing diagram. Initially, the comparator is reset when the rising edge of the trigger pulse (f_{s1}) propagates through an OR gate. Subsequently, the clk_{in1} goes low for the first time after the falling edge of f_{s1} . The comparator compares the two input signals at the falling edge of clk_{in1} and generates two outputs (out_p , out_n), either 'high' or 'low'. An NAND gate is used to detect the two outputs and further creates the clk_1 . After the comparator completes the comparison, the rising edge of clk_1 appears for the first time. A J-K latch combining the clk_1 and $clk_{1,td}$ is utilized to create the following phases of clk_{in1} , where the $clk_{1,td}$ represents the delayed version of the clk_1 . When the $clk_{1,td}$ goes low, the clk_{in1} starts to go

Figure 5-2: (a) Diagram of internal clock generator. (b) Timing diagram of internal clock generator.

high and resets the comparator. Thus the clk_1 is kept low. After a delay of t_{d1} , the

Figure 5-3: RC delay circuit based on cross-coupled inverter.

clk_{in1} goes low due to the rising edge of clk_{1_td} and the comparator starts a new comparison again. This completes one cycle for the internal clock generator. Because the rising edge of clk_{in1} is generated after the comparator completes the comparison, hence this method gives the comparator sufficient comparison time for the small input signals.

From Fig. 5-2(b), the clk_{1_td} plays an important role in the entire cycle to create the clk_{in1} . Hence, the delay circuit is the key block in this internal clock generator. To achieve a microsecond delay, a tunable RC delay circuit as shown in Fig. 5-3 is utilized in this work. It is composed of a RC network (M1, C) and a dynamic

Figure 5-4: Output waves of internal clock generator. (a) Simulation undergoes with $V_{bias1} = 0.44$ V. (b) Simulation undergoes with $V_{bias1} = 0.52$ V.

cross-coupled inverter. When clk_1 is high, the output is connected to ground. At the falling edge of clk_1 , the capacitor is charged and the output acts as a ramp signal. The pulse will not be generated until the rising edge of clk_1 happens again. This pulse as one input drives an AND gate to create the clk_{1_td} . The delay time is controlled by turning the V_{bias1} manually from an external voltage source. In order to reduce the charge and discharge power consumed by the capacitor, the value of C should be kept as low as possible (36 fF in this work). This RC delay element has been used in

With $M1$ ($0.44 \mu/5 \mu$) and $C=36$ fF, Fig. 5-4 shows the simulated results of internal clock generator. A fully differential sinusoidal signal with common mode voltage of 0.9 V and the amplitude of 10 mV is set as the input signal and the dynamic latch comparator (Fig. 3-12) is chosen to compare the input voltages. The comparator is reset at the rising edge of f_{s1} and started to work at falling edge. With $V_{bias1} = 0.44$ V, the t_{d1} is $7.6 \mu\text{s}$ and the t_c is 1.244 ns with 20 mV peak-to-peak inputs whereas this time is 1.322 ns at $30 \mu\text{s}$ as shown in Fig. 5-4a due to the smaller inputs (5 mV_{pp}). Hence, the clk_{in1} 's duration of 'low' varies with the input's amplitude. Fig. 5-4b shows the simulated output waveform under the $V_{bias1} = 0.52$ V. With the same inputs, the t_{d1} is reduced to $3.3 \mu\text{s}$.

The same SAR logic mentioned in Chapter 4 is used to generate the switch control signals for the first DAC. For a better illustrate, the block diagram of SAR logic is presented in Fig. 5-5. It is controlled by the clk_{in1} shown in Fig. 5-2(b). As the

pulse width ('low') of clk_{in1} is quite short, the width of the transistors controlled by clk_{in1} should be increased. In this work, the transistor's width is five times wider than the minimum width. The final DFF on the far right side generates the trigger pulse (f_{res}) for the gain-stage. The same SAR logic architecture is implemented in the second-stage except the clock is clk_{in2} .

5.3.3 Control Logic of Gain-stage

The 3-stage CCP architecture as shown in Chapter 4 has been used to provide a voltage gain of 8. To achieve such voltage gain, three phases for sampling ($\phi_{1_s}, \phi_{2_s}, \phi_{3_s}$) and three phases for amplifying ($\phi_{1_a}, \phi_{2_a}, f_{s2}$) are inevitable. Fig. 5-6 illustrates the control logic. It is composed of four delay elements and each one supplies a delay of

Figure 5-6: Diagram of control logic of 3-stage CCP gain-stage.

t_{d2} . When f_{res} is high, the output of first delay element is 'low' until the delay time up to t_{d2} . During the same time period, the f_{res} propagates through the NAND gate and the signal 'a' with a delay of t_{d2} is generated. By choosing the f_{res} and 'a' as the input signals of an AND gate, the first sampling phase ϕ_{1_s} with pulse width of t_{d2} is created. The rest of sampling phase can be achieved by using the same method except the input pulse should be the previous sampling phase. Two OR gates are utilized to create the reset signal and ϕ_{1_a} by connecting the inputs to the relevant outputs of NAND gates (b, c, d) as shown in Fig. 5-6. Finally, the timing diagram of the 3-stage CCP gain-stage is shown in Fig. 5-7.

5.4 CCP Gain-stage with Source Follower Implementation

The implementation of 3-stage CCP gain-stage with source followers is shown in Fig. 5-8(a). Since single CCP stage provides a gain of 2 [76], a voltage gain of 8 can be achieved by using 3 stages. Aiming to reduce the power consumption, the NMOS source-followers have been used in this work as the unity-gain buffers to prevent the charge sharing between stages. While the source follower buffers are simple and power efficient, they shift the DC level of the signals [43], thereby causing

Figure 5-7: Timing diagram of 3-stage CCP gain-stage.

Figure 5-8: (a) 3-stage CCP with source follower. (b) NMOS source follower.

an accumulated offset error, limiting the output swing and generating large distortions. Furthermore, the gain error needs to be compensated as well.

5.4.1 Offset Error Compensation

The total charge (Q_1) on C_1 is $(V_{cm} \pm v_{in} - \Delta v - V_{cm1})C_1$ during phase $\phi_{1.s}$, where Δv is the offset error of the source follower stage. At phase $\phi_{1.a}$, the v_{in} is connected to the bottom plate of the capacitor, while the capacitor maintains its charge from previous phase. According to the charge conservation, we have

$$(V_{out1} - V_{cm} \mp v_{in} + 2\Delta v)C_1 = (V_{cm} \pm v_{in} - \Delta v - V_{cm1})C_1. \quad (5.1)$$

Thus the V_{out1} shown in Fig. 5-8 can be expressed as

$$V_{out1} = V_{cm} \pm 2v_{in} + V_{cm} - 3\Delta v - V_{cm1}. \quad (5.2)$$

To compensate the offset error, it requires

$$V_{cm1} = V_{cm} - 3\Delta v. \quad (5.3)$$

During phase $\phi_{2.s}$, the total charge (Q_2) is $(V_{out1} - V_{cm2})C_2$, due to the charge conservation, and the V_{out2} is expressed as

$$V_{out2} = V_{cm} \pm 4v_{in} + V_{cm} - \Delta v - V_{cm2}. \quad (5.4)$$

Thus, the offset error in Eq. (5.4) can be compensated by setting the $V_{cm2} = V_{cm} - \Delta v$.

5.4.2 Noise

The noise from source follower and sampling switch are the main noise sources at $\phi_{1.s}$. Since the bandwidth of unity gain frequency of the source follower buffer is $\frac{g_{m1}}{C_1}$, where the g_{m1} is the transconductance of M1 in Fig. 5-8(b), the total noise power at $\phi_{1.s}$ is given by

$$\overline{v_{n,\phi_{1.s}}^2} = \frac{kT}{C_1} 2g_{m1}R_{on} + \overline{v_{n,buf}^2}, \quad (5.5)$$

and the total input noise power of buffer which can be expressed as [43]

$$\overline{v_{n,buf}^2} = \frac{2kT}{3C_1} \left(1 + \frac{g_{m2}}{g_{m1}}\right), \quad (5.6)$$

where k is the Boltzmann constant, T is the absolute temperature and the g_{m2} is the transconductance of M2. At phase $\phi_{2.s}$, the bandwidth is $\frac{g_{m1}}{C_2}$, thus the total noise power is

$$\overline{v_{n,\phi_{2.s}}^2} = \frac{kT}{C_2} 4g_{m1}R_{on} + \frac{2kT}{3C_2} \left(1 + \frac{g_{m2}}{g_{m1}}\right). \quad (5.7)$$

To verify the noise estimation, a test bench with the first CCP stage was simulated in 0.18- μm CMOS. With $g_{m1}=8.3 \mu\text{A/V}$, $g_{m3}=2.9 \mu\text{A/V}$, $R_{on}=8.7 \text{ k}\Omega$ and $C_2=5.5 \text{ pF}$, the simulation shows that the total noise at $\phi_{2,s}$ is $1.06 \times 10^{-9} \text{ V}^2$. Fig. 5-9 shows the simulated result. Reusing the above parameters, the total noise power from Eq. (5.7) is $0.9 \times 10^{-9} \text{ V}^2$ which is close to the simulated result. Hence the total input referred

Figure 5-9: The noise in C_2 at phase $\phi_{2,s}$.

noise power of the first-stage CCP is the sum of Eq. (5.5) and Eq. (5.7) which is

$$\overline{v_{n,tot,1}^2} = \frac{kT}{C_1} 2g_{m1}R_{on} + \frac{2kT}{3C_1} \left(1 + \frac{g_{m2}}{g_{m1}}\right) + \frac{1}{2^2} \overline{v_{n,\phi_{2,s}}^2}. \quad (5.8)$$

Eq. (5.7) can be used for the total noise power at sampling phase for the following stages. Thus, for the 3-stage CCP, the total input referred noise power can be derived as

$$\begin{aligned} \overline{v_{n,tot,input}^2} = & \frac{kT}{C_1} 2g_{m1}R_{on} + \frac{2kT}{3C_1} \left(1 + \frac{g_{m2}}{g_{m1}}\right) \\ & + \frac{\overline{v_{n,\phi_{2,s}}^2}}{2^2} + \frac{\overline{v_{n,\phi_{3,s}}^2}}{2^4} + \frac{\overline{v_{n,\phi_{3,a}}^2}}{2^6}. \end{aligned} \quad (5.9)$$

In order to maintain the input referred noise power below the quantization noise power of 14-bit ADC ($1.01 \times 10^{-9} \text{ V}^2$), the C_1 of 6.1 pF is chosen, which is calculated from Eq. (5.9). This is under assumption that the $C_2=C_3=5.5 \text{ pF}$, $C_4=4 \text{ pF}$, where the C_4 represents the total capacitance of the second-stage DAC. Incorporating additional design margins, the $C_1=7 \text{ pF}$, $C_2=C_3=6.5 \text{ pF}$ and $C_4=4 \text{ pF}$ are chosen which result in a total input referred noise power of $0.87 \times 10^{-9} \text{ V}^2$. Due to the source follower's weak capacity of supply noise rejection, an external high accuracy supply source is inevitable to improve the performance of ADC.

Table 5-1: Source follower gain performance

$V_{dd}=1.8\text{ V}$	unity-gain		
Temperature	Min.	Max.	3σ
-40 °C	0.9946	0.9952	325.8e-6
0 °C	0.9945	0.995	281.7e-6
27 °C	0.9944	0.9949	260.9e-6
85 °C	0.9942	0.9946	233.3e-6

5.4.3 Source Follower and 3-stage CCP Simulation

The NMOS source follower (Fig. 5-8(b)) is used in design of the CCP gain-stage in 0.18- μm CMOS technology. To determine the impact of process variations and device mismatch on the source follower gain, 200 Monte Carlo simulations were performed. With $V_{dd}=1.8\text{ V}$, $V_{bias}=0.5\text{ V}$, M1 ($8\text{ }\mu/0.8\text{ }\mu$) and M2 ($0.5\text{ }\mu/4\text{ }\mu$), Table 5-

Figure 5-10: Simulated output wave of 3-stage CCP with source follower

1 summarizes the simulated gain of the source follower across process corners and at a temperature range of -40°C to 85°C. As the table shows the source follower maintains its gain sufficiently constant. In addition, the simulated 2nd order harmonic distortion (HD₂) was -85.2 dB with an output swing of 225 mV which can support the resolution of the second-stage ADC. Furthermore, the simulated output common mode (CM) voltage of the source follower is 608 mV with typical corner at the temperature of 27°C.

Fig. 5-10 shows an example of the simulated output waveform of the 3-stage CCP. To compensate the offset error, the V_{cm1} and V_{cm2} are set at 35 mV and 0.6 V, respectively. The input signal ($V_{res,in}$) shown in Fig. 5-10 represents the residue signal of the first sub-ADC which is $(900 + v_{in})$ mV. With the v_{in} of 7.5 mV and 19 mV, the corresponding output signals are 58 mV and 147 mV respectively, which indicate a voltage gain of 7.7 for 3-stage CCP. The gain error caused by the source follower is compensated by tuning the reference voltage of second DAC.

5.5 First-stage and Second-stage DACs Implementation

The segmented binary-weighted capacitive DAC with $k=3$ serves as the 7-bit first-stage to reduce the unit capacitor value and the chip area. Aiming to find the mismatch-limited C_{u1} , the Monte Carlo simulation involved 100 runs simulating the worst-case DAC switching scenario. The simulation shows that the three times worst-case standard deviation of DNL ($3\sigma_{max}$) is 101 μ V with $C_{u1}=90$ fF which is less than 1 LSB of 14-bit ADC. Incorporating some design margin for the unit capacitor, a Metal-insulator-Metal (MIM) capacitor with the value of 120 fF is chosen to design the segmented DAC resulting a total capacitance of 15.4 pF which also satisfies the thermal noise requirement.

Since the gain-stage supplies a voltage gain of 8, an additional capacitor $C_x = 7C_{tot}$ is necessary to compensate for the reduced signal swing. In order to alleviate the increased total capacitance of second DAC, the split capacitor array based DAC [65] forms the 8-bit second-stage. This DAC consists of a 4-bit main DAC and 4-bit sub-DAC to further reduce the power. Because the total capacitance of DAC is also the load capacitance of the gain-stage, to maintain the total input-referred noise of gain-stage is below the quantization noise of 14-bit ADC, an unit MIM capacitor $C_{u2}=31$ fF is chosen yielding a total capacitance of 4 pF. Such total capacitance also satisfies the mismatch and thermal noise requirements of the second-stage ADC. The conventional bootstrapped switch with a 17-bit linearity at 10 kHz is used to achieve the input sampling switch (S_1 in Fig. 5-1) for the first sub-ADC. Simple inverters and transmission gate are used to implement the DAC switches and the second sub-ADC's input sampling switch (S_2), respectively.

5.6 Simulation Results

A 14-bit pipelined SAR ADC with asynchronous clock generators was designed and simulated in 0.18- μ m CMOS. Fig. 5-11 shows the layout of the proposed ADC. To evaluate the ADC performance, a 10 kHz external trigger pulse with a 7.6% duty cycle is used for the simulation. The amplitude of the input signals are set to -0.5 dBFS. To compensate the gain error caused by the source followers in the gain-stage,

Figure 5-11: Layout of the proposed ADC.

the reference voltage of the second-stage DAC is set to 1.79 V. Simulations were performed with the typical transistor models and a temperature of 27°C. The V_{cm1} and V_{cm2} shown in the Fig. 5-8 are set at 35 mV and 600 mV, respectively. A 0.44 V voltage is chosen as the bias voltages of RC-delay elements (V_{bias1}, V_{bias2}) to create a delay of 7.6 μ s. Fig. 5-12 and Fig. 5-13 provide the simulated FFT spectrum of the proposed ADC with 1 kHz and 4.3 kHz inputs. The noise has been taken into account in the post-layout simulations. Simulated results show that the proposed ADC achieves a stable SNDR of 83.5 dB with a near-DC input tone and a Nyquist input tone.

Table 5-2 summarizes the ADC performance. With $V_{dd} = 1.8$ V for the analog and digital parts, the total power consumption is 2.39 μ W while the asynchronous clock generators consume 423 nW. The corresponding Schreier FoM of the proposed ADC is 176.7 dB. Thus, the above results demonstrate the correct operation and effectiveness of the proposed asynchronous clock generator.

To find the impact of the process corners on the entire ADC performance, three simulations were performed where the transistors are set as typical corner, fast corner and slow corner, respectively. Table 5-3 shows the simulated ADC performance across process corners at a temperature of 27°C. It is observed that the ADC could achieve a SNDR around 13.5-bit by tuning the V_{cm1} , V_{cm2} , V_{bias1} and V_{bias2} . Thus, for a fixed process corner, the optimal voltages of V_{cm1} , V_{cm2} and bias voltages of RC delay elements can be found which result in a best SNDR. Here, it should be pointed out that the delay generated by the RC network is still 7.6 μ s.

However, The above simulations are carried out at a temperature of 27°C. The effect of temperature on the ADC performance also needs to be evaluated. Table 5-4 presents the ADC performance with the typical corner but at a temperature range of

Figure 5-12: Simulated 2048-point FFT spectrums with 1 kHz input at 10 kS/s.

Figure 5-13: Simulated 2048-point FFT spectrums with 4.3 kHz input at 10 kS/s.

-40°C to 85°C. In order to create a delay of 7.6 μ s, the V_{bias1} and V_{bias2} are set as the following values shown in Table 5-4. With the $V_{cm1} = 35$ mV and $V_{cm2} = 600$ mV, the ADC maintains an acceptable SNDR at a temperature range of -40°C to 40°C. But, when the temperature is above 50°C, the SNDR drops fast due to the accumulated offset error caused by the source-follower utilized in the gain-stage. To compensate the offset error, the values of V_{cm1} and V_{cm2} should be readjusted. Table 5-5 provides the simulated results with the new V_{cm1} and V_{cm2} . It is seen that the ADC remains

Table 5-2: ADC performance summary

CMOS	0.18- μ m
Resolution (bits)	14
Sampling rate (kS/s)	10
SNDR (dB)	83.5 @ 1 kHz
SFDR (dB)	94.6 @ 1 kHz
ENOB (bits)	13.58 @ 1 kHz
Power Breakdown	
Asyn-clock generators (μ W)	0.423
SAR ADCs (μ W)	0.796
Gain-stage (μ W)	1.17
Total Power (μ W)	2.39
FoM (dB)	176.7

Table 5-3: ADC performance across process corners

Temperature 27°C	V_{cm1} (mV)	V_{cm2} (mV)	$V_{bias1} = V_{bias2}$ (mV)	SNDR (dB)	ENOB (bits)
CMOSTM	35	600	440	83.5	13.58
CMOSWP	83	600	380	83.6	13.59
CMOSWS	20	550	512	82.2	13.36

Table 5-4: ADC performance with different temperature, $V_{cm1} = 35$ mV and $V_{cm2} = 600$ mV

CMOSTM	$V_{bias1} = V_{bias2}$ (mV)	SNDR (dB)	ENOB (bits)
-40°C	606	79.4	12.9
0°C	510	83.4	13.56
27°C	440	83.5	13.58
40°C	405	80	13.0
50°C	375	63.8	10.3
85°C	275	48.7	7.8

its SNDR of 80 dB at a temperature of 85°C by choosing $V_{cm1} = 170$ mV and $V_{cm2} = 660$ mV.

From table 5-4, the bias voltages (V_{bias1} , V_{bias2}) vary with the temperature to generate a delay of 7.6 μ s. It indicates that the proposed RC delay is sensitive to the temperature. However, the variable delay time (t_{d1}) caused by the temperature will not affect the entire performance of the ADC if this value is still larger than the redistribution time of the DAC. In this work, simulation results show that the maximum settling time for the DAC is around 25 ns with 14-bit accuracy. Whereas, with $V_{bias1} = 0.44$ V, the minimum delay (t_{d1}) is 1.05 μ s under 85°C at the fast process corner. This delay is still long enough for the DAC to settle all the digital

Table 5-5: ADC performance versus temperature under different V_{cm1} , V_{cm2}

CMOSTM	V_{cm1} (mV)	V_{cm2} (mV)	$V_{bias1} = V_{bias2}$ (mV)	SNDR (dB)	ENOB (bits)
-40°C	10	387	606	81	13.16
0°C	10	530	510	83.7	13.61
27°C	35	600	440	83.5	13.58
40°C	55	625	405	83.3	13.54
50°C	70	645	375	82.8	13.46
85°C	170	660	275	80	13.0

codes. The simulation was performed under such conditions (85°C, fast corner) to verify this point. With $1.05 \mu\text{s}$ redistribution time for the DAC, the simulated SNDR is 80.9 dB. It should be mentioned that the $V_{bias2} = 220 \text{ mV}$ in order to maintain a amplifying time of $7.6 \mu\text{s}$ for the gain-stage.

In this work, the main purpose is to verify the functionality of the proposed clock generator. The delay is generated by the simple RC element which is sensitive to the temperature and further reduces the robustness of the ADC. Hence, it remains as a future work to find a robust delay solution instead of using the RC element.

5.7 Summary

An asynchronous clock generator for a low-speed, low-power two-stage pipelined SAR ADC was presented in this work. The proposed clocking scheme enabled to efficiently allocate the available time for the sub-DACs, the comparator and the gain-stage. The 3-stage capacitive charge pump with source follower as the gain-stage provided a voltage gain of 7.7. Using the proposed asynchronous clock generator and the gain-stage, a 14-bit two-stage pipelined SAR ADC was designed in $0.18\text{-}\mu\text{m}$ CMOS technology. The simulation results demonstrated the correct operation and effectiveness of the proposed asynchronous clock generator.

Chapter 6

Conclusions and Future Work

6.1 Conclusions

To detect the environmental information and the bio-potential signals, high-resolution (>12 -bit) ADCs with low-sampling rates (several kS/s) are required. Pipelined SAR ADC is an efficient architecture to achieve high-resolution for low-power applications. Design considerations for such ADC and the performance requirements of the key blocks were described in **Chapter 2**. Three pipelined SAR ADCs were presented in **Chapter 3**, **Chapter 4** and **Chapter 5**, respectively.

A 15-bit, 1 kS/s two-stage pipelined SAR ADC implemented in $0.35\text{-}\mu\text{m}$ CMOS process was presented in **Chapter 3**. A detailed analysis of the power consumption of the various sub-blocks facilitated the choice of suitable sub-ADC resolutions for the two pipeline stages. By employing substantial inter-stage gain reduction, the specifications of the OTA used in the residue amplifier were relaxed. Appropriate choice of DAC topologies in the sub-ADCs yielded considerable area and power savings by reducing the total capacitance requirement. Prototyped in a $0.35\text{-}\mu\text{m}$ CMOS process, the ADC achieves a competitive FoM among related works while maintaining an ENOB > 12.1 -bit up to the Nyquist bandwidth.

Aiming to further reduce the open-loop gain requirement of the OTA, the 3-stage capacitive charge pump as the gain-stage for a 14-bit two-stage pipelined SAR ADC was presented in **Chapter 4**. By employing the CCP as the gain-stage, the high open-loop gain OTA in the SC integrator was avoided while also reducing the design complexity. The prototype ADC achieved a peak SNDR of 75.6 dB at a sampling rate of 20 kS/s and 76.1 dB at a sampling rate of 200 kS/s while consuming $7.68\text{ }\mu\text{W}$ and $96\text{ }\mu\text{W}$, respectively. Due to the tunable bandwidth of CCP, the proposed ADC achieves a SNDR > 75 dB up to 260 kHz. The ADC also provides a competitive FoM among related works. Hence the multi-stage capacitive charge pump shows another

solution to achieve the function of the gain-stage instead of using the SC integrator for the low-speed, two-stage pipelined SAR ADC application.

Chapter 5 presented a 14-bit asynchronous two-stage pipelined SAR ADC. As the sensors might be active only for very short time triggered by an external pulse, an asynchronous clock generator was implemented in this work. The proposed flexible clocking scheme enabled to efficiently allocate the available time for the sub-DACs, the comparator and the gain-stage. The source follower as the analog buffer was used in the 3-stage CCP gain-stage. Using the proposed asynchronous clock generator and gain-stage, a 14-bit two-stage pipelined SAR ADC was designed in $0.18\text{-}\mu\text{m}$ CMOS technology. The correct operation and effectiveness of the proposed asynchronous clock generator were demonstrated by the simulation results. The ADC achieves an ENOB of 13.58-bit at a sampling frequency of 10 kHz, with a total power consumption of $2.39\text{ }\mu\text{W}$.

6.2 Future Work

In this thesis, the two-stage pipelined SAR ADC was utilized to achieve a resolution of 14-bit or 15-bit. The resolution of the sub-ADCs were allocated around half of the total resolution and the accuracy of the sub-ADCs were maintained below 12-bit even though the gain-reduction method was used. However, when the accuracy of the sub-ADCs is above 12-bit, the design of a SAR ADC with such resolution poses formidable challenges due to the requirements on the comparator noise and the capacitor matching. For instance, the 8-bit and 10-bit are allocated to the first and second sub-ADCs to achieve a 17-bit resolution. Also assuming the gain-stage provides a voltage gain of 16, then the accuracy of the second-stage should be 13-bit. Considering the complexity of designing a 13-bit SAR ADC, the two-stage pipelined SAR ADC is no longer a good candidate to meet with the 17-bit resolution. To mitigate the accuracy requirement of the sub-ADCs, a three-stage pipelined SAR ADC could be one solution. Therefore, the use of multi-stage (> 3) pipelined SAR ADC architecture to achieve a higher resolution needs to be investigated.

It is also realized during the chip measurement that a DC voltage generator with high precision and low noise is inevitable for a high-resolution ADC test. The noise from the reference generator should be as low as the quantization noise of the ADC. In this thesis, an external generator (Agilent B2962A) was used which has a very close noise specification. The noisy reference source becomes a primary concern for accuracy measurement. To alleviate this constraint, a low-noise on-chip regulator [81–83] could be implemented in the future. For the asynchronous clock generator proposed in Chapter 5, a delay-locked loop (DLL) could be used in the future work to generate a stable delay.

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Appendix A

Published Papers

Journals

- K. Chen, P. Harikumar, and A. Alvandpour, “Design of a 12.8 ENOB 1kS/s pipelined SAR ADC in 0.35- μm CMOS”, *Journal of Analog Integrated Circuits and Signal Processing*, vol. 86, no. 1, pp. 87-98, 2016. © Springer 2016.
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Conferences

- K. Chen, Q. T. Duong, and A. Alvandpour, “Power Analysis for Two-Stage High Resolution Pipelined SAR ADC”, *22nd Mixed Design of Integrated Circuits and Systems*, Toruń, Poland, pp. 496-499, June 25-27. 2015. © IEEE 2015.
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Papers

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