Design and analysis of high-speed split-segmented switched-capacitor DACs

Quoc-Tai Duong, Ameya Bhide and Atila Alvandpour

Journal Article

N.B.: When citing this work, cite the original article.

This is a copy of the original publication which is available at www.springerlink.com:

Quoc-Tai Duong, Ameya Bhide and Atila Alvandpour, Design and analysis of high-speed split-segmented switched-capacitor DACs, Analog Integrated Circuits and Signal Processing, 2017.

<http://dx.doi.org/10.1007/s10470-017-0981-8>

Copyright: Springer Verlag (Germany)

<http://www.springerlink.com>

Postprint available at: Linköping University Electronic Press

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-137058>

Design and Analysis of High-Speed Split-Segmented Switched-Capacitor DACs

Quoc-Tai Duong, *Student Member IEEE*, Ameya Bhide, *Student Member IEEE*,
and Atila Alvandpour, *Senior Member IEEE*

Abstract— In order to achieve high speed and high resolution for switched-capacitor (SC) digital-to-analog converters (DACs), an architecture of split-segmented SC DAC is proposed. The detailed design considerations of kT/C noise, capacitor mismatch, settling time and simultaneous switching noise (SSN) are mathematically analyzed and modelled. The design area $W-C_u$ is defined based on that analysis. It is used not only to identify the maximum speed and resolution but also to find the design point (W , C_u) for certain speed and resolution of SC DAC topology. The segmentation effects are also considered. An implementation example of this type of DACs is a 12-bit 6-6 split-segmented SC DAC designed in 65 nm CMOS. The linear open-loop output driver utilizing derivation superposition (DS) technique for nonlinear cancellation is used to drive off-chip load for the SC array without compromising its performance. The measured results show that the SC DAC achieves a 44 dB spurious free dynamic range (SFDR) within a 1 GHz bandwidth of input signal at 5 GS/s while consuming 50 mW from 1 V digital and 1.2 V analog supplies. The overall performance that was achieved from measurement is poorer than expected due to lower power supply rejection ratio (PSRR) in fabricated chip. This DAC can be used in transmitter baseband for wideband wireless communications.

Index Terms— high-speed DACs, SC DACs, 12-bit split-segmented DACs, linear output driver, wideband wireless communications.

I. INTRODUCTION

HIGH-SPEED digital-to-analog converters (DACs) are in demand for many modern electronic systems, including instrumentation applications, radar systems, and wideband reconfigurable radios. High-data-rate communication requires increasingly larger bandwidths, such as the recent wideband standards for UWB [1] and 60-GHz [2] radios.

The current-steering DAC architecture has received a lot of focus for wideband high-speed applications due to its simplicity and good performances among DACs [3-9]. Another class of DACs, which also has good potential in wideband high-speed applications, is the switched-capacitor DACs (SC DACs). However, it has not been drawn much attention except for few recent publications [10-12]. Fig. 1 shows the conceptual architecture of SC DACs. It consists of the SC array and output driver to drive the off-chip load (50Ω). Table I shows the overall comparison table of current

Figure 1. The conceptual architecture of SC DACs.

Figure 2. The SC DAC with track-and-hold circuit in [11].

TABLE I. THE OVERALL COMPARISON TABLE OF CURRENT STEERING AND SWITCHED-CAPACITOR DACs

Considerations	Current-steering DACs	Switched-capacitor DACs
Mode	Current	Voltage
Applications	Wireline and wireless applications	Wireless due to low output swing. For wireline, calibration of output driver is needed.
Frequency/BW	GHz range of BW, even higher	≤400 MHz signal BW so far
Used/popularity	Both “signal-path” DACs in transmitters and in feedback line of ADC are popular	Mostly used in ADC feedback like SAR ADC, except for 2 recent works [10, 11] about “signal-path” DACs in transmitters
Element matching	Requirement on current sources	Usually capacitor has better matching feature
Timing matching	Required	Required
Output impedance	Usually it limits DAC linearity	Not an issue for SC
Driving ability for off-chip loads	Good	Poor, need output driver
Power	Usually high due to static current sources	Usually low due to charge-redistribution based
Headroom/high supply	Need headroom	Just need for output drivers
PSRR	High/ good	Bad
Clock feed-through	Not an issue	Issue for pipeline SC arrays

-steering and switched-capacitor DACs. It can be seen that SC DACs have some advantages [10, 11]. Specifically, capacitors in SC DACs has good matching feature. The switches in the SC DAC arrays are realized by MOS transistors in the triode region which substantially relaxes the voltage headroom

Manuscript received January 24, 2017. This work was supported by Swedish Foundation for Strategic Research.

The authors are with the Dept. of Electrical Engineering, Linköping University, SE-581 83, Sweden, (email: quocaiduong@ameyabhi@gmail.com, atila@isy.liu.se).

Figure 3. The clock feed-through signal propagating to output in pipeline SC arrays.

Figure 4. The clock feed-through signal charged/discharged to supply/ground in segmented SC arrays.

requirement. The SC arrays thus have a supply-voltage scaling potential for more advanced deep sub-micron technology node. However, output driver still needs head-room and is not friendly with technology scaling. The power consumption can be low as its operation is based on charge redistribution.

The first part of capacitive DACs is the SC array. Previous implementations of high-speed capacitive DACs use the so-called pipeline architecture [10, 11]. Additionally, a time-interleaved topology of the pipeline SC was utilized to improve the speed of the DAC [11]. However, it can only work up to 800 MS/s due to the finite bandwidth of the track-and-hold circuit, as shown in Fig. 2. In order to meet the kT/C noise requirements, a large capacitor is required for the hold-operation, which limits speed. Moreover, based on the earlier study we have found that the pipeline capacitor array suffers from clock feed-through effect for high-resolution (12-bit) DACs [12]. Fig. 3 shows an example of the clock feed-through signal propagating to output. When switch Φ_2 is going to be off, the spike appears at node B. Then switch Φ_3 is on and transmitting it to node C since Φ_1 is off at that time. The spike will be added into the feed-through signal caused by Φ_3 at node C. Similarly the feed-through voltage is accumulated and propagated to output and causes distortion. The pipeline SC DAC also needs a precise multiple-phase clock, which is on-chip generated and resulting in some amount of power dissipation. The analysis in [12] shows that it is not feasible to design beyond 8-bit resolution DAC at 3 GS/s.

Another important part of capacitive DACs is the output driver. The ability to drive off-chip load of SC arrays is poor, so a suitable output driver is necessary. This driver is critical for the linearity of a capacitive DAC when a high output voltage swing is required [11]. One solution to this problem is using a closed-loop architecture where the circuit linearity is improved by negative feedback [10]. However, the performance of this technique cannot be maintained at high

frequencies (> 1 GHz) due to the loop bandwidth limitation. Another solution is an open-loop driver design that can be supported by a pre-distortion calibration [11]. However, it requires a huge memory of a lookup table for dynamic pre-distortion. For example, it would need 562 TB of memory for 12-bit DAC calibration [13]. Moreover, only static nonlinearities can be calibrated using a low-but-accurate ADC (in feedback loop), while the presence of significant dynamic nonlinearities would force the ADC to sample at least at the DAC update rate [14].

A split-segmented SC array topology can overcome the above limitations of the pipeline SC DAC arrays, such as the clock feed-through problem, since it can get rid of pipelined charge propagating to the output. As shown in Fig. 4, any clock feed-through voltage will be charged/discharged to supply/ground since either switch U_i or U_{b_i} is on at any time. Moreover, this SC array works based on charge/voltage division so it does not need the track-and-hold circuit. Also, by avoiding the multiple-phase clocks for the proposed SC array, power can be saved and timing challenges due to multi-phase clocks can be avoided. The split-segmented SC array can work at even higher speed (5 GS/s) since it is not limited by kT/C noise due to absence of the track-and-hold circuit.

This work proposes an architecture of split-segmented SC DAC to overcome the clock feed-through issue from pipeline SC DAC. The detailed design considerations of kT/C noise, capacitor mismatch, settling time and simultaneous switching noise (SSN) are mathematically analyzed and modelled to define design area $W-C_u$. It is used not only to identify the maximum speed and resolution but also to find the suitable design point (W, C_u) for certain speed and resolution of SC DAC topology. The segmentation effects are also considered.

In order to design a driver to be able to work at high frequency (> 1 GHz) without using any form of calibration, this work also proposes a linear open-loop driver which uses the technique of derivative superposition (DS) [15] for canceling both second and third-order harmonic distortion to drive the proposed split-segmented SC array. Since the output swing of DAC is low suitable for wireless applications, non-linearity of driver is found not the main limiting factor.

The most recent implementations of SC DACs have previously been reported a maximum sampling rate up to 800 MS/s [11] for a BW of 400 MHz. Hence, this work aims to further extend the signal BW of SC DACs up to 1 GHz using a proposed split-segmented architecture and an open-loop output driver. Additionally, the design and analysis of the output driver using Volterra Series [16] are also presented. The experimental prototype shows that SC DAC can work up to more than 3 GS/s. However, SFDR is limited by SSN which requires sufficient PSRR. It has potential to improve SFDR when SSN still has room to be reduced by using more advanced packaging techniques such as flip-chip, 3-D packaging. Another way for reducing SSN effect is to use additional circuits to improve PSRR for SC arrays.

The remainder of this paper is arranged as follows. In Section II the split-segmented SC DAC architecture is presented. Analyses of the SC array are provided in Section

Figure 5. The n -bit split-segmented (m) SC DAC architecture.

III. The definition of design area W - C_u and the way how to find design point (W , C_u) are described in this section. Section IV presents the output driver design and analysis. Section V provides chip implementation and measured results of the complete 12-bit SC DAC. Conclusions are formulated in the last section.

II. A SPLIT-SEGMENTED SC DAC ARCHITECTURE

The proposed capacitive DAC architecture is shown in Fig. 5. Assuming segmentation of m most significant bit (MSB) thermometer bits and $(n-m)$ least significant bit (LSB) binary bits for n -bit resolution SC DACs is considered. Moreover, two attenuated capacitors in the middle for reducing capacitance spread [17] create two split-binary segments of k_1 bits and k_2 bits. The mux-based thermometer decoder can be used to convert m MSBs of the input to (2^m-1) unary bits since it is more suitable for high speed than the logic-based decoder [18]. It can be designed based on the previous work of the 5–32 decoder in [5] with some modifications according to the particular specifications. The SC cell is based on capacitor/voltage divider and linearly proportional to reference voltage V_{ref} , unit capacitance C_u , output capacitance C_{filter} according to (1-2).

The charge-divider based SC array topology shown in Fig. 4 is used to eliminate clock feed-through issue. The feed-through voltage at the internal node A between switch U_i and Ub_i in

Fig. 5 will be immediately charged/ discharged to V_{ref}/GND since when one of these switches is off, another will be on, and vice versa. How to design unit capacitance C_u and switch size W will be described in section III. The linear open-loop output driver which will be described in details in Section IV is used to drive off-chip load ($50\ \Omega$ matching from equipment). Neglecting all parasitic capacitances for simplicity, the output voltage of SC arrays is linearly dependent on the values of the input data U_i , b_i , supply V_{ref} , unit capacitance C_u , and output capacitance C_{filter} as

$$V_{out} = V_{ref} G_c \left(\sum_{i=0}^{2^m-1} U_i + \frac{1}{2^{k_1}-1} \left(\sum_{i=0}^{k_1-1} b_i 2^i + \frac{1}{2^{k_2}-1} \sum_{i=0}^{k_2-1} b_i 2^i \right) \right), \quad (1)$$

where

$$G_c = \frac{C_u}{(2^m-1)C_u + C_{filter}}, \quad (2)$$

and the attenuation capacitances C_{atten1} and C_{atten2} are proportional to the unit capacitance C_u [17], $C_{atten1} = 2^{k_1} C_u / (2^{k_1}-1)$, $C_{atten2} = 2^{k_2} C_u / (2^{k_2}-1)$.

III. THE ANALYSES OF SC ARRAY

In order to identify the maximum speed and resolution that SC DAC can work and find the suitable values for the switch sizes and unit capacitance for certain speed and resolution, this section describes the analysis of kT/C noise, capacitor mismatch, settling time effect and simultaneous switching noise (SSN) in the n -bit split-segmented SC arrays. The design

Figure 7. V_{DNL} standard deviation comparison of estimated model (11) and SpectreRFTM MC simulations against 1/6 LSB voltage of 12 bit DAC.

Figure 8. Equivalent circuit model for on/off-resistance: a) high data (charge); b) low data (discharge).

are assumed ideal and the simulation count is 100. A very low clock frequency was used to verify the static V_{DNL} with input data of MSB transition [27]. We usually use 3σ standard, meaning that $3\sigma(V_{DNL})$ should be less than a half of V_{LSB} . The limitation line shown in Fig. 7 is therefore one sixth of V_{LSB} of 12-bit resolution DAC which is 12 μ V with $V_{FS} = 0.3$ V. The V_{DNL} standard deviations are in [0.1-1] nV range while those from simulation are tracking with around half less than this. The results from simulation are lower than the ones from estimation because in calculation we assumed total variation of mismatch as maximum [27] while the variation of unit capacitors mismatch in Monte-Carlo (MC) simulation is randomly distributed. Importantly, the both values are by orders of magnitude less than the limitation voltage of 12-bit DAC. Therefore the limit due to the capacitor mismatch can be neglected for 12-bit resolution and metal-to-metal unit capacitor.

C. Settling time

Due to imperfections of the transistor switches (R_{off} / R_{on} resistances) the leakage and incomplete settling in the capacitor array result in voltage errors which degrade DAC linearity [19]. Firstly the upper bound of on-resistance of switch is estimated. When switch is on, the time-constant will be $R_{on}C_u$ due to $C_{filter} \gg C_u$ as shown in Fig. 8. The maximum charged/discharged voltage error due to settling time should be less than a half LSB voltage of n -bit DAC

$$V_{ref} e^{\frac{-t_{on}}{R_{on}C_u}} < \frac{1}{2} \frac{V_{FS}}{2^n}, \quad (13)$$

where $t_{on} \approx T_s/2 = 1/2f_s$ is pulse width of clock cycle T_s , V_{ref} is voltage supply for SC, C_u is value of unit capacitance. Therefore for assuming $V_{ref} = V_{FS}$, one of upper bounds of R_{on} can be found as

$$R_{on} < \frac{1}{2f_s C_u} \frac{1}{\ln(2^{n+1})}. \quad (14)$$

For example, with $n = 12$, $C_u = 10$ fF, $f_s = 3$ GS/s, $C_{filter} = 2$ pF, the on-resistance of switches should be less than 1.85 K Ω .

The circuit model due to off-resistance effect is shown in Fig. 8. If data is high, transistor switches to supply V_{ref} shown in Fig. 8a while data is low switch is on to GND shown in Fig. 8b. In both cases, the voltage error due to leakage is the same

$$\Delta V = \frac{R_{on}}{R_{on} + R_{off}} V_{ref}. \quad (15)$$

We have to keep this voltage error less than a half LSB of n -bit DAC with the same assumption of $C_{filter} \gg C_u$ as

$$\frac{R_{on}}{R_{on} + R_{off}} V_{ref} < \frac{1}{2} \frac{V_{FS}}{2^n}. \quad (16)$$

From this condition, the lower bound of off-resistance can be obtained

$$R_{off} > (2^{n+1} - 1) R_{on}. \quad (17)$$

However, this voltage error does not cause distortion for DAC output since it has the same effect for all of branches with assumption that all switches have the same R_{on} and R_{off} . Instead, it reduces output swing due to voltage drop on R_{on} by leakage current through R_{off} . Simulation shows that R_{off} has negligible effect on the linearity of DAC.

D. Capacitance parasitic effects

Parasitic capacitances C_{parp} and C_{parn} of PMOS and NMOS switches in Fig. 9 cause distortion through settling time by adding more capacitances. When $b_k = 1$, the node at $V_{ref,k}$ is supposed to charge to V_{ref} . For the worst case, while we assume voltage at V_{out} now is zero the total capacitance to be charged is $(C_k + C_{parn,k}) = (C_u + C_{par})$ for assumption of $C_{parp} = C_{parn} = C_{par}$. The parasitic will be added to C_u in equation (14) for the upper bound of R_{on}

$$R_{on} < \frac{1}{2f_s (C_u + C_{par})} \frac{1}{\ln(2^{n+1})}. \quad (18)$$

The upper bound of C_u is calculated from (18) as

$$C_u < \frac{1}{2f_s R_{on}} \frac{1}{\ln(2^{n+1})} - C_{par}. \quad (19)$$

It can be seen in (19) that parasitic capacitance C_{par} narrows down the range of unit cap C_u .

Figure 9. Equivalent circuit model for parasitic capacitances.

Figure 10. (a) Wire-bonding model. (b) Separating supplies to reduce noise.

Figure 11. Damping/filtering noise on signal paths for improving PSRR.

E. Simultaneous switching noise (SSN)

The linearity of high-resolution and high-speed SC DAC is significantly limited by simultaneous switching noise (SSN) caused by the parasitic inductance of the bonding wires shown in Fig. 10a. The decoupling capacitors (de-caps) C_{decap} are locally used on-chip for keeping the internal supply stable and have equivalent parasitic resistance R_{decap} . Each supply has two bonds V_{DD} and V_{SS} which can be modelled as RCL [20-23]. Typically, the inductances L_{DD} and L_{SS} are dominant and cause ripple/noise on internal supply since the series resistances (R_{SS} , R_{DD}) and package capacitances (C_{DD} , C_{SS}) have less effects.

The self-inductances (L_{DD} , L_{SS}) of a round wire can be estimated as [23]

$$L \approx \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{R}\right) - 0.75 \right], \quad (20)$$

where L stands for the inductance per unit length, R for radius of the conductor, l for length of bond wires, and μ_0 for permittivity of free space. For typical bond wires, L approximates 1 nH/mm. The maximum SSN voltage is estimated in [21] as

$$v_{n,max} \approx \frac{mkL_{SS}\beta_n}{2kt_r + 2m(k-1)L_{SS}\beta_n} V_{DD}, \quad (21)$$

where m is number of drivers, β_n is the device transconductance value near the switching threshold voltage $V_{switch} \approx V_{DD}/2$, $\beta_n \approx \mu_n C_{ox}(W/L)_n(V_{switch} - V_{th})[A/V^{\alpha}]$. For sub-micron MOSFETs, alpha (α) is in the range of {1-2}. The t_r is the rise time. The constant $k = 3$ can be used according to [21], the formula (21) can be rewritten as

$$v_{n,max} \approx \frac{mL_{SS}\beta_n}{2t_r + 1.3mL_{SS}\beta_n} V_{DD}. \quad (22)$$

There are several ways to reduce SSN. Separating supplies as shown in Fig. 10b is one of the ways which can be used to avoid noise effect each other with different supplies. The deep-NWell (DNW) layer and guard rings can also be used to eliminate the body effect and to have more isolation respectively. Based on the voltage error model in (22) SSN can be reduced by minimizing inductance L . Using multiple bond-wires, n wires for example, of each supply makes the effective inductances lower by $1/\sqrt{n}$ due to mutual effects. Quite big de-caps (MIM cap and MOS cap) can be utilized to locally suppress noise as long as area is allowed. Many parallel de-caps with different values to achieve different self-resonant frequencies (SRF) and equivalent series resistances (ESR) are soldered on-board to filter out different-frequency noise. Damping resistors can also be used to eliminate noise [20-21].

Another damping/ filtering technique applied on the signal path were introduced and used in this design as shown in Fig. 11. Simulation shows that it can improve around 6 dB SSN since ripple voltage on signal path is reduced around half. It can be understood from another perspective that this filtering technique improves power supply rejection ratio (PSRR) for SC DACs. The low values of $R = 10 \Omega$, $C = 600$ fF are used to avoid the signal loss which causes reducing the voltage swing of DAC. Since voltage drop on R is negligible and its cut-off frequency is high ($f_c = 53$ GHz) this technique has no side effect on the output. This RC filter helps to improve DAC performance not by filtering signal, but by suppressing SSN through damping resistor R hence improving PSRR.

The SSN on the supply of switch-driver is the most critical since bigger sizes of switches have been used for fast switching. The upper bound of transistor sizes can be found based on (22). This maximum noise voltage should be less than a half LSB of n -bit DAC

$$v_{n,max} < \frac{1}{2} \frac{V_{FS}}{2^n}. \quad (23)$$

From (22-23), the upper bound of switch sizes can be found

Figure 12. SFDR of SC DAC versus SSN voltage (RMS).

Figure 13. Reference generator to enhance PSRR.

$$\left(\frac{W}{L}\right)_n < \frac{2t_r V_{FS}}{\mu_n C_{ox} \left(\frac{V_{DD}}{2} - V_{th}\right) (mL_{SS} V_{DD} 2^{n+1} - 1.3mL_{SS} V_{FS})}. \quad (24)$$

Based on formula (24), the transistor sizes of switches in the switch-driver can be chosen depending on the rise time of clock t_r , supply (V_{DD}), the output swing (V_{FS}), the DAC resolution (n), parasitic inductance of bonding-wires (L_{SS}) and technology ($\mu_n C_{ox}$).

Fig. 12 shows SFDR change versus SSN voltage with assumption signal voltage of 400 mV_{pp} (output swing of SC arrays), PSRR of SC DAC equal to 0 dB. SSN voltage of 0.1 mV_{rms} is required to have 60 dB SFDR which is very tough to achieve. It is therefore necessary to have reference voltage generator to provide sufficient power supply rejection ratio (PSRR). One of the simple ways is to use a reference generator shown in Fig. 13.

F. Define design area W - C_u

In order to identify the maximum resolution and sampling rate that SC DAC can be designed, this section defines the design area W - C_u based on the above analytical considerations of kT/C noise, capacitor mismatch, settling time and SSN. The parameters W and C_u are the width of switches with minimum length and value of unit capacitance, respectively. This methodology is also used to select an appropriate design point (W , C_u) for a certain resolution and speed of SC DACs.

First, kT/C noise (8) is considered. Fig. 14 shows the quantization and kT/C noise versus sizes of switches and unit capacitance at 5 GS/s for different resolutions. Fig. 14a shows that kT/C noise does not limit performance for 12-bit (6-6

Figure 14. Quantization and kT/C noise versus sizes of switches and unit capacitance at 5 GS/s for different resolutions (12 bits and 13 bits).

Figure 15. SSN and half LSB versus switch sizes with different resolutions (12 bits and 13 bits) at 5 GS/s for PSRR $\approx$ 40 dB.

segmentation) DACs since it is always less than quantization noise (assuming the output swing of overall DAC equal to 0.3 V_{pp}). Theoretically, it is possible to design 13-bit (7-6 segmentation) DACs if either $C_u > 30$ fF for small W (≈ 1 um) or $C_u > 40$ fF for large W (≈ 40 um) is chosen as shown in Fig. 14b. The kT/C noise is almost independent on clock frequency.

Second, simultaneous switching noise (SSN) (22) is considered. Fig. 15 shows SSN versus switch sizes with different resolutions at 5 GS/s for PSRR $\approx$ 40 dB. SSN is mainly dependent on the sizes of switch drivers and independent on C_u (22). In this case the assumption that the main switch size is two times bigger than the switch driver size is used. PSRR of 40 dB can be achieved from reference generator, big decoupling capacitors and several techniques that are described in SSN section above. By comparing between SSN voltage and half LSB voltage, the bounds of $W < 3.5$ um for 12 bits and $W < 0.3$ um for 13 bits are found in Fig. 15. This higher bound of switch sizes will change according to PSRR. A larger range of W can be achieved with higher PSRR and vice versa.

SSN is also dependent on clock frequency and Fig. 16 shows SSN versus switch sizes with different sampling rates of 5 GS/s and 8 GS/s for PSRR $\approx$ 40 dB and 12-bit resolution. By comparing between SSN voltage and half LSB voltage, the

Figure 16. SSN versus switch sizes with different sampling rates ($f_s = 5$ GHz and $f_s = 8$ GHz) for PSRR ≈ 40 dB and 12-bit resolution.

bounds of $W < 3.5$ μm for 5 GS/s and $W < 2.2$ μm for 8 GS/s are found in Fig. 16.

Design area W - C_u :

The design area W - C_u is defined based on the lower and upper bounds of W and C_u caused by kT/C noise, SSN, settling time and capacitor mismatch. For example, Fig. 17 shows design area W - C_u of 12-bit (6-6 segmentation) and 13-bit (7-6 segmentation) SC DACs for clock frequency $f_s = 5$ GHz. The solid lines which consist of SSN (22), settling time (19) and mismatch (12) are upper/lower bounds of 12-bit SC DACs. The mismatch coefficients in (12) are taken from 65 nm CMOS process. The parasitic capacitance of each switch in (18) is assumed to 5 fF maximum. The kT/C noise is not considered for 12-bit resolution since it meets requirement shown in Fig. 14a. The area, which is limited by $W < 3.5$ μm from SSN, $C_u > 0.4$ fF from capacitor mismatch, $C_u <$ the solid line from settling time effect, is the design area W - C_u of 12-bit SC DAC at 5 GS/s. The design point of $(W, C_u) = (2$ $\mu\text{m}, 15$ fF) can be chosen for implementation as shown in Fig. 17. Similarly, the design area W - C_u of 13-bit SC DAC at 5 GS/s can be defined. However, this area is much shrunk and closed to the origin since SSN condition pushes $W < 0.3$ μm . Moreover, the effect of kT/C noise appears for 13-bit DAC as shown in Fig. 14b. It means that the design area now does not exist anymore since another lower bound of $C_u \approx 35$ fF from kT/C noise appears in Fig. 17.

Another example is to consider the effect of the clock frequency on the design area W - C_u which is shown in Fig. 18. It is only bounded by the effects of SSN, settling time and capacitor mismatch since kT/C noise is always less than quantization noise (shown in Fig. 14a). Fig. 18 shows that it is theoretically possible to design a 12-bit SC DAC at 8 GS/s.

Segmentation effects:

The design area W - C_u is affected by segmentation ratio since kT/C and SSN are dependent on number of thermometer bits m . Segmentation does not have much effect on settling time and mismatch since time-constant RC is normalized for every switch and only the worst case is considered, respectively.

From Fig. 14b and Fig. 17, it can be seen that it is not

Figure 17. Design area (W - C_u) of 12-bit and 13-bit SC DACs for clock frequency $f_s = 5$ GHz.

Figure 18. Design area W - C_u for 12-bit SC DAC with clock frequency $f_s = 5$ GHz and $f_s = 8$ GHz.

(a) Segmentation ratios (7-6) (b) Segmentation ratios (5-8)

Figure 19. Quantization and kT/C noise versus sizes of switches and unit capacitance at 5 GS/s with different segmentation ratios (7-6 and 5-8) for 13-bit SC DACs.

possible to design 13-bit SC DAC at 5 GS/s with the 7-6 segmentation. However, if the 5-8 segmentation is used, DAC performance is not limited by kT/C anymore as shown in

Figure 20. Design area ($W-C_u$) of different segmentation ratios (5-8 and 7-6) for clock frequency $f_s = 5$ GHz and 13-bit SC DACs.

Figure 21. (a) Source-follower (SF) buffer. (b) Second and third-order distortion terms of the buffer using ST 65nm CMOS process.

Fig.19b and design area now exists although it is small as shown in Fig. 20. Theoretically it is possible to design 13-bit SC DAC with 5-8 segmentation at 5 GS/s. Segmentation ratio of split-binary bits does not have much effect on design area.

IV. OUTPUT DRIVER DESIGN AND ANALYSIS

A. Design

The output driver is used to drive the off-chip load (50 Ω) of the capacitive DACs since the SC array does not have the driving capability [10–11]. The driver appears as the most critical circuit causing distortion for capacitive DACs unless the required output voltage swing is low. One solution to this problem is using a closed-loop architecture where the circuit linearity is improved by negative feedback [10]. This technique, however, cannot work well at high frequencies (> 1 GHz). Open-loop output drivers that can be supported by a pre-distortion technique [11] is another solution. However, the latter is usually limited by an assumption of minimum memory effect of the nonlinear object and requires highly precise ADC in the feedback path [13–14].

To avoid the complicated calibration and be able to work at high frequency (GHz range), the open-loop output driver with non-linearity cancellation technique can be used [12]. It shows potential for wireless application which needs around 300 mV_{pp} of DAC output to drive mixers. In this design of output

Figure 22. (a) DS technique in SF buffer. (b) Third-order distortion terms of the main transistor (g_{3n}), auxiliary transistor (g_{3p}), and total output (g_3). (c) Second-order distortion terms of the main transistor (g_{2n}), auxiliary transistor (g_{2p}), and total output (g_2) using ST 65nm CMOS process.

Figure 23. Equivalent circuit of the proposed linear output driver.

driver, we also used open-loop topology and the derivative superposition (DS) technique to achieve high linearity, low power with standard supply of 1.2 V.

The conventional source-follower (SF) buffer is shown in Fig. 21a. The optimal bias for minimizing the third-order transconductance g_3 is very narrow around $V_{bias} = 0.9$ V as shown in Fig. 21b. Moreover, the g_2 is quite high at the same bias point. The derivative superposition (DS) technique introduced in [15] was used to cancel the third-order harmonic distortion for the radio frequency (RF) amplifier. Using DS technique, this proposed output driver achieves the cancellation of both g_3 and g_2 at the same input range (0.8 – 1.2 V) as shown in Fig. 22.

B. Analysis using Volterra series model

The equivalent model of output driver is shown in Fig. 23. The parasitic resistances and capacitances r_{oA} , r_{oB} , C_{gsA} and C_{gsB} of the two transistors can be merged as $Z_{out} = (Z_{load} \parallel r_{oA} \parallel r_{oB})$ and $C_{gs} = C_{gsA} + C_{gsB}$.

The harmonic distortion of output driver can be estimated using the Volterra series model [16]. The two-tone (ω_A and ω_B) sinusoidal signal with the same amplitude A for each is applied at the driver input. We focus on the third-order distortion as it prevails over the other distortions

$$HD3 = \frac{1}{4} \frac{|G_3(j\omega_1, j\omega_1, j\omega_1)|}{|G_1(j\omega_1)|} A^2, \quad (25)$$

Figure 24. HD3 comparison of analytical expressions (26) and SpectreRF™ simulations for the proposed output driver.

Figure 25. HD3 and HD2 versus frequency with 5% mismatch.

Figure 26. HD3 and HD2 versus bias voltage with 5% mismatch.

Figure 27. HD3 and HD2 versus temperature with 5% mismatch.

where $\omega_1 = \pm\omega_A$ or $\pm\omega_B$. Using (25) and (A.16-A.19) of Appendix-B we can calculate HD3 of the output voltage of the proposed circuit as

$$HD3 = \frac{A^2}{4} \left| \frac{Z_{OUT}(\omega_1 + \omega_2 + \omega_3) \left[(g_{3A} + g_{3B})(1 - G_1(\omega))^3 - 2(g_{2A} - g_{2B})[G_2(\omega_1 + \omega_2) - \overline{G_2(\omega_1 + \omega_2)}G_1(\omega)] \right]}{Z_{OUT}(\omega)(g_{1A} + g_{1B} + j\omega C_{gs})} \right|, \quad (26)$$

$$\times \left| \frac{1 + Z_{OUT}(\omega)(g_{1A} + g_{1B} + j\omega C_{gs})}{1 + Z_{OUT}(\omega_1 + \omega_2 + \omega_3)[g_{1A} + g_{1B} + j(\omega_1 + \omega_2 + \omega_3)C_{gs}]} \right|$$

where $(\omega_1 + \omega_2) = (\pm\omega_A \pm \omega_B)$, $(\omega_1 + \omega_2 + \omega_3) = (\pm\omega_A \pm \omega_B \pm \omega_B)$ or $(\pm\omega_A \pm \omega_B \pm \omega_A)$ in general [16]. The comparisons of HD3 between analytical expressions (26) and SpectreRF™ simulations for the proposed output driver with supply of 1.2V are shown in Fig. 24. They are quite match with different values of parasitic capacitance C_{gs} .

The nominator of second term in (26) is supposed to be closed to zero at low frequency in the working bias range in Fig. 22b. It is a function of frequency which makes degradation for HD3 at high frequency in Fig. 24. Looking at the third term in (26), we can see that C_{gs} help to improve HD3 at high frequency because its denominator is proportional with $3x\omega$ while the nominator is a function of $1x\omega$. This phenomenon can be seen by simulation verification shown in Fig. 24. Both curves of analytical and simulated results where $C_{gs} = 2$ pF is applied are better than the ones where smaller C_{gs} is used.

C. Thermal noise analysis

The output noise due to thermal noise of output driver is calculated based on the previous work [12] as

$$\overline{e_n^2} \approx 4kT \left(\frac{\gamma}{g_m} + \frac{1}{g_m^2 R_{OUT}} + \frac{R_B}{2} \right) \left(\frac{1}{1 + \frac{1}{g_m R_{OUT}}} \right) \quad (27)$$

where $g_m = g_{1A} + g_{1B} = 129$ mS is the total trans-conductance of driver, $R_{OUT} = 50 \Omega$ is load resistance, $R_B = 1$ k Ω is the bias resistance, $\gamma \approx 2/3$. It approximates -173 dB/Hz. The total noise at frequency of 5 GHz for example is -76 dB which is less than -72 dB required for 12-bit resolution.

D. Simulation results

With specification of 300 mV output swing and assuming 5 % between two branches of pseudo-differential circuitry, the output driver is simulated in 65 nm CMOS technology. Within the band of 0.5–4 GHz, HD2 < -82 dB and HD3 < -78 dB are attained as shown in Fig. 25. The dependence of HD2 and HD3 on the bias voltage is demonstrated in Fig. 26. HD3 < -81 dB and HD2 < -82 dB are achieved with the change of bias voltage from 0.85 V to 1.25 V. The temperature variation effect on the linearity of driver is also verified and shown in Fig. 27. HD2 is better with higher temperature whereas HD3 is always less than -80 dB in the range of -20–100 °C.

Under different corner of process as shown in Table II, both HD2 and HD3 are better than -74 dB which is good enough for driving the 12-bit SC DAC.

TABLE II. HD2 AND HD3 VERSUS DIFFERENT CORNERS WITH 5% MISMATCH

Corner	HD2 (dB)	HD3 (dB)
TT	-84	-81
FF	-94	-81
FS	-85	-80
SF	-96	-81
SS	-74	-75

Figure 28. Measurement setup of DAC with on-chip memory.

Figure 29. Overall clock distribution.

V. CHIP IMPLEMENTATION AND MEASURED RESULTS

The measurement setup with on-chip memory for SC DAC testing is shown in Fig. 28. An integrated circuit (IC) was fabricated in a standard 65-nm CMOS technology and bonded to an RF PCB. In order to generate 12-bit data input for full speed testing of the DAC, the 1-Kbit memory has been implemented on-chip [24]. It is written into serially at a low speed (1 MHz) by an FPGA and then read at full speed internally during the DAC operation. The 32-bit data is split into two 16-bit streams representing odd and even data, then multiplexed using $f_s/2$ clock to obtain two 8-bit data. However, this design only uses 12 bits of the 16 bits. Therefore the memory allows only a 64-point deep signal to be tested and hence the minimum frequency bin spacing in the input signal is $f_s/64$. The sinusoidal differential signal is provided by signal generator and converted to rectangular wave by the internal clock drivers. The strategy of overall clock distribution is shown in Fig. 29. The two-channel interleaving of 16 bits uses $f_s/2$ for reading data out. The H-tree topology is used to distribute pseudo-differential clocks for the switch-drivers of switched-capacitor arrays. The total chip occupies 1.2x1.7 mm² shown in Fig. 30. Almost half of the chip area is occupied by the memory and decaps. Metal-to-metal capacitors are used for both unit and attenuated capacitor since it has better a matching. Moreover, MIM capacitors cannot be used since its minimum value is limited by the foundry process.

Figure 30. Chip photo.

Figure 31. Measured 44 dB SFDR with a 1 GHz single tone at 5 GS/s.

Figure 32. Measured 64 dB SFDR with a 16 MHz single tone at 1 GS/s.

Figure 33. Measured IM3 of -38 dBc with two tones (860 MHz and 1.02 GHz) at 5 GS/s.

In order to reduce parasitic capacitance to the substrate, the bottom plate of C_{atten} is connected towards the output. To have more density layout for saving area, the multi-layer (M2-M3, M3-M4, M4-M5) metal-to-metal capacitors were used.

Similar to the current-steering DACs having limiting factors such as device noise, output impedance, signal swing and switching speed described in [28], design of layout to meet the target specifications mentioned in section III for switched-capacitor DACs is challenging.

Figure 34. Measured SFDR comparison of this work with others (CS: current-steering, SC: switched-capacitor).

Figure 35. Measured SFDR versus output frequency (f_{out}) at 5 GS/s with 1.2 V and 0.9 V supply.

Figure 36. Measured SFDR versus output frequency (f_{out}) with different f_s .

Figure 37. Measured IM3 versus tone spacing with different f_{out} at $f_s = 5$ GHz.

Figure 38. Measured spectral mask to show potential for use in 60-GHz radio.

TABLE III. POWER AND AREA BREAKDOWN OF THE DAC BY FUNCTION

Power		Area	
Function	Power (mW)	Block	Area
Decoder	11	Decoder	$100 \times 120 \mu\text{m}^2$
SW Driver	14	SW Driver	$40 \times 700 \mu\text{m}^2$
SC	7	SC	$140 \times 700 \mu\text{m}^2$
Output Driver	10	Output Driver	$230 \times 220 \mu\text{m}^2$
Clock Distr.	8	-	-
Total	50	Total	0.19 mm^2

The main layout challenges can be described. For high resolution DAC, 12 bit for example, there are a large number of unit cells distributed in large layout areas. In order to provide clock to them with minimum skew and mismatch is one of the main challenges. To implement clock distribution as shown in Fig. 29 optimization of numbers of buffers and their sizes is required, especially at high frequency (> 1 GHz). Parasitic of routings could affect unit capacitance and on-resistance so it is necessary to position unit cells in a good way and use high layers of metals for minimizing parasitic. The connections of output signals of DACs have to be taken care as well. The top layers of metal and tree-architecture are used to equalize and minimize parasitic.

Moreover, routings of supplies to switch drivers and unit cells also use similar strategy for reducing supply impacts. To reduce mismatch and parasitic, the active devices have to be placed closed together limiting spaces for internal decoupling capacitors to keep internal supplies stable.

SC DAC can work up to 5 GS/s for 1 GHz bandwidth (BW) and achieves 44 dB SFDR as shown in Fig. 31. In silicon chip, more SSN and worse PSRR than expected degrade linearity of DAC. It has potential to improve SFDR when SSN still has room to be improved by using more advanced packaging techniques such as flip-chip, 3-D packaging. Another way for reducing SSN effect is to use additional circuits to improve PSRR for SC arrays. Nonlinearity of output driver is not the most critical in this case since the output swing is low (300 mV_{pp}) and it has used circuit techniques of linearization. At lower frequency ($f_s = 1$ GS/s, BW = 16 MHz), the better SFDR of 64 dB is achieved as shown in Fig. 32.

As mentioned above, due to a 64-point deep signal to be tested the minimum frequency bin spacing in the input signal is $f_s/64$. Fig. 33 shows the measured IM3 of -38 dBc at $f_s = 5$ GS/s for 860 MHz and 1.02 GHz of two tones. The measured SFDR, IM3 of this work and comparison with others are shown in Fig. 34. For the bandwidth up to 1 GHz of input signal the SFDR > 44 dB are achieved. The SFDR is better than 50 dB for input frequency up to 800 MHz while IM3 is lower than -50 dBc for $f_{in} < 700$ MHz. This design achieves the highest speed among the previous reported works in the same type of SC DACs. The total power consumption is 50 mW from 1 V digital (40 mW) and 1.2 V (10 mW) analog supplies. The power and area breakdown of the SC DAC is shown in Table III. The total core area including clock distribution is approximate 0.2 mm^2 .

TABLE IV. COMPARISON OF THIS WORK WITH STATE-OF-THE-ART REPORTED DACS

Ref	DAC type	Tech. [nm]	Supply [V]	Fclk [GHz]	BW [GHz]	SFDR [dB]	IM3 [dB]	Noise [dBc/Hz]	Swing [Vppd]	Power [mW]	Bits	FOM3 [10 ¹²]
[24] Ameya JSSC15	$\Delta\Sigma$	65	1.2/1	11	1.1	53	-49	-	0.5	117	8	2.1
[9] Erik JSSC 15	Current steering	28	1	11	5.5	>50	<-50	-130	0.425	110	9	6.7
[8] Georgi TVLSI 15	Current steering	28	2.5/1.4	7	1	50	-50		0.25	145	6	0.55
[26] Yuriy ISSC 11	Current steering	65	2.5/1.1	56	26.9	30	-		0.6	750	6	0.7
[7]Shiyu JSSC 15	Hybrid	65	2.5/1.2	1	0.5	75	-	-162	0.4*	430	12	3
[4] Lin JSSC 09	Current steering	65	2.5	2.9	0.66	50	-67		2.5	188	12	3.8
[11] Daigle ASSC 10	SC	90	2.5/1.2	0.8	0.4	53	-	-140	2.9	103	12	5
[10] Manganaro JSSC 04	SC	500	3.3	0.2	0.034	70	-		2	693	10	0.3
This work	SC	65	1.2	5	0.8/1	50/44	-45/-38	-169	0.3	44/50	12	1.7/1

(*) Estimated.

To prove the scalability of this SC DAC for more advanced technology it is measured at lower supply of 0.9 V. The achieved performance of the DAC at low supply in term of SFDR is similar to the DAC with standard supply of 1.2 V, as shown in Fig. 35. The power dissipation and output swing are lower in this case.

The measured SFDR versus the output frequency f_{out} with different clock frequency f_s is shown in Fig. 36. The performance of SFDR from low frequency to Nyquist for each $f_s = 1$ GHz, 3 GHz and 5 GHz is plotted respectively. SFDR is degraded with both BW and clock. However, BW appears more critical for degradation of SFDR in region of higher frequency (case of 5 GHz). Additionally the simultaneous switching noise (SSN) which is described in section III has more effects at high frequencies (> 3GHz) and contributes more to that degradation.

Fig. 37 shows the measured IM3 versus tone spacing with different the output frequency f_{out} at $f_s = 5$ GHz. As mentioned above, due to a 64-point deep signal to be tested the minimum frequency bin spacing in the input signal is $f_s/64$. The higher clock frequency is the wider tone spacing is available to test. With $f_s = 5$ GHz, the tone spaces will be integer multiple of 78.125MHz. In general, IM3 does not vary much unless spacing is too wide (> 1GHz) as shown in Fig. 37.

This SC DAC can be used in baseband transmitter for wideband wireless communications such as UWB and 60-GHz radios. In order to show the potential of this design to be used in 60-GHz radio, the spectral mask is measured and shown in Fig. 38. It is the spectral mask of 16-QAM modulation scheme with the IEEE 802.11ad (WiGig) standard. Single-carrier 16-QAM encoded random data with a frequency bin spacing of approximation 80 MHz between 0 to 880 MHz is first generated and pulse-shaped in Matlab with an 18th-order root-raised-cosine (RRC) filter having a 0.25 roll-off factor [25].

conditions at 5.28 GS/s operation. It can be observed that the mask of the IEEE 802.11ad (WiGig) standard is met and the out-of-band quantization noise from SC DAC is found not to be a limiting factor. The measured INL and DNL are 0.1LSB and 0.08LSB, respectively, on a 12 bit level. It shows that linearity of DAC is not limited by static non-linearity but limited by dynamic one, mainly from SSN.

The measurement results show total output noise of -72 dBm, equivalent with PSD = -169 dBc/Hz at 5 GHz sampling frequency. The thermal noise at the output of DAC is dominated by noise from output driver since this number is closed to the one in the output driver section (PSD = -173 dBc/Hz). Therefore the noise due to kT/C noise of SC arrays is negligible which agrees with analytical results shown in Fig. 14a.

For comparing to other works, we used the figure-of-merits (FOMs) listed in [5]. There are 5 definitions of FOMs but only FOM3 is more generic and relevant i.e. suitable for any kind of DAC types.

$$FOM3 = \frac{V_{swing}}{P_{total}} BW_{10}^{\frac{SFDR}{20}}, \quad (28)$$

where BW is the signal bandwidth, P_{total} is the total power consumption, whereas V_{swing} and $SFDR$ stand for the differential output swing and spurious free dynamic range of DACs, respectively. Table IV shows comparison with the recent state-of-the-art reported works. For SC DAC, only 2 designs have recently reported in [10, 11]. The clock frequencies in those designs are not greater than 800 MHz and signal bandwidth not greater than 400 MHz. This design achieves the highest speed among the previous reported works of the same type of SC DACs. The FOM3 of this work is calculated at 5 GS/s for 2 input frequencies f_{in} of 800 MHz and 1 GHz for SFDR of 50 dB and 44 dB, respectively.

The linearity of this design is poorer than expected due to more SSN (worse PSRR) in fabricated chip. It has potential to improve SFDR when SSN still has room to be improved by

Fig. 38 shows the measured spectral mask under these

using more advanced packaging techniques such as flip-chip, 3-D packaging. Another way for reducing SSN effect is to use additional circuits to improve PSRR for SC arrays.

VI. CONCLUSION

This work proposes the split-segmented SC DAC topology which is more suitable for high-resolution and high-speed DACs as compared with pipeline SC DACs. The detailed analyses of kT/C noise, capacitor mismatch, settling-time, and switching noise in SC array are described to define design area W - C_u and find a suitable design point (W , C_u). It also proposes the open-loop output driver where both third- and second-order distortions are cancelled to drive SC DAC arrays. Among reported capacitive DACs, this design achieves highest clock frequency (5 GS/s) and highest BW (1 GHz) with SFDR of 44 dB. The SSN is the most critical factor degrading the linearity of SC DACs for high frequency operation. There is a room to improve linearity of SC DAC by improving PSRR. This design has potential for use in the baseband of transmitters for wideband wireless communications such as UWB and 60-GHz radios.

APPENDIX A

DERIVATION OF THE SC-ARRAY NOISE ANALYSIS

From Fig. 6, impedance of each branch in the second binary segment is described as

$$Z_{b2}(i) = \frac{R_{on}}{2^i} + \frac{1}{j\omega C_u 2^i} \quad (A.1)$$

The total admittance of the second binary segment is

$$Y_{b2} = \sum_{i=0}^{k_2-1} \frac{1}{Z_{b2}(i)} \quad (A.2)$$

The total impedance of the second binary segment and C_{atten2} is found

$$Z_{b2,atten2} = \frac{1}{Y_{b2}} + \frac{1}{j\omega C_{atten2}} \quad (A.3)$$

The total admittance of the first, second binary segments and C_{atten2} is

$$Y_{b1-2,atten2} = \frac{1}{Z_{b2,atten2}} + \sum_{i=0}^{k_1-1} \frac{1}{Z_{b2}(i)} \quad (A.4)$$

The total impedance of the first, second binary segments and C_{atten1} , C_{atten2} is

$$Z_{b1-2,atten1-2} = \frac{1}{Y_{b1-2,atten2}} + \frac{1}{j\omega C_{atten1}} \quad (A.5)$$

Impedance of each branch in thermometer segment is as

$$Z_{th} = R_{on} + \frac{1}{j\omega C_u} \quad (A.6)$$

The total admittance of all thermometer branches is as

$$Y_{th} = \frac{2^m - 2}{Z_{th}} \quad (A.7)$$

APPENDIX B

DERIVATION OF THE VOLTERRA OPERATORS FOR THE PROPOSED OUTPUT DRIVER

For the equivalent circuit shown in Fig. 23 the current and voltage equations follow

$$i_A = g_{1A} v_{gsA} + g_{2A} v_{gsA}^2 + g_{3A} v_{gsA}^3 \quad (A.8)$$

$$i_B = g_{1B} v_{sgB} + g_{2B} v_{sgB}^2 + g_{3B} v_{sgB}^3 \quad (A.9)$$

$$i_{OUT} = i_A - i_B + (v_{in} - v_{OUT}) sC_{gs} \quad (A.10)$$

$$v_{gsA} = v_{in} - v_{OUT}, v_{sgB} = v_{OUT} - v_{in} \quad (A.11)$$

$$v_{OUT} = Z_{OUT} i_{OUT} \quad (A.12)$$

where g_{iA} and g_{iB} are the i^{th} -order coefficients of M_A and M_B , accordingly, obtained by taking the derivative of the drain dc current I_{DS} with respect to the gate-source voltage V_{GS} at the dc bias point

$$g_{iA} = \frac{1}{i!} \frac{\partial^i I_{DSA}}{\partial V_{GSA}^i}, g_{iB} = \frac{1}{i!} \frac{\partial^i I_{SDB}}{\partial V_{SGB}^i} \quad (A.13)$$

Applying the Volterra series to the output voltage

$$v_{OUT} = G_1 \circ v_{in} + G_2 \circ v_{in}^2 + G_3 \circ v_{in}^3 \quad (A.14)$$

Substituting (A.8-A.11) into (A.12), we have

$$v_{OUT} = Z_{OUT} (g_{1A} + g_{1B} + sC_{gs})(v_{in} - v_{OUT}) + Z_{OUT} (g_{2A} - g_{2B})(v_{in} - v_{OUT})^2 + Z_{OUT} (g_{3A} + g_{3B})(v_{in} - v_{OUT})^3 \quad (A.15)$$

Next, using (A.14) and (A.15) the Volterra transfer functions G_1 , G_2 , and G_3 are obtained

$$G_1(\omega) = \frac{Z_{OUT}(\omega)(g_{1A} + g_{1B} + j\omega C_{gs})}{1 + Z_{OUT}(\omega)(g_{1A} + g_{1B} + j\omega C_{gs})} \quad (A.16)$$

$$G_2(\omega_1 + \omega_2) = \frac{Z_{OUT}(\omega_1 + \omega_2)(g_{2A} - g_{2B})(1 - G_1(\omega))^2}{[1 + Z_{OUT}(\omega_1 + \omega_2)(g_{1A} + g_{1B} + j(\omega_1 + \omega_2)C_{gs})]^3} \quad (A.17)$$

$$G_3(\omega_1 + \omega_2 + \omega_3) = \frac{Z_{OUT}(\omega_1 + \omega_2 + \omega_3)(g_{3A} + g_{3B})(1 - G_1(\omega))^3}{1 + Z_{OUT}(\omega_1 + \omega_2 + \omega_3)[g_{1A} + g_{1B} + j(\omega_1 + \omega_2 + \omega_3)C_{gs}]} - \frac{2Z_{OUT}(\omega_1 + \omega_2 + \omega_3)(g_{2A} - g_{2B})[G_2(\omega_1 + \omega_2) - G_2(\omega_1 + \omega_2)G_1(\omega)]}{1 + Z_{OUT}(\omega_1 + \omega_2 + \omega_3)[g_{1A} + g_{1B} + j(\omega_1 + \omega_2 + \omega_3)C_{gs}]} \quad (A.18)$$

where

$$\overline{G_2(\omega_1 + \omega_2)G_1(\omega)} = \frac{[G_2(\omega_1 + \omega_2)G_1(\omega_3) + G_2(\omega_1 + \omega_3)G_1(\omega_2) + G_2(\omega_3 + \omega_2)G_1(\omega_1)]}{3} \quad (A.19)$$

REFERENCES

- [1] "High Rate Ultra Wideband PHY and MAC Standard," *Standard ECMA-368*, Dec. 2008.
- [2] "WirelessHD Specification v1.1 overview," *Standard*, May 2010. (<http://www.wirelesshd.org/>)

- [3] X. Wu, et al., "A 130nm CMOS 6-bit Full Nyquist 3 GS/s DAC," *IEEE J. Solid-State Circuits*, vol. 43, pp. 2396-2403, Nov. 2008.
- [4] C. H. Lin, et al., "A 12 bit 2.9 GS/s DAC with IM3 < -60 dBc Beyond 1 GHz in 65nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, pp. 3285-3293, Dec. 2009.
- [5] P. Palmers, et al., "A 10-Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS," *IEEE TCASI*, vol. 57, pp. 2870-2879, Nov. 2010.
- [6] Wei-Te Lin, et al., "A 12-bit 40 nm DAC achieving SFDR > 70 dB at 1.6 GS/s and IMD < -61 dB at 2.8 GS/s with DEMDRZ technique," *IEEE J. S.S. Circuits*, vol. 49, pp. 708-717, Mar. 2014.
- [7] Shiyu Su, et al., "A 12 bit 1 GS/s Dual-Rate Hybrid DAC with an 8 GS/s unrolled pipeline delta-sigma modulator achieving > 75 dB SFDR over the Nyquist Band," *IEEE J. S.S. Circuits*, vol. 50, pp. 896-907, Apr. 2015.
- [8] Georgi I. Radulov, et al., "A 28-nm CMOS 7-GS/s 6-bit DAC with dft clock and memory reaching SDFR > 50 dB up to 1 GHz," *IEEE Trans. VLSI*, vol. 49, pp. 1941-1945, Sep. 2015.
- [9] Erik Olieman, et al., "An interleaved full Nyquist high-speed DAC technique," *IEEE J. S.S. Circuits*, vol. 50, pp. 704-713, Mar. 2015.
- [10] G. Manganaro, et al., "A Dual 10-b 200-MSPS Pipeline D/A Converter With DLL-Based Clock Synthesizer," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1829-1838, Nov. 2004.
- [11] C. Daigle, et al., "A 12-bit 800-MS/s Switched-Capacitor DAC with Open-loop Output Driver and Digital Predistortion," *IEEE Asian Solid-State Circuits Conference*, pp. 1-4, Nov. 2010.
- [12] Quoc-Tai Duong, et al., "Design and Analysis of High Speed Capacitive Pipeline DACs," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 80, pp. 359-374, July. 2014.
- [13] C. Daigle, *Switched-capacitor DACs using open-loop output drivers and digital predistortion*. PhD dissertation, 2010.
- [14] Y. M. Zhu, "Generalized Sampling Theorem," *IEEE TCASII*, vol. 39, pp. 587-588, Aug. 1992.
- [15] B. Kim, et al., "A new linearization technique for MOSFET RF amplifier using multiple gated transistors," *IEEE Microwave and guided wave letter*, vol. 10, no. 9, pp. 270-273, Jan. 2000.
- [16] B. H. Leung, *VLSI for Wireless Communication*. Englewood Cliffs, NJ: Prentice-Hall, 2002.
- [17] Franco Maloberti, *Data Converters*. Springer, 2008.
- [18] G. A. M. V. D. Plas, et al., "A 14-bit intrinsic accuracy Q^2 random walk CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1708-1718, Mar. 1999.
- [19] F. J. Wang, et al., "A quasipassive CMOS pipeline D/A converter," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1752-1755, Dec. 1989.
- [20] Li Ding and Pinaki. M., "Simultaneous switching noise analysis using application specific device modeling," *IEEE Trans. VLSI*, vol. 11, pp. 1146-1152, Dec. 2003.
- [21] Yungseon Eo, et al., "New simultaneous switching noise analysis and modeling for high-speed and high-density CMOS IC package design," *IEEE Trans. Advanced packaging*, vol. 23, pp. 303-312, May. 2000.
- [22] Srinivasa R. V., "Accurate simultaneous switching noise estimation including velocity-saturation effects," *IEEE Trans. Components, packaging and manufacturing technology*, vol. 19, pp. 344-349, May. 1996.
- [23] T. Lee, *The Design of COS Radio-Frequency Integrated Circuits*. 2nd Edition, Cambridge University Press, 2004.
- [24] Bhide A, et al., "An 11-GS/s 1.1-GHz bandwidth Interleaved $\Delta\Sigma$ DAC for 60-GHz Radio in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, pp. 2306-2318, Oct. 2015.
- [25] M. Tokumaru, et al., "A 14.6th-order 3.456 GHz transmit baseband filter in 110 nm CMOS for millimeter-wave communication systems," *IEEE CICC*, pp. 175-178, 2009.
- [26] Yuriy M. G, et al., "A 56GS/s 6b DAC in 65nm CMOS with 256x6b Memory," *ISSC*, vol. 10, pp. 194-195, Dec. 2011.
- [27] T. Wakimoto, et al., "Statistical Analysis on the Effect of Capacitance Mismatch in a High-resolution Successive-Approximation ADC," *IEEE Transactions on electrical and electronic engineering*, vol. 6, pp. s89-s93, 2001.
- [28] Balasubramanian, VJ Patel, W Khalil, chapter "Current and emerging trends in the design of digital-to-analog converters," in book: *Design, modeling and testing of data converters* , pp. 83-116, 2014.

management.

Ameya Bhide (S'10) received the M.Sc. and PhD degrees in electrical engineering from Linköping University, Sweden in 2004 and 2015 respectively. Prior to that he received the B.Eng. degree in electronics and communication engineering from Bangalore University, India in 2001. Between 2005 and 2009, he was with the SoC-Enabling Group, Intel Corporation, Bangalore, India, where he worked on DDR memory and front side bus controllers for Intel's 65-nm and 32-nm mobile platforms. He currently works as an analog design engineer at Catena Microelectronics, Netherlands. His research interests include data converters, digitally assisted analog circuits, I/O interface circuits and high speed digital design.

Atila Alvandpour received the M.S. and Ph.D. degrees from Linköping University, Sweden, in 1995 and 1999, respectively. From 1999 to 2003, he was a senior research scientist with Circuit Research Lab, Intel Corporation. In 2003, he joined the department of Electrical Engineering, Linköping University, as a Professor of VLSI design. Since 2004, he is the head of Electronic Devices division. His research interests include various issues in design of integrated circuits and systems in advanced nano-scale technologies, with special focus on efficient radio frontends, data converters, clock generators/synthesizers, and digital circuits for high-speed communication links as well as low-power sensors and medical devices. He has published more than 100 papers in international journals and conferences, and holds 24 U.S. patents. Prof. Alvandpour is a senior member of IEEE, and has served as member of many technical program committees of IEEE and other international conferences, including the IEEE Solid-State Circuits Conference, ISSCC, and European Solid-State Circuits Conference, ESSCIRC. He has also served as guest editor for IEEE Journal of Solid-State Circuits.