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A Low Noise RC-based Phase Interpolator in 16-nm CMOS

Anders Jakobsson, Adriana Serban, and Shaofang Gong, *member, IEEE*

Abstract—This paper describes a passive analog phase interpolator, utilizing a switched RC-network. The proposed circuit eliminates the current sources in a phase interpolator based on constant-slope charging. By eliminating the current source, the noise is significantly reduced due to the reduction in thermal and flicker noise. The phase interpolator has a resolution of 6 bits and is implemented in a 16-nm CMOS process. The maximum differential non-linearity is measured to be 0.1 LSBs at a 192 ps input time delta. The circuit draws 0.2 mW from a 0.8 V supply, and occupies 0.004 mm².

Index Terms—Phase interpolator, PLL, low noise, high linearity

I. INTRODUCTION

PHASE INTERPOLATORS (PIs) are used to generate a controllable phase shift, based on the phase relation of two input clocks. They are used in a variety of applications, e.g., clock- and data recovery (CDR) circuits [1], [2], for phase acquisition in phase-locked loops (PLL) [3], [4], phase ramp generator in sub-sampling PLLs [5]. A PI can potentially replace a digital-to-time converter (DTC) in many applications to generate a time delay. Several PI topologies have been proposed; Delay line based [6], [7], trigonometric [2], [8], [9], current-weighting [1], [3], [4], [10], [11], charge-steering [12] and constant-slope charging [5], [13].

The sub-sampling PLL presented in [5] and shown in Fig. 1, uses a DTC in the reference path and a PI in the feedback path to align the phase of the voltage-controlled oscillator (VCO) with the phase of the reference clock, thereby enabling fractional-N operation. The PI interpolates one VCO cycle per reference period, as illustrated in Fig. 1. The 5-bit PI consists of a cascaded chain of 1-bit PI-unit cells based on constant-slope charging. By dividing the VCO phase by 32, the DTC needs to cover a much smaller range. A wave-shaper (WS) returns the square wave output of the PI to a form suitable for the sub-sampling phase detector (SSPD). The PI-units use current sources to charge a capacitor, injecting noise into the PLL loop. The noise transfer function of the PI noise is given by

$$H_{PI}(s) = \frac{-L(s)}{1 + L(s)} \quad (1)$$

where $L(s)$ is the forward transfer function of the PLL. The noise of the current source is inversely proportional to its output current [5]. Using current sources also leaves little headroom at lower supply voltages. In this paper, we propose an RC-based phase interpolator using passive components and switches. The proposed circuit uses fewer components, thereby easing component matching, and shows superior noise performance and linearity. The prior art is further described in Section II, the proposed circuit is introduced in Section III, simulation results are shown in Section IV and measurement results are shown in Section V.

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Fig. 1. Fractional-N sub-sampling PLL augmented by a phase interpolator.

Fig. 2. Simplified schematic of PI-stage based on three PI-units. Unit A and C pass through the phase difference of the input.

II. BACKGROUND

A simplified view of the PI-stage in [5], [13] is shown in Fig. 2. The input signals are the two clocks Φ_{IN1} and Φ_{IN2} . The falling edges of Φ_{IN1} and Φ_{IN2} are separated by Δt seconds. There are two operating modes for a PI-unit, pass-through and interpolating. Unit A and C are configured for pass-through mode by having both inputs connected to the same signal (unit A to Φ_{IN1} and unit C to Φ_{IN2}). When Φ_{IN1} or Φ_{IN2} goes low, the output capacitors are simultaneously charged through the two current sources. The propagation delay through unit A and C is given by (2), where V_{TH} is the threshold voltage of the following stage.

$$t_{DLY,P} = C \cdot \frac{V_{TH}}{2 \cdot I_B} \quad (2)$$

Since unit A and C have the same delay, they thereby pass the phase difference of the two inputs. Unit B, shown in Fig. 3, operates in interpolating mode. It has one input connected to Φ_{IN1} and the other to Φ_{IN2} . The capacitor is thereby charged by I_B between t_1 and t_2 , and thereafter by $2I_B$. The voltage over the capacitor at time t_2 is

$$v_1(t_2) = \frac{\Delta t \cdot I}{C} \quad (3)$$

Fig. 3. Simplified schematic of PI-stage based on three PI-units. Unit B interpolates the phase difference of the inputs.

Fig. 4. A cascade of several 1-bit stages form a multi-bit PI.

and the interpolation delay through unit B is

$$\begin{aligned} t_{DLY,I} &= \Delta t + C \cdot \frac{V_{TH} - v_I(t_2)}{2 \cdot I_B} \\ &= t_{DLY,P} + \frac{\Delta t}{2} \end{aligned} \quad (4)$$

The phase difference between ϕ_{OUT1} and ϕ_{OUT2} , and between ϕ_{OUT2} and ϕ_{OUT3} , is therefore half that of the input phase difference. To generate a multi-bit PI, several stages are cascaded as shown in Fig. 4. Linearity is determined by the component matching between the current sources and capacitors of the three units of each stage, as well as the matching of the threshold voltages of the following stage. Simulation results show that the main noise contributor of the circuit in Figs. 2-3 is flicker noise of the current source, as shown in Fig. 10. However, flicker noise is not elaborated on in [5]. In the following section, we present a way to reduce the component count and replace the current sources with passive devices. We will also show through simulation results and measurements that this leads to lower noise and better linearity.

III. RC-BASED PHASE INTERPOLATION

The proposed phase interpolator unit is shown in Fig. 5. The key concept of the proposed interpolator is that a logarithmic charging slope works just as well as a linear one with regard to linearity. The easiest way to implement a logarithmic slope is to replace the current sources in Figs. 2-3 with resistors. Furthermore, the inter-stage switches in Fig. 4 are moved into the unit. In this way, a single unit can be configured to operate in either pass-through mode (Fig. 5a) or interpolating mode (Fig. 5b), instead of using separate units for each mode. The PI-unit in Fig. 5 interpolates the falling edge of the input, but the same principle can be applied for interpolating the rising edge by turning the unit “upside-down” as shown on the right of Fig. 9. The circuit can also be modified to interpolate the rising

Fig. 5. Proposed phase interpolator unit in (a) pass-through mode and (b) interpolating mode.

Fig. 6. Capacitor voltage during (a) pass-through mode and (b) interpolating mode.

or falling edge, as shown in Fig. 7a and Fig. 7b respectively. The drawback to using the double-edge interpolator is that the loading on the clock input is doubled, and the switch control logic is more complicated.

For the pass-through mode, the capacitor charging waveform is shown in Fig. 6a, and given by

$$v_P(t) = \begin{cases} 0, & t \leq t_1 \\ V_{DD} \cdot \left(1 - e^{-\frac{t-t_1}{RC}}\right), & t > t_1 \end{cases} \quad (5)$$

where V_{DD} is the supply voltage. Setting $v_P(t) = V_{TH}$ and solving for $t - t_1$, gives the pass-through delay

$$t_{DLY,P} = -RC \cdot \ln \left(1 - \frac{V_{TH}}{V_{DD}}\right) \quad (6)$$

For the interpolating mode, the capacitor charging waveform is shown in Fig. 6b. For $t_1 \leq t \leq t_2$ the capacitor is first charged through one resistor, and for $t > t_2$ through both. The voltage over the capacitor is given by

$$v_I(t) = \begin{cases} 0, & t \leq t_1 \\ V_{DD} \cdot \left(1 - e^{-\frac{t-t_1}{RC}}\right), & t_1 \leq t \leq t_2 \\ v_I(t_2) + \Delta V \left(1 - e^{-\frac{t-t_2}{RC}}\right), & t > t_2 \end{cases} \quad (7)$$

where $\Delta V = V_{DD} - v_I(t_2)$. Expanding (7) for the case $t > t_2$ gives

$$v_I(t) = V_{DD} \cdot \left(1 - e^{-\frac{t-t_1 - \frac{\Delta t}{2}}{RC}}\right) \quad (8)$$

This is equivalent to charging the capacitor through both resistors from $t = t_1 + \frac{\Delta t}{2}$, as shown by the dashed line in Fig. 6b. We can

Fig. 7. Circuit for interpolating (a) the rising edge and (b) falling edge.

Fig. 8. Unary-coded, multi-bit PI-unit.

show this by, again, setting $v_l(t) = V_{TH}$ and solving for $t - t_1$. The resulting interpolation delay is

$$\begin{aligned} t_{DLY,I} &= -RC \cdot \ln \left(1 - \frac{V_{TH}}{V_{DD}} \right) + \frac{\Delta t}{2} \\ &= t_{DLY,P} + \frac{\Delta t}{2} \end{aligned} \quad (9)$$

Equation 9 shows that the input phase difference has been interpolated by a factor of two.

The principle can be generalized to an m -bit unit as shown in Fig. 8. $N = 2^m$ resistors and switches are connected in parallel. The PMOS switches $S_{R,0} - S_{R,N-1}$ are controlled by ϕ_{IN1} or ϕ_{IN2} through input switches $S_{I,0} - S_{I,N-1}$. For a given interpolation factor k , $N - k$ PMOS switches are controlled by ϕ_{IN1} and k PMOS switches are controlled by ϕ_{IN2} . Similar to (7), the capacitor voltage can be expressed as

$$v_l(t) = \begin{cases} 0, & t \leq t_1 \\ V_{DD} \cdot \left(1 - e^{-\frac{(N-k) \cdot (t-t_1)}{N \cdot RC}} \right), & t_1 \leq t \leq t_2 \\ v_l(t_2) + \Delta V \left(1 - e^{-\frac{t-t_2}{RC}} \right), & t > t_2 \end{cases} \quad (10)$$

And expanding (10) for the case $t > t_2$ gives

$$v_l(t) = V_{DD} \cdot \left(1 - e^{-\frac{t-t_1 - \frac{k}{N} \Delta t}{RC}} \right) \quad (11)$$

The delay is linearly dependent on k as given by

$$t_{DLY,I} = t_{DLY,P} + \frac{k}{N} \Delta t \quad (12)$$

The input phase difference can in this way be interpolated with a step size of $\Delta t/N$. The upper limit on N is given by practical layout considerations. The RC-constant, $\tau = \frac{RC}{N}$, is chosen to ensure that $v_l(t_2) < V_{TH}$.

Fig. 9. Cascade of multiple stages, each consisting of two units.

Fig. 10. Simulated capacitor noise voltage for a PI-unit based on current source (solid line) and resistors (dashed line).

If even finer delay steps are required, several stages can be cascaded, as shown in Fig. 9. Since the PI-unit is inverting, every other PI-unit is turned “upside-down”. Because the inter-stage switch was moved into the unit, each unit can connect to both inputs, and thus be configured for either pass-through or interpolation. Therefore, only two units are needed per stage, as compared to three for the design in [5]. This further increases component matching and thereby linearity of the interpolator.

Replacing the current sources in Fig. 2 with resistors has the advantage of removing the current source flicker noise contribution. Fig. 10 compares simulated noise voltage over the capacitor for a PI-unit based on current sources (solid line) and resistors (dashed line). For a fair comparison, the two units have the same average charging current and are of similar physical size. Additionally, the thermal voltage noise power spectral density is given by [14]

$$\frac{\overline{v_n^2}}{\Delta f} = 4kT\gamma g_m \cdot r_0^2 \approx 4kT\gamma \frac{2}{V_{eff} I_B} \quad (13)$$

which, for the same average charge current I_B , is typically one to two orders of magnitude smaller than the $4kTR$ noise of the RC-based PI.

IV. TEST CIRCUIT

A. PI core

The multi-bit PI-unit in Fig. 8 was designed in a 16-nm FinFET process with $R = 100 \Omega$, $C = 3.8$ pF and $N = 64$, giving a resolution of 6 bits. Metal-oxide-metal capacitors, metal gate thin film resistors and minimum size transistors were used. The unit was designed for an input Δt of 192 ps, giving a step size of $192 \text{ ps}/64 = 3$ ps. Fig. 11 shows simulated differential non-linearity (DNL) and integral non-linearity (INL) from 64 Monte-Carlo simulations (solid) and for process corners (dashed) on the schematic. Simulation results

Fig. 11. Simulated DNL and INL of a 6-bit PI-unit (schematic) for Monte-Carlo (solid) and corner (dashed).

Fig. 12. Circuit used to measure the DNL of the PI.

for SS, SF, FS, and FF process corners are also shown. The DNL is within ± 0.01 LSBs, equivalent to about ± 30 fs. Maximum INL is 0.05 LSBs. Simulated power consumption of the PI core is 0.2 mW at an 81MHz operating frequency.

B. Test stimuli

To measure delay differences in the order of tens of femtoseconds, the phase modulation method is used [15]. The delay control word is periodically changed between d_0 and $d_0 + d_S$ with a frequency f_{MOD} , resulting in phase-modulation side-bands at the output of the circuit. The side-band power can be measured using a spectrum analyzer, and the delay difference can be calculated from the side-band power as

$$\tau = t_{MOD} \cdot 10^{\frac{P_{SPUR}}{20}} \quad (14)$$

where t_{MOD} is the modulation frequency, and P_{SPUR} is the side-band power in dBc.

The test circuit consists of the PI core, input- and output buffers and a circuit to generate the phase modulation stimulus, as shown in Fig. 12. This circuit mimics the typical use case in a sub-sampling PLL [5], where the PI would output one interpolated edge every reference clock period. The input signals are clk_{IN} , dly_{IN} and dly_{STEP} . The period of clk_{IN} is equal to Δt . The reference clock period is $64 \times \Delta t$. The test circuit outputs $reset$, Φ_{IN1} , Φ_{IN2} and the modulated delay control word dly_{MOD} to the 6-bit PI-unit core. Fig. 13 shows the timing diagram of the stimulus signals. The implemented PI-unit is only designed to interpolate the falling edge of the input. The output is therefore divided by two, so that only the falling edges of the output are considered. The output is further buffered and matched to 50 Ω . Simulated power consumption of the Input buffer, Stimulus block and Output buffer are 0.56, 0.25 and 1.6 mW, respectively.

Fig. 13. Timing diagram of the test control circuit.

Fig. 14. Parasitic aware simulated phase-noise of complete test circuit (solid line) and the PI core (dashed line).

Fig. 14 shows simulated phase noise of the complete test circuit and the PI core. Unfortunately, the output buffer add a substantial amount of noise, making it difficult to evaluate the noise performance of the PI core, but correlation between simulated and measured noise of the test circuit can still be investigated.

V. MEASUREMENT RESULTS

Fig. 15 shows the measured DNL and INL of 4 samples of the test circuit (solid lines), together with simulated linearity of a parasitic aware extracted view (dashed line). The DNL is within ± 0.1 LSBs, equivalent to about ± 300 fs. Maximum INL is ± 0.25 LSBs. The measured linearity shows a good match with simulated linearity. The INL is an order of magnitude higher than the values predicted by schematic simulations. The higher INL was later confirmed to be the result of sub-optimal supply routing. Fig. 15 also shows simulated results for a post facto redesigned layout (dotted lines). This is an indication of the maximum performance obtainable with a carefully conducted layout design, but the measurement of the redesigned PI layout remains a topic for future work. INL is also

Fig. 15. Comparison between measured (solid lines) and simulated (dashed lines) results for (a) DNL and (b) INL .

Fig. 16. Measured INL across different input Δt .

Fig. 17. Measured phase noise of test circuit (solid line), and clock source before and after division by 128 (dashed lines). The clock source noise plus simulated circuit noise is also shown for comparison (dotted line).

stable across input Δt , as shown in Fig. 16. For larger Δt , $v_i(t_2)$ in (10) starts to increase above V_{TH} . For $\Delta t < 120$ ps, the input clock buffer stops working. Fig. 17 shows the phase noise measured at the circuit output. A Keysight E8663D RF signal generator was used as a 5.2 GHz clock source during this measurement. The measured phase noise of this source is also shown in Fig. 17. The phase noise is reduced by $20\log_{10}(128)$ due to the test circuit's total division ratio of 128. Finally, the simulated phase noise of the test circuit plus measured clock source noise is also plotted in Fig. 17 for comparison. A performance summary and comparison of key parameters with state-of-the-art phase interpolators of different topologies is found in Table I. The operating frequency (how often the PI generates an output) greatly affects power consumption. For a fair comparison, power consumption normalized to 1 MHz is also shown. The proposed phase interpolator shows the lowest measured DNL and power consumption.

VI. CONCLUSION

A phase interpolator based on the constant-slope charging topology was introduced, where traditionally used current sources are replaced by resistors. As current sources are an important source of flicker and thermal noise, the new proposed topology greatly reduces the noise of the interpolator, as demonstrated through simulations in this paper. Moreover, the proposed interpolator has improved linearity and lower power consumption as compared to previous reported phase interpolators. The implemented circuit has a 6-bit resolution, with a measured differential non-linearity of 0.1 LSBs. The area is 0.004 mm² and the power consumption is 0.2 mW.

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TABLE I
PERFORMANCE COMPARISON WITH PHASE INTERPOLATORS.

	[5]	[10]	This work
Technology	65-nm	65-nm	16-nm
Architecture	current-steering	current-weighting	RC-based
Supply voltage	1 V	1.0 V	0.8 V
Input Δt	400 ps	440 ps	192 ps
Operating frequency	40 MHz	500 MHz	81 MHz
Resolution (bits)	5	4	6
Nominal step (ps)	3.125	-	3
DNL (LSBs)	0.18 ^{1,2}	0.23 ¹	0.1
INL (LSBs)	0.1 ^{1,2}	0.6 ¹	0.5
Power (mW)	2.3	1.5	0.2
Power/freq. (μ W/MHz)	58	3	2.5
Area (mm ²)	0.0055 ²	-	0.004

¹ Simulated

² Estimated from figure

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