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Elimination of step bunching in the growth of large-area monolayer and multilayer graphene on off-axis 3C-SiC (111)

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ABSTRACT

Multilayer graphene has exhibited distinct electronic properties such as the tunable bandgap for optoelectronic applications. Among all graphene growth techniques, thermal decomposition of SiC is regarded as a promising method for production of device-quality graphene. However, it is still very challenging to grow uniform graphene over a large-area, especially multilayer graphene. One of the main obstacles is occurrence of step bunching on the SiC surface, which significantly influences the formation process and the uniformity of the multilayer graphene. In this work, we have systematically studied the growth of monolayer and multilayer graphene on off-axis 3C-SiC(111). Taking advantage of the synergistic effect of periodic SiC step edges as graphene nucleation sites and the unique thermal decomposition energy of 3C-SiC steps, we demonstrate that the step bunching can be fully eliminated during graphene growth and large-area monolayer, bilayer, and four-layer graphene can be controllably obtained on high-quality off-axis 3C-SiC(111) surface. The low energy electron microscopy results demonstrate that a uniform four-layer graphene has been grown over areas of tens of square micrometers, which opens the possibility to tune the bandgap for optoelectronic devices. Furthermore, a model for graphene growth along with the step bunching elimination is proposed.

1. Introduction

Graphene has been attracting much attention for next-generation electronic and optoelectronic devices due to its extraordinarily electronic properties [1-4]. Several methods containing exfoliation of highly oriented pyrolytic graphite (HOPG), chemical vapor deposition (CVD), chemical reduction of graphite oxide and thermal sublimation/decomposition have been widely used for graphene fabrication [2, 5-7]. Among these techniques, the epitaxial growth of graphene by thermal sublimation of silicon carbide (SiC) is recognized as a promising method for production of large-area high-quality graphene. A considerable advantage of this method is that devices can be processed directly on graphene which is grown on insulating SiC substrates without any transfer process which is needed in the case of graphene produced by exfoliation or CVD on metals. The growth of monolayer graphene on commercial on-axis hexagonal SiC (6H-SiC, 4H-SiC) substrates has been extensively studied [7]. Recently, an interest in multilayer graphene has emerged because of its potential to induce a bandgap for optoelectronic applications [8, 9]. However, it is still challenging to control the uniformity of multilayer graphene over a wafer size area, typically, small, finger-like domains, islands or stripes are observed [10-12].

The growth mechanism of graphene on hexagonal SiC surfaces has been elucidated in the literature [11]. It is described that the nucleation of graphene on the SiC surface starts from step edges where the highest density of dangling bonds exists [13]. Particularly, at high temperatures, the Si atoms sublime from the step edges leaving behind carbon-rich areas, where graphene starts to form and enlarge on the step terrace [10]. Nominally on-axis and off-axis hexagonal (4H-, 6H-) SiC substrates have been used for the growth of graphene by thermal sublimation. It has been observed that upon thermal etching at elevated temperatures such surfaces exhibit step bunching [14, 15], which is defined as the formation of high steps (a few unit cells of SiC, ranging from a

few nanometers to tens of nanometers) and wide terraces (ranging from a few hundreds of nanometers to micrometers).

The step bunching of the SiC surface significantly influences the morphology of graphene layers. The formation of high steps and large terraces prevents the growth of uniform thickness monolayer graphene and suppresses the formation of uniform thickness multilayer graphene. It has been demonstrated that as a result of SiC step bunching, the graphene formed at step edges on nominally on-axis 4H- and 6H-SiC substrates is commonly thicker than graphene on the (0001) terraces [12, 16]. This also applies for graphene on off-axis 4H- and 6H-SiC substrates. For instance, it was shown that the bilayer graphene was formed on the step edges while the monolayer graphene was grown on (0001) terraces on off-axis 4H-SiC substrates [17]. As a consequence, the electronic properties of graphene are influenced by the morphology (step edges/terraces) of the SiC surface because they strongly depend on the number of graphene layers. It has been experimentally demonstrated that graphene devices covering steps have much higher resistance than the ones fabricated on step terraces, moreover, the resistance increases with the increase in step height [18]. Hence, for graphene on SiC device applications the step bunching should be eliminated and a homogeneous growth of monolayer or multilayer graphene over a large area should be mastered.

The presence of step bunching on 4H- and 6H-SiC surfaces has been discussed in terms of different thermal decomposition energies of steps [19]. Specifically, 4H-SiC has two different step decomposition energies and 6H-SiC has three different step decomposition energies. This results in different step decomposition rates. Upon sublimation or thermal etching, the steps with highest decomposition rate would catch up with the steps with lower rate and bunch into higher steps with wider terraces. In this regard, cubic silicon carbide (3C-SiC) is a promising substrate since it

1 possesses the same decomposition energy for all steps which energetically drives an identical
2 decomposition rate of steps.

3 In contrast to the hexagonal SiC, free standing, high-quality 3C-SiC substrates are not
4 commercially available. The growth of graphene on 3C-SiC thin films on Si substrates has been
5 recently reported [20]. However, due to fundamental limitations of 3C-SiC/Si material system, the
6 crystalline quality of 3C-SiC is much lower compared to its hexagonal counterparts. The CVD
7 grown 3C-SiC on Si substrates always exhibits a large residual stress (wafer bowing) and a high
8 density of defects due to the large lattice constant and thermal expansion coefficient mismatch
9 between Si and SiC. Therefore, it is challenging to obtain a continuous and uniform graphene layer
10 on such material [21, 22]. Moreover, a strong defect-related D-peak from Raman measurements
11 on graphene grown on 3C-SiC/Si is commonly observed [20] indicating deteriorated graphene
12 quality. Besides the quality of 3C-SiC on Si, the use of Si substrates limits the growth temperature
13 for 3C-SiC and graphene to a temperature lower than the Si melting point ($\sim 1410^\circ\text{C}$). Also, an
14 excessive Si evaporation from Si substrates makes the control of graphene growth on 3C-SiC/Si
15 even more challenging.

16 In contrast to 3C-SiC/Si, the sublimation grown 3C-SiC on commercial 4H- or 6H-SiC wafers
17 can be a promising substrate for the growth of high-quality graphene [19]. Recently, our group
18 reported that under certain growth conditions even a single-domain 3C-SiC with a high crystalline
19 quality can be grown on 4° off-axis 4H-SiC substrates [23, 24]. Since the step bunching is not
20 energetically favorable during the graphene growth on 3C-SiC, we believe that such high quality
21 3C-SiC surface with periodic steps is a viable route for a large-area growth of multilayer graphene.
22 To our knowledge, a comprehensive study of epitaxial growth of multilayer graphene, especially
23 thicker than 3 layers (3L), on off-axis 3C-SiC has not been done, although, a promising electronic

structure (flat band near the Fermi level) of the multilayer graphene grown on off-axis 3C-SiC has been validated [25].

In this work, we demonstrate a method to fully eliminate the step bunching and achieve the growth of uniform large-area monolayer, bilayer, and four-layer graphene on off-axis 3C-SiC(111). First, high-quality 3C-SiC(111) is grown on 4° off-axis 4H-SiC(0001) substrates. Then, a selected thickness (mono-, bi- and four-layer) graphene is grown on 3C-SiC(111) surface by tailoring the annealing time at high temperature in Ar atmosphere. The surface topography, the number of graphene layers and the uniformity were systematically studied using atomic force microscopy (AFM), Raman spectroscopy, spectroscopic photoemission low-energy electron microscopy (SPELEEM) and low-energy electron diffraction (LEED). Based on these results, a model of graphene growth along with the step bunching elimination is proposed.

2. Experimental

Bulk-like off-axis 3C-SiC(111) samples with the thickness of ~1 mm were grown on 4° off-axis 4H-SiC substrates (SiCrystal) by the sublimation process [23, 24]. Then 300~400 μm thick free-standing 3C-SiC layers for the growth of graphene were obtained by polishing away the 4H-SiC substrates. To remove contaminations and oxide from the surface, the 3C-SiC substrates were chemically cleaned by acetone, ethanol, H₂O: NH₃: H₂O₂ (5:1:1), H₂O: HCl: H₂O₂ (6:1:1) and hydrofluoric acid (HF). Before the growth of graphene on 3C-SiC (111), we measured AFM on as-grown substrates in order to select macro-defect free samples which exhibited regular steps. For the growth of graphene, the samples were annealed in an inductively heated furnace at 1800 °C with a ramping rate of 25 °C/min under 850 mbar Argon atmosphere for 0, 1, 2, 5 minutes, and a range of 10~45 minutes, respectively. For the growth of thicker (>3L) layer graphene, the sample was annealed at 2000 °C for 30 minutes. After annealing at the target temperature, all samples

were cooled down to the room temperature naturally by switching off the system. A schematic diagram showing in Fig. S1 displays temperature profiles for all samples. The temperature ramping up rate and cooling down condition are identical for all samples. We only change the annealing target temperature (either 1800 °C or 2000 °C) and durations for graphene growth.

The height and phase contrast images were characterized on a $2 \times 2 \mu\text{m}^2$ area by AFM in tapping mode before and after the growth of graphene. Raman maps were acquired using 532 nm laser with spot diameter of about 800 nm on the sample. The micro-Raman system is equipped with a 100× objective coupled to a monochromator (Jobin Yvon HR460) with a CCD camera. The spectral resolution with the 600 grooves per mm grating used in the experiments is $\sim 5 \text{ cm}^{-1}$. The SPELEEM images and μ -LEED patterns provide information on the presence of buffer layer, as well as on the number of graphene layers and the surface structure. The measurements were carried out using the SPELEEM instrument at beamline I311 in the Max-lab synchrotron radiation laboratory, Lund, Sweden. Before measurements, the samples were annealed in-situ at 600 °C for 20 minutes to remove surface contamination. The μ -LEED patterns were acquired from the sampling areas with the range of 500~1000 nm, matching the size of the corresponding graphene domains.

3. Results and discussion

The surface morphology of the pristine and with graphene 3C-SiC samples were compared. Fig. 1 shows the evolution of surface morphologies as an effect of graphene growth time at 1800 °C under 850 mbar Ar pressure. The AFM topography images (a-e), phase images (f-j), and the histogram of the statistic step height (k-o), respectively, are compared for the pristine 3C-SiC and 3C-SiC annealed for 0-5 minutes. The surface morphology of the pristine 3C-SiC substrate is

characterized by highly uniform periodic steps with step height of ~ 1.5 nm and terrace width of ~ 50 nm, as shown in Fig. 1a. The statistical histogram of step height of the pristine 3C-SiC (Fig. 1k) indicates that the most of steps are distributed around 1.5 nm, which corresponds to the 6 Si-C bilayers of SiC crystalline structure (the height of one SiC bilayer height is 0.25 nm), that is, the size of 2-unit cells of 3C-SiC. The AFM phase image of the pristine 3C-SiC surface shown in Fig. 1f exhibits a highly uniform contrast. This implies that the surface is composed of only 3C-SiC since the contrast of the phase image is sensitive to different materials on the surface.

Fig. 1. The AFM topography $2 \times 2 \mu\text{m}^2$ images (a-e), phase images (f-j) generated at the same region as topography images, and the histograms (k-o) of the statistic step heights for the pristine 3C-SiC and the graphene samples grown on 3C-SiC at 1800 °C for 0-5 minutes, respectively. The step height profiles of the indicated lines with a dimension of 500 nm are shown in the insets of images (a-e).

The sample annealed at 1800 °C for 0 minute contains wide terraces widths (150~200 nm) and high steps (4~6 nm), as seen in Fig. 1b and Fig. S2a. This indicates that 3~4 steps of the 3C-SiC are bunching together to form a larger terrace with a higher step height. The phase image (Fig. 1g) reveals that the large terraces show a bright contrast coverage of 81% and few small steps show dark contrast with a coverage of 19%. The LEEM results (Fig. 3a, f) confirm that the large terraces are covered with quite uniform buffer layer with a coverage of 80% while the small dark steps are covered with monolayer (1L) graphene with a coverage of 20%, in nice agreement with the phase image in AFM. As an example, the step profile and its phase contrast shown in the inset of Fig. 1b and g clearly demonstrate that the small step is covered with a dark contrast area (region A), which, by a comparison of phase image and LEEM results, is confirmed to be the monolayer graphene.

As shown in Table 1, the AFM phase results provide essentially the same uniformity as that measured from LEEM.

Table 1. A comparison for the coverage of graphene layers obtained from AFM and LEEM.

Note: The coverage of the buffer, monolayer and bilayer graphene obtained from AFM phase images (Fig. 1g, h, j) and LEEM results (Fig. 3a, b, c) for the graphene samples grown on 3C-SiC at 1800 °C for 0, 1, 5 minutes, respectively.

Fig. 1c shows clearly the decomposition of bunched steps on 3C-SiC annealed at 1800 °C for 1 minute. For instance, as indicated in the region B of Fig. 1c, the large step starts to decompose and one small step with a similar step height and terrace width to that of the pristine 3C-SiC forms. The comparison (Table 1) of AFM phase image (Fig. 1h) and the LEEM result (Fig. 3b) shows that these small decomposed steps are covered with monolayer graphene while large steps are still covered with the buffer layer. Compared to the sample annealed for 0 minute, the sample annealed for 1 minute shows that more small steps are decomposed. Along with the decomposition of bunched steps, the coverage of the buffer layer decreases to 75% while the monolayer graphene increases to 25%. The phase image shows identical coverage proportions of buffer layer and monolayer graphene as obtained by LEEM (Table 1).

With increasing the annealing time to 2 minutes, a further decomposition of bunched steps occurs. As an example, the step height profile in the region C shown in the inset of Fig. 1d indicates that one large bunched step is decomposed to form three small steps and the phase image of this region (Fig. 1i) shows quite uniform contrast over these small steps. With further increase of the annealing time to 5 minutes, all large steps are decomposed into small steps with very similar step height and terrace width as that of the pristine 3C-SiC (Fig. 1e). The phase image reveals quite

uniform contrast over these small steps. Along with the full decomposition of bunched steps, the coverage of the monolayer graphene is simultaneously increasing to 96%, which is confirmed by the LEEM (field of view = 5 μm , see Fig. 3c). Again, the AFM phase image supports the LEEM results and indicates identical coverage uniformity of the monolayer graphene (see Table 1). We notice that in this case the remaining $\sim 4\%$ are due to coverage with bilayer graphene.

A full decomposition of bunched steps is clearly confirmed also by a comparison of the step height statistics for the pristine 3C-SiC and the samples annealed for 0, 1, 2, and 5 minutes (see Fig. 1k-o and suppl. information Fig. S2). The sample annealed for 0 minute (Fig. 1l and suppl. information Fig. S2a) shows a significant increase of the step height. These large steps are formed by bunching of 3~4 steps of the pristine 3C-SiC. With increasing the annealing time from 0 to 5 minutes, these large bunched steps are gradually decomposed into small steps similar to the steps of the pristine 3C-SiC. It is important to note that the annealing time of 5 minutes enables is sufficient for a 100% decomposition of bunched steps (see Fig. 1o and suppl. information Fig. S2d).

Fig. 2. The AFM topography $2 \times 2 \mu\text{m}^2$ images (a, b), phase images (c, d) generated at the same region as topography images, and the histograms (e, f) of the statistic step heights for the graphene samples grown on 3C-SiC at 1800 $^{\circ}\text{C}$ for 15 and 30 minutes, respectively. The step height profiles of the indicate lines with a dimension of 500 nm are shown in the insets of images (a, b).

The samples annealed at 1800 $^{\circ}\text{C}$ for 15 and 30 minutes, respectively, exhibit the same terrace width and step height as those on the pristine 3C-SiC surface, as seen in Fig. 2. Indeed, the systematic study of the effect of annealing time on the decomposition of bunched steps during

graphene growth is reflected by Fig. 4 which shows the decomposition degree of bunched steps as a function of annealing time at 1800 °C. Here, the decomposition degree is defined as a ratio of the number of steps with height in the range of the pristine 3C-SiC steps to the total number of the steps in statistical histograms. It clearly shows a 100% elimination of the step bunching after 5 minutes annealing. Further increase of the annealing time from 5 to 45 minutes at 1800 °C does not result in any step bunching again (see Fig. 2, 4 and suppl. information Fig. S2).

Fig. 3. (a-e) LEEM images (field of view = 5 μm) of the graphene samples grown on 3C-SiC at 1800 °C for 0, 1, 2, 5, 15, 30 minutes, which were measured with an electron energy of 3.46, 3.25, 5.15, 5.06 and 5.88 eV, respectively. (f-j) The electron reflectivity curves collected from the labeled regions in (a-e). The number of graphene layers is determined by the number of dips in electron reflectivity curves. (k-o) The μ -LEED patterns collected on the buffer layer (a, b), monolayer graphene (c, d), and bilayer graphene (e) are measured at 43.0, 48.1, 48.2, 47.7 and 47.0 eV, respectively. A probing area of 500~1000 nm was used during μ -LEED measurements. Bright graphene spots (red arrows) and surrounding ($6\sqrt{3}\times 6\sqrt{3}$) R30° buffer layer spots, as well as SiC (1×1) spots (green arrows) are indicated by arrows.

As confirmed by the LEEM results in Fig. 3, the increase of the annealing time from 0 to 5 minutes gives rise to the decomposition of bunched steps, a simultaneous decrease of the apparent buffer coverage from 80% to 0%, and an increase of the monolayer coverage from 20% to 96%. This indicates that graphene nucleated on each step can form a uniform large-area layer over steps. It is worth noting that, as shown in Fig. 3d, the sample annealed at 1800 °C for 15 minutes still exhibits quite uniform monolayer graphene with a coverage of 91%, indicating that there exists a rather large growth window of annealing time for the growth of uniform monolayer graphene. It is known that from stoichiometry alone, the formation of a single graphene sheet requires

decomposition of 3.14 Si-C bilayers of SiC substrate and subsequent sublimation of Si and C atoms [26]. The sublimed C atoms are reabsorbed and coalesced to the remaining C atoms on the surface to form the next layer graphene. By increasing the annealing time to 30 minutes, the LEEM results (field of view = 5 μm , see Fig. 3e) demonstrate that the sample is covered by 10% monolayer, 87% bilayer, and 3% trilayer graphene. This designates that the high-density steps on off-axis 3C-SiC can provide more nucleation sites contributing to the formation of uniform multilayer graphene. In Fig. 3f-j, the number of graphene layers is determined by the number of dips in electron reflectivity [27], the curves are collected from the labeled regions in Fig. 3a-e.

Fig. 4. The decomposition degree of bunched steps, defined as a ratio of the number of steps with height in the range of the original 3C-SiC steps to the total number of the steps from the statistic histograms, as a function of annealing time at 1800 °C. It clearly shows a 100% elimination of step bunching after 5-minute annealing.

The structural properties of graphene layers are also characterized by μ -LEED measurements. Fig. 3k-o shows the LEED patterns of graphene samples grown at 1800 °C with annealing time from 0 to 30 minutes. The LEED pattern for the sample annealed at 1800 °C for 0 minute (Fig. 3k) displays bright (1×1) graphene spots and surrounding $(6\sqrt{3}\times 6\sqrt{3})$ R30° buffer layer spots, as well as SiC (1×1) spots but without $(\sqrt{3}\times \sqrt{3})$ R30° spots, illustrating that the surface is already covered with C-rich reconstruction and graphene [28]. With increased annealing time, the sharp bright (1×1) graphene diffraction spots dominate the LEED patterns, indicating a high-quality crystalline graphene. Moreover, as the annealing time is increased to 30 minutes, the second layer of graphene

forms on the first graphene layer (Fig. 3e) and the LEED patterns show sharp bright graphene spots (Fig. 3o).

Considering the challenge to grow multilayer (> 3 layers) graphene on nominally on-axis hexagonal SiC substrates, the off-axis 3C-SiC can provide periodic steps which act as nucleation sites for graphene growth. Consequently, the uniform monolayer and bilayer graphene can be grown in a large area on such off-axis 3C-SiC by selecting the annealing time. In order to grow thicker graphene layers, we further increased the annealing temperature to 2000 °C for 30 minutes. As seen in Fig. 5a, the AFM result reveals that the step height and terrace width are identical to those of the pristine 3C-SiC, indicating that no step bunching has occurred at these growth conditions during multilayer graphene growth. The LEEM results shown in Fig. 5b, d clearly demonstrate that four-layer graphene with a coverage of 70% has been grown on such off-axis 3C-SiC. The sharp bright LEED pattern (Fig. 5c) indicates a high crystalline quality of multilayer (1×1) graphene. Thus, we note that in this work we demonstrate that uniform four-layer graphene can be grown over areas of tens of square micrometers, which has not been reported yet in the literature. A prerequisite for this is high quality 3C-SiC material.

Fig. 5. The AFM topography $2 \times 2 \mu\text{m}^2$ image (a) and LEEM image (b) recorded in the field of view of $10 \mu\text{m}$ with an electron energy of 2.89 eV for the four-layer graphene (70% coverage) grown on 3C-SiC at 2000 °C for 30 min. (c) The μ -LEED pattern taken on the four-layer region with a kinetic energy of 49.9 eV. (d) The electron reflectivity curve collected from the labeled regions in (b).

Raman maps were performed to further characterize the structural properties of the graphene layers. Fig. 6a shows typical Raman spectra obtained from the four samples grown at 1800 °C for

0, 15, 30 minutes and 2000 °C for 30 minutes, respectively. In all samples we observe the G and 2D peaks, which are typical characteristics of graphene. The G peak located around 1600 cm^{-1} is the first-order Raman scattering process in the first Brillouin zone while the 2D band located from 2730 cm^{-1} to 2750 cm^{-1} originates from the second-order scattering [29]. In addition, a double-band structure including two bands peaking around 1360 and 1600 cm^{-1} is observed in the samples. This structure resembles the spectrum from the buffer layer underlying the graphene on hexagonal polytypes [30], therefore, we attribute it to the buffer layer on off-axis 3C-SiC. We notice that the intensities of the G and 2D peaks in the Raman map of the sample annealed at 1800 °C for 0 minute exhibit strong variations and both intensities are significantly (at least by a factor of five) than those in monolayer graphene, in agreement with the low monolayer coverage observed by LEEM. Note that the G peak overlaps the high-energy band of the buffer layer, whereas the D peak, whenever presents, would overlap the low-energy band of the buffer layer since its position ($\sim 1350 \text{ cm}^{-1}$) nearly coincides with the top of the low-energy band at $\sim 1360 \text{ cm}^{-1}$. We notice no significant contribution from the defect-activated D peak [31], which suggests good crystalline quality of the grown graphene. The D-peak contribution might be anticipated in the sample annealed at 1800 °C for 0 minute, because of the presence of edges associated with incomplete monolayer coverage but are not observed probably because of the overall weak contribution from the monolayer in the spectra of this sample. For this sample, the 2D peak exhibits a single Lorentzian shape with a full width at half maximum (FWHM) of $\sim 47 \text{ cm}^{-1}$, indicating the feature of monolayer graphene. For the sample annealed at 1800 °C for 15 minutes, the LEEM result shows a coverage of 96% monolayer graphene and the Raman spectrum exhibits strong G and 2D peaks. The 2D peak again shows a single Lorentzian shape with a full width at half maximum (FWHM) of $\sim 42 \text{ cm}^{-1}$. For the samples grown at 1800 °C for 30 minutes and 2000 °C for 30 minutes (green and purple), the 2D

peaks exhibit asymmetric shape and show a clear blueshift of the peak position as well as a significant increase of the FWHM to $\sim 70 \text{ cm}^{-1}$. This typical change of 2D peak is explained by the evolution of the electronic band with increasing the number of graphene layer [32]. In order to accumulate some statistics on the Raman spectra variation over the surface, we also performed $3 \times 3 \text{ }\mu\text{m}^2$ Raman maps on these four samples (Suppl. information Fig. S3). The histograms of the 2D peak width (FWHM) obtained from the Raman maps are shown in Fig. 6c-f. They clearly illustrate the increase of the 2D-peak FWHM with increase of graphene thickness. The larger FWHM in the case of multilayer graphene is due to the several components composing the 2D peak [29]. As seen in Fig. 6b, the position of Raman 2D peaks in our graphene/3C-SiC samples corresponds well to the 2D peaks of graphene grown on 4H- or 6H-SiC and measured with the same laser wavelength in other studies. This indicates that the use of off-axis 3C-SiC does not influence the graphene properties significantly. It is worth to note that the D peak is very weak or even non-observable, in contrast to previously reported results on graphene grown on 3C-SiC/Si [33]. A low intensity of D-peak or small intensity ratio of I_D/I_G implies a high crystalline quality [28].

Fig. 6. (a) Raman spectra of graphene samples grown on 3C-SiC at 1800 °C for 0, 15, 30 minutes and 2000 °C for 30 minutes. The spectra shown here are after subtraction of a reference spectrum of the 3C-SiC substrate. (b) Positions of the 2D peaks obtained from the graphene grown on the off-axis 3C-SiC in comparison with previous results measured on graphene grown on 4H- or 6H-SiC substrates using the same laser wavelength. (c-f) Histograms of the 2D FWHM counted from the Raman maps (see Fig. S3b) of four samples displayed in Raman spectra.

Considering a possible mechanism for step bunching during the growth of buffer layer and a complete decomposition of bunched steps during graphene growth on off-axis 3C-SiC, we propose a growth model which includes step bunching, decomposition of bunched steps and monolayer graphene formation processes. Consider a pristine 3C-SiC surface containing six periodic steps as shown schematically in Scheme 1a. A schematic illustration of the crystal structure of 3C-SiC and its orientation in the steps is shown in Scheme 1h. As presented above, we observed that the height of majority of steps on pristine 4 degrees off-axis 3C-SiC(111) surface is about 1.5 nm (6 bilayers). During the buffer layer formation, the thermal etching of SiC steps and the restructuring of carbon atoms on the surface occur simultaneously. The buffer layer, in a form of small islands, starts to nucleate at step edges, where the density of dangling bonds is the highest [34]. This leads to some disturbances/irregularities in step rate over step edges. As demonstrated in Scheme 1b, if the step edges are not covered with buffer layer islands (position A, C), they are etched faster than the covered ones (position B) giving rise to a wandering step edge structure. Since the step 3 and 4 are not covered with buffer layer islands, both have a faster etching rate compared to the one at position B. Therefore, during etching process the step 4, first, merges together with step 5 (see location B in Scheme 1c) and then, the step 3 also merges with steps 4 and 5 to form a large bunched step, as shown in position B in Scheme 1d. Region D, E and F shown in Scheme 1d are the other random buffer layer nucleation sites where step bunching occurs by merging of 3 steps. Consequently, each bunched step and the entire surface is fully covered with a buffer layer. Here, as an example, we take 3 steps to explain the formation of bunched steps. However, based on AFM results (Fig. 11), we observed that macro-steps on the pristine 3C-SiC surface could be formed of up to 4 steps (24 bilayers or 6 nm). These kinds of step height might be related to minimizing the surface energy [35].

Scheme 1. A schematic illustration of the step bunching process and the decomposition process of the bunched steps. (a) 3C-SiC substrate with six periodic steps. (b-d) The formation of step bunching during the buffer layer growth. (e-g) The decomposition of bunched steps during monolayer graphene growth. Color code: 3C-SiC (green-yellow), buffer layer (orange), monolayer graphene (red). As indicated by the different lengths of blue arrows in (b), the steps without buffer layer has a higher thermal etching rate than steps covered by the buffer layer.

Upon further annealing, there is a decomposition process of bunched steps. Given the same thermal decomposition energy of 3C-SiC steps, the bunched steps are supposed to be etched at the same rate as well. Here, the topmost of the step edge moves out preferentially because the topmost step edge can be etched faster where the density of dangling bonds is higher than the underlying one. Therefore, a new small step D' is decomposed from position D as shown in Scheme 1e. Along with this decomposition, as drawn in Scheme 1e, the residual carbon atoms form a monolayer graphene at the terrace of the new decomposed small step D'. This is confirmed by the AFM and LEEM results. As described in Fig. 1c, d, along with the decomposition of bunched steps, monolayer graphene is formed simultaneously on the small decomposed steps.

Once the topmost step D' (Scheme 1f) moves away from its previous position in the bunched step edge, the step edge of the middle step is exposed and another new small step D'' is decomposed as a higher density of dangling bonds contributes to a faster etching rate again. Simultaneously, a new graphene monolayer domain forms and incorporates into the former one into a larger and continuous graphene domain. Eventually, as seen in Scheme 1g, all the bunched steps decompose into small steps which have the same step height as that of pristine 3C-SiC and

monolayer graphene is simultaneously covering the decomposed small steps. With further increasing of the annealing time, the new multilayer graphene can be formed on the top of monolayer graphene/3C-SiC without occurrence of step bunching, as confirmed by the AFM and LEEM results shown in Fig. 1-3. The underlying reason is because the underneath 3C-SiC, which is fully covered by the graphene layer, would have the identical step decomposition rate during the next layer growth of the multilayer graphene.

4. Conclusions

We have successfully demonstrated a full elimination of the step bunching of SiC and a controllable growth of large-area monolayer, bilayer, and four-layer graphene on free standing samples of off-axis 3C-SiC(111) produced from 4H-SiC(0001). The AFM and LEEM results show that during the buffer layer growth, several steps (up to 4) of pristine 3C-SiC merge together while the bunched steps can be fully decomposed during the monolayer graphene growth. Along with the full elimination of step bunching, large area uniform monolayer and multilayer graphene were grown on off-axis 3C-SiC. The number of graphene layers can be accurately controlled by adjusting growth time and temperature. The micro-Raman spectra and their maps verify that the quality of the graphene layers is similar to that grown on hexagonal SiC substrates. A growth model is proposed to explain the observed decomposition of bunched steps during graphene growth. Particularly, we demonstrate the growth of uniform four-layer graphene over areas of tens of square micrometers, which opens up the possibility to tune the bandgap for electronic and photonic devices.

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Author Contributions

J. Sun, R. Yakimova, M. Syväjärvi conceived the research idea. Y. Shi performed the growth of graphene and 3C-SiC and AFM measurements with the help of G.R. Yazdi and V. Jokubavicius. A. A. Zakharov performed the LEEM and LEED measurements. I. G. Ivanov performed the Raman characterizations. Y. Shi contributed to the initial elaboration of the manuscript. J. Sun wrote the manuscript with inputs from all co-authors. J. Sun supervised the project.

Notes

The authors declare no competing financial interest.

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Table

Table 1. A comparison for the coverage of graphene layers obtained from AFM and LEEM.

Note: The coverage of the buffer, monolayer and bilayer graphene obtained from AFM phase images (Fig. 1g, h, j) and LEEM results (Fig. 3a, b, c) for the graphene samples grown on 3C-SiC at 1800 °C for 0, 1, 5 minutes, respectively.

Figures

Fig. 1. The AFM topography $2 \times 2 \mu\text{m}^2$ images (a-e), phase images (f-j) generated at the same region as topography images, and the histograms (k-o) of the statistic step heights for the pristine 3C-SiC and the graphene samples grown on 3C-SiC at 1800 °C for 0-5 minutes, respectively. The step height profiles of the indicated lines with a dimension of 500 nm are shown in the insets of images (a-e).

Fig. 2. The AFM topography $2 \times 2 \mu\text{m}^2$ images (a, b), phase images (c, d) generated at the same region as topography images, and the histograms (e, f) of the statistic step heights for the graphene samples grown on 3C-SiC at 1800 °C for 15 and 30 minutes, respectively. The step height profiles of the indicate lines with a dimension of 500 nm are shown in the insets of images (a, b).

Fig. 3. (a-e) LEEM images (field of view = 5 μm) of the graphene samples grown on 3C-SiC at 1800 °C for 0, 1, 2, 5, 15, 30 minutes, which were measured with an electron energy of 3.46, 3.25, 5.15, 5.06 and 5.88 eV, respectively. (f-j) The electron reflectivity curves collected from the labeled regions in (a-e). The number of graphene layers is determined by the number of dips in electron reflectivity curves. (k-o) The μ -LEED patterns collected on the buffer layer (a, b), monolayer graphene (c, d), and bilayer graphene (e) are measured at 43.0, 48.1, 48.2, 47.7 and 47.0 eV, respectively. A probing area of 500~1000 nm was used during μ -LEED measurements. Bright graphene spots (red arrows) and surrounding ($6\sqrt{3} \times 6\sqrt{3}$) R30° buffer layer spots, as well as SiC (1×1) spots (green arrows) are indicated by arrows.

Fig. 4. The decomposition degree of bunched steps, defined as a ratio of the number of steps with height in the range of the original 3C-SiC steps to the total number of the steps from the statistic histograms, as a function of annealing time at 1800 °C. It clearly shows a 100% elimination of step bunching after 5-minute annealing.

Fig. 5. The AFM topography $2 \times 2 \mu\text{m}^2$ image (a) and LEEM image (b) recorded in the field of view of $10 \mu\text{m}$ with an electron energy of 2.89 eV for the four-layer graphene (70% coverage) grown on 3C-SiC at 2000 °C for 30 min. (c) The μ -LEED pattern taken on the four-layer region with a kinetic energy of 49.9 eV. (d) The electron reflectivity curve collected from the labeled regions in (b).

Fig. 6. (a) Raman spectra of graphene samples grown on 3C-SiC at 1800 °C for 0, 15, 30 minutes and 2000 °C for 30 minutes. The spectra shown here are after subtraction of a reference spectrum of the 3C-SiC substrate. (b) Positions of the 2D peaks obtained from the graphene grown on the off-axis 3C-SiC in comparison with previous results measured on graphene grown on 4H- or 6H-SiC substrates using the same laser wavelength. (c-f) Histograms of the 2D FWHM counted from the Raman maps (see Fig. S3b) of four samples displayed in Raman spectra.

Scheme

Scheme 1. A schematic illustration of the step bunching process and the decomposition process of the bunched steps. (a) 3C-SiC substrate with six periodic steps. (b-d) The formation of step bunching during the buffer layer growth. (e-g) The decomposition of bunched steps during monolayer graphene growth. Color code: 3C-SiC (green-yellow), buffer layer (orange), monolayer graphene (red). As indicated by the different lengths of blue arrows in (b), the steps without buffer layer has a higher thermal etching rate than steps covered by the buffer layer. (h) Schematic of atomic structure and the crystallographic axes of 3C-SiC, which is a side view of (a). The terrace and step are indicated.

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Sample	0 minute		1 minute		5 minutes	
	buffer	monolayer	buffer	monolayer	monolayer	bilayer
AFM Phase	81%	19%	74%	26%	90%	10%
LEEM	80%	20%	75%	25%	96%	4%

Table 1. A comparison for the coverage of graphene layers obtained from AFM and LEEM.

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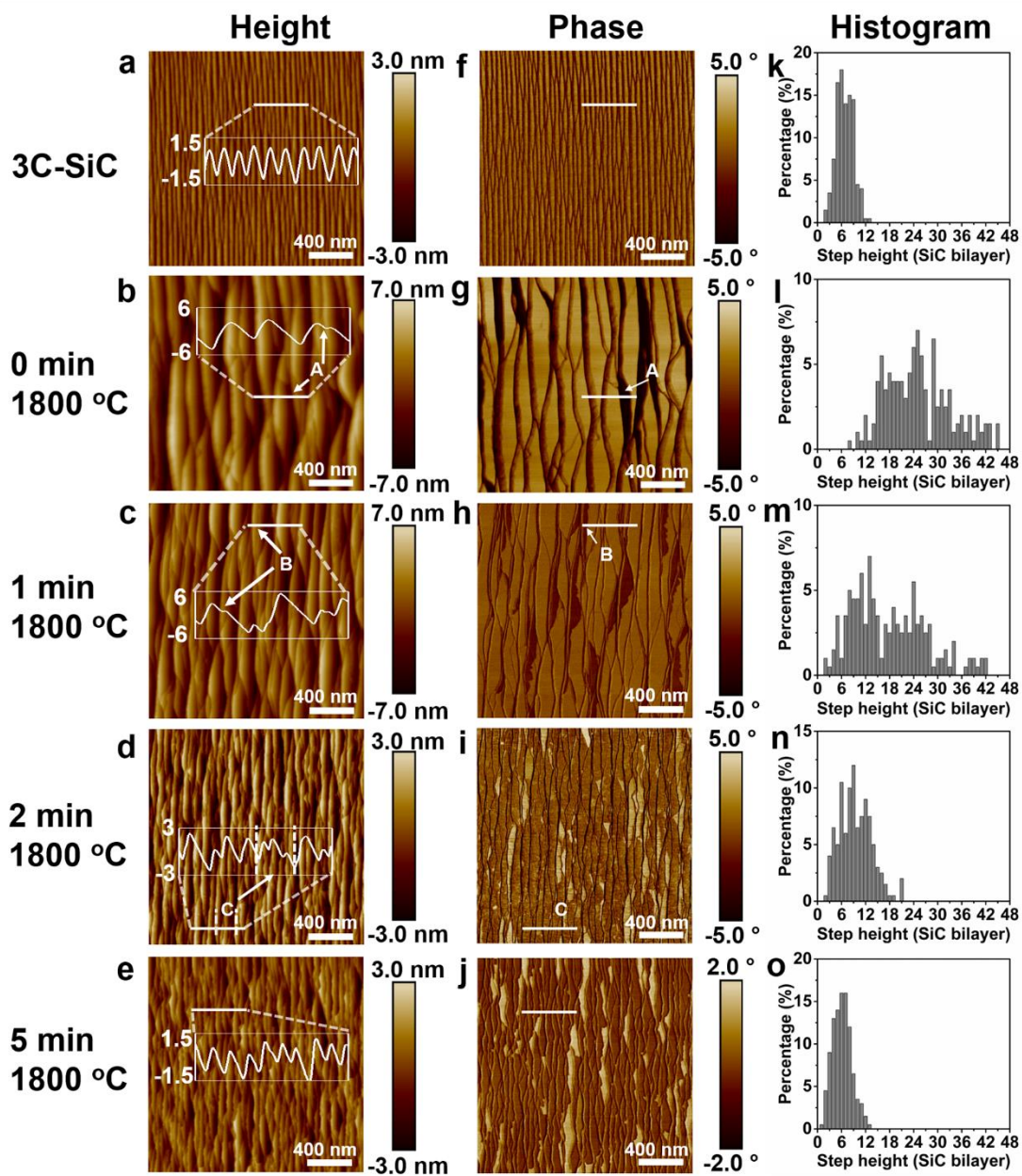


Fig. 1.

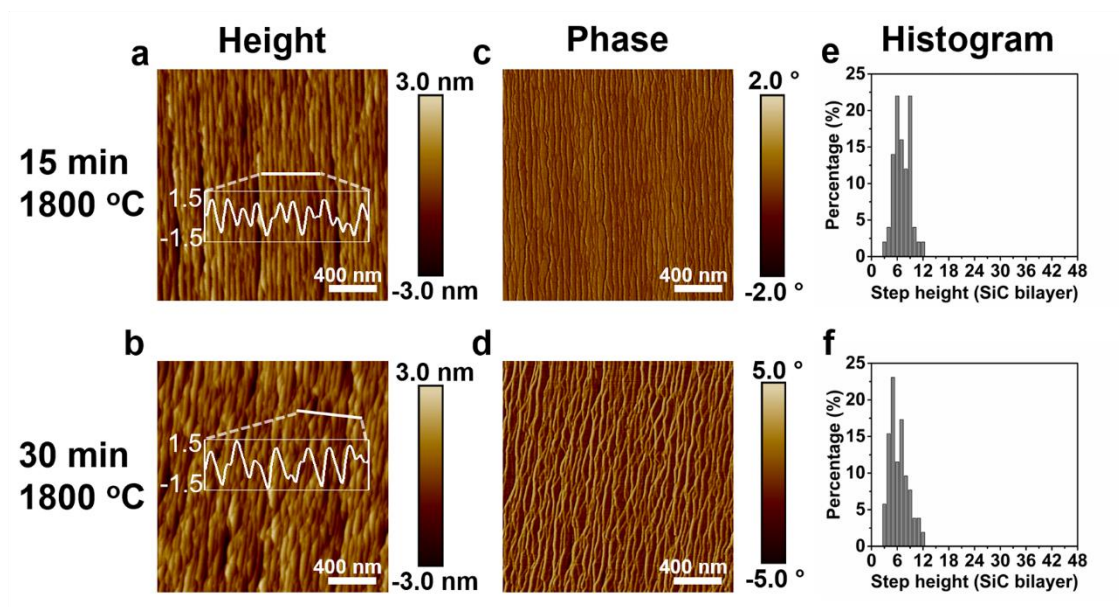


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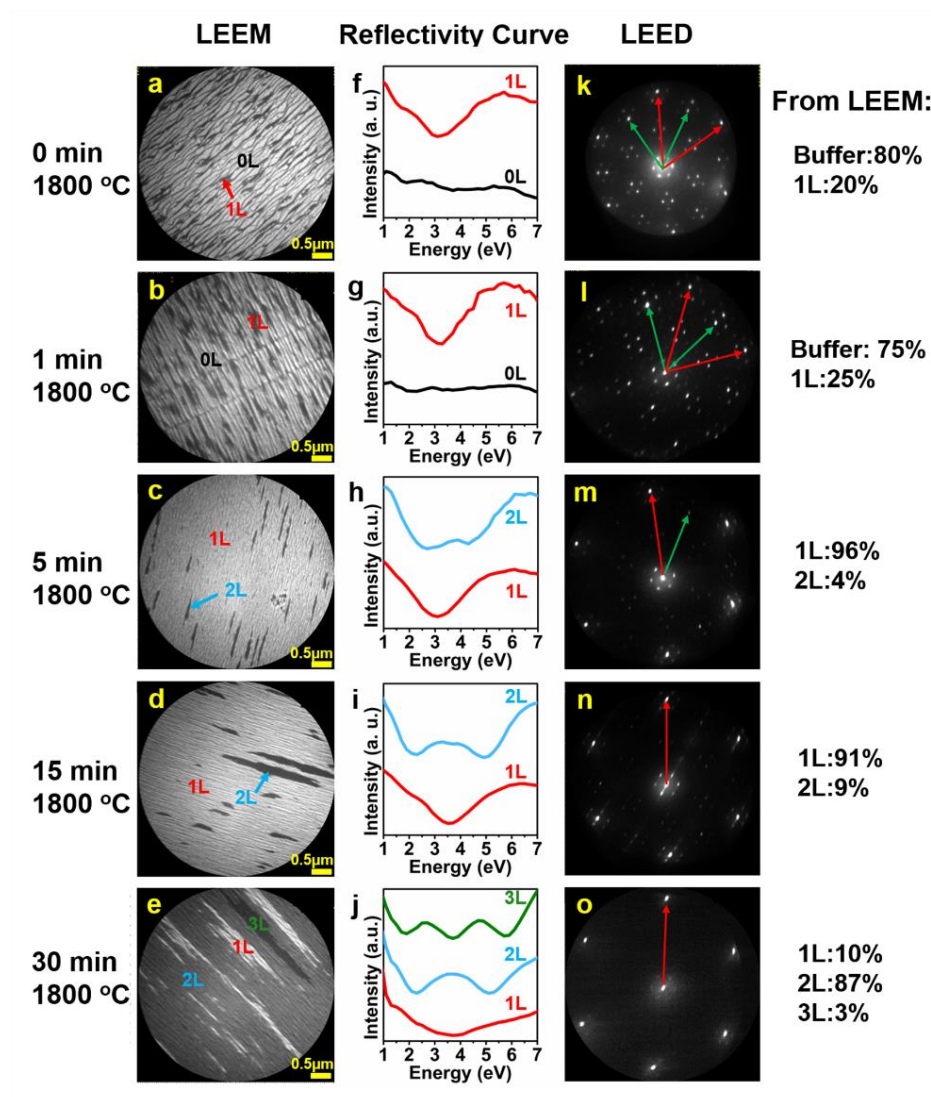


Fig. 3.

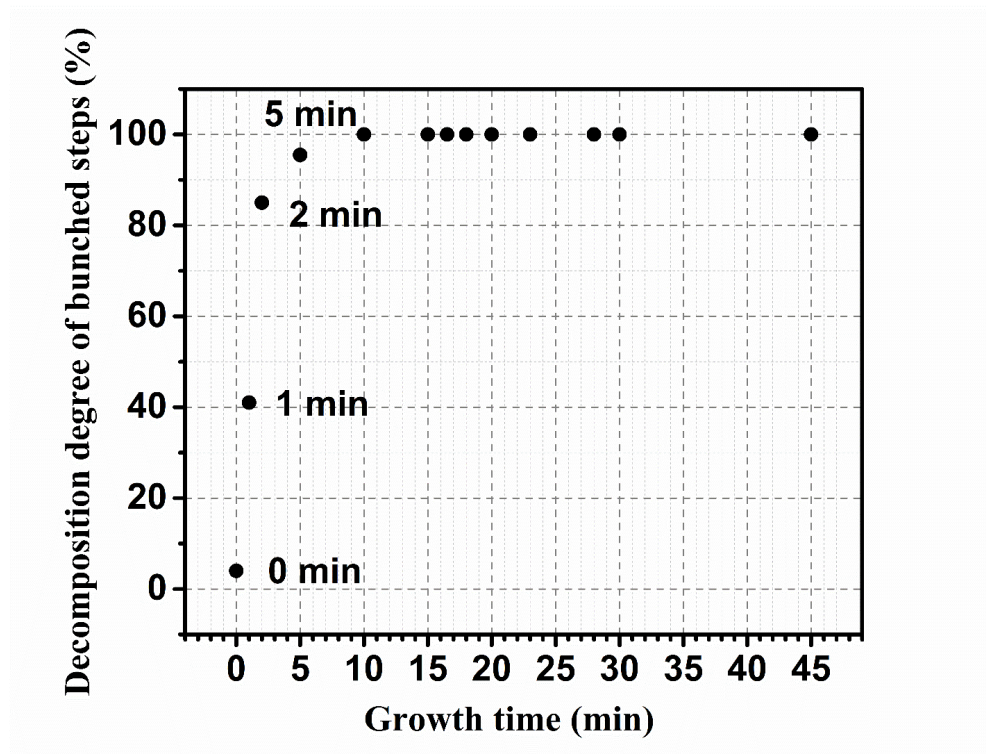


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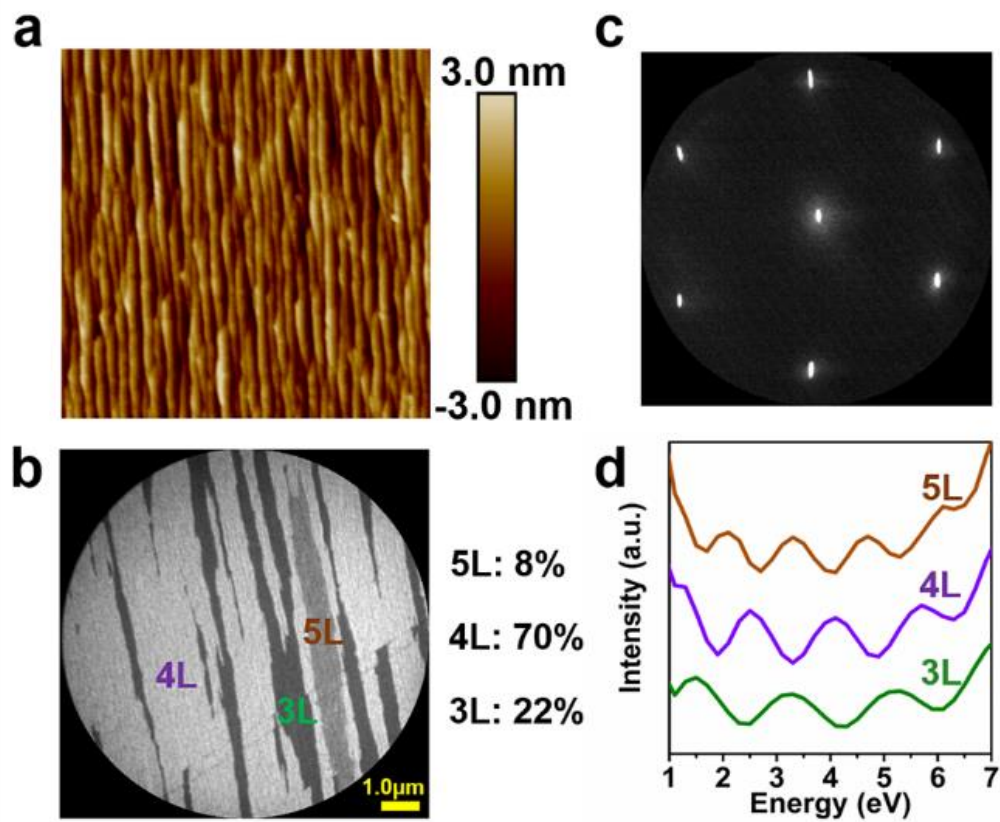


Fig. 5.

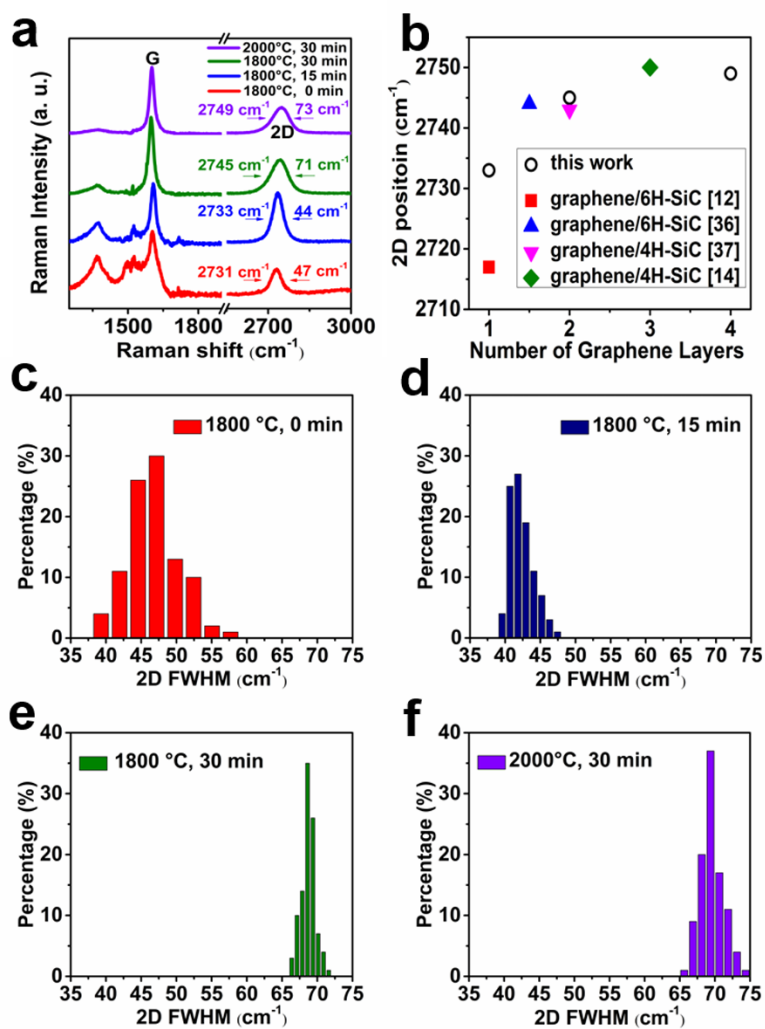
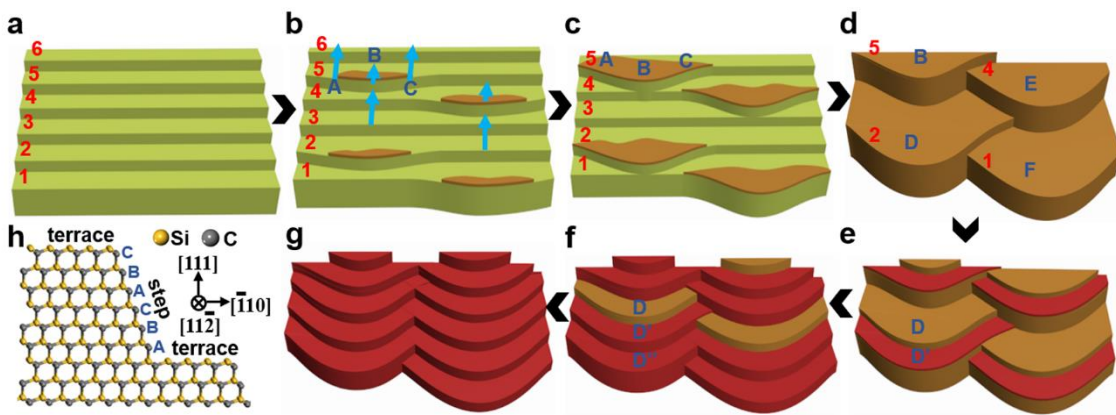


Fig. 6.



Scheme 1. A schematic illustration of the step bunching process and the decomposition process of the bunched steps.