4H-SiC epitaxy investigating carrier lifetime and substrate off-axis dependence

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Cover: 2 μm x 2 μm atomic force microscopy image of an 8 μm thick epilayer grown on a 1.02° off-cut substrate with step heights of 1.5 nm to 6 nm.

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To my family

ABSTRACT

Silicon carbide (SiC) is a wide bandgap semiconductor with unique material properties making it useful for various device applications using high power, high frequency and high temperature. Compared to Si-based electronics, SiC based electronics have an improved energy efficiency. One of the most critical problems is to reduce this planets power consumption, where large improvements can be made enhancing the energy efficiency. Independent on how the electrical power is generated, power conversion is needed and about 10% of the electrical power is lost for every power conversion step using Si-based electronics. Since the efficiency is related to the performance of the semiconductor device, SiC can make contributions to the efficiency. Compared to Si, SiC has three times larger bandgap, about ten times higher breakdown electric field strength and about three times higher thermal conductivity. The wide bandgap together with the chemical stability of SiC makes it possible for SiC electronic devices to operate at much higher temperatures ($>250^{\circ}\text{C}$) compared to Si-based devices and do not require large cooling units as with Si power converters.

The current status for 4H-SiC devices regard unipolar devices ($\leq 1700\text{ V}$), such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and Schottky barrier diodes (SBDs), are now on the market for mass production. The

research focus is now on high-voltage (>10 kV) bipolar devices, such as, bipolar junction transistors (BJTs), p-i-n diodes and insulated-gate bipolar transistors (IGBTs).

The focus of this thesis are material improvements relevant for the development of 4H-SiC high-voltage bipolar devices. A key parameter for such devices is the minority carrier lifetime, where long carrier lifetimes reduce the on-resistance through conductivity modulation. However, too long carrier lifetimes give long reverse recovery times leading to large switching losses. Thus, a tailored carrier lifetime is needed for the specific application. Carrier lifetimes of the epilayers can both be controlled by the CVD growth conditions and by post-growth processing, such as thermal oxidation and carbon implantation followed by thermal annealing. Emphasis in this thesis (**Paper 1-2**) is to find optimal CVD growth conditions (growth temperature, C/Si ratio, growth rate, doping) improving the carrier lifetime. Since the main lifetime limiting defect has shown to be the $Z_{1/2}$ center, identified as isolated carbon vacancies, growth conditions minimizing the $Z_{1/2}$ concentration are strived for.

To achieve high-voltage bipolar devices, thick epilayers of high quality is needed. An important factor is then the growth rate that needs to be relatively high in order to reduce the fabrication time, and thus the cost of the final device. In this thesis the growth process has been optimized for high growth rates ($30\text{ }\mu\text{m/h}$) using standard silane and propane chemistry (**Paper 3**), compared to other chemistries that includes chlorine, which results in corroded reactor parts and new defects in the epitaxial layers.

Another important parameter for 4H-SiC bipolar devices is the basal plane dislocations (BPDs) in the substrate and epilayers, since the BPDs can act as source of nucleation and expansion of Shockley stacking faults (SSFs). The expanded SSFs give a lowered carrier lifetime and form a potential barrier for carrier transport leading to an increased forward voltage drop which in turn leads

to bipolar degradation. The bipolar degradation is detrimental for 4H-SiC bipolar devices. Several strategies are developed to reduce the density of BPDs including buffer layers, growth interrupts and decreasing the substrates off-cut angle. **Paper 4-6** is focused on developing a CVD growth process for low substrate off-cut angles (1° and 2°) compared to the today's standard off-cut angle of 4° . By reducing the substrate off-cut angle the number of BPDs intersecting the substrate surface is reduced. In addition, the conversion from BPDs to threading edge dislocations (TEDs) during epitaxial growth is increased with lower off-cut angles.

POPULÄRVETENSKAPLIG SAMMANFATTNING

Kiselkarbid (SiC) är ett viktigt halvledarmaterial för framtidens elektronik, särskilt för tillämpningar med höga spänningar, höga frekvenser och höga temperaturer. I jämförelse med kiselbaserad elektronik ger elektronik baserad på SiC mindre energiförluster, speciellt vid omvandlingar mellan växelström och likström som kommer att spela en större roll i framtiden. En av framtidens största utmaningar är att minska jordens energikonsumtion och där kan förbättringar göras genom att öka energieffektiviteten. Oberoende av hur den elektriska energin är genererad krävs kraftomvandlingar och idag förloras ca 10% av den elektriska energin för varje omvandling då kiselbaserad elektronik används. Här kan kiselkarbid ge stora bidrag till energieffektivisering jämfört med kisel (Si), tack vare egenskaper som större bandgap, högre kritisk fältstyrka samt högre termisk konduktivitet. Det stora bandgapet och den kemiska stabiliteten hos SiC gör att SiC-komponenter kan arbeta vid betydligt högre temperaturer än motsvarande Si-komponenter, varvid stora kylaggregat inte längre krävs.

På marknaden finns redan idag unipolära kiselkarbidkomponenter ($\leq 1700\text{V}$) medan utveckling fortfarande krävs av bipolära komponenter för höga spänningar ($> 10\text{kV}$). Denna avhandling fokuserar på relevanta materialförbättringar för bipolära SiC komponenter tänkta för höga spänningar.

En avgörande parameter för bipolära komponenter är livstiden hos minoritetsladdningsbärarna. Livstiden har studerats för olika tillväxtförhållanden under kemisk förångningsdeposition (CVD) av kiselkarbid. För att åstadkomma bipolära komponenter för höga spänningar krävs tjocka epitaxiella skikt och således höga tillväxthastigheter för att minska komponenternas kostnad. En process för hög tillväxthastighet ($30\mu\text{m/h}$) har utvecklats med silan- och propanskemi, till skillnad mot andra processer där klor används vilket leder till korrosion av reaktordelar samt nya defekter i materialet. För att bibehålla kristallstrukturen hos SiC under deponeringen används substrat med lutande kristallplan, dock leder detta till att dislokationer i basalplanet kommer upp till substratets yta och fortsätter in i det epitaxiella SiC skikt som deponeras. Nackdelen med dessa dislokationer är att de kan omvandlas till staplingsfel i kristallen då höga strömmar går genom komponenten, vilket leder till ökad resistans och slutligen förstörs komponenten (bipolär degradering). I denna avhandling har tillväxtförhållanden utvecklats för att möjliggöra epitaxiell tillväxt på substrat med en mindre lutning (1° och 2°) av kristallplanet, jämfört med dagens standardvinkel 4° , med avsikten att minska problemet med bipolär degradering.

PAPERS INCLUDED IN THE THESIS

PAPER 1

L. Lilja, I. Booker, J. Hassan, E. Janzén and J. P. Bergman

Influence of growth conditions on carrier lifetime in 4H-SiC epilayers

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PAPER 2

L. Lilja and J. P. Bergman

Influence of n-type and p-type doping on carrier lifetime in 4H-SiC epilayers

Manuscript

PAPER 3

L. Lilja, J. Hassan, E. Janzén and J. P. Bergman

Smooth 4H-SiC epilayers grown with high growth rates with silane/propane chemistry using 4° off-cut substrates

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PAPER 4

L. Lilja, J. Hassan, E. Janzén and J. P. Bergman

Improved epilayer surface morphology on 2° off-cut 4H-SiC substrates

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PAPER 5

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In-grown stacking faults in 4H-SiC epilayers grown on 2° off-cut substrates

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PAPER 6

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Comparison of 4H-SiC epitaxial layers grown on 1°, 2° and 4° off-cut substrates

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CONTENTS

ABSTRACT.....	v
POPULÄRVETENSKAPLIG SAMMANFATTNING	ix
PAPERS INCLUDED IN THE THESIS	xi
PAPERS NOT INCLUDED IN THE THESIS	xiii
AKNOWLEDGEMENTS.....	xv
PART 1: Introduction to the field.....	1
1 Introduction	3
2 Silicon carbide	5
2.1 Silicon carbide historically.....	5
2.2 Crystal structure of silicon carbide	6
2.3 Electronic properties of silicon carbide.....	8
3 Silicon carbide growth.....	13
3.1 Bulk crystal growth	13
3.2 Epitaxial growth	17
3.3 Chemical vapor deposition.....	18

3.3.1 Epitaxial growth on off-cut substrates	24
3.3.2 High epitaxial growth rates using standard chemistry	27
3.3.3 Epitaxial growth conditions effect on carrier lifetime	29
4 Characterization techniques	31
4.1 Optical microscopy	31
4.2 Thickness measurements	32
4.3 Doping measurements	33
4.4 Atomic force microscopy	34
4.5 Low temperature photoluminescence	35
4.6 Time-resolved photoluminescence.....	37
4.7 Cathodoluminescence.....	42
4.8 Deep level transient spectroscopy.....	43
4.9 X-ray topography	45
5 References	49
PART 2: Papers.....	57
SUMMARY OF INCLUDED PAPERS	59
MY CONTRIBUTION TO THE PAPERS	63
PAPERS 1 - 6	

PART 1: Introduction to the field

1 Introduction

The World's energy consumption is constantly increasing and one important area of improvement is to enhance the energy efficiency of power electronics. Regardless of how electrical energy is generated, power conversion is needed and for each power conversion step about 10% of the electrical energy is lost today [1]. Particularly conversions between AC and DC will play a larger impact in the future and for such conversions, replacing silicon (Si) to silicon carbide (SiC) in the electronics would improve the energy efficiency. Thanks to the outstanding electrical and physical properties of SiC, SiC could replace Si in electronic devices intended for high power applications. 4H-SiC unipolar devices (≤ 1700 V), such as metal-oxide-semiconductor field-effect transistors (MOSFETs) and Schottky barrier diodes (SBDs) are already on the market, however more research is needed to realize high-voltage (> 10 kV) bipolar devices such as bipolar junction transistors (BJTs), p-i-n diodes and insulated-gate bipolar transistors (IGBTs) [2].

The work in this thesis is focused on material improvements of 4H-SiC in order to realize bipolar electronic devices intended for high-voltage applications. In order to achieve SiC bipolar devices with very high blocking voltages and low-loss conduction, the drift layers must have long carrier lifetimes to achieve

sufficient conductivity modulation [3]. Carrier lifetime improvements can either be done using proper epitaxial growth conditions [4-8] or by post-growth processing techniques [9, 10]. The first two papers relate the chemical vapor deposition (CVD) growth conditions (growth temperature, C/Si ratio, growth rate, doping) to the material property minority carrier lifetime. The observed difference in minority carrier lifetime is also related to the concentration of the main lifetime limiting defect, the $Z_{1/2}$ center, identified as isolated carbon vacancies [11]. To make SiC high-voltage bipolar devices attractive to the market the price needs to be lowered. One step in that direction is to enhance the epitaxial growth rate and in paper 3 we demonstrate 30 $\mu\text{m}/\text{h}$ using standard silane/propane chemistry, without any addition of chlorine. Adding chlorine results in corroded reactor parts and new defects in the epitaxial layers [12]. In order to preserve the crystal structure during epitaxial growth, substrates with a slight off-cut angle is used. However, this leads to that basal plane dislocations (BPDs) propagates to the substrate surface and continues into the epilayer. BPDs can act as a source of nucleation and expansion of Shockley stacking faults (SSFs) when high currents go through the device, which leads to increased resistance and ultimately destroys the device, a phenomenon called bipolar degradation [13]. To achieve high-voltage 4H-SiC bipolar devices, the density of BPDs must be reduced. There are several strategies to reduce the density of BPDs including buffer layers, growth interrupts and decreasing the substrates off-cut angle [14-16]. By reducing the substrate off-cut angle the number of BPDs intersecting the substrate surface is reduced and the conversion from BPDs to the less dangerous threading edge dislocations (TEDs) is expected to increase, minimizing the problem with bipolar degradation. The last three papers of this thesis are focused on developing CVD growth conditions for 1° and 2° off-cut substrates compared to the today's standard 4° off-cut substrates.

2 Silicon carbide

In this section silicon carbide will be described historically, since it is not only known as a semiconductor material. Further, the crystal structure and electronic properties of silicon carbide will be described.

2.1 Silicon carbide historically

Even though silicon carbide has existed for billions of years, it was not until 1824 when the Swedish chemist Jöns Jakob Berzelius synthesized silicon carbide (SiC) for the first time SiC received increasing attention. Berzelius published a paper where the existence of a chemical bond between Si and C was proposed [17]. Natural silicon carbide, the mineral Moissanite, was found for the first time in 1905 by Henri Moissan in a meteorite in Canyon Diablo, Arizona [18]. In 1892, Edward Acheson developed the first commercial manufacturing process for making an industrial abrasive of silicon carbide, which he called “carborundum” [19]. The first applications of SiC were thus related to its hardness and SiC was used as an abrasive. But already in 1907, electroluminescence was observed in silicon carbide by Henry Joseph Round [20].

2.2 Crystal structure of silicon carbide

Silicon carbide is an IV-IV compound semiconductor and is constructed of silicon (Si) and carbon (C) atoms in 1:1 ratio. Each Si atom binds to four C atoms and each C atom binds to four Si atoms. The structural unit of SiC is a tetrahedron, that either can be represented by one C atom surrounded by Si atoms or one Si atom surrounded by C atoms, see Figure 2.1. The bond between Si and C is 88% covalent and 12% ionic, where C is more electronegatively charged [21]. The distance between either two neighboring Si atoms or C atoms is 3.08 Å and the bond length between Si and C is 1.89 Å [21]. The distance between the Si atom on the top to the C atom in Figure 2.1 (a) appears to have a longer distance compared to the three other Si atoms viewed from the side. Therefore, cleaving the crystal orthogonal to the c-axis this bond is most likely broken. The resulting crystals will then have two different faces, denoted Si-face and C-face. Those two different faces will be further discussed in section 3.2, regarding different properties of the faces during epitaxial growth.

Figure 2.1: The tetrahedron building block of SiC, that either can be represented with a C atom in the center bonded to four Si atoms (a) or a Si atom in the center bonded to four C atoms (b).

The SiC crystal can be described by closely packing of the above mentioned tetrahedrons giving a crystal composed of Si-C bilayers in a certain stacking sequence with an interlayer distance of 2.52 Å. There are three possible ways of stacking the tetrahedrons, referred to as A, B and C. The different possibilities of stacking the tetrahedrons give rise to something called polytypism which is a one-dimensional type of polymorphism. That SiC exhibits polytypism, means that SiC exists in different structural modifications where each polytype is built up of stacking layers, which are identical in structure and composition, and the difference is in their stacking sequence [22]. Three examples of different SiC polytypes can be seen in Figure 2.2. 3C-SiC with stacking sequence ABC, 4H-SiC with stacking sequence ABCB and 6H-SiC with stacking sequence ABCACB. Polytypes are described with Ramsdell notation [23], where the capital letter corresponds to the crystal symmetry (C for a cubic crystal structure and H for a hexagonal crystal structure) and the number refers to the periodicity (the number of Si-C bilayers in the unit cell).

Figure 2.2: Three polytypes of SiC and their corresponding stacking order, 3C-SiC (ABC), 4H-SiC (ABCB) and 6H-SiC (ABCACB).

Polytype	Stacking sequence	Lattice parameters [Å]	Hexagonality [%]	Bandgap [eV]
3C-SiC	<i>ABC</i>	$a = 4.3596$	0	2.39
2H-SiC	<i>AB</i>	$a = 3.076$ $c = 5.048$	100	3.33
4H-SiC	<i>ABCB</i>	$a = 3.073$ $c = 10.053$	50	3.26
6H-SiC	<i>ABCACB</i>	$a = 3.0806$ $c = 15.1173$	33	3.02

Table 2.1: Properties of some common SiC polytypes at room temperature [24, 25].

Due to the different stacking sequence, the different polytypes have different material properties, see Table 2.1. For example, the bandgap varies from 2.39 eV for 3C-SiC to 3.33 eV for 2H-SiC, with the smallest bandgap for the pure cubic crystal and the largest bandgap for the pure hexagonal crystal. Thus, a larger percentage of hexagonality means a larger size of the bandgap [24]. All other polytypes are mixtures of cubic and hexagonal and therefore with a size of the bandgap in between those. As an example, 4H-SiC with a bandgap of 3.26 eV.

2.3 Electronic properties of silicon carbide

The properties of SiC is strongly dependent on the polytype and since the focus of this thesis is material improvements of SiC intended for high-voltage bipolar devices, 4H-SiC is the polytype of choice. This section will motivate the use of SiC and the choice of the 4H-SiC polytype, but comparisons will also be made to other SiC polytypes and other semiconducting materials.

Silicon carbide is a wide bandgap semiconductor with an indirect bandgap. The bandgap (E_g) is defined as the energy difference between valence band maximum (valance band edge) to the conduction band minimum (conduction

band edge). If the valence band edge and the conduction band edge lies at the same momentum (k-value), it is a direct bandgap and an electron in the conduction band can recombine with a hole in the valence band and the energy is conserved by emitting a photon (radiative transition). If the valence band maximum and conduction band minimum lies at different k-values, it is an indirect bandgap and to conserve the momentum the electron and hole recombine with the assistance of a phonon [26]. This multiparticle interaction has a lower probability and thus, the recombination efficiency is much lower in indirect bandgap materials than in direct bandgap materials. For that reason, indirect bandgap materials are used for electronic devices while direct bandgap materials are used for light-emitting-diodes (LED) and laser diodes.

The strong bonding between Si and C in silicon carbide gives the material a high hardness, high thermal conductivity and chemical inertness. The strong bonding is also an important factor for the wide bandgap and a high breakdown electric field strength. The SiC has unique semiconductor properties since it can have a wide doping range from about $1 \times 10^{14} \text{ cm}^{-3}$ to $1 \times 10^{19} \text{ cm}^{-3}$, both n-type and p-type. Compared to Si, SiC possess properties such as a three times larger bandgap, ten times higher breakdown electrical field strength and three times higher thermal conductivity, which are summarized in Table 2.2. Thanks to the wide bandgap of 4H-SiC, the material has a high breakdown electric field. The ten times higher breakdown electric field of 4H-SiC compared to Si implies that 4H-SiC can have one-tenth of the thickness for the voltage-blocking layers and about two orders of magnitude higher doping concentration. This results in lower resistance of the drift-layer which is important in high-voltage devices, since it determines the on-resistance of the power devices [1]. The high electron saturated drift velocity in 4H-SiC makes it possible to reduce the size of the device, since it is possible to use a higher current per unit area. The wide bandgap together with

	Si	4H-SiC	6H-SiC	3C-SiC	GaN
Bandgap [eV]	<i>1.12</i>	<i>3.26</i>	<i>3.02</i>	<i>2.39</i>	<i>3.39</i>
Thermal conductivity [Wcm ⁻¹ K ⁻¹]	<i>1.3-1.5</i>	<i>3.3-4.9</i>	<i>4.9</i>	<i>3.6</i>	<i>1.3</i>
Breakdown electric field (material with doping 10 ¹⁶ cm ⁻³) [MV/cm]	<i>0.3</i>	<i>2.2-2.8</i>	<i>2-3</i>	<i>1.2</i>	<i>3.3</i>
Electron saturated drift velocity [cm/s]	<i>1.0x10⁷</i>	<i>2.2x10⁷</i>	<i>2.0x10⁷</i>	<i>2.0x10⁷</i>	<i>2.5x10⁷</i>
Electron mobility [cm ² /Vs] (perpendicular to c-axis)	<i>1350</i>	<i>1020</i>	<i>380</i>	<i>900</i>	<i>900</i>

Table 2.2: Electrical properties of 4H-SiC in comparison with other polytypes and other semiconductors [1, 25, 27-29].

the chemical stability of SiC makes it possible for SiC electronic devices to operate at much higher temperatures (>250°C) compared to Si and do not require large cooling units [1]. A high thermal conductivity means that the produced heat during device operation can be removed more efficiently. All those factors make 4H-SiC high-voltage bipolar devices attractive to the market and could offer higher energy efficiency as a result of lower losses during power conversion and thanks to weight savings due to smaller devices and no need for large cooling units. One example of large power savings using SiC, are presented in a report by Mitsubishi Electric Corporation [30]. They have demonstrated 40% savings in power consumption using railcar traction inverter using all-SiC power modules installed in an urban train in Japan, tested during a period of four months. Gallium nitride (GaN) has some interesting properties according to Table 2.2, however,

compared to 4H-SiC, GaN is less attractive for high-voltage bipolar power devices due to a direct bandgap and thus short minority carrier lifetimes [27]. Nevertheless, for low-voltage applications GaN is a promising candidate but suffers from a less established process technology compared to SiC.

3 Silicon carbide growth

There are several techniques to growth the silicon carbide crystal. This chapter will describe both bulk crystal growth, used for the growth of the crystal boule that is later sliced into substrates and epitaxial growth, which is the growth of a thin high-quality layer continuing the crystal structure of the substrate. Finally, the growth method used in this thesis, chemical vapor deposition (CVD) will be described in detail.

3.1 Bulk crystal growth

The first commercial method used for SiC growth was the “Acheson process”, where the SiC crystal was synthesized in an electrical resistance furnace from a mixture of silica (SiO_2), coke (carbon), sawdust and salt (NaCl) [31], as illustrated in Figure 3.1 (a). In the center a core of graphite and coke is mounted, through which a large current is passed creating a heater element. The reactant mixture is placed around the core and the furnace is heated to a temperature of about 2700 °C for certain time and is then gradually decreased. The role of the sawdust is to create porosity in the mixture, making it possible for carbon monoxide and other gases to disappear. Whereas the role of NaCl is to act as a purifier and to react with impurities, which are transported away in the form chloride vapors. There

are different temperatures in different regions of the furnace. Outermost the temperature is lowest, and thus the reactants remain unreacted. In between the outermost region and the core, amorphous SiC is formed. In the core region, the temperature is highest, and SiC is formed. However, SiC decomposes to graphite and silicon when the temperature increases. The graphite remains at the core and carbon from neighboring cooler regions reacts with silicon vapors and forms crystalline SiC. Platelets with size up to 2-3 cm can be found in cavities formed from the escape of carbon monoxide. However, the size of the formed crystallites decreases with increasing distance from the core. The method is not very reproducible in size and quality of the crystals, but the formed crystals can for example be used as seeds in physical vapor growth [21, 32].

In 1955, Jan Anthony Lely developed a sublimation process, “Lely method”, for producing SiC crystals [33]. The crystals produced with the Lely method had higher quality and larger size compared to crystals grown with Acheson process and had thus potential for the semiconductor industry. For synthesis with the Lely method, a cylindrical graphite crucible filled with SiC lumps that is closed with a SiC or graphite lid is placed inside a furnace, see Figure 3.1 (b). The furnace is

Figure 3.1: Three types bulk growth methods (a) Acheson process [21], (b) Lely method [21] and (c) the modified Lely method.

heated to about 2500 °C in an argon atmosphere and the SiC powder close to the crucible walls sublimates due to the higher temperature close to the walls. At the inner surface of the cylinder the temperature is slightly lower and thus, SiC crystals start to nucleate at the inner surface. SiC platelets are formed at the porous inner walls and thicker layers are formed on the lids. The process continues until all of the SiC lumps are graphitized. This process gives crystals of high quality and purity, but the growth rate is low and not suitable for industrial scale. However, the SiC platelets could be used either as seed crystals for bulk growth or as substrates for epitaxial growth [21, 32].

In 1978, Tairov and Tsvetkov presented a seeded sublimation growth technique or “modified Lely method” [34]. Compared to the original Lely method, this process has minimized the spontaneous nucleation and has thus a controlled growth on the seed. Further, the modified Lely method led to polytype control to some extent. The seeded sublimation growth is based on the material transport by a thermal gradient, from the source to the seed, where the seed has a slightly lower temperature than the source. Growth is performed within a quasi-closed graphite crucible, which is inductively heated to 1800 - 2600 °C. A single crystal SiC crystal is attached to the top of the crucible and the SiC source (powder) is placed at the bottom of the crucible, see Figure 3.1 (c). The SiC sublimates into Si and C containing species at higher temperatures and are transported along the temperature gradient from the source to the seed crystal, where the SiC growth takes place. The seeded sublimation technique enabled growth of larger crystals with a higher growth rate [32]. By this technique the SiC boules were grown and the first SiC wafers could be sliced and polished. This technique (also known as physical vapor transport) is still used with some modifications for the growth of SiC crystal substrates that are commercially available today.

In addition to seeded sublimation growth, bulk SiC crystal can be grown from gases with a technique called high temperature chemical vapor deposition

(HTCVD) first published in 1996 by Kordina et al. [35]. The HTCVD reactor has a vertical geometry with a gas inlet at the bottom and an outlet at the top. The graphite crucible is built up of a bottom plate, cylinder and a lid, all made of graphite. The graphite crucible is enclosed by graphite foam (insulation) and is placed inside an air-cooled quartz tube (Figure 3.2). The carrier gas is either hydrogen, argon or a mixture of both. Silane is used as the silicon source and propane as carbon source. The HTCVD technique also use carbon from the graphite walls as a carbon source. The technique is essentially a CVD process, but as the name indicates it is performed at higher temperatures of about 1800 – 2300 °C and at higher growth rates, up to 0.5 mm/h [35]. The main advantage with HTCVD is the possibility to grow high-purity materials, thanks to the availability of high-purity gas sources and reactor parts. However, seeded sublimation is by far the most mature technique and most widely used for substrate production today.

Figure 3.2: Illustration of HTCVD, reprinted from [35], with the permission from AIP Publishing.

3.2 Epitaxial growth

The properties of the SiC substrates cut from the crystal boule in above mentioned bulk growth techniques are not of sufficient quality to be directly used as a part of an electronic device, why growth of one or more epitaxial layers is necessary onto the substrate. The electronic properties of the epilayers are tailored for the specific application in terms of conductivity, dopant concentration and epilayer thickness.

The word epitaxy comes from the two Greek words, *epi* meaning above and *taxis* meaning in ordered manner. Accordingly, epitaxial growth refers to the deposition of a crystalline layer (epitaxial layer) which continues the crystal structure of the substrate. Either the substrate and epilayer are the same material and the process is called *homoepitaxy* (e.g. 4H-SiC on 4H-SiC) or the substrate and epilayer are different materials and the process is called *heteroepitaxy* (e.g. 3C-SiC on 4H-SiC). The performance of the electronic devices is highly dependent on the epilayer crystalline quality, doping concentration and thickness, why the development of epitaxial growth is of major importance for electronic devices. Fabrication of devices most often requires multilayer structures with alternating doping type and/or doping concentration, which can be achieved by an epitaxial growth process.

The first homoepitaxial growth of SiC were performed at very high growth temperatures, since the substrates were still of poor quality. In the late 1980s, there was an important breakthrough in SiC epitaxy, when Matsunami and coworkers presented a step-controlled homoepitaxial growth of SiC using vapor phase epitaxy [36]. This made it possible to grow SiC at significantly lower temperatures (about 300 – 400 °C lower) of about 1350 – 1500 °C. The idea of SiC step-controlled epitaxy is that the polytype can be controlled by the step density of the substrates, that is, the surface steps act as a template to replicate the substrate polytype to the epilayer [37]. To achieve a stepped surface, the SiC crystal is

sliced with a slight off-angle rather than exactly perpendicular to the c-axis, giving the substrate surface a high density of atomic steps. The cutting is normally done towards the [11-20] direction, since the (11-20) plane has the highest density of atoms. Performing SiC epitaxial growth on off-cut substrates has made it possible to grow thick, high-quality epilayers on large area substrates.

Cutting the crystal perpendicular (or with a slight off-angle) to the c-axis will result in a substrate with two different faces, one Si-face (0001) and one C-face (000 $\bar{1}$). Epitaxial growth is mostly done using the Si-face since it will help reduce the residual nitrogen background doping concentration which is related to the site-competition theory [38]. The site-competition theory describes doping control by adjusting the C/Si ratio, which is possible since in n-type doping N replaces the C atom and in p-type doping Al replaces the Si atom. For example, increasing the C/Si ratio during epitaxial growth the n-type concentration will decrease since C outcompetes N regarding the C sites in the crystal. Further reasons to use the Si-face for epitaxial growth is that a wider doping range could be used, especially highly p-type concentrations results in two- and three-dimensional nucleation if grown on the C-face [1]. However, using low off-cut angles one advantage of using C-face for epitaxial growth is due to the low surface free energy that suppress step bunching [39].

3.3 Chemical vapor deposition

Chemical vapor deposition (CVD) is the most established and best suited technology to grow epilayers with device quality and is the technique of choice for this thesis. CVD is defined as the formation of a thin solid film on a substrate by chemical reactions of vapor-phase precursors [40]. By this definition, CVD can be distinguished from physical vapor deposition (PVD) techniques, which involves adsorption of atomic or molecular species onto the substrate. CVD techniques are suitable for semiconductor epitaxial growth, since the atoms

needed for the crystal growth are received as gases, which can be delivered with very high purity from the manufacturers giving rise to very high purity semiconductor crystals.

For CVD growth different reactor geometries can be used, such as horizontal or vertical configurations and cold wall or hot wall configurations. In cold wall reactor types, only the part of the susceptor where the substrate is placed is heated, while in hot wall reactor types the whole susceptor is heated. The development of the hot wall concept for epitaxial growth of SiC was first presented at Linköping University by Kordina et al. in 1995 [41]. The advantage of using the hot wall configuration compared to the cold wall configuration is a more effective and uniform heating of the susceptor and consequently, a more effective cracking of the precursors. In this thesis, a horizontal hot-wall CVD configuration is used and will be described in more detail.

The horizontal hot-wall CVD reactor (cross-section view in Figure 3.3) is made up of a graphite susceptor with a surface coating of either tantalum carbide (TaC) or SiC. The susceptor is covered with a porous graphite insulation and put inside an air-cooled quartz tube. An RF generator is connected to water cooled copper tubes, formed as a coil around the quartz tube, heating the susceptor inductively by the RF field. The reason to have a coil surrounding the quartz tube is to get a homogenous temperature in the growth cell. Due to the porosity, the graphite insulation does not couple with the RF field and will thus not get heated. After loading a substrate into the susceptor the whole assembly is evacuated with a turbomolecular pump to a pressure of 10^{-7} - 10^{-6} mbar. A low pressure prior to growth is needed, since any residual gas in the growth chamber can cause not desired side reactions or a doped SiC crystal. A major part of the CVD reactor is the gas mixing system, where a carrier gas, most often hydrogen gas (H_2), is mixed with precursor gases. The most common silicon and carbon precursors for SiC growth are silane (SiH_4) and propane (C_3H_8) or ethylene (C_2H_4). As dopants, most

Figure 3.3: Cross-section view of the growth chamber of the horizontal hot-wall CVD reactor including RF coil, quartz tube, liner, inlet, susceptor with rotating satellite, graphite insulation and the carrier gas and precursors used for SiC growth.

often nitrogen gas (N₂) is used as n-type dopant and trimethylaluminum (Al(CH₃)₃ or TMA) as p-type dopant. The gas mixture is then led through the quartz tube via a quartz liner, to the susceptor where the SiC deposition takes place. There is also an additional gas line for gas foil rotation (GFR) with a small flow of argon (Ar) making the satellite rotate. By rotating the satellite, it is possible to achieve very uniform epitaxial layers on the substrate, both in terms of thickness and doping. During the growth process there is a continuous flow of precursors in a carrier gas over the substrate and a process pump controlled by a throttle valve is used to keep gases flowing through the reactor and to maintain a desired process pressure (about 100 - 200 mbar). After passing the process pump the gases are led through a scrubber in order to remove any toxic molecules from the gas mixture.

The most important process during the CVD growth occurs in the gas layer just above the substrate surface, called the “boundary layer”. In the boundary layer, the gas moves more slowly compared to the rest of the gas flow through the susceptor, as illustrated in Figure 3.4. CVD reactors are constructed to have a laminar gas flow above the substrate surface, which means gas flows in parallel layers above the substrate surface with no mixing (in contrast to turbulent flow, which is defined by chaotic flow patterns). In a laminar flow regime, the gas

Figure 3.4: Gas velocity profile just above the substrate surface in the boundary layer, where μ_0 is the gas velocity far above the substrate surface and δ is the boundary layer thickness.

velocity above a flat surface (substrate) is zero and increases up to μ_0 far above the substrate surface. The boundary layer is defined as the region where the gas velocity is lower than μ_0 . The thickness of the boundary layer $\delta(x)$ at any position, x , on the substrate in the gas flow direction is proportional to:

$$\delta(x) \propto \frac{x}{\sqrt{Re}} \quad (1)$$

where Reynolds number (Re) is defined as:

$$Re = \frac{\mu_0 x}{v} \quad (2)$$

where v ($cm^2 s^{-1}$) is the kinematic viscosity of the gas. Combining (1) and (2):

$$\delta(x) \propto \sqrt{\frac{xv}{\mu_0}} \quad (3)$$

gives that the boundary layer thickness is inversely proportional to the square root of the gas velocity. The boundary layer thickness can thus be adjusted by changing

the viscosity and gas velocity of the carrier gas. This is important to control since the reactants in the gas phase must diffuse through the boundary layer in order to reach the substrate surface. To achieve uniformity during growth one can manipulate the substrate in order to have a more uniform boundary layer. One way is to rotate the substrate during deposition, which evens out the boundary thickness difference over the substrate surface. Another way is to have an inclined substrate holder. The inclined substrate gives the effect that the boundary layer thickness does not increase along the substrate in the x direction.

The growth rate in CVD can be generalized into three different growth rate limited regimes dependent on the temperature, as illustrated in Figure 3.5. At low temperatures the growth rate is limited by reaction kinetics, that is the growth rate becomes limited by the slowest reaction in the gas phase or at the surface. In this region the growth rate is independent on the CVD growth conditions and it is thus difficult to control the growth. Then the growth rate increases with increasing temperature and when the temperature is high enough the growth rate becomes limited by the mass transfer through the boundary layer. In this region the growth rate is relatively independent on the growth temperature and the growth rate is

Figure 3.5: CVD growth rate limited regimes dependence on growth temperature, including kinetic, mass transport and thermodynamic regimes.

instead controlled by the partial pressures of the precursors and it is thus possible to grow reproducible epilayers. Increasing the temperature further, the growth rate decreases with increasing temperature. This region is referred to as the thermodynamically limited regime and the decreased growth rate is related to several factors such as parasitic side reactions in the gas phase, increased deposition on the reactor walls upstream of the substrate and increased desorption of atoms from the growing film [40].

An illustration of the reactions taking place on the substrate surface and in the gas phase just above the substrate is shown in Figure 3.6. First of all, there is evaporation and transport of precursors in the main gas flow into the growth zone. When the precursors reach the growth zone in the susceptor, gas phase reactions of precursors occur and reactive intermediates are produced as well as gaseous by-products. Thereafter, the reactants are transported to the substrate surface, by means of mass transport. Once at the substrate surfaces, reactants adsorb to the surface and diffuse to growth sites where nucleation and surface chemical reactions occurs. Either the reactants nucleate and grow by island formation on a smooth surface or they attach to a step on the surface, leading to film formation. At the same time, desorption and mass transport away from the surface occurs, including desorbed precursors and fragments of decomposed precursors [40].

Figure 3.6: Precursor transport and reactions during the CVD process.

3.3.1 Epitaxial growth on off-cut substrates

Since the introduction of the step-controlled epitaxy of 6H-SiC in the late 1980s made by Matsunami et al. [36], the development of high-quality epitaxial layers has been progressing fast. Homoepitaxial growth of 4H-SiC was first attempted on 5° off-cut substrates [42, 43], which means that the crystal boule is sliced into substrates which are tilted 5° towards the $[11\bar{2}0]$ direction. A schematic illustration of epitaxial growth on off-cut substrates are shown in Figure 3.7. Off-axis substrates have thus a slight tilt giving rise to an atomic step structure on the substrate surface as compared to on-axis substrates that are cut exactly perpendicular to the c-axis. During epitaxial growth on off-cut substrates, adsorbed species migrate on the substrate surface and attach to the crystal when reaching a step, where the potential is lower. On off-cut substrates the step density is high, and the terrace width is small, making the adsorbed species able to reach the steps. Using on-axis substrates, the step density is low and crystal growth occurs instead on terraces by two-dimensional nucleation as a result of high supersaturation on the surface. The incorporation of adsorbed species into the crystal on a step, is determined by bonds from the step. Thus, homoepitaxial growth on off-cut substrates can be seen as lateral growth from the steps and are referred to as “step-flow growth”. By this step-flow growth the epitaxial layer is

Figure 3.7: Schematic illustration 4H-SiC homoepitaxial growth on off-cut substrates, where the stacking sequence is inherited from the substrate to the epilayer and thus, replicating the polytype from substrate to epilayer.

inheriting the stacking sequence of Si-C bilayers from the substrate and thus, the surface steps are acting as a template to replicate the polytype from the substrate to the epilayer. Since the introduction of 4H-SiC homoepitaxial growth of off-axis substrates, growth has mainly been developed on first 8° off-cut substrates and later on 4° off-cut substrates [44-46].

However, the disadvantage with epitaxial growth using off-cut substrates is that basal plane dislocations (BPDs) propagates to the substrate surface and continues into the epilayer. When high currents go through the device, the BPDs can act as a source of Shockley stacking faults formation which lead to increased resistance and ultimately destroys the device, a phenomenon called bipolar degradation [13]. This motivates today's research which is focused towards lower off-cut angles and on-axis epitaxial growth [39, 47-48]. A lower off-cut angle implies that the amount of BPDs intersecting the substrate surface is decreased, giving a substrate with a lower BPD density. Further, the conversion of BPDs to TEDs during epitaxial growth is expected to increase using substrates with lower off-cut angles [47].

In the scope of this thesis, CVD processes for epitaxial growth of 4H-SiC on 1° and 2° off-cut substrates have been developed (Paper 4-6). Specular epilayer surfaces are achieved during the epitaxial growth on 1° and 2° off-cut substrates with low densities of surface morphological defects, as earlier demonstrated on substrates with off-cut angles of 4° and 8° . This can be put in comparison to homoepitaxial growth on on-axis substrates giving rise to epilayers with high surface roughness with the need for chemical-mechanical polishing (CMP) before processing to devices and also with difficulties in replicating the substrate polytype. Decreasing the off-cut angle from 4° to 2° and 1° is narrowing the CVD growth parameter window considerably and the in-situ etching prior to growth becomes more critical. The in-situ etching is a process of etching the substrate surface during temperature ramp up and at the growth temperature prior to

Figure 3.8: 10 μm x 10 μm AFM images of epilayers grown on (a) 4° and (b) 2° off-cut substrates with a z-scale of 5 nm.

epitaxial growth start, with the purpose of revealing a stepped surface. For epitaxial growth on both 2° and 4° off-cut substrates, a short in-situ etching in a pure hydrogen ambient prior to growth is needed. Figure 3.8 shows AFM images of epilayers grown on 2° and 4° off-cut substrates, both substrate surfaces prepared with an in-situ etching in pure hydrogen ambient. Decreasing the off-cut angle to 1°, a small additive of SiH_4 during in-situ etching is needed in order to avoid 3C-inclusions, as shown in Figure 3.9. There might be several reasons for the need of SiH_4 prior to growth. Adding SiH_4 is altering the net etching of the substrate, but the added SiH_4 also increases the number of Si-species above the substrate surface altering the surface free energy which is discussed in Paper 6.

Figure 3.9: Nomarski microscopy images of epilayers grown on 1° off-cut substrates, with either (a) SiH_4 and hydrogen or (b) pure hydrogen in-situ etching.

Further, somewhat higher growth temperatures are needed for epitaxial growth on 1° off-cut substrates. Lower off-cut substrates have lower density of steps and consequently wider step terraces. Higher temperatures are needed to increase the diffusion length of the growth species in order for the growth species to reach steps on the substrate surface.

Metal-oxide semiconductor (MOS) capacitors were fabricated on epilayers grown on 1°, 2° and 4° off-cut substrates and the MOS capacitors showed very similar C-V characteristics and density of interface traps for all off-cut angles as presented in Paper 6. The density of interface traps is important to characterize since the interface determines essential properties of MOS field-effect transistors (MOSFETs) and the current gain of bipolar junction transistors (BJTs) and since the MOS capacitor is a part of the insulated-gate bipolar transistor (IGBT).

3.3.2 High epitaxial growth rates using standard chemistry

To achieve high-voltage bipolar devices, very thick epilayers with high-quality is needed. For such devices to be attractive to the market, the production cost needs to be reduced. One part in reducing the cost is to increase the epitaxial growth rate making the growth process shorter. High growth rates have been achieved by adding hydrochloric acid (HCl) to the standard chemistry process or by using other chlorinated precursors [49-51]. However, introducing chlorine to the growth process give drawbacks in terms of corrosion of reactor parts and results in new lifetime limiting defects [12]. In paper 3 we present epitaxial growth rates of 30 $\mu\text{m/h}$ on 4° off-cut substrates using standard $\text{SiH}_4/\text{C}_3\text{H}_8$ chemistry, without adding chlorine to the process. Epilayers with RMS values below 0.2 nm without step-bunching and thickness up to 100 μm are demonstrated. The key parameter to achieve high-quality epilayers with such high growth rates is a fine adjustment of in-situ etching conditions and the starting growth conditions, as illustrated in Figure 3.10. The in-situ etching conditions were adjusted to a minimal etching,

Figure 3.10: (a) 10 μm x 10 μm AFM image of an epilayer grown with $\text{C/Si} = 0.95$ and (b) the Si-droplets formed as shown by optical microscopy for the growth conditions in (a). (c) and (d) 10 μm x 10 μm AFM images of epilayers grown with C/Si ratios 1.2-1.0 and 1.1-0.95 respectively. Z-scale in AFM images are 5 nm. Figure reprinted from [52], with the permission from Trans Tech Publications.

which means that etching occurs only during the temperature ramp to the growth temperature and no additional etching is needed at the growth temperature. Further the C/Si ratio during the beginning of the growth is ramped from $\text{C/Si} = 1.1$ to $\text{C/Si} = 0.95$, as shown in Figure 3.10 (d). The initial higher value of the C/Si ratio is to ensure that no Si droplets are formed in the substrate/epilayer interface, as can be compared to a fixed C/Si ratio of 0.95 giving rise to Si droplets (Figure 3.10 (a) and (b)). The final lower value of the C/Si ratio is to promote a step-flow growth with no step-bunching. This can be compared to having a slightly higher C/Si ratio as shown in Figure 3.10 (c) giving rise to step-bunching.

3.3.3 Epitaxial growth conditions effect on carrier lifetime

To achieve 4H-SiC high-voltage bipolar devices, it is important to control the minority carrier lifetime since long carrier lifetimes are needed to reduce the on-resistance through conductivity modulation [3]. The carrier lifetime can be controlled to large extent by choosing suitable CVD growth conditions, such as growth temperature, C/Si ratio, growth rate and doping concentration. There are also ways of improving the carrier lifetime of the grown epilayers by post-growth processing, including thermal oxidation and carbon implantation followed by thermal annealing [9, 10]. However, in the scope of this thesis, lifetime improvements concerns finding optimal CVD growth conditions. The main lifetime limiting defect in 4H-SiC is the $Z_{1/2}$ center, which is identified as isolated carbon vacancies [11]. Therefore, growth conditions minimizing the $Z_{1/2}$ center concentration are aimed for.

In Paper 1 the effect of CVD growth conditions on carrier lifetime was studied. With decreasing growth temperature, the carrier lifetime increased continuously and were accompanied with decreasing $Z_{1/2}$ concentration. The obtained formation energy of the $Z_{1/2}$ center corresponded well with the formation energy of the carbon vacancy. An increasing C/Si ratio during growth resulted in decreased $Z_{1/2}$ concentrations, which is expected due to the carbon vacancy nature of the $Z_{1/2}$ center. However, no strict correlation to the carrier lifetime was found for all the C/Si ratios in the growth series. For C/Si ratios in the range 0.7-1.0 and 1.2-1.6 in two different reactors the carrier lifetime showed an increase with increasing C/Si ratio (and correspondingly lower $Z_{1/2}$ concentrations). Increasing the growth rate showed a slight decrease in carrier lifetime but no clear correlation to $Z_{1/2}$ concentrations. Thus, in order to grow epilayers with high carrier lifetimes and low $Z_{1/2}$ concentrations (low $1 \times 10^{12} \text{ cm}^{-3}$) low growth temperatures in combination with high C/Si ratios should be considered.

The effect of n-type and p-type doping in the epitaxial growth of 4H-SiC is considered in Paper 2, where increasing doping concentrations resulted in decreased carrier lifetimes. This was confirmed not to be related to the $Z_{1/2}$ concentrations but related to enhanced influence of direct band-to-band and Auger recombinations at high doping concentrations, both n-type and p-type.

4 Characterization techniques

A number of characterization techniques have been used in order to investigate the physical, electrical and luminescence properties of the grown epilayers. The techniques used in this thesis will be summarized in this chapter.

4.1 Optical microscopy

The first technique to evaluate the outcome of an epitaxial growth process is to observe the epilayer surface with optical microscopy, which gives feedback regarding the epilayer surface morphology and the surface morphological defects. Features observed on the epilayer surface could be carrots (on epilayers grown on 8° off-cut substrates), triangular defects (on epilayers grown on 4° off-cut substrates), Si droplets, polytype inclusions and downfalls. The microscope type used is a Nomarski differential interference contrast (NDIC) microscope. The NDIC microscope is dependent on dual-interference optics that transforms the difference in optical pathlength into different contrast of an object on the epilayer surface. The NDIC microscope uses polarized light and beam-splitting Nomarski prisms to both generate and recombine the two optical paths. If the two paths have different optical path length due to surface features, they are differentially shifted in phase. Due to the phase difference the two paths will interfere with each other

and some areas will appear brighter and some areas darker. The result of the NDIC is that the image appears with shadow effects, which gives features on the epilayer surface a three-dimensional appearance [53].

An additional feature of the NDIC microscope used in this thesis is a motorized stage that can be used to collect microscope images of the whole sample, which are put together into one image by image processing. Having the whole sample in one image simplifies calculations of surface morphological defect densities.

4.2 Thickness measurements

To determine the epilayer thickness Fourier transform infrared reflectance spectroscopy (FTIR) was used. This method is non-destructive and gives a fast feedback of the epitaxial growth process regarding growth rate. The requirement for the method is a difference in doping between the substrate and epilayer, which is related to a difference in the dielectric function for low and high free carrier concentrations. Most 4H-SiC substrates have a doping in the range 10^{18} - 10^{19} cm⁻³, while the epilayers often have a doping in the order of 10^{15} cm⁻³ and thus the substrate and epilayer behaves different optically. This give rise to interference fringes in a reflectance spectrum, as shown in Figure 4.1. The interference fringes are used to determine the epilayer thickness. The interference fringes are visible in the region of about 220 - 600 cm⁻¹ on the low frequency side of the reststrahl peak and one can observe that the difference in the dielectric functions increases with decreasing frequency. The measured spectrum is compared to a calculated spectrum with epilayer thickness as fitting parameter. The epilayer thickness parameter is varied until the spacing of the fringes in the calculated spectrum matches the spacing of the fringes in the measured spectrum. Thickness measurements are performed at room temperature in the mid-infrared range

Figure 4.1: Reflectance spectrum from FTIR thickness measurement of a 43 μm n-type ($2 \times 10^{15} \text{ cm}^{-3}$) epilayer on a n-type ($3 \times 10^{18} \text{ cm}^{-3}$) substrate. Figure reprinted from [53], with the permission from Springer-Verlag.

(220 - 4500 cm^{-1}) using CsI beamsplitter and a deuterated triglycerine sulfate (DTGS) detector with CsI window. The thickness can be measured with an uncertainty of $\pm 0.02 \mu\text{m}$ down to a thickness of about 1 μm for substrate doping of at least $1 \times 10^{18} \text{ cm}^{-3}$ [54].

4.3 Doping measurements

Capacitance-voltage (C-V) measurements were used to determine the net donor ($N_d - N_a$) and net acceptor ($N_a - N_d$) concentrations in the grown epilayers using a mercury-probe station. This is a non-destructive technique and it gives a fast feedback to the epitaxial growth process of the doping type and concentration. Liquid mercury is used to form both an Ohmic and a Schottky temporary contact and both are put on the epilayer surface. The Ohmic contact has a much larger contact area than the Schottky contact. The C-V technique is based on the fact that the width of space charge region (when reverse-biased) of a metal/semiconductor junction depends on the applied voltage. During the C-V measurement the diode is reverse-biased and the capacitance (C) is measured to

obtain the net doping concentration. For a n-type epilayer the net donor concentration density ($N_d - N_a$) is given by:

$$N_d - N_a = \frac{2}{q\epsilon\epsilon_0 A^2 d(1/C^2)/dV}$$

where $d(1/C^2)/dV$ is obtained from the slope of a $1/C^2$ -V curve, q is the elementary unit charge, ϵ is the material dependent relative dielectric constant, ϵ_0 the permittivity in vacuum and A is the diode area. The depth at which the doping is obtained is given by:

$$W = \frac{\epsilon \epsilon_0 A}{C}$$

and accordingly, W represents the width of the space charge region.

4.4 Atomic force microscopy

Atomic force microscopy (AFM) was used in order to characterize the surface morphology and step structure of the epilayer surface. AFM is a non-destructive technique that can visualize features in the nanoscale by scanning a sharp tip over the sample surface, as schematically shown in Figure 4.2. There are several modes to run the AFM, such as contact mode, tapping mode and non-contact mode. In this thesis tapping mode is used which operates by scanning an oscillating cantilever with a tip attached to it over the sample surface. The oscillation occurs at a frequency at or slightly below the resonance frequency of the cantilever and the tip touches (“taps”) the sample surface during the oscillation at its lowest position. During the scanning a feedback system ensures a constant oscillation amplitude (a constant interaction between sample and tip) by adjusting the z-position of the scanner and from that, creating a topographic image of the sample surface. From the measurements a surface roughness (RMS) value can be

Figure 4.2: Schematic illustration of the atomic force microscope.

obtained which is calculated as the standard deviation of the z-values within the measured area:

$$RMS = \sqrt{\frac{\sum(Z_i)^2}{N}}$$

where Z_i is the current Z value and N is the number of points within the measured area.

4.5 Low temperature photoluminescence

Low temperature photoluminescence (LTPL) is a technique to obtain information about the excitonic band gap of the material and the purity of the epilayer. In the LTPL spectrum one can observe lines from recombinations of excitons bound to N donors and Al acceptors as the most common doping impurities as well as presence of other impurities and optical signature of stacking faults. In case of very pure crystals, the N doping concentration can be determined by comparing the photoemission intensity of nitrogen-bound exciton to the intensity of free exciton [55, 56].

The measurements are normally done at liquid helium temperature (2 K) and the sample is excited by laser illumination (either 244 nm or 351 nm) with an energy larger than the bandgap. The excitation creates excess electrons and holes, which will recombine radiatively. The luminescence is then dispersed with a single monochromator and detected with a CCD camera cooled with liquid nitrogen. The technique is non-destructive and no pretreatment of the samples is needed. A typical LTPL spectrum is shown in Figure 4.3. The created excess electrons and holes can form electron-hole pairs bound by Coloumb interaction and are called *free excitons* (FE). The FE are mobile and can move freely in the crystal lattice. The FE can recombine radiatively and release a photon, but the FE can also be trapped at an impurity and are then referred to as a *bound exciton* (BE). The BE (for example nitrogen-bound exciton, N-BE) can either recombine in a process where the impurity atom takes the momentum giving rise to zero-phonon lines (P_0 or Q_0 in Figure 4.3, where Q_0 and P_0 represent hexagonal and cubic sites respectively) or the recombination of the BE occurs via a phonon-assisted process giving rise to phonon replicas in the spectrum. In addition to the P_0 and Q_0 lines,

Figure 4.3: Typical LTPL spectrum of the near band edge emission of a 40 μm n-type epilayer ($3 \times 10^{15} \text{ cm}^{-3}$), measured at 2 K.

there exists P_{xx} or Q_{xx} lines which represents the related phonon replicas. The subscript xx denotes the energy of the phonon involved in the recombination. Phonon assisted recombinations of FE are represented by I_{xx} , where xx denotes the energy of the phonon involved in the recombination.

Since 4H-SiC is an indirect bandgap material, the recombination process must be assisted by a phonon in order to conserve the momentum and thus, phonon replicas are observed in the spectrum. However, the exception is when an impurity (e.g. N) in BE takes the excess momentum giving rise to no-phonon lines. The energy of a recombination of a FE is:

$$E = \hbar\omega = E_g - E_{FE} - E_{phonon}$$

where E_g is the bandgap energy, E_{FE} the Coloumb binding energy to form the free exciton and E_{phonon} is the energy of the phonon conserving the momentum. The energy of the recombination of a BE is:

$$E = \hbar\omega = E_g - E_{FE} - E_{BE}$$

and when the recombination of a BE is phonon-assisted:

$$E = \hbar\omega = E_g - E_{FE} - E_{BE} - E_{phonon}$$

where E_{BE} is the energy of binding the exciton to the impurity.

4.6 Time-resolved photoluminescence

The minority carrier lifetime, a very fundamental parameter for 4H-SiC intended for high voltage bipolar devices, was measured by time-resolved photoluminescence (TRPL) at room temperature. The main recombination mechanisms (shown in Figure 4.4) determining the carrier lifetime are

Figure 4.4: Recombination mechanisms: (a) SRH, (b) radiative and (c) Auger.

Shockley-Read-Hall (SRH) recombinations (τ_{SRH}) occurring via defect centers, radiative recombinations (τ_{rad}) and Auger recombinations (τ_{Auger}) and the lifetime can be written as:

$$\frac{1}{\tau} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}}$$

The SRH recombinations occur through the recombination of electron-hole pairs via deep-level impurities or traps, with a density N_T at energy level E_T . The SRH lifetime is given by [57]:

$$\tau_{SRH} = \frac{\tau_p(n_0 + n_1 + \Delta n) + \tau_n(p_0 + p_1 + \Delta p)}{p_0 + n_0 + \Delta n}$$

where

$$\begin{aligned} n_1 &= n_i \exp\left(\frac{E_T - E_i}{kT}\right) & p_1 &= n_i \exp\left(-\frac{E_T - E_i}{kT}\right) \\ \tau_p &= \frac{1}{\sigma_p v_{th} N_T} & \tau_n &= \frac{1}{\sigma_n v_{th} N_T} \end{aligned}$$

and n_0 and p_0 are the equilibrium concentrations of electrons and holes respectively, Δn and Δp are the excess carrier densities of electrons and holes respectively, n_i is the intrinsic carrier concentration, σ_n and σ_p are the capture cross-sections for electrons and holes respectively, E_i is the Fermi level of the material and v_{th} is the thermal velocity. For low-level injection conditions (at which most measurements are done) the expression of SRH lifetime (p-type material) can be simplified since $\Delta n \ll p_0$:

$$\tau_{SRH} \approx \tau_p \left(\frac{n_1}{p_0} \right) + \tau_n \left(1 + \frac{p_1}{p_0} \right)$$

and since $n_1 \ll p_0$ and $p_1 \ll p_0$ the expression can be further simplified to:

$$\tau_{SRH} \approx \tau_n$$

The radiative recombinations are of low importance since SiC has an indirect bandgap and the radiative recombination must be assisted by a phonon in order to conserve the momentum. Since band-to-band recombination requires presence of electrons and holes at the same time, the radiative lifetime is inversely proportional to the carrier concentrations and is given by [57]:

$$\tau_{rad} = \frac{1}{B(p_0 + n_0 + \Delta n)}$$

where B is the radiative recombination coefficient. For low-level injection conditions the radiative lifetime can be rewritten as (p-type material and $\Delta n \ll p_0$):

$$\tau_{rad} \approx \frac{1}{Bp_0}$$

In Auger recombinations an electron-hole pair recombines and gives the energy to a third particle. Auger recombinations thus either involves two electrons and one hole (e-e-h) or two holes and one electron (h-h-e) in n-type and p-type materials respectively. The Auger recombinations plays a significant role at high carrier concentrations, either because of high excess carrier concentrations or high doping concentrations. The Auger lifetime is inversely proportional to the square of the carrier concentrations and is given by [57]:

$$\tau_{Auger} = \frac{1}{C_p(p_0^2 + 2p_0\Delta n + \Delta n^2) + C_n(n_0^2 + 2n_0\Delta n + \Delta n^2)}$$

$$\approx \frac{1}{C_p(p_0^2 + 2p_0\Delta n + \Delta n^2)}$$

where C_p and C_n are the Auger recombination coefficients for holes and electrons respectively. The simplification is valid for p-type material. For low-level injection conditions, the excess minority carrier concentration is low relative to the equilibrium majority carrier concentration ($\Delta n \ll p_0$) and thus the Auger lifetime can be rewritten as (p-type material):

$$\tau_{Auger} \approx \frac{1}{C_p p_0^2}$$

In TRPL, excess carriers are created by optical excitation. A frequency tripled Nd:YAG laser emitting at 355 nm is used to create the excess carriers by a short pulse of photons with an energy larger than the bandgap. The near band edge photoluminescence decay resulting from radiative electron-hole recombination is selected by interference filters and detected by a photomultiplier tube (PMT). A digital oscilloscope is recording and averaging the measured

Figure 4.5: Schematic illustration of the TRPL setup.

signal. A schematic drawing is shown in Figure 4.5. The epilayer to be measured is placed on a motorized xy-table, making it possible to do carrier lifetime mappings of whole wafers. In the scope of this thesis, measurements are done using low-level injection conditions meaning that the excess carrier concentration is below the doping concentration of the measured epilayer. Temperature dependent TRPL measurements are possible and are done in the temperature range 300 K – 500 K of n-type and p-type epilayers in Paper 2 of this thesis. The time resolution of the setup is approximately 20 ns, which is limited by the pulse length of the laser. The spatial resolution is approximately 20 μm and is limited by the diffusion length.

To extract the minority carrier lifetime from the TRPL measurements, single exponential fitting to the transient is used. The intensity of the photoluminescence signal can be written as:

$$I = I_0 e^{-\frac{t}{\tau}}$$

where I_0 is the incident intensity, t is the time and τ is the carrier lifetime. Taking the natural logarithm of both sides gives:

$$\ln I = \ln I_0 - \frac{t}{\tau}$$

and from this the carrier lifetime can be extracted from the negative inverse of the slope.

4.7 Cathodoluminescence

Cathodoluminescence (CL) is a technique to investigate electronic and optical properties of the grown material and has been used in this thesis to visualize and obtain spectra of in-grown stacking faults in the epilayers. In contrast to photoluminescence techniques, creation of excess carrier in CL is achieved by bombarding the epilayer surface with high energy electrons. CL is a non-destructive technique and there is no need for any pretreatment of conductive samples. The CL equipment is a part of a scanning electron microscope (SEM) and thus, imaging is possible by scanning the electron beam over a selected area

Figure 4.6: Panchromatic CL image of a 2SSF together with room temperature CL spectrum of the in-grown stacking fault and LTPL spectrum measured at 2 K. Figure reprinted from [58], with the permission from John Wiley and Sons.

of the epilayer surface and either panchromatic or monochromatic images can be acquired. In addition, spectroscopy can be performed by using a CCD camera. Even though the technique is based on radiative recombination and is beneficial for direct semiconductors, it also works for indirect semiconductors which emit weak cathodoluminescence. An example of an acquired panchromatic CL image of an in-grown stacking fault (double Shockley stacking fault, 2SSF) is shown in Figure 4.6, together with a room temperature CL spectrum of the 2SSF and LTPL at 2 K from the same region.

4.8 Deep level transient spectroscopy

Deep level transient spectroscopy (DLTS) is a method to characterize electrically active traps in semiconductors. The most common type is capacitance DLTS. It is based on thermal emission of carriers (electrons to the conduction band or holes to the valence band) and the corresponding change of the depletion region. By using DLTS one can find the energy level, the concentration and the capture cross section of electron or hole traps. To know the concentration of deep defects/impurities is of major importance for high-power bipolar devices, since the carrier lifetime is determined by the concentration of deep impurities even though the trap concentration (N_T) is lower than the doping concentration (N_a or N_d).

During a DLTS measurement the depletion region (or space charge region) under a Schottky contact on the epilayer will change in width dependent on the applied bias, which is normally pulsed between 0 V and -10 V. This is illustrated for n-type material in Figure 4.7, where the upper image illustrates no applied bias (0 V) and the lower image a reverse bias of -10 V. When no bias is applied, the depletion region is small and traps below the Fermi level are filled with electrons. In this scenario the capture rate (c_n) is larger than the emission rate (e_n). Applying a reverse bias of -10 V causes a widened depletion region and traps

Figure 4.7: Change in depletion region with applied bias for n-type material during DLTS.

that are above the Fermi level will start to emit electrons to the conduction band. In this scenario the emission rate (e_n) is larger than the capture rate (c_n). The emission rate is temperature dependent and will result in temperature dependent capacitance transients.

The result from the DLTS measurements is a plot showing the change in capacitance versus temperature, as shown in Figure 4.8. The change in capacitance is normally obtained using a double boxcar technique that determines the emission rate window [59]. The change in capacitance is $C(t_2) - C(t_1)$. The

Figure 4.8: Typical DLTS plot of a 45 μm n-type epilayer with peaks corresponding to $Z_{1/2}$ and $\text{EH}_{6/7}$.

presence of a trap will appear either as a positive or negative peak in the plot indicating if it is a majority or minority carrier trap. The height of the peak is proportional to the concentration of the trap and the position of the peak is determined by the thermal emission properties of the trap.

4.9 X-ray topography

X-ray topography is a useful technique that can be used to image defects and strain fields in the semiconductor crystal. X-ray topography has some important advantages compared to transmission electron microscopy, mainly that it is a non-destructive technique with no need for any special sample preparation and that larger areas can be imaged.

In the scope of this thesis the structure of in-grown stacking faults has been visualized using synchrotron white beam x-ray topography (SWBXT) in back reflection mode at the Synchrotron Radiation Facility ANKA in Karlsruhe in Germany. There are several advantages using a synchrotron source. The beam has a high degree of collimation which increases the resolution of the topographic image and a high beam intensity. The principle is that an incident beam, in our

case white beam meaning that beam consists a continuous spectrum of x-ray wavelengths, hits the sample surface and Bragg diffraction occurs. An important advantage of using white beam is that there will always be one wavelength in the incident beam that will fulfill Bragg diffraction and it is therefore not necessary with very precise sample adjustment as when using monochromatic beams. The result is a pattern of several diffraction spots which is recorded on a photographic film. There are two types of contrast in a topographic image, orientation and extinction contrast [60]. Orientation contrast arises if a part of the crystal is misoriented so that the Bragg condition is not fulfilled as in the rest of the crystal. Such a part could be a defect in the crystal and would appear brighter compared to the surroundings. Extinction contrast arises as a result of local changes of scattering power. An example of such a region is stress fields in the vicinity of dislocations, which scatters more than the rest of the crystal and thus appear darker compared to the rest of the crystal. An edge dislocation will be visible (give contrast) during x-ray topography measurements if [60]:

$$g \cdot (b \times l) \neq 0$$

where g is the diffraction vector, b is the Burger vector and l is the dislocation line. A screw dislocation will be visible if [60]:

$$g \cdot b \neq 0$$

Typical features found in 4H-SiC epilayers like micropipes, basal plane dislocations (BPDs), threading screw dislocations (TSDs), threading edge dislocations (TEDs), stacking faults and polytype inclusions can be visualized using SWBXT. An example is shown in Figure 4.9.

Figure 4.9: SWBXT image of an epilayer grown on a 2° off-cut substrate showing two types of IGSFs (2SSF and 3SSF) and a triangular defect. The white dots are TSDs. Figure reprinted from [58], with the permission from John Wiley and Sons.

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PART 2: Papers

SUMMARY OF INCLUDED PAPERS

In **Paper 1** the influence of CVD epitaxial growth conditions on the minority carrier lifetime were investigated and correlated to lifetime limiting $Z_{1/2}$ defect concentrations. Growth was conducted using standard chemistry (silane/propane) using horizontal hot-wall CVD and comparisons were also made using two different generations of reactors with the main differences including rotating substrate satellite and TaC coated susceptor in the newer generation. It was found that low growth temperatures and low C/Si ratios are beneficial for obtaining longer carrier lifetimes. Growth rate only showed a small effect on the carrier lifetime. Corresponding $Z_{1/2}$ concentrations are low for low growth temperatures and low C/Si ratios. The older generation of reactor showed almost one order of magnitude shorter carrier lifetimes and correspondingly one order of magnitude higher $Z_{1/2}$ concentrations, indicating $Z_{1/2}$ as the main lifetime limiting defect.

In **Paper 2**, the effect of n-type and p-type doping concentrations in the range 2×10^{14} - 4×10^{18} cm⁻³ on the minority carrier lifetime was studied and correlated to different recombination mechanisms. Increasing the doping concentration, both n-type and p-type, the carrier lifetime drops drastically. From DLTS measurements it is obvious that the $Z_{1/2}$ center is not responsible for the lifetime

drop. It is rather an effect of enhanced contribution from direct band-to-band and Auger recombinations at higher doping concentrations. At doping concentrations reaching $4 \times 10^{18} \text{ cm}^{-3}$, Auger recombinations are thought to be the main recombination mechanism.

Paper 3 describes the optimization of in-situ etching conditions and CVD epitaxial growth conditions in order to achieve high quality epitaxial layers grown by high growth rates ($30 \text{ } \mu\text{m/h}$) using standard silane/propane chemistry on 4° off-cut substrates. Smooth epilayers with $\text{RMS} < 0.2 \text{ nm}$ without step-bunching and thickness of $100 \text{ } \mu\text{m}$ are presented. The main idea is to use a very short etching prior to growth and a ramping of the C/Si ratio during the beginning of the growth. This growth process can be compared to growth processes where hydrochloric acid is added or by using chlorinated precursors, leading to corrosion of reactor parts and introduction of new epitaxial defects.

In **Paper 4** epitaxial CVD growth conditions are optimized for growth on 2° off-cut substrates using standard silane/propane chemistry. In-situ etching conditions in pure hydrogen and in hydrogen with a small amount of silane added are compared. Other optimizations concern mostly the C/Si ratio during growth. It was found that an in-situ etching in pure hydrogen followed by epitaxial growth using a C/Si ratio of 0.9 resulted in smooth epilayer surfaces without step-bunching together with the lowest density of surface morphological defects.

In **Paper 5** epitaxial layers grown on 2° off-cut substrates were further investigated. In-grown stacking faults in an epilayer grown with non-optimized growth conditions were characterized in detail using combined PL and microscopy mappings of the epilayer, SWBXT, PL at 2 K and room temperature as well as cathodoluminescence at room temperature. Several stacking faults were

found and identified as 2SSF, 3SSF and bar-shaped SFs, as previously observed in epilayers grown on both 4° and 8° off-cut substrates. However, due to the lower off-cut angle the geometrical size of the stacking fault on the epilayer surface is larger.

In **Paper 6** the epitaxial growth process is further optimized for the growth on 1° off-cut substrates and is compared to growth on 2° and 4° off-cut substrates. Growth on 2° and 4° off-cut substrates are more similar in terms of optimal epitaxial growth conditions, where an in-situ etching in pure hydrogen is sufficient and growth temperatures are similar. Epitaxial growth on 1° off-cut substrates requires slightly higher growth temperatures and a small amount of silane has to be added to the hydrogen ambient during in-situ etching. Further, MOS capacitors were fabricated on epilayers grown on the different off-cut angles. There was no significant difference in C-V characteristics or no indication that the interface trap density depends on the off-cut angle.

MY CONTRIBUTION TO THE PAPERS

For all the included papers, I have planned and performed all the epitaxial growth experiments. I have done the main part of the characterization of the grown epilayers, with exception of the DLTS/MCTS characterization in Paper 2 and partly in Paper 1, SWBXT in Paper 5 and fabrication and characterization of MOS capacitors in Paper 6. I have written the first drafts of all the manuscripts and finalized the papers with input from my co-authors.

Papers

The papers associated with this thesis have been removed for copyright reasons. For more details about these see:

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-152500>