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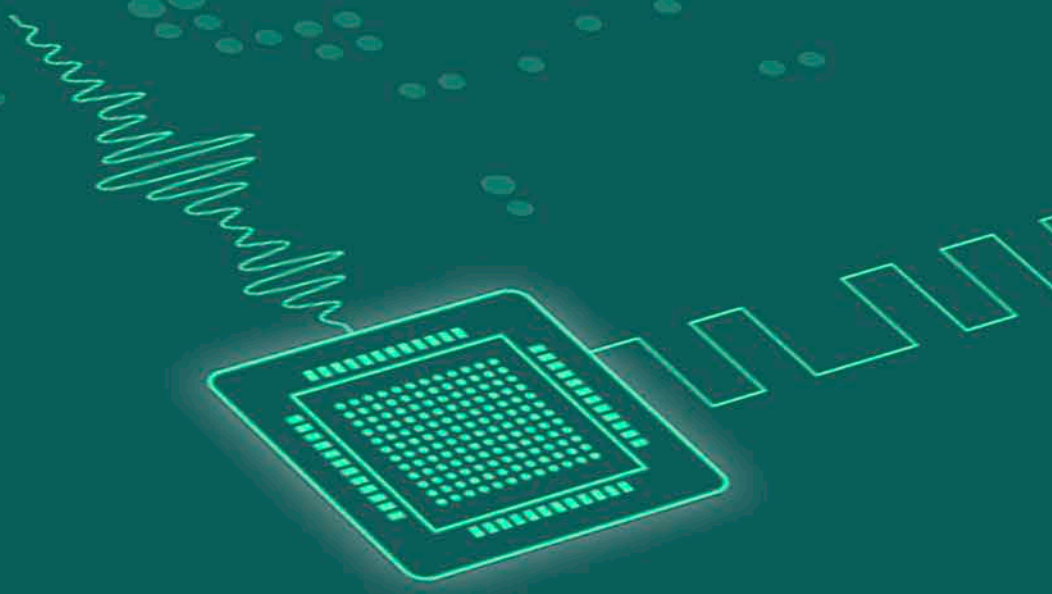
All-Digital PWM Transmitters

Muhammad Touqir Pasha



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Linköping, 2019.

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To the loving memory of my grand parents,

Abstract

Electronic devices with wireless connectivity are fast becoming a part of daily life. According to some estimates, in the next five years, 10 billion new devices with internet connectivity would be produced. To lower the costs and extend the battery life of electronic circuits, there is an increased interest in using low-cost, low-power CMOS circuits. By taking advantage of the higher integration capabilities of modern CMOS, the analog, digital, and radio circuits can be integrated on a single die, typically called a radio-frequency system-on-chip (RF-SoC).

In an RF-SoC, most of the power is usually consumed by the radio circuits, especially the power amplifier (PA). Hence, to take advantage of the improved switching capability of transistors in modern CMOS, the use of switch-mode PAs (SMPAs) is becoming more popular. SMPAs exhibit a much higher efficiency as compared to their linear counterparts and can be easily integrated with the digital baseband circuits.

To satisfy the demand for higher data throughput, modern wireless standards like LTE and IEEE 802.11 generate envelope-varying signals using advanced modulation schemes like M-QAM and OFDM. Among several other techniques, pulse-width modulation (PWM) allows for the amplification of the envelope-varying signals using SMPAs.

The first part of this thesis explores techniques to improve the spectral performance of PWM-based transmitters. The proposed transmitters are fully digital, and the entire signal chain up to the PA can be implemented using the digital design flow, which is especially beneficial in sub-micron CMOS processes with low voltage headroom. A new transmitter is proposed that compensates for the aliasing distortion in polar PWM transmitters by using outphasing. The transmitter exhibits an improvement of up to 9 dB in dynamic range for a 1.4 MHz LTE uplink signal. The idea is extended to compensate for both image and aliasing distortions in all-digital implementations of polar PWM transmitters. By using a field programmable gate array (FPGA) and Class-D SMPAs, the proposed transmitter shows an improvement of up to 6.9 dBc in the adjacent channel leakage ratio (ACLR) and 10% in the error vector magnitude (EVM) for a 20 MHz LTE uplink signal. The proposed transmitter is fully programmable and can be easily adapted for multi-band and multi-standard transmission.

To enhance the phase linearity of all-digital PWM transmitters, a new trans-

mitter architecture based on outphasing is presented. The proposed transmitter uses outphasing to improve the phase resolution and exhibits an improvement of 2.8 dBc and 3.3% in ACLR and EVM, respectively.

The difference between the polar and quadrature implementations of RF-PWM based transmitters is explored. By using mathematical derivations and simulations, it is shown that the polar implementation outperforms the quadrature implementation due to the lower quantization noise. An RF-PWM based transmitter that eliminates both image and aliasing distortions is presented. The proposed transmitter has an all-digital implementation, uses a single SMPA, and eliminates the need for a power combiner resulting in a more compact design. For a 1.4 MHz LTE uplink signal, the proposed transmitter exhibits an improvement of up to 11.3 dBc in ACLR.

The second part of this work focuses on the design of all-digital area-efficient architectures of time-to-digital converters (TDCs). A TDC is essentially a stopwatch with a pico-second resolution and can be used to accurately quantify the pulse width and position of PWM signals.

A Vernier delay line-based TDC is presented that replaces the conventionally used sampling D flip-flops by a single transistor. This resulting implementation does not suffer from blackout time associated with D flip-flops allowing for a more compact design. The proposed TDC achieves a time resolution of 5.7 ps, and consumes 1.85 mW of power while operating at 50 MS/s.

A modified switching scheme to reduce the power consumed by the thermometer-to-binary encoder used in the TDCs is presented. By taking advantage of the operating nature of the TDCs, the proposed switching scheme reduces the power consumption by up to 40% for a 256-bit encoder.

Populärvetenskaplig sammanfattning

Trådlös elektronik har snabbt blivit en del av vår vardag. Enligt uppskattningar kommer tio miljarder nya enheter anslutas till internet de närmaste fem åren. För billig och strömsnål elektronik vill man gärna använda CMOS-kretsar. Genom att utnyttja den höga integrationsförmågan med CMOS kan digitala, analoga och radiokretsar läggas samman på ett enda chip, kallat ett RF-SoC (Radio Frequency System-on-Chip).

Den största energiförbrukningen i ett RF-SoC är oftast i radiokretsarna, speciellt i sändarförstärkaren. Genom att utnyttja de allt snabbare CMOS-transistorerna kan switchade förstärkare användas. Dessa har mycket mindre energiförluster jämfört med sina linjära motsvarigheter och kan enkelt integreras med digitala elektronik i en CMOS-krets.

För att tillgodose efterfrågan på högre dataöverföring används i modern trådlös datakommunikation signaler med varierande amplitud och fas samt hög bandbredd. Om vi skall kunna använda switchade förstärkare med sådana signaler, måste sändarnas arkitektur anpassas. Pulsbreddsmodulering (PWM) är en teknik som möjliggör detta.

Den första delen av denna avhandling undersöker tekniker för att förbättra spektralprestandan hos PWM-baserade sändare. De föreslagna sändarna kan konstrueras med helt digitala kretsblock fram till sändarförstärkaren.

En ny sändararkitektur som kompenserar för spegelförvrängning i polära PWM-sändare genom att använda utfasning (en klassisk teknik i äldre förstärkare) har studerats. Arkitekturen har förbättras för att kompensera för olika typer av förvrängningar av signalen som ofta uppkommer i konventionella digitala polära PWM-sändare. Genom att använda en Field-Programmable Gate Array (FPGA, 'på-plats-programmerbar grindmatris') och switchade klass D-förstärkare, har viktiga sändarparametrar i den föreslagna sändaren förbättrats. Sändaren är helt programmerbar och kan enkelt anpassas för multiband- och multistandard-sändning.

För att förbättra faslinjäriteten hos digitala PWM-sändare presenteras en ny sändararkitektur baserad på utfasning i avhandlingen.

Skillnaden mellan polära och kvadraturimplementeringar av RF-PWM-baserade sändare har undersökts. Genom matematiska härledningar och simuleringar visar det sig att den polära implementeringen är bättre än kvadraturimplementering på grund av det lägre kvantiseringsbruset. En RF-PWM-baserad sändare som eliminerar både spegelförvrängningar och vikningsdistorsion pre-

senteras. Den föreslagna sändaren är helt digital, använder en enda switchad förstärkare och kan konstrueras utan den annars nödvändiga effektkombineraren, vilket resulterar i en mer kompakt konstruktion.

Den andra delen av detta avhandlingsarbetet är inriktat på utformningen av helt digitala yteffektiva arkitekturer av tid-till-digital-omvandlare (time-to-digital converter, TDC). En TDC är i huvudsak ett stoppur med picosekundsupplösning och kan användas för att exakt kvantifiera pulsbredd och position för PWM-signaler.

En Vernier-fördröjningsbaserad TDC presenteras som ersätter de samplade D-vippor som brukar användas i sådana kretsar med en enda transistor. Den föreslagna kretsen lider inte av dödtider som kretsar baserade på D-vippor gör, vilket möjliggör en mer kompakt design.

Ett modifierat växlingsschema för att reducera effektförbrukningen i termometer-till-binär-kodare som används i TDC:er föreslås. Genom att utnyttja TDC:ns karakteristiska beteende kan strömförbrukningen minskas med upp till 40% för en 256-bitars kodare.

Acknowledgments

Praise be to Allah, the Cherisher and the Sustainer of all the worlds for giving me the strength to complete this work.

So begins probably the most read page of this thesis. During my Ph.D, I have met many marvelous people who have taught me valuable life lessons and helped me develop as a person, thank you for being a part of this journey. Additionally, I would like to express my sincere and deepest gratitude towards the following people:

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Muhammad Touqir Pasha
January, 2019
Linköping, Sweden.

List of Papers

The research presented in this thesis was conducted at the Division of Integrated Circuits and Systems, Department of Electrical Engineering, Linköping University, Sweden.

Appended Publications

The following papers are included in this thesis

- **Paper A** M. F. U. Haque, M. T. Pasha, and T. Johansson, "Aliasing-Compensated Polar PWM Transmitter," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 8, pp. 912-916, Aug. 2017.
- **Paper B** M. T. Pasha, M. F. U. Haque, J. Ahmad, and T. Johansson, "A Modified All-Digital Polar PWM Transmitter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 758-768, Feb. 2018.
- **Paper C** M. T. Pasha, M. F. U. Haque, J. Ahmad, and T. Johansson, "An All-digital PWM Transmitter with Enhanced Phase Resolution," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 11, pp. 1634-1638, Nov. 2018.
- **Paper D** M. F. U. Haque, M. T. Pasha, T. Malik, and T. Johansson, "A Comparison of Polar and Quadrature RF-PWM," presented at NORCAS 2018, Oct. 30-31, Tallin, Estonia.
- **Paper E** M. F. U. Haque, M. T. Pasha, and T. Johansson, "A Power-Efficient Aliasing-Free PWM Transmitter," accepted for publication in IET Circuits, Systems and Devices, Oct. 2018.

- **Paper F** M. T. Pasha, N. U. Andersson, and M. Vesterbacka, "Power-Efficient Time-to-Digital Converter for All-Digital Frequency Locked Loops," presented at ECCTD 2015, Aug. 24-26, Trondheim, Norway.
- **Paper G** M. T. Pasha and M. Vesterbacka, "A Modified Switching Scheme for Multiplexer-Based Thermometer-to-Binary Encoders," presented at NORCHIP 2014, Oct. 27-28, Tampere, Finland.

Other Publications

The following publications are not included in this thesis. The work of these publications partially overlaps with the appended papers or is out of the scope of this thesis.

- M. T. Pasha and M. Vesterbacka, "Frequency control schemes for single-ended ring oscillators," presented at ECCTD 2011, Aug. 29-31, Linköping, Sweden.
- M. T. Pasha and M. Vesterbacka, "Performance Analysis of Digitally Controlled Delay-Lines," presented at SSoCC 2014, May 12-13, Linköping, Sweden.
- M. T. Pasha, Y. A. Shah, and J. Wikner, "A wide range all-digital delay locked loop for video applications," presented at ECCTD 2015, Aug. 24-26, Trondheim, Norway.

Thesis

Some of the work presented in this thesis has previously been a part of the following Licentiate thesis

- M. T. Pasha, "Circuit Design for All-Digital Frequency Synthesizers," Tekn. Lic. Thesis, Department of Electrical Engineering, Linköping University, Linköping, Sweden, 2015.

Contents

Background

Chapter 1

Introduction

Communicating with others has always been part of human nature. Over the years, light signals, beating drums and even pigeons have been used to send and receive information. With the advent of electricity, new communication techniques involving the use of electronic signals and electromagnetic waves were introduced. The story of modern communications started with the telegraph first introduced in 1837 followed by the introduction of the first telephone system patented in 1876 by Graham Bell [1]. Both telegraph and telephone required a wired medium for the transmission of the involved electrical signals. During the same era, Marconi showed the possibility of communicating using electromagnetic waves leading to the first successful transatlantic communication in 1902.

Modern wireless communications devices are required to support multiple communication standards like GSM (2G), WCDMA (3G), LTE (4G) and the different standards of WLAN. Depending on the geographical location, the same communication standard might operate in different frequency bands. For example, ETSI has specified 70 bands operating bands for LTE and mobile devices are required to operate in most of the allocated frequency bands. In addition, a mobile phone is also expected to be affordable, portable, feature-rich and must have a long battery life.

Furthermore, the requirements set by each communication standard must also be fulfilled. For example, for a GSM audio call with a data rate of several hundred kbps (typically 270 kbps), a transmit power as high as 4 W [2] might be required in certain remote areas for the 1800 MHz band. However, in case of a WLAN transmission, where the hotspots are located in close proximity,

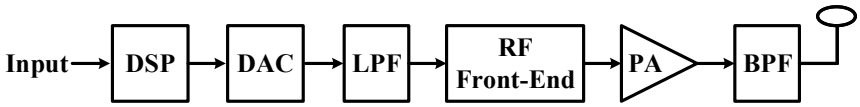


Figure 1.1: A typical RF transmitter signal chain.

the required transmit signal power is much less, around 200 mW on average; although the required data rate is much higher (typically 450 Mbps for IEEE 802.11n) [3]. Due to the very different transmission requirements, to maintain an optimum performance, a separate transmitter would be required for each communication standard. However, this is not practical as the resulting devices would be expensive, have a higher power consumption and would be very bulky in size.

1.1 Towards Software-Defined Radios

A conventional RF transmitter is shown in Figure 1.1 where the input is processed by a digital signal processing block (DSP) to generate a baseband signal. A digital-to-analog converter (DAC) converts the digital baseband signal into analog form, which is lowpass filtered (LPF) to remove the images due to sampling. The resulting signal is upconverted to the carrier frequency, which is then amplified by the power amplifier (PA) and transmitted through the antenna.

The performance of the various transmitter blocks is usually specified in terms of linearity, gain, bandwidth, power dissipation, etc. Depending on the communication standard, the design parameters of each block have to be selected differently in order to fulfill the requirements set forth by that particular standard. The simplest way to design a multi-standard RF transmission system would be to combine the transmitters for different standards on to a single chip as shown in Figure 1.2. For all communications standards, the input is processed by a single DSP block and then passed to the respective transmitter. Such a system exhibits very good performance characteristics as each of the transmitters is optimized for a particular communication standard [4]. The downside of such a system would be the high engineering cost to implement the different transmitters on a single chip in addition to a large chip size. Moreover, to add a new standard would require a new chip design and verification cycle, which could be expensive

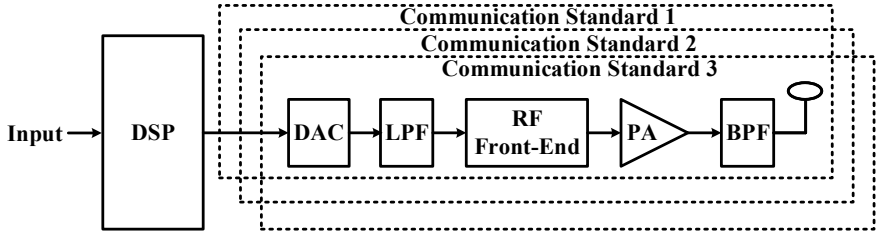


Figure 1.2: A typical SDR implementation.

and not feasible in some cases.

The multi-standard transmitter shown in Figure 1.2 can be optimized by redesigning components like the DAC and LPF such that they can be reused for the different standards in addition to the DSP block as shown in Figure 1.3. To satisfy the stringent requirements set forth by the different communication standards, each standard has a dedicated PA and a bandpass filter.

A more interesting approach would be to design a single system containing transceivers for the different communication standards. Although the initial cost of designing would be high, the resulting system would have a smaller chip size, while being flexible and power efficient. Furthermore, if all the blocks in the system are programmable, support for new communication standards could easily be added. Such a system is often referred to as a software defined radio (SDR) and is very popular due to the its potential usage for internet of things (IoT) applications and vehicle-to-everything (V2X) communications [5].

In a truly flexible SDR, the PA has to be flexible as shown in Figure 1.4. Designing a PA that is both power efficient and linear to satisfy the requirements of all communication standards is very challenging. However, relatively high

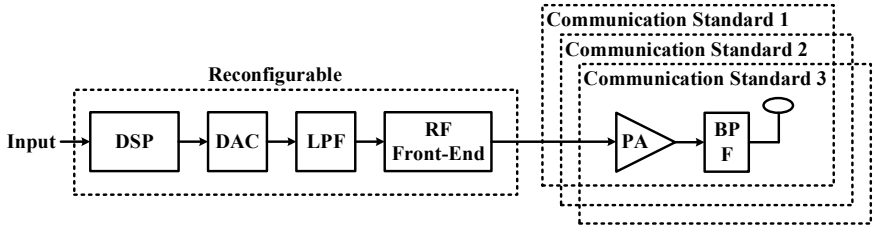


Figure 1.3: An improved SDR implementation.

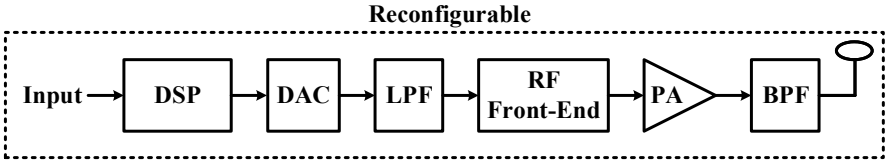


Figure 1.4: A fully programmable SDR.

bandwidth PAs like [6–8] might be re-used between two or more standards at the cost of power efficiency or linearity.

Hence, it comes down to trade-offs between the various performance parameters, flexibility and user requirements. For example, a GSM and a IEEE 802.11n signal have to be transmitted using the signal chain shown in Figure 1.4. For GSM, a high output power PA with relaxed linearity is required [9], whereas for WLAN, a low output power PA with high linearity is required. The obvious choice is to use a linear PA that would satisfy the requirements for both standards. However, in case of a WLAN signal at peak power, the PA is operating well below the 1 dB point resulting in a lower efficiency. Moreover, for GSM, using a linear PA instead of a power efficient SMPA results in lower efficiency. In this case flexibility is achieved at the cost of lower efficiency for both standards.

To conclude, it is safe to say that there is no optimal solution that works for all scenarios and some compromises have to be made to achieve an acceptable design with good performance and flexibility. Similarly, the operating characteristics of other transmitter blocks like DAC and LPF have to be tweaked for the different communication standards.

1.2 History of Fully Integrated Transceivers

In 1958, Jack Kilby while working at Texas Instruments developed the first integrated circuit (IC) comprising simple circuits like oscillators, flip-flops etc. connected using bond wires [10, 11]. However, the method proposed by Kilby was not suited for large-scale fabrication. Around the same time, independently of Kilby's invention, Robert Noyce while working at Fairchild semiconductors developed a more elaborate IC using a planar process. The IC consisted of a transistor, resistor and a capacitor connected together using an aluminum metal strip placed on an oxide layer [12].

In 1960, the first metal oxide semiconductor FET (MOSFET) was fabricated

at the Radio corporation of America (RCA) by Dawon Kahng [13]. In MOSFETs, the conduction region is either p-channel (PMOS) or n-channel (NMOS), the latter being faster due to the higher mobility of electrons. The complementary metal oxide semiconductor (CMOS) process that made possible the integration of both PMOS and NMOS devices on a single silicon wafer was developed at Fairchild Semiconductor in 1963. The circuit consisted of an inverter and a ring oscillator [14] and from the tests it was noted that the standby power for CMOS circuits was reduced by up to six orders of magnitude as compared to bipolar transistors [15].

In 1965, Gordon Moore, also working at Fairchild Semiconductors wrote the famous paper "Cramming more components onto Integrated Circuits" [16], predicting that the density of devices on an IC would double every 12 months, later known as Moore's law. Over the years, the ICs have become more complex packing more functionality with every new process node. In 2017, Intel corporation announced a new 10 nm process that packs 100 million transistors per mm^2 [17].

In the recent years, the CMOS RF circuits have become quite popular [18]. In addition to active components, RF circuits also require passive components like capacitors and inductors used in oscillators, amplifiers, and filters. During the 1960s, it was considered impossible to fabricate inductors with practical inductance values and high-quality factors [19, 20]. In the early 1970s, the first RF circuit, a low-noise amplifier (LNA) with an integrated inductor was fabricated using GaAs MESFETs at Plessey [21]. Gold-plated metallization in combination with the low-loss GaAs substrate enabled the inductor to achieve a quality factor of 60 at 10 GHz [22]. Soon after, Hewlett-Packard successfully demonstrated fully integrated broadband amplifiers. The circuits operated at frequencies above 1 GHz, and did not use any surface mounted components. Hence, the integrated ICs had a significantly smaller size and a higher reliability as compared to the circuits using discrete components.

By the 1980s, fully-integrated GaAs monolithic microwave integrated circuits (MMICs) featuring transmitters/receivers, high power PAs and other circuits using both active and passive devices had become mainstream [21–23]. For silicon-based technologies, the main hurdle in realizing a radio frequency integrated circuit (RFIC) was the integration of on-chip inductors with good performance characteristics. It was argued that realizing on-chip inductors with a reasonable quality factor was almost impossible due to the high substrate losses [20]. However, as the silicon processes adopted thicker dielectric layers and metal

layer stack-up built-up, it was possible to place the inductors in the higher metal layers, isolated from the lossy substrate using relatively thick silicon dioxide insulation (usually several micro-meters thick) [24]. Although, the losses are higher in silicon metal lines as compared to the gold-plated lines in GaAs MMICs, the isolation and interconnect density is much higher.

By the mid-1990s, the first commercial silicon-based RFICs had been introduced driven mainly by the demand for RFIC transceivers used in mobile phones. In the early 2000s, BiCMOS mixed-signal ICs integrating analog, digital and RF circuits for wireless communication had become dominant mainly due to the low cost and high integration capabilities of silicon-based technologies. To reduce the costs even further, the CMOS processes were introduced, which exhibit a reasonably good RF performance. However, for very high frequency applications, the BiCMOS and III-V devices are still preferred due to the superior performance over CMOS devices.

Implementing RF circuits in CMOS also has certain challenges. For example, the size of the inductor does not scale with technology. Moreover, the quality factors of the inductors are low as compared to other fabrication technologies. To ensure reasonable performance over the process corners, larger sized components have to be used, thus reducing benefits of scaling. Moreover, the supply voltage in sub-micron CMOS processes is limited due to the thin oxide layer of transistors. For example, Class E PAs have long-term reliability issues as the peak drain voltage can be as high as 3.6 times the supply voltage [25], [26]. Despite these challenges, the benefits of designing fully integrated RF-transmitters in sub-micron CMOS are numerous and outweigh any disadvantages.

1.3 Towards Fully Digital Transmitters

Due to the advancements in signal processing algorithms and CMOS fabrication, the transmitters designed using CMOS processes have a good RF performance and cost less to fabricate as compared to BiCMOS processes. In sub-micron CMOS processes, as the feature size reduces, the design of analog circuits becomes cumbersome as the voltage headroom is reduced due to supply voltage scaling. As the modern CMOS processes have been developed keeping digital circuits in mind, with each new process generation, the performance of digital circuits improves. Digital circuits do not require a large voltage headroom to operate and are more immune to process, voltage, and temperature (PVT) variations as compared to analog circuits. Finally, the dynamic power consumption decreases

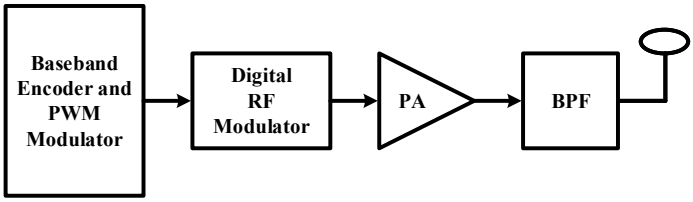


Figure 1.5: A fully digital multi-standard transmitter.

due to the scaling of the supply voltage. Thus, to take full advantage of modern CMOS processes, the use of all-digital techniques is becoming more popular.

A fully digital architecture for an SDR is shown in Figure 1.5. The architecture can be divided into the baseband part and the RF part. The output of the baseband part is a binary signal, which is upconverted to RF and amplified by the PA. The elimination of the DAC makes the architecture of Figure 1.5 more flexible as new communication standards can be added by just making changes to the software controlling the DSP block. The complete baseband part of the transmitter can be designed using standard logic gates with the provision to add new communication standards to it. Furthermore, the baseband design process can easily be automated by using the digital process flow, thus making the baseband design easily portable to newer processes. The operating bands of the transmitter shown in Figure 1.5 would be limited by the bandwidth of the PA, since it is quite cumbersome to design a PA with a very wide bandwidth and good enough linearity. As the entire signal chain up to the PA is digital, the natural choice would be to use switch-mode PAs (SMPA) over linear PAs.

The aim of this thesis is to make the baseband and RF parts of the transmitter more flexible, as shown in Figure 1.5. The entire signal path up to the PA is programmable and can be easily adapted to the different communication standards. All-digital implementations of the baseband and RF part signal path are explored so as to replace the analog components like DAC with digital circuits and using the digital process flow to improve portability and simplify the design cycle.

1.4 Switch-Mode Power Amplification

Battery life is an important parameter dictating the future trends in modern portable devices. In the current market, among other product features a longer

battery life is an important selling point for both cell phones and other portable devices. Efforts are underway to find new materials for the battery that have a higher charge storing capacity while being light weight. However, no significant breakthroughs have yet been commercialized and for the time being most users have to recharge their smart phones at least once a day.

Nevertheless, optimizations at the circuit level are also useful in extending the battery life performance of mobile devices. Although the use of digital circuits in the deep sub-micron CMOS has helped in reducing the dynamic power consumption of the baseband circuits, the main source of power dissipation in any transmitter is the PA. Thus, by making the PA more power efficient, significant gains in battery life can be achieved. PAs can broadly be categories into two categories

- Linear PAs
- Switch-mode PAs

The linear PAs (Class A, AB, B, and C) exhibit high linearity at the cost of reduced power efficiency. On the other hand, the switched Class D, E and F PAs collectively called switch-mode PAs (SMPAs) are non-linear but highly efficient (theoretically up to 100% [25], [26]) and more suitable for architectures with digital baseband processing. However, SMPAs can only be used with constant-envelope signals, as the transistors operate as switches, so at any given time the output of the SMPA is either high or low.

Typically, the RF carrier is modulated according to either the amplitude, frequency or phase of the baseband signal for transmission. Modern communication standards use a combination of these characteristics to achieve a higher spectral efficiency. In case of SMPAs, constant envelope signal (phase or frequency modulated signal) can be amplified directly, however, amplification of non-constant envelope signals (amplitude modulated signal) is not directly possible. Techniques like polar modulation, outphasing, and pulse-width modulation allow the SMPAs to be used with spectrally-efficient schemes like IEEE 802.11 [27] and LTE [28] that generate non-constant envelope signals.

1.5 Continuous-Time Digital Circuits

Pulse-width modulation (PWM) allows the possibility to use amplitude modulated signals with SMPAs. In PWM, signals with varying amplitude levels are represented by digital pulses with duty cycle proportional to the input signal

amplitude. In amplitude-varying signals the information is represented in voltage domain, whereas for PWM signals, the information is represented in the time domain. As the voltage headroom decreases and the time resolution of CMOS devices improves with process scaling due to the increasing transition frequency (f_T), the use of time domain techniques like PWM becomes advantageous.

The time domain PWM signal has to be quantized for digital processing and the quantization step has to be fine enough to accurately quantify the information contained being conveyed by the PWM signal. Although a traditional sample-and-hold circuit could be used to quantize the PWM signals, there are two problems with this approach. First, the power consumed by the sample-and-hold circuit would be very high as the circuit would be required to operate at a very high frequency (several GHz), which might be unfeasible. Second, designing registers capable of operating at GHz frequencies would be very challenging.

Time domain circuits present a low power/high resolution alternative to the traditional sample-and-hold circuits. Like ADCs, that quantize the voltage domain signal information into a digital code, time-to-digital converters (TDC), quantize the time domain signal information into a digital code. TDCs can easily achieve a time resolution in the order of pico-seconds and is only limited by the target CMOS implementation process. As the CMOS scaling continues, the time resolution is set to further improve thus making time domain circuits very suitable for use in sub-micron CMOS.

1.6 Summary of this thesis

All modern communication devices contain transceivers supporting multiple communication standards. The focus of this thesis on the design and digital implementation of reconfigurable RF transmitters. The use of digital techniques allows for the design process to be automated, i.e., automatic place and route tools can be used for the on-chip circuit implementations of the digital circuits thus saving valuable design time and cost.

The first part of this thesis focuses on techniques to enhance the efficiency, amplitude and phase linearity of PWM transmitters and their all-digital implementations (**Paper A** - **Paper E**). In the second part, different techniques for the area and power efficient design of TDCs is explored (**Paper F** - **Paper G**).

In **Paper A**, an aliasing compensated PWM transmitter (AC-PWMT) is presented. The transmitter combines PWM and outphasing to reduce the image and amplitude aliasing distortions. The proposed implementation results in an

improved spectral performance as compared to other PWM transmitters without any significant effect on the transmitter efficiency.

In **Paper B**, an all-digital implementation of AC-PWMT is presented. The entire signal path from baseband to RF is implemented using an FPGA, which makes the design suitable for multi-standard transmission.

In **Paper C**, a technique to enhance the phase resolution of PWM transmitters is presented, which is usually limited by the phase modulator implementation. The proposed technique doubles the available phase resolution of a conventional phase modulator by using asymmetric outphasing.

In **Paper D**, a study of the different implementations of all-digital RF-PWM transmitters is presented. Mathematical formulations for the polar and quadrature implementations are derived, and the spectral performance of the two implementations is compared.

In **Paper E**, an area and power efficient transmitter architecture is presented. The proposed transmitter eliminates both image and aliasing distortions, has an all-digital implementation and requires a single SMPA.

In **Paper F**, an 8-bit area efficient time-to-digital converter is presented, which exhibits a time resolution of 5.7 ps and maximum sampling rate of 50 MS/s.

In **Paper G**, a modified switching scheme for the thermometer-to-binary encoder used in TDCs is presented. The proposed technique reduces the power consumption of the encoder by up to 40%.

Chapter 2

Transmitter Architectures for SMPAs

Modern wireless systems use multiple frequency bands and advanced modulation schemes to achieve high data rate. As discussed in Chapter 1, it is desirable to employ a single transmitter for the multi-band transmission, such that the spectral and RF requirements of each band are satisfied. Communication standards like IEEE 802.11 and LTE generate envelope-varying signals, which can be amplified using linear PAs. However, the efficiency of linear PAs is low and is further reduced if the PA is operated at back-off power to satisfy the linearity requirements. SMPAs have a much higher efficiency, as the transistors are operated as switches. However, they cannot directly amplify envelope-varying signals directly without the use of linearization.

The first part of this chapter discusses the different classes of SMPAs. In the second part of this chapter, commonly used techniques that allow the use of SMPAs with envelope-varying signals are discussed.

2.1 Switch-mode Power Amplifier

In switch-mode power amplifiers (SMPAs) transistors are turned on or off depending on the input signal. SMPAs can theoretically achieve 100% efficiency and are generally categorized into three main classes depending on the output tuning network,

- Class D SMPA
- Class E SMPA

- Class F SMPA

Each of the PA classes has different performance parameters usually characterized by parameters like efficiency, linearity and normalized power output capability [25, 26, 29, 30].

Efficiency: Since a PA is the most power-hungry block in the transmitter chain, its power efficiency is very important. Usually, the PA efficiency is defined in terms of either the drain efficiency or the power added efficiency [30–33]. The drain efficiency is the ratio of the average power delivered to the load (P_{load}) to the average dc power supplied to the PA (P_{DC}).

$$\eta_{Drain} = \frac{P_{load}}{P_{DC}}. \tag{2.1}$$

Power added efficiency (PAE) also takes into account the input signal power(P_{in}) supplied to the PA. It is expressed as

$$\eta_{PAE} = \frac{P_{load} - P_{in}}{P_{DC}}. \tag{2.2}$$

Linearity: The linearity of the PA defines the accuracy with which an input signal is amplified. For linear PAs, both amplitude and phase linearity of a PA is important whereas for SMPA only phase linearity is important. Usually, the linearity of a PA is characterized by its adjacent channel leakage ratio ($ACLR$), which is a measure of the signal power leaking into the adjacent channels due to spectral regrowth [32, 33].

$$ACLR = \frac{P_{desired}}{P_{adjacent}} \tag{2.3}$$

where $P_{desried}$ is the average signal power in the desired band and $P_{adjacent}$ is the signal power in the adjacent band.

Normalized power output capability: The normalized power output capability is an indication of the relative stress a PA might be subjected during operation. It is defined as the ratio of the output power P_{load}, to the product of maximum drain voltage $V_{d,max}$ and Id, max [25, 26].

$$P_N = \frac{P_{load}}{V_{d,max} \times Id, max} \tag{2.4}$$

Error vector magnitude (EVM) is also used to characterize the linearity of a PA. In case of a transmitter, to obtain EVM first an error vector is calculated as the difference between the measured transmitted signal and a reference signal

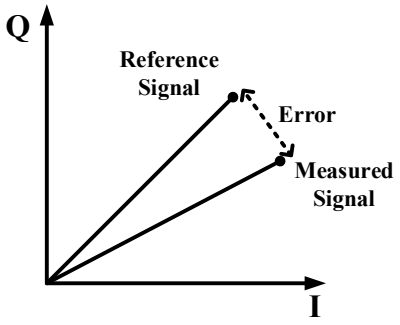


Figure 2.1: I/Q constellation for error vector calculation.

using an I/Q constellation as shown in Figure 2.1 [32, 33]. EVM is then calculated as ratio of error signal vector V_e and the reference signal V_{ref}.

$$EVM(dB) = 20\,log\left(\frac{V_e}{V_{ref}}\right) \tag{2.5}$$

2.1.1 Class D SMPA

A Class D SMPA [26, 34–37] can be implemented as an inverter driving an output load R_L. Ideally, a Class D PA would exhibit 100 % percent efficiency (ignoring the parasitics). A typical implementation of a Class D SMPA and the corresponding drain voltage and current plot is shown in Figure 2.2. It can be seen that the output voltage and current have a non-overlapping relationship leading to a 100 % efficiency.

However, in actual implementations, the efficiency is limited due to the presence of the parasitics capacitances and the finite rise/fall time of input signals causing short circuit current between the power supply and ground.The normalized power output capability of Class D SMPAs is $P_N = 1/\pi = 0.318$, highest among all PA classes [37–39].

2.1.2 Class E SMPA

The loss in efficiency due the charging and discharging of parasitic capacitances can be somewhat compensated by designing a tuned LC network at the output of the PA such that the overlap regions in current-voltage curve can be avoided [26, 40, 41]. A simplified block diagram of a Class E SMPA is shown in Figure 2.3.

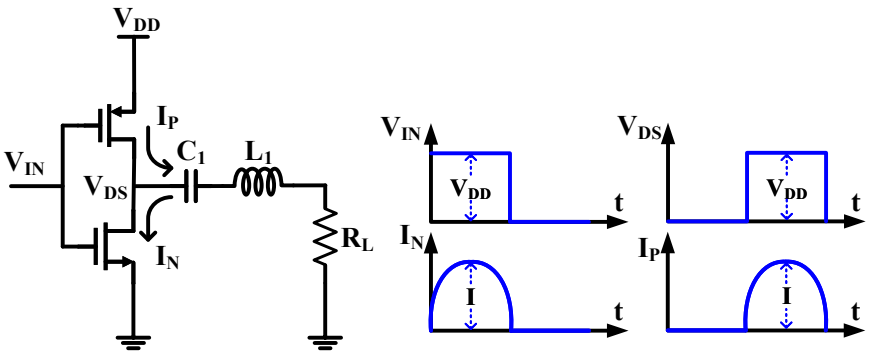


Figure 2.2: Class D SMPA and corresponding waveforms.

When the NMOS is turned ON, both V_d and I_{C1} is zero, the drain current I_d takes on a sinusoidal shape due to the resonator network L_2C_2. When the NMOS is turned off, the sinusoidal current flows through C_1 to the ground charging V_d. The values of the components C_1, C_2, L_1 and L_2 are chosen such that the following conditions are satisfied at the drain of the NMOS.

- During turn OFF, I_d and V_d do not overlap.
- When the switch turns ON, V_d should be zero and $\frac{dV_d(t)}{dt}$.

The presence of C_1 satisfies the first condition. As the NMOS turns OFF, C_1 starts charging preventing V_d from going high and dissipating through the NMOS. The second condition is satisfied by preventing the overlap of V_d and I_d in case of finite rise and fall times of the input signal or power supply variations [42–44].

A well-designed Class E SMPA satisfying the above conditions exhibits a higher efficiency as compared to a Class D PA. However, during the off state, the peak drain voltage in case of Class E PAs can go as high as $3.6\,V_{dd}$ [26, 30, 39] stressing the transistor and causing long-term reliability issues. The normalized power output capability of Class E SMPAs is $P_N = 1/(3\pi) = 0.106$, which is the lowest among all PA classes [25, 26, 39].

2.1.3 Class F SMPA

Class F SMPA [26, 30, 45] use a quarter-wave transmission line along with a tuned LC network to reduce the switching losses of the transistors. The transmission line is designed to exhibit a characteristic impedance equal to the

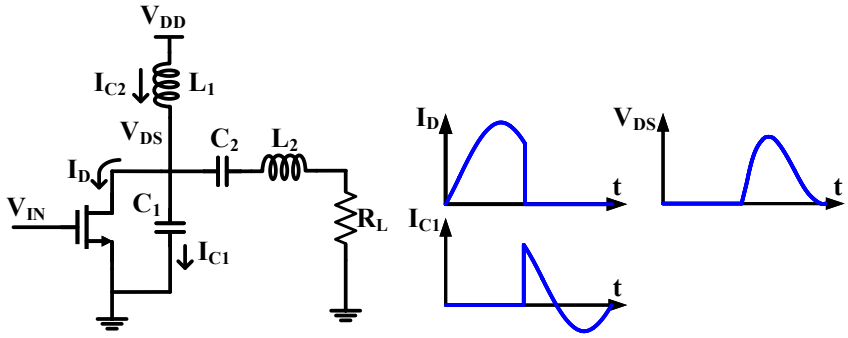


Figure 2.3: Class E SMPA and corresponding waveforms.

load R_L. For a high-quality LC network and reasonably large values of L_{Choke}, C_{Block}, the tuning network allows the fundamental frequency to pass through while the odd harmonics see an infinite impedance. As a result, V_d is a square wave while I_d is a half-sinusoidal wave as shown in Figure 2.4. Since V_d and I_d non-overlapping, the Class F SMPA can achieve a much higher efficiency. The normalized power output capability of Class F SMPAs is $P_N = 1/(2\pi) = 0.16$, which is much lower than Class D PAs [25, 26]. Furthermore, the on-chip implementations of a Class F PA required a larger chip area [25].

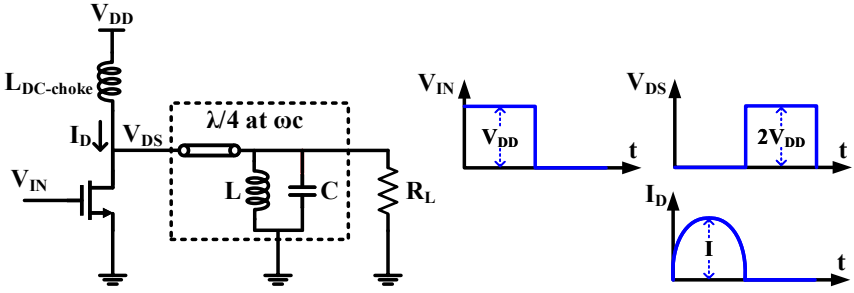


Figure 2.4: Class F SMPA and corresponding waveforms.

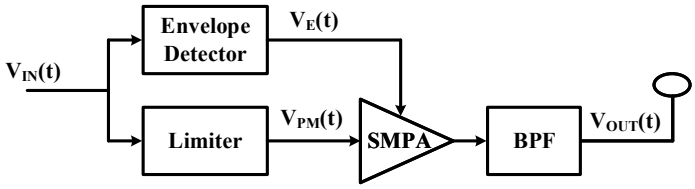


Figure 2.5: Block diagram of a polar modulation transmitter.

2.2 Transmitters Architectures

The most common techniques that allow the use of SMPAs with envelope-varying signals are polar modulation [30, 46, 47], outphasing [30, 46, 48], and pulse-width modulation [9, 49, 50].

2.2.1 Polar modulation

The idea of polar modulation is based on the Envelope Elimination and Restoration technique introduced by Kahn in 1952 [47]. Polar modulation or sometimes referred to as Kahn transmitter uses an efficient envelope amplifier along with an SMPA to allow for power-efficient transmission of envelope-varying signals.

The block diagram of a Kahn transmitter is shown in Figure 2.5. Using an envelope detector, a low-frequency envelope varying signal $V_E(t)$ is generated from the input signal $V_{IN}(t)$ (2.6), which modulates the supply voltage of the SMPA. A phase- modulated constant-envelope signal $V_{PM}(t)$(2.7) is generated using a limiter, which is power amplified by the SMPA. The final output signal $V_{out}(t)$, given in (2.8), contains both the amplitude and phase information of the input signal. However, the performance of the polar modulator of Figure 2.5 is degraded due to the non-linearity of the envelope detector and the AM/PM conversion in the limiter [30].

$$V_{IN}(t) = V_E(t)\cos\left(\omega_c t + \phi\left(t\right)\right) \tag{2.6}$$

$$V_{PM}(t) = \cos\left(\omega_c t + \phi\left(t\right)\right) \tag{2.7}$$

$$V_{out}(t) = AV_E(t)\cos\left(\omega_c t + \phi\left(t\right)\right) \tag{2.8}$$

An improved implementation of the Kahn transmitter is shown in Figure 2.6 [30, 51–53]. The implementation uses a coordinate rotation digital computer(CORDIC) [54] to split the input signal into amplitude and phase

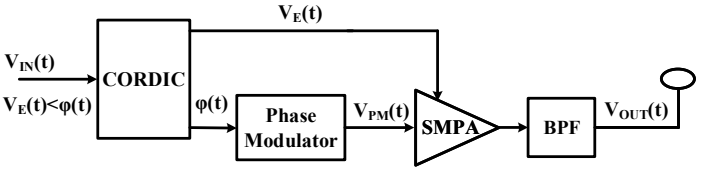


Figure 2.6: A common implementation of the polar transmitter.

components $a(t)$ and $\phi(t)$, respectively. A carrier signal is modulated using $\phi(t)$ whereas $a(t)$ modulates the supply voltage of the SMPA to generate the output signal $V_{OUT}(t)$. However, a delay mismatch between the $V_E(t)$ and $V_{PM}(t)$ degrades the performance of the polar modulator in this case.

2.2.2 Outphasing

In outphasing [30, 46, 48, 55, 56],an envelope-varying input signal, $V_{in}(t)$ given in (2.9), is decomposed into two constant-envelope signals $V_1(t)$, $V_2(t)$ (2.10), which are amplified by two separate PAs (SMPA or linear PA in saturation) and then combined to generate the power-amplified output signal. $V_1(t)$, $V_2(t)$ are phase shifted by an angle $\theta(t)$ called the outphasing angle, which is related to the amplitude of $a(t)$ of the input signal, (2.13). The output signal is an amplified version of the amplitude-varying input signal. Since the technique uses SMPAs or linear PAs in saturation, outphasing is also known as linear amplification with non-linear components (LINC) [46].

$$V_{in}(t) = a(t)\cos\left(\omega_c t + \phi\left(t\right)\right) \tag{2.9}$$

$$V_1(t) = \frac{1}{2}\cos\left(\omega_c t + \phi(t) + \theta(t)\right) \tag{2.10a}$$

$$V_2(t) = \frac{1}{2}\cos\left(\omega_c t + \phi(t) - \theta(t)\right) \tag{2.10b}$$

$$\theta = \cos^{-1}\left(a\left(t\right)\right) \tag{2.11}$$

The concept of outphasing is shown in Figure 2.7. The combiner is shown as an addition sign, indicating that it adds the two outphasing signals V_1 and V_2 to generate an amplified version of the input signal. For the outphasing transmitters, the main challenge is to ensure a good matching between the outphasing paths. A gain or phase mismatch between the outphasing paths introduces additional terms to the output signal, resulting in distortion and

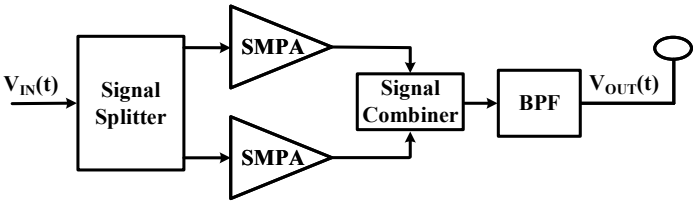


Figure 2.7: Block diagram of an outphasing transmitter.

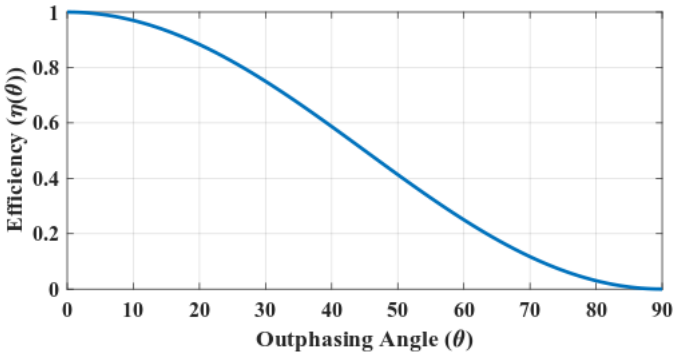


Figure 2.8: Instantaneous efficiency versus outphasing angle for a Wilkinson combiner.

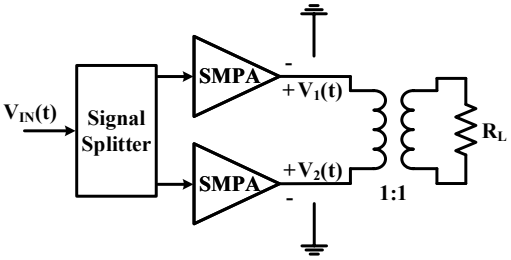
spectral regrowth. Furthermore, the performance characteristics of the combiner also affect the linearity and efficiency of the transmitter [30, 57]. The combiners are usually classified into the following two types

- Isolating combiners.
- Non-Isolating combiners.

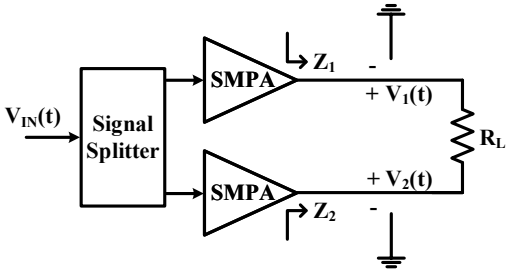
Isolating combiners perfectly isolate the outphasing paths thus preventing any load variations at the output of the PAs [30]. However, as the outphasing angle θ increases, the losses in the combiner also increase due to isolation port losses. As a result, the overall efficiency of the transmitter decreases. A popular example of an isolated combiner is the Wilkinson combiner [58] whose efficiency is related to the outphasing angle as given in (2.12) and is plotted in Figure 2.8 [59].

$$\eta_W = \cos^2(\theta(t)) \tag{2.12}$$

Several techniques have been explored to address the issue of reduced efficiency at larger outphasing angles. In [60, 61], a technique to reuse the RF power



(a)



(b)

Figure 2.9: (a) Outphasing transmitter with a transformer (b) simplified circuit.

delivered to the combiner is proposed therefore enhancing the efficiency as compared to the standard Wilkinson combiner. The efficiency of the combiner can also be enhanced by using multi-level outphasing [62–64].

In non-isolating combiners the signals from outphasing paths might corrupt one another resulting in spectral regrowth at the combiner output [30, 62, 65, 66]. A typical example of a non-isolated combiner is a transformer as shown in Figure 2.9a. Assuming the transformer has a gain of 1, and both the PAs have a gain of 1, Figure 2.9a can be redrawn for simplicity as Figure 2.9b. The impedance seen by the two PAs varies with the outphasing angle as given in (8) [30], distorting the output signal.

$$Z_1 = Phasor\left(\frac{V_1(t)}{I_{12}}\right) = \frac{R_L}{2} - j\frac{R_L}{2}\cot\left(\theta\left(t\right)\right) \tag{2.13a}$$

$$Z_2 = Phasor\left(\frac{V_2(t)}{I_{12}}\right) = \frac{R_L}{2} + j\frac{R_L}{2}\cot\left(\theta\left(t\right)\right) \tag{2.13b}$$

Chapter 3

Baseband PWM Transmitters

In pulse-width modulation (PWM) transmitters, the amplitude information of envelope-varying signals is encoded into a sequence of digital pulses with varying duty cycle. This allows the entire signal chain up to the SMPAs to be designed using digital circuits, thus benefiting from the advancements in CMOS processes.

3.1 Baseband PWM Transmitters

In baseband PWM transmitters [57, 67–72], the amplitude information of the input signal is encoded into a PWM signal of frequency ω_{IF} and mixed with a phase modulated carrier signal of frequency ω_c to generate the transmit signal. Baseband PWM transmitters are also referred to as polar PWM transmitters (PPWMTs) and its block diagram is shown in Figure 3.1. The baseband input signal $x(t)$, (3.1) is split into its amplitude component $a(t)$ and phase component $\phi(t)$.

$$x(t) = a(t)e^{j\phi(t)} \tag{3.1}$$

A PWM signal is generated by modulating the pulse-width τ of a pulse train to generate a PWM signal as given in 3.2, where T is the repetition period of the PWM signal.

$$a(t) = \frac{\tau(t)}{T}. \tag{3.2}$$

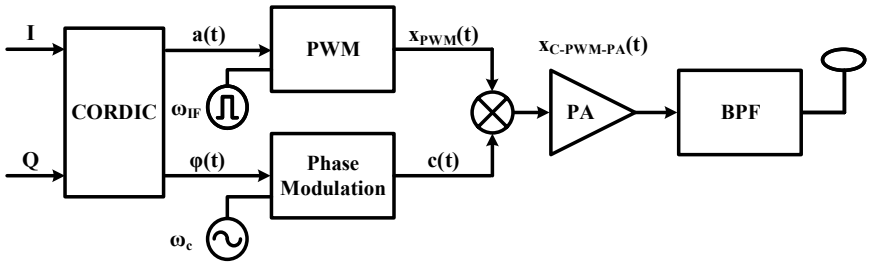


Figure 3.1: Block diagram of a polar PWM transmitter.

The generated PWM signal is given in (3.3), where k is the harmonic number, and ω_{IF} is the repetition frequency of the PWM signal.

$$x_{PWM} = \frac{\tau(t)}{T} + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(t)}{T}\right) \cos(\omega_{IF} k t) \tag{3.3}$$

The input signal $x(t)$ and the corresponding PWM signal are shown in Figure 3.2(a)-(b). The phase component, $\phi(t)$ of the input signal $x(t)$ shown in Figure 3.2(c) modulates the phase of a carrier signal with frequency ω_c, (3.4). The phase-modulated carrier is shown in Figure 3.2(d).

$$c(t) = cos(\omega_c t + \phi(t)) \tag{3.4}$$

x_{PWM} and $c(t)$ are multiplied, resulting in a carrier-modulated PWM (C-PWM), (3.5) shown in Figure 3.2(e).

$$x_{CPWM} = \left(\frac{\tau(t)}{T} + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(t)}{T}\right) \cos(\omega_{IF} k t)\right) \cos\left(\omega_c t + \phi(t)\right). \tag{3.5}$$

The $x_{CPWM}$is then amplified by the PA and filtered to generate the amplified envelope-varying output signal shown in Figure 3.2(f).

3.2 Challenges in Baseband PWM Transmitter Design

The following factors need to be considered when designing polar PWM transmitters.

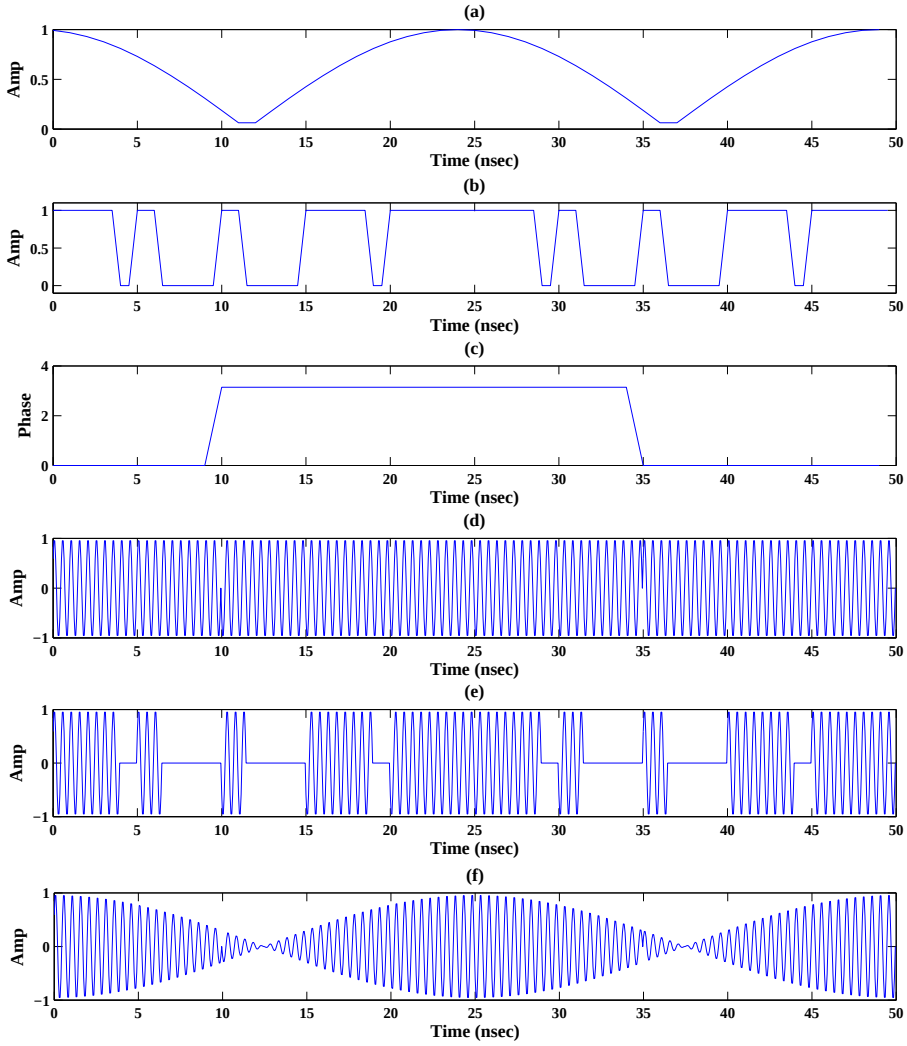


Figure 3.2: (a) Amplitude component of input signal $x(t)$, (b) PWM signal corresponding to $x(t)$, (c) Phase component of input signal $x(t)$, (d) Phase-modulated carrier signal $c(t)$, (e) Carrier modulated PWM signal $X_{CPWM}(t)$, (f) Envelope varying amplified output signal.

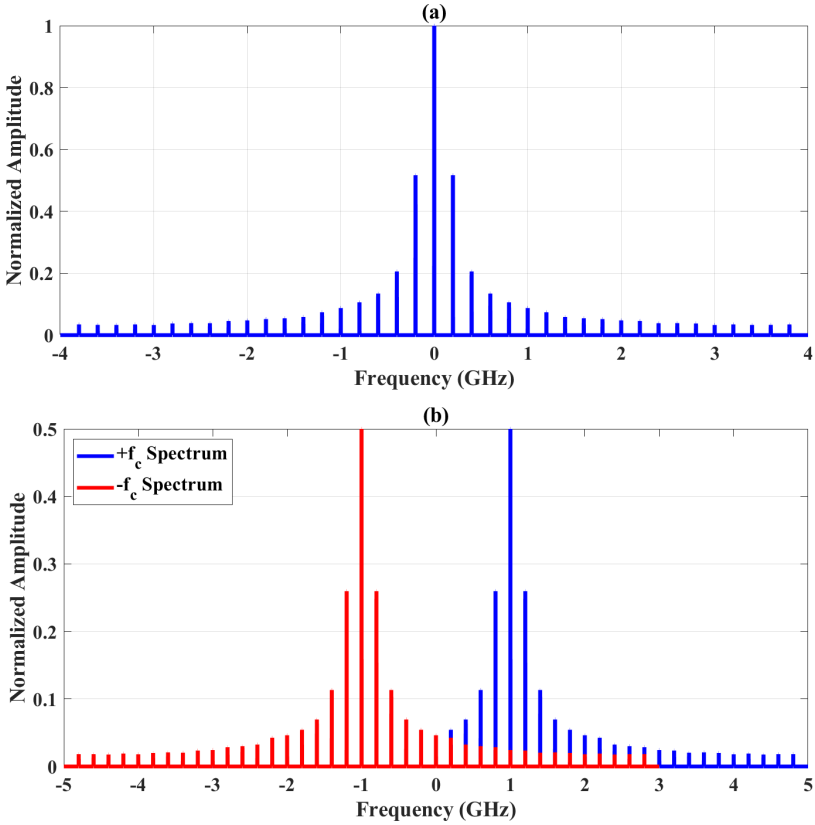


Figure 3.3: (a) Spectrum of the baseband PWM signal for $\omega_{IF} = 2\pi \times 200\ M\ rad/s = 200\ MHz$ (b) Spectrum of the upconverted PWM signal for $\omega_c = 2\pi \times 1\ G\ rad/s = 1\ GHz$.

3.2.1 Filtering Requirements

For baseband PWM signals, the distortion peaks occur at multiples of ω_{IF}, [49, 71, 73]. The spectrum of the baseband PWM signal is shown in Figure 3.3(a). The desired signal component occurs at DC and its harmonics can be observed at multiples of 200 MHz. After multiplication with the carrier, the desired component as well as the harmonics are up-converted to the carrier frequency as shown in Figure 3.3(b). The bandpass filter attenuates the harmonics while allowing the desired signal component to pass. A high order bandpass filter is required if the harmonics are in close proximity to the desired signal. Higher values of ω_{IF} can be used to move the harmonics farther away from the desired

signal, thus relaxing the filter order. However, this saving comes at the cost of a reduced dynamic range due to image distortion. In case of all-digital implementations, the dynamic range is also affected by the amplitude aliasing distortion.

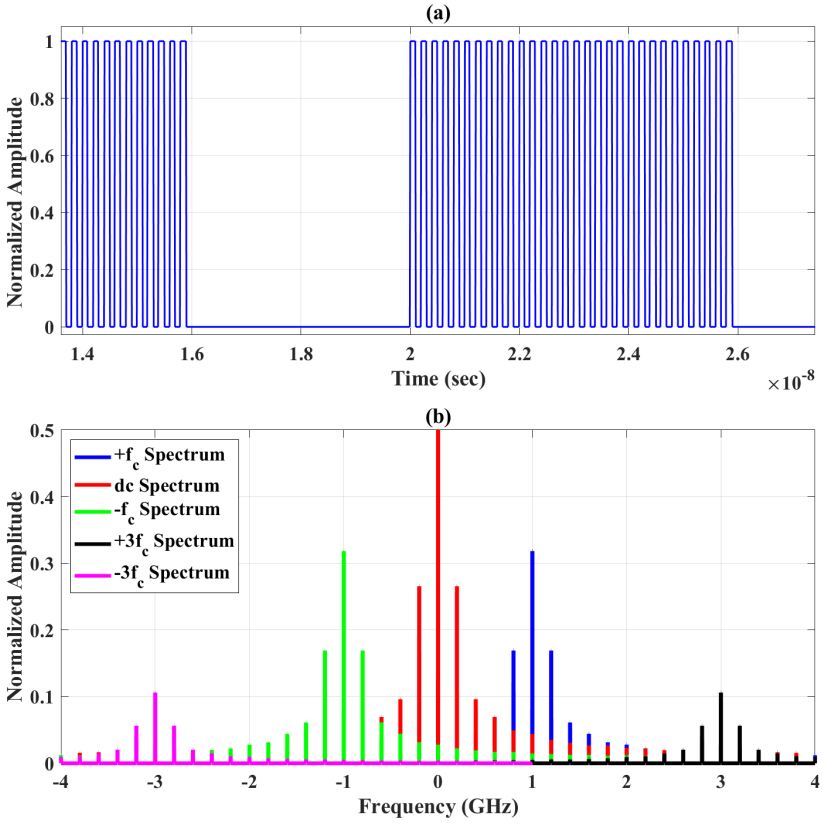


Figure 3.4: (a) Time domain representation of the SMPA output (b) Spectrum of the signal at SMPA output.

3.2.2 Image Distortion

When the baseband PWM is upconverted to $+\omega_c$, a copy is also upconverted to $-\omega_c$ as shown in Figure 3.4. As the PWM signal has infinite harmonic components, some of them would end up in the desired transmit signal band. The harmonics cannot be filtered out by the bandpass filter. This kind of distortion is referred to as image distortion and affects the SMPA output more

adversely than linear PAs [71, 74]. As the SMPA converts the carrier from sinusoidal to square wave form (see (3.5), Figure 3.2(f)), the image distortion increases as compared to (3.5). The signal at the output of the SMPA is given as (3.6) and is shown in Figure 3.4 for $\omega_{IF} = 2\pi \times 200\ Mrad/s$ and $\omega_c = 2\pi \times 1\ Grad/s$. From Figure 3.4(b), it can be seen that multiple harmonic components exist in the transmit signal band resulting in an increased image distortion.

$$x_{SMPA}(t) = \left(\frac{\tau(t)}{T} + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(t)}{T} \right) \cos(\omega_{IF} k t) \right) \left(\frac{1}{2} + \frac{2}{\pi} \cos\left(\omega_c t + \phi(t)\right) + \sum_{m=2}^{\infty} \frac{2}{q\pi} \sin\left(\frac{q\pi}{2} \right) \cos\left(q\omega_c t + q\phi(t)\right) \right). \tag{3.6}$$

3.2.3 Image Distortion Compensation

The effect of image distortion in PPWMT can be reduced by

- Exploiting the gap between the desired transmit signal and its adjacent harmonics.
- Eliminating the harmonic components causing the image distortion altogether.

3.2.3.1 Exploiting Image Gap

Exploiting image gap (EIG), [74], proposes selecting the values of ω_{IF} and ω_c such that the harmonic components that cause the image distortion do not overlap with the desired signal. As ω_c is usually fixed according to the communication standard, the only choice left is the selection of ω_{IF}. Figure 3.5a shows the spectrum of the upconverted PWM signal for arbitrary value of ω_{IF}, whereas Figure 3.5 shows the spectrum for the PWM with value of ω_{IF} chosen according to EIG.

When using linear PAs, the image distortion is completely eliminated by using EIG. However, in case of SMPAs, the effect of image distortion is reduced and not fully eliminated. Furthermore, strict bandpass filtering is required to remove the distortion components from the desired signal band.

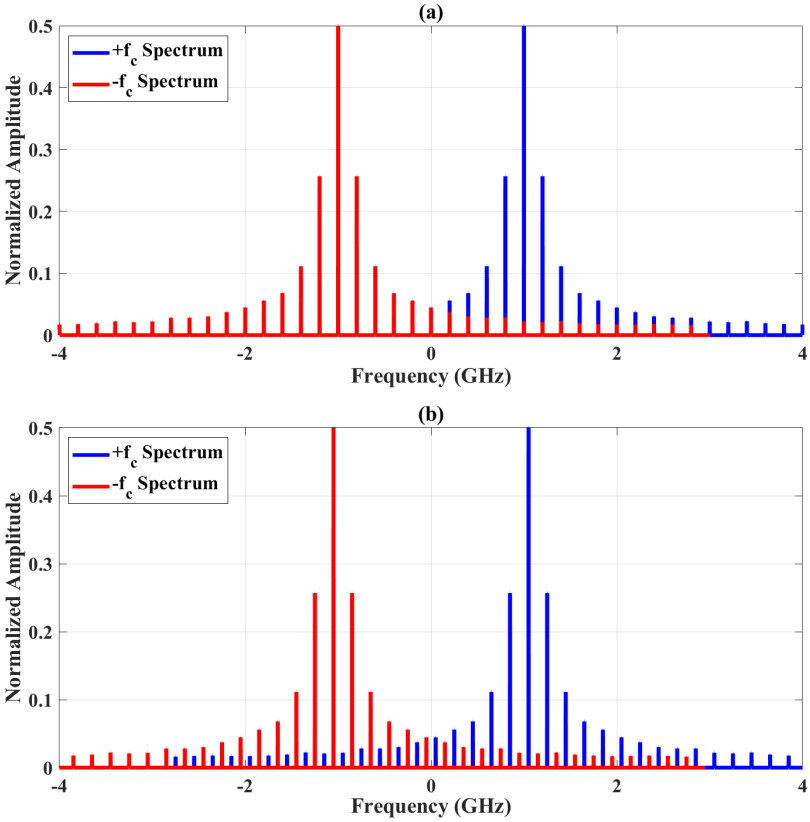


Figure 3.5: Upconverted PWM signal (a) spectra with image distortion due to the random selection of ω_{IF} (b) spectra with no image distortion due to EIG.

3.2.3.2 Elimination of Image Distortion

The image distortion in the transmit signal can also be eliminated by quantizing the amplitude component $a(t)$ of the baseband signal used for the PWM signal generation [74]. In order to quantize $a(t)$, first the image component with the highest amplitude value is determined as

$$q = round\left(\frac{k\omega_c}{\omega_{IF}}\right). \tag{3.7}$$

where $k = 1$ for SMPAs and $k = 2$ for linear PAs and differential SMPAs. Next the quantization is performed as

$$\hat{a} = \Delta_q \times round\left(\frac{a\,(t)}{\Delta_q}\right) \tag{3.8}$$

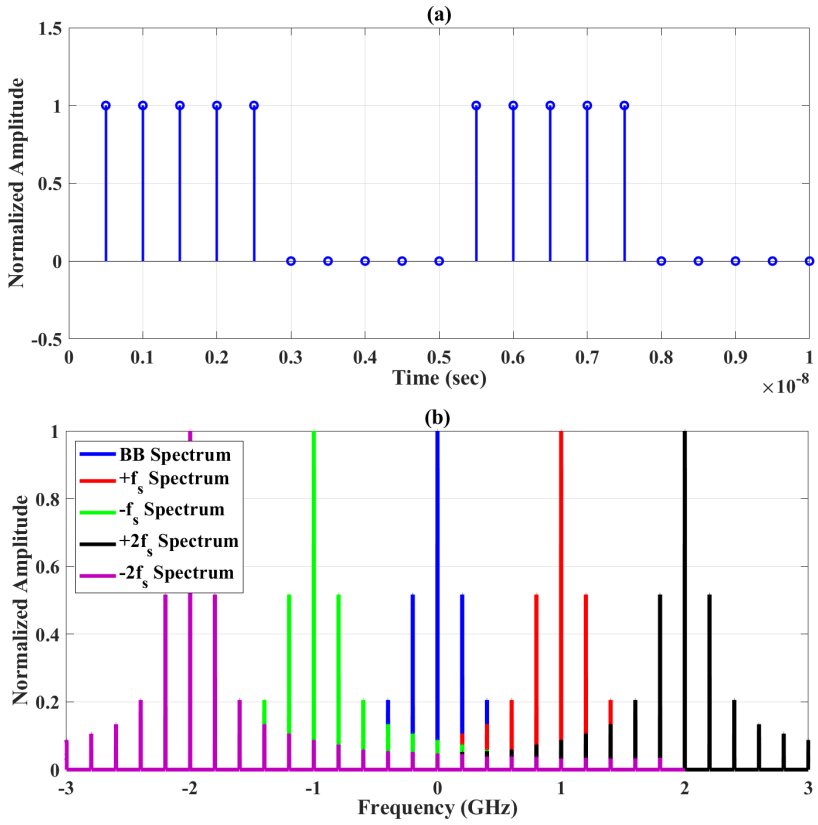


Figure 3.6: (a) Time domain waveform of the digital PWM signal (b) Spectrum of the digital PWM signal for $\omega_{IF} = 2\pi \times 200\ M\ rad/s$ and $\omega_s = 2\pi \times 1\ Grad/s$.

where $\Delta_q = 1/q$ is the quantization interval. This technique reduces the image distortion but due to the quantization, the output signal has a much higher quantization noise.

3.2.4 Amplitude Aliasing Distortion

In digital implementations of PMW, the analog PWM spectrum is repeated due to the sampling nature of digital systems. As a result, the rising or falling edge occurs once every sampling clock period. The time and frequency domain representation of the digital PWM is given in (3.9) and (3.10) where n is the

sampling index and T_s is the sampling period [75, 76]

$$x_{PWM}(nT_s) = \left(\frac{\tau(nT_s)}{T} + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(nT_s)}{T} \right) \cos(\omega_{IF} k n T_s) \right) \tag{3.9}$$

$$X_{PWM}\left(e^{j\omega}\right) = \frac{1}{T_s} \sum_{\rho=-\infty}^{\infty} X_{PWM}\left(j\left(\frac{\omega}{T_s} - \frac{2\pi\rho}{T_s} \right) \right) \tag{3.10}$$

Figure 3.6 illustrates the time-domain and frequency plots for the digital PWM signal. The spectrum is repeated at the multiples of ω_s, with some of the components falling in the desired signal band thus distorting the baseband signal amplitude. This phenomenon is referred to as amplitude-aliasing distortion [71, 76, 77] and results in a decreased dynamic range at the transmitter output.

3.2.4.1 Aliasing-Free PWM Transmitter

The image and aliasing distortion can be eliminated by using only a limited number of harmonics for the baseband PWM signal. This transmitter is referred to as the aliasing-free PWM transmitter (AF-PWMT), [77, 78] and is shown in Figure 3.7.

After splitting the input signal $x(t)$ into its amplitude $a(t)$ and phase components $\phi(t)$, a bandlimited PWM (BL-PWM) signal is generated using $a(t)$. The BL-PWM signal only contains a limited number of harmonics and is given as

$$x_{BL-PWM}\left(nT_s\right) = \frac{\tau\left(nT_s\right)}{T} + \sum_{k=1}^{K} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau\left(nT_s\right)}{T} \right) \cos\left(\omega_{IF} k n T_s\right) \tag{3.11}$$

where $\tau(nT_s) = a(nT_s)T, a(nT_s)$ is the baseband signal amplitude at the timing instance nT_s and K is the number of harmonics in the BL-PWM signal. The

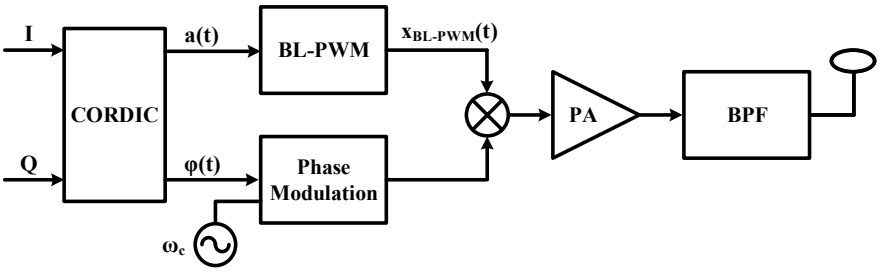


Figure 3.7: Block diagram of the aliasing-free PWM transmitter.

transmit signal will be free from image and aliasing distortions if the following conditions are satisfied for a carrier frequency ω_c.

$$\left.\begin{aligned} K\omega_{IF} &< 2\pi/T_s \\ K\omega_{IF} &< \omega_c \end{aligned}\right\}. \tag{3.12}$$

The spectrum of the BL-PWM signal is shown in Figure 3.8, which is then converted into analog form using a digital-to-analog converter and is given as

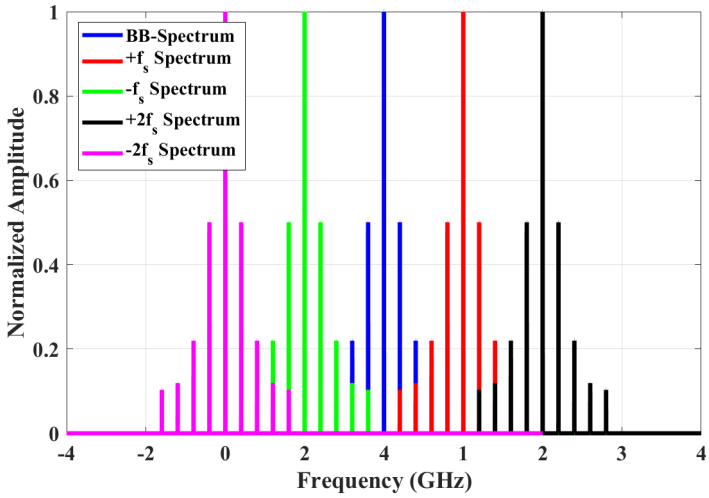


Figure 3.8: Spectrum of the BL-PWM signal.

$$x_{BL-PWM}(t) = \frac{\tau(t)}{T} + \sum_{k=1}^{K} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(t)}{T}\right) \cos(\omega_{IF} k t). \tag{3.13}$$

The phase component, $\phi(t)$, of the baseband signal modulates the carrier, which is multiplied with the BL-PWM signal to generate the carrier-based BL-PWM signal given in (3.14) and shown in Figure 3.9.

$$\begin{aligned} x_{CBL-PWM}(t) = {} & \frac{\tau(t)}{T} \cos(\omega_c t + \phi(t)) \\ & + \left(\sum_{k=1}^{K} \frac{2}{k\pi} \sin\left(\frac{k\pi\tau(t)}{T}\right) \cos(\omega_{IF} k t)\right) \cos(\omega_c t + \phi(t)). \end{aligned} \tag{3.14}$$

The spectrum of the carrier-based BL-PWM signal is shown in Figure 3.10, which is free from aliasing and image distortions.

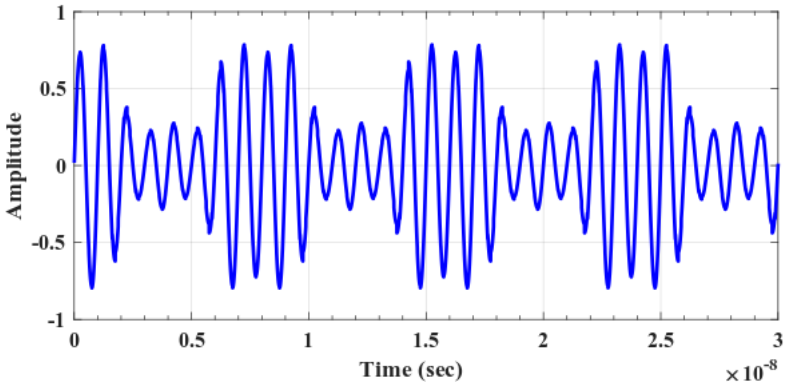


Figure 3.9: The carrier-based BL-PWM signal in the time-domain.

Finally, the carrier-based BL-PWM is transmitted after power-amplification. Although the aliasing and image distortions are eliminated, AF-PWMT can only be used with linear PAs as the carrier-based BL-PWM signal has varying envelope. As a result, the overall efficiency of the transmitter is limited by the type of the used PA [79].

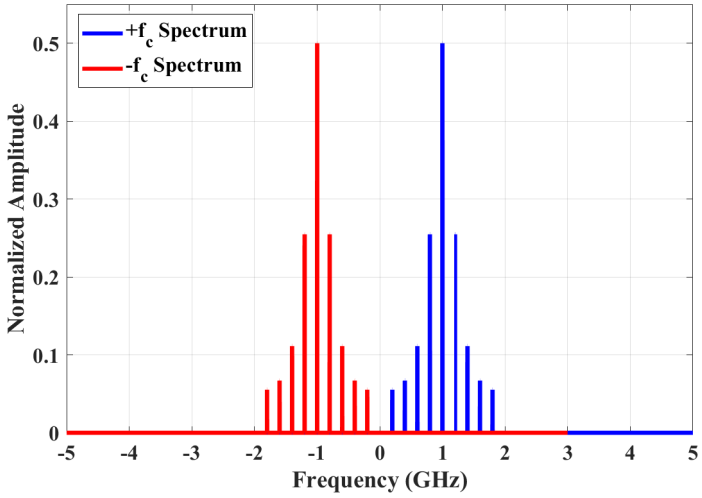


Figure 3.10: The spectrum of carrier-based BL-PWM signal.

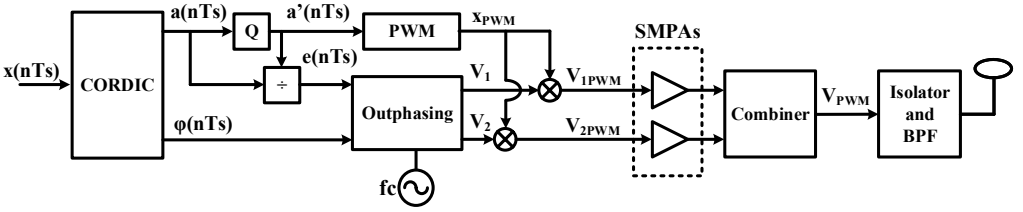


Figure 3.11: Block diagram of the aliasing-compensated PWM transmitter.

3.2.4.2 Aliasing-Compensated PWM Transmitter

The aliasing-compensated PWM transmitter (AC-PWMT) presented in **Paper A** uses a combination of baseband PWM and outphasing to compensate for the amplitude aliasing and image distortions. The block diagram of the proposed transmitter is shown in Figure 3.11, where the input signal is split into its amplitude and phase components $a(t)$ and $\phi(t)$, respectively. A quantized version of $a(t)$ is used to generate a band-limited PWM signal, X_{PWM}. Next an error signal $e(t)$ is generated as

$$e(t) = \frac{a(nT_s)}{a^{'}(nT_s)} \tag{3.15}$$

where $a^{'}(nT_s)$ is the quantized amplitude of the baseband signal. The error signal $e(t)$ is then added and subtracted to the phase component, $\phi(t)$ to generate two outphasing angles, which phase modulate the carrier signal to generate two outphasing carriers V_1 and V_2. Two carrier-based PWM signals, V_{1PWM} and V_{2PWM} are generated by the multiplication of X_{PWM} with V_1 and V_2, respectively, which are power amplified, combined and filtered to generate an amplitude aliasing and image distortion-free PWM signal.

AC-PWMT can use linear PAs at their saturation power as well as SMPAs resulting in a higher efficiency as compared to the AF-PWM transmitter. The theoretical efficiency of AC-PWMT for different PAs is compared to that of an AF-PWM transmitter in Figure 3.12.

3.2.4.3 A Modified All-Digital PWM Transmitter

In **Paper B**, an all-digital implementation of the aliasing-compensated PWM transmitter [79] is presented. The entire transmitter, from baseband up to the PA input is implemented using an FPGA. The FPGA implementation of the transmitter is shown in Figure 3.13. The design of the transmitter can be split

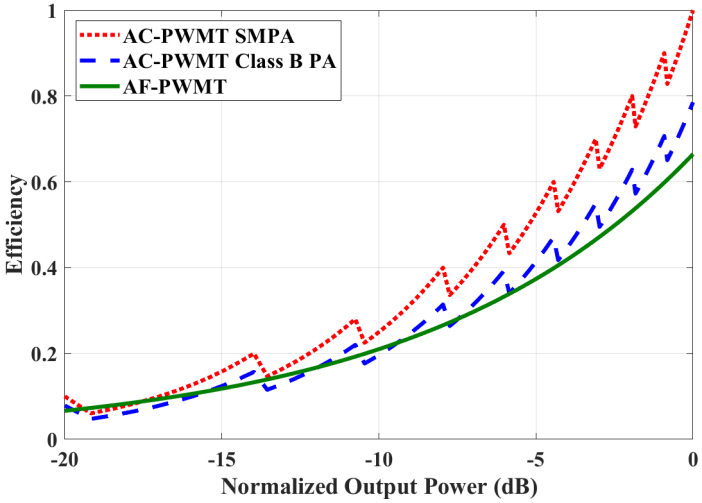


Figure 3.12: Comparison of the theoretical efficiency of AC-PWMT and AF-PWMT.

into two parts with respect to its FPGA implementation. The PWM signal generation is implemented in the FPGA core resources, whereas the outphasing is implemented as a pulse-position modulation (PPM) operation using the FPGA core and high-speed transceivers.

The PWM block is implemented using a 10-bit wide look-up table (LUT) and it stores the PWM signals corresponding to the 4-bit quantized amplitudes $a(nT_s)$. The output of the PWM LUT is readout serially using a core serializer, which is implemented as a shift register. The two PPMs are implemented using a combination of two 20-bit wide LUT and two high speed transceivers. A 5-bit intermediate signal, representing the multiplication of the x_{PWM} and the composite angles V_1 and V_2, is used to select the output of the PPM LUTs. Finally, the PPM LUT output is serialized using the transceiver and fed to the PA for amplification. The output frequency depends on the PPM resolution and the transceiver output frequency.

Figure 3.14 compares the amplitude linearity of the proposed transmitter and the digital PWM transmitter [71], which suffers from amplitude aliasing and image distortion. In general, the higher the phase resolution, the greater would be the amplitude linearity of the transmitter. However, it should be noted that the gain in amplitude linearity becomes less significant as the number of phases increase and becomes almost linear for 86 phases.

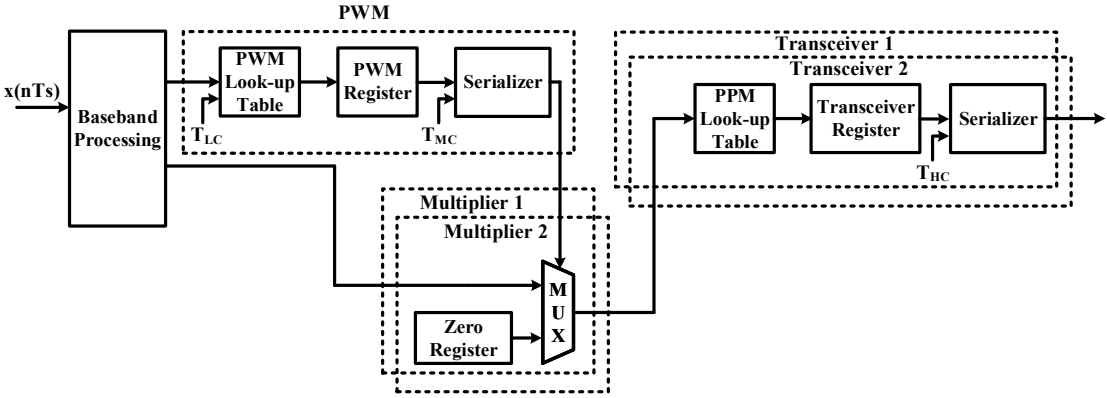


Figure 3.13: FPGA implementation of the modified all-digital PWM transmitter.

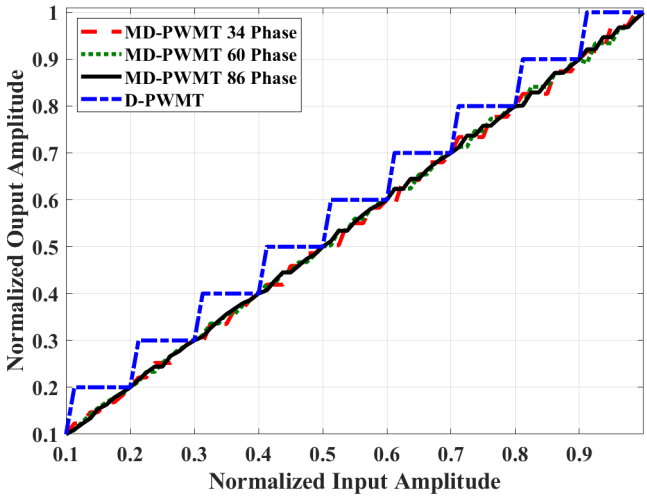


Figure 3.14: Amplitude linearity of the digital PWM transmitter and the modified all-digital PWM transmitter for different phase resolutions.

3.2.5 Phase Aliasing Distortion

A second phenomenon related to the digital implementations of polar PWM transmitters is the increased phase non-linearity and is referred to as phase-aliasing distortion [71, 80]. In digital implementations, the phase of the carrier is modulated using pulse-position modulation (PPM), but its resolution is usually limited. The PPM can be implemented either as a sample-and-hold circuit in

which case the maximum achievable resolution is limited by the sampling clock speed [71, 76, 80]. Alternatively, delay lines can also be used to implement PPM but in this case the PPM resolution is limited to a unit delay, which is set by the target CMOS technology [69, 70]. In both cases the total number of available phases N_{ppm} is given in (3.16) where ω_s is the maximum sampling frequency of the sample-and-hold system or the inverse of the unit delay in case of a delay line, and ω_c is the carrier frequency.

$$N_{ppm} = \frac{\omega_s}{\omega_c} \tag{3.16}$$

As compared to an analog implementation of PPM where the phase step can be arbitrary, in digital implementations it is limited by ω_s. However, as the CMOS processes continue to scale down it has become possible to achieve very fine delays using delay line e.g. in 65 nm CMOS, a delay as small as 15 ps can be achieved [81].

3.2.5.1 An All-Digital PWM Transmitter with Enhanced Phase Resolution

The phase resolution of all-digital PWM transmitters is usually limited by the implementation of the phase modulator in the digital domain. A digital phase modulator can be implemented as a delay line in full-custom implementations or by using some sort of over-sampling as shown in **Paper B**. In the first case, the achievable phase resolution is limited by the unit-element delay of the delay line. In the second case, the phase resolution is limited by the maximum clock rate of the over-sampling clock. In **Paper C**, baseband PWM is combined with asymmetric outphasing to improve the phase resolution for digital implementations of PWM transmitters.

The block diagram of the proposed transmitter is shown in Figure 3.15. A CORDIC processor splits the input signal into its amplitude and phase components $a(t)$ and $\phi(t)$, respectively. For a phase resolution of N, the phase component $\phi(t)$ is quantized into $2N$ levels. The quantized phase $\phi_q(t)$ is used to generate two outphasing angles ψ_1 and ψ_2, which phase modulate the carrier. The phase modulated carriers are either symmetrical or shifted by the phase modulator's minimum step.

The amplitude component $a(t)$ is converted into a PWM signal after predistortion, which is done to compensate for the error introduced due to outphasing. The PWM signal is then multiplied with the phase modulated carriers and power amplified, to generate amplified phase modulated PWM carriers. The

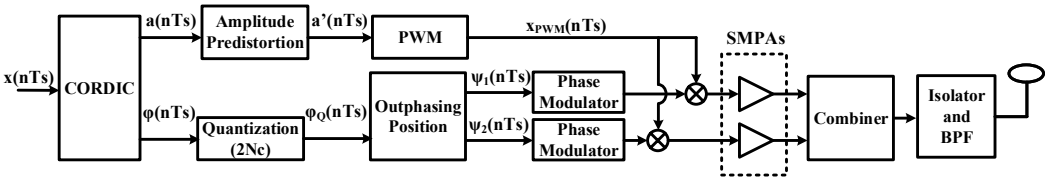


Figure 3.15: Block diagram of the all-digital PWM transmitter with enhanced phase resolution.

transmit signals are finally combined and filtered to generate the final transmit signal.

The transmitter was implemented on the same FPGA as **Paper B** and as compared to the digital PWM transmitter the error vector magnitude (EVM) was reduced by 4.1% for a 1.4 MHz LTE signal with a carrier frequency of 700 MHz.

Chapter 4

Radio-Frequency PWM Transmitters

In Radio-Frequency Pulse-Width Modulated Transmitters (RF-PWMT), the amplitude information of the input signal is encoded into the pulse width of a pulse train, whereas the pulse position represents the phase of the input signal. Unlike baseband PWM, the pulse train is at RF frequency ω_c allowing for a single pulse transmission per carrier clock period. As a result, the harmonics appear at multiples of ω_c relaxing the filtering process, which is the main advantage of RF-PWM over baseband PWM.

The block diagram of an RF-PWM transmitter is shown in Figure 4.1, where the CORDIC processor splits the input signal $x(t)$ into its amplitude and phase components $a(t)$ and $\phi(t)$ respectively. The RF-PWM block generates a PWM signal according to the value of $a(t)$, which is pulse-position modulated according to $\phi(t)$. The constant envelope RF-PWM in (4.1) is then power amplified and filtered to generate the final transmit signal.

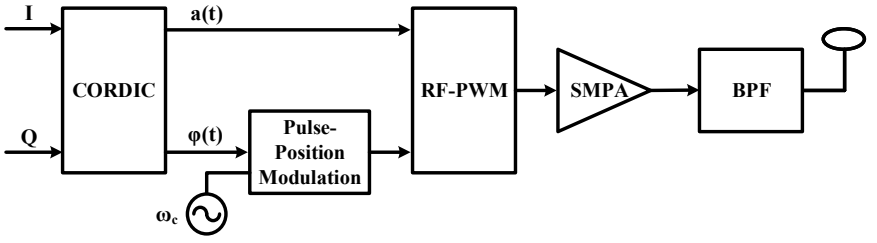


Figure 4.1: Block diagram of an RF-PWM transmitter.

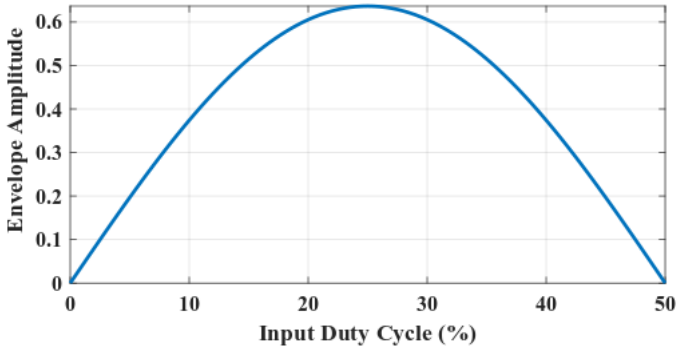


Figure 4.2: Relation between envelope amplitude and RF-PWM duty cycle.

$$v_{PWPM} = a(t) + \sum_{k=1}^{\infty} \frac{2}{k\pi} \sin\left(k\pi a(t)\right) \cos\left(k\omega_c t + \phi(t)\right) \tag{4.1}$$

4.1 Limitations of RF-PWM

The following factors are to be considered for the design of RF-PWM based wireless transmitters.

4.1.1 Limited Amplitude Resolution

In RF-PWM a non-linear relation exists between the input signal amplitude and the envelope of the transmit signal. For $k = 1$, the amplitude of the first harmonic component (envelope of transmit signal) in above (4.1) is

$$a_1 = \frac{2}{\pi} \sin(a(t)\pi) \tag{4.2}$$

and

$$a(t) = D = \frac{\tau}{t} \tag{4.3}$$

where τ is the pulse-width, t is the pulse-repetition period and D is the duty-cycle of the RF-PWM signal. A plot of (4.2) is shown in Figure 4.2 for the desired signal component, which indicates that only 50% of the duty-cycle of the RF-PWM can be used to represent the amplitude of the input signal.

In digital implementations of RF-PWM, the number of available quantization levels is much less than in baseband PWM, resulting in an increased quantization noise. However, using a higher sampling frequency can significantly reduce the

effect of the in-band quantization, which would be limited by the target CMOS technology.

4.1.2 Pulse Swallowing

In RF-PWM, pulse swallowing is a major issue, since the pulse width of the PWM signal should be wide enough for the PA to switch. In high power PAs, large transistors are used to handle large currents. As a result, the gate capacitance and hence the associated RC delay is very large. PWM pulses narrower than the RC delay of the PA would be swallowed i.e., would have no effect on the PA output.

4.2 A Power Efficient Aliasing-Free PWM Transmitter

A power and area efficient transmitter that eliminates the aliasing and image distortions in the PWM transmitters is presented in **Paper E**. To remove aliasing distortion for the transmit signal, the proposed transmitter reduced the number of harmonics in the generated PWM signal and uses RF-PWM to transmit the generated signal using an SMPA to ensure high efficiency.

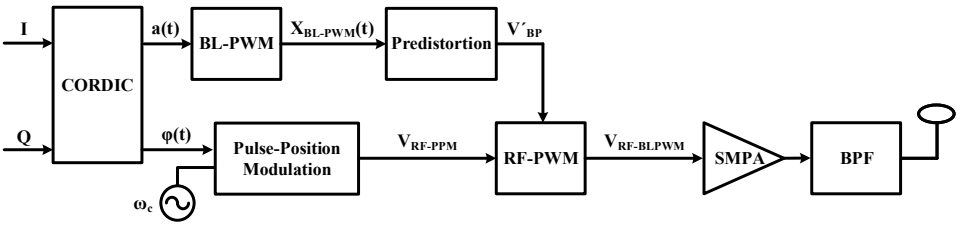


Figure 4.3: Block diagram of the power-efficient aliasing-free PWM transmitter.

The block diagram of the proposed transmitter is shown in 4.3. A CORDIC processor splits the input signal into its amplitude and phase components $a(t)$ and $\phi(t)$ respectively. Using the $a(t)$, a PWM signal with limited harmonics called the band-limited PWM (BL-PWM) signal is generated, which has a varying envelope and cannot be directly used with an SMPA. The proposed transmitter uses the varying amplitude of the BL-PWM signal to generate an RF-PWM signal, which is phase modulated according to $\phi(t)$, power amplified and finally filtered to generate the transmit signal.

Chapter 5

Time-to-Digital Converters

A time-to-digital converter (TDC) is an asynchronous circuit used to quantify the time interval between two or more events with a pico-second resolution [82–84]. TDCs are not only used in PLLs but are also employed for time-of-flight measurements, positron emission tomography (PET) in medical imaging and in laser range finders. The requirements that each of the above mentioned applications have on the TDC are different due to which many different architectures of TDCs exist.

In the context of PWM based RF transmitters, TDC can be used to accurately determine the duty of the generated PWM signals. In RF-PWM, the input signal amplitude has a non-linear relationship with the duty cycle of the output signal [85]. Hence it is important to measure any deviations in the duty cycle of the PWM signal and compensate for it. In sub-micron CMOS processes, the focus has been to use digital gates or standard cells to design circuits used for the processing of analog signals.

Since the early applications of TDCs the important parameters to determine the performance of a TDC have been the time resolution and input sampling rate [86]. Although the implementation technology has significantly evolved from the days of vacuum tubes, the notion and the methodology of dividing time into smaller intervals has remained almost similar. Depending on their structure and working nature the TDCs can be classified into two main classes

- Delay Line TDCs
- Oscillator-based TDCs

In this chapter we limit the discussion to Delay-line TDCs. The following section presents a brief overview of the delay-line TDCs and their limitations.

5.1 Delay line TDCs

Delay line TDCs are the most popular of the TDC architectures because of simple implementation and higher sampling rates as compared to other TDC architectures [81]. A delay-line TDC is shown in Figure 5.1, where the Start signal is injected into a chain of delay elements and as the Start signal propagates through the delay chain a delayed version of the Start pulse is created at every delay element. When the Stop signal arrives, the output of all the delay elements is sampled using latches or flip-flops as shown in Figure 5.2.

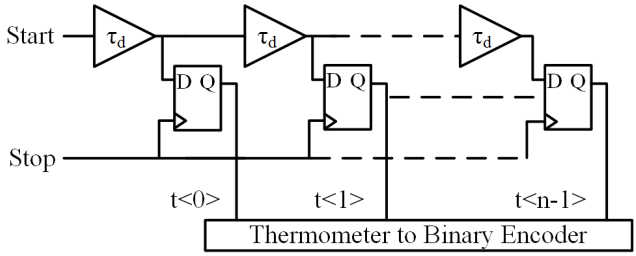


Figure 5.1: Basic implementation of a delay-line TDC.

With the arrival of the Stop signal, the state of the delay line is stored and is then read out. The output code is in thermometer form and it is converted to its equivalent binary value using a thermometer encoder for post processing. The output is high for all the delay stages the Start signal has propagated through, while for the remaining stages the output is low. The position of the first low value in the delay line indicates the time difference $\triangle$ in terms of number of delay elements between the Start and Stop signals and is given as

$$\triangle T = N\ T_{res} + \epsilon \tag{5.1}$$

where N is the number of delay elements the Start signal has propagated through, T_{res} is the propagation delay per delay element and ϵ is the quantization error. Figure 5.1 shows the schematic of a delay-line TDC where each delay cell can be realized using a buffer or an inverter. The time resolution of such a TDC is however limited to a single gate delay, which can be in the order of 15 ps for a 65 nm CMOS process [81].

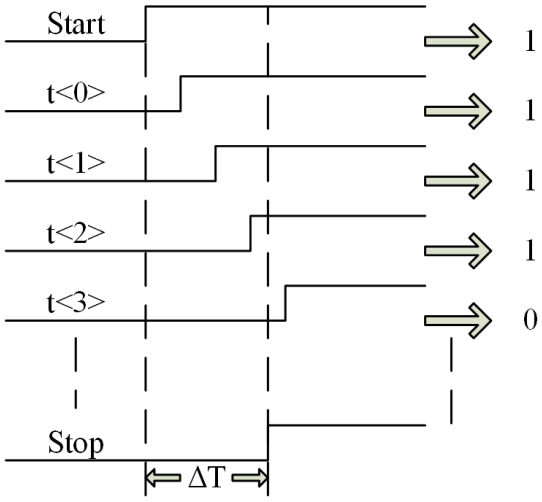


Figure 5.2: Timing diagram of a delay-line TDC.

The delay-line TDCs are popular due to straight forward implementation and do not require complex controlling schemes. The dynamic range of the delay-line TDCs can be increased by using a looped structure [87]. The performance of delay-line TDCs is expected to improve with process scaling due to increasing f_T. However, there are some limitations; the most significant of which is that their time resolution is dictated by process technology. Secondly the layout of the delay-line TDCs requires special attention in making sure that each stage has to drive the same RC load otherwise the TDC might exhibit non-linear characteristics.

The time resolution of the delay-line TDCs is limited by the CMOS process technology node used to implement the design. In order to quantize signals with a sub-gate delay resolution different techniques have been proposed that are briefly discussed here.

The Vernier delay-line TDCs [87] use two delay lines with slightly different propagation delays as shown in Figure 5.3. The Start signal propagates through the delay line with a propagation delay of t_{slow} while the Stop signal propagates through the second delay line with a propagation delay of t_{fast} and registers the output value of each stage in the slow delay line. When both the signals have arrived after each stage the time difference between the two signals is reduced by a factor T_{res}, i.e., the TDC time resolution, which is given as

$$T_{res} = t_{slow} - t_{fast} \tag{5.2}$$

Since the Stop signal has to undergo a smaller propagation delay it eventually catches up to the Start signal. For the remaining stages the Stop signal leads the Start signal. A high value is registered as the output for the stages where the Start signal has propagated through, and a low value is registered for the remaining stages through which the Start signal is yet to propagate through.

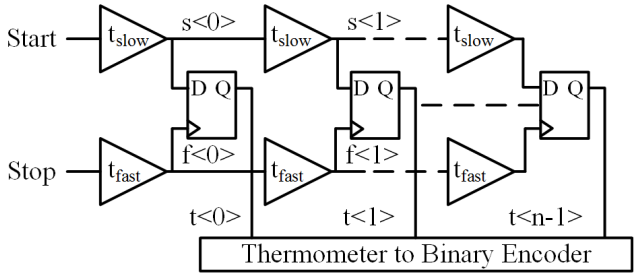


Figure 5.3: Schematic diagram of a Vernier delay-line TDC.

The time resolution of the Vernier TDC does not depend on the individual propagation delay of each stage. It rather depends on the time difference of the propagation of the two delay lines. In principle the time resolution of the Vernier TDC can be made very small but in practice this is limited due to device noise and other parameters. The increased resolution, however comes at a price of increased area and higher power consumption.

The time resolution of the delay line TDC can also be enhanced by using time amplifiers (TAs) [88]. The TDCs employing TAs use a two-step method to quantize the time difference between the input signals as shown in Figure 5.4. In TDCs that use TAs, the input time difference between the TDC inputs is amplified using the TA, after it is fed into the conventional delay-line TDC. On each tap of the TDC delay line a separate TA is required that amplifies the residue between its inputs and passes it on to a residue multiplexer. The output of the TDC is a thermometer code and just as for a delay-line TDC the output is high for all the stages through which the Start signal has propagated through and low for the remaining stages. A logic circuit detects high to low transition and then selects the appropriate residue from the residue multiplexer. The amplified residue is then passed to a second TDC stage with a finer resolution for further processing.

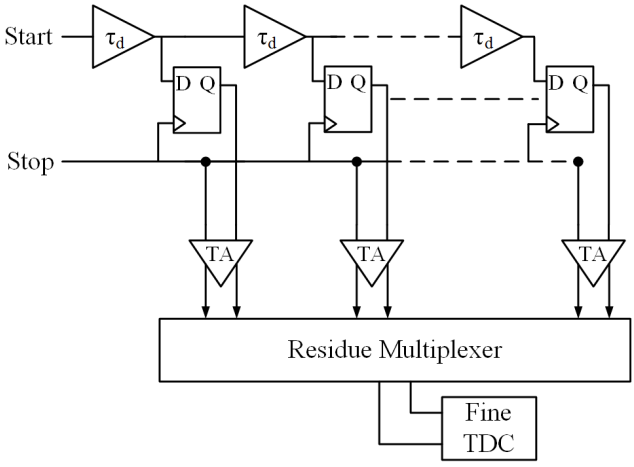


Figure 5.4: Schematic diagram of a time amplifier delay Line TDC.

Noise in TAs is a critical issue for TA-based TDCs. The stability of latches used in the TA is highly prone to noise, couplings and other non-linear effects. The performance of the TAs is also sensitive to supply noise, which might affect its linear operation range. This problem has been addressed in [81] where a fully digital TA with well-controlled gain is presented.

The total number of stages in the delay line have to be increased to extend the dynamic range of a delay-line TDC. As a result, the area and power consumption grow linearly with increasing dynamic range and finer time resolution. Another problem is the increased power consumption of the thermometer-to-binary encoder. This is because the output of the slow delay line is processed by that of the fast delay line at every cycle until the Stop signal has propagated through the fast delay line.

5.2 A Synthesizeble TDC Architecture

This section explored the possibility of using the automated design tools for synthesizing TDCs. The selected TDC architecture uses multiplexers from the standard cell library as delay and for sampling as shown in Figure 5.5 [89]. The used multiplexers are based on transmission gates and are less prone to blackout window effects as compared to flip-flops.

When the rising edge of the Start pulse arrives, it starts propagating through the slower delay line incrementing the output thermometer code at each stage.

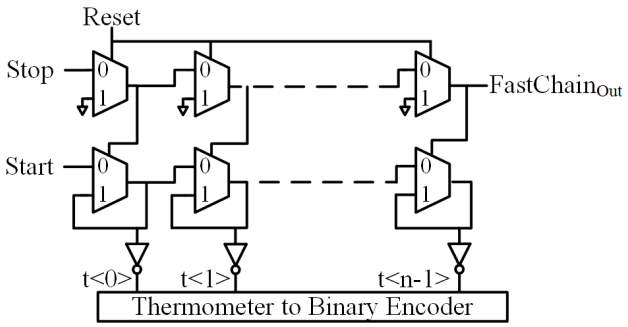


Figure 5.5: Multiplexer based Vernier TDC.

At the rising edge of the Stop pulse, the Stop pulse begins propagating through the faster delay line and initially is lagging behind the Start signal by the time difference between the two pulses. As the Stop pulse propagates through the delay line, it latches the output of every multiplexer in the slow line to a high value since the Start pulse has already propagated through. At the M^{th} stage, the Stop pulse catches up to the Start pulse as it experiences less delay through the fast delay line and locks the multiplexers in the following stages of the slow delay line to a low value as the Start pulse has not yet propagated through it. The thermometer code at the output then yields the relative time difference between the two pulses.

The same standard cell block is used to implement both the delay chains so that both the chains experience similar process variations and other fabrication effects. Inverters are added to the output of one of the chains to make it slower. The addition of inverters also serves in decoupling the delay chain from the thermometer-to-binary converter which would have loaded some stages of the delay chain more than the others. For a delay line with a fixed number of stages, the size of load inverter sets the dynamic range and the time resolution of the TDC.

5.3 Automatic Place and Route

A major challenge for the standard cell-based implementation is the mismatch introduced by automatic P&R tool. Although the TDCs can easily be described in a hardware descriptive language (HDL), the automatic P&R will introduce significant mismatches if allowed to place cells freely. Since the most critical

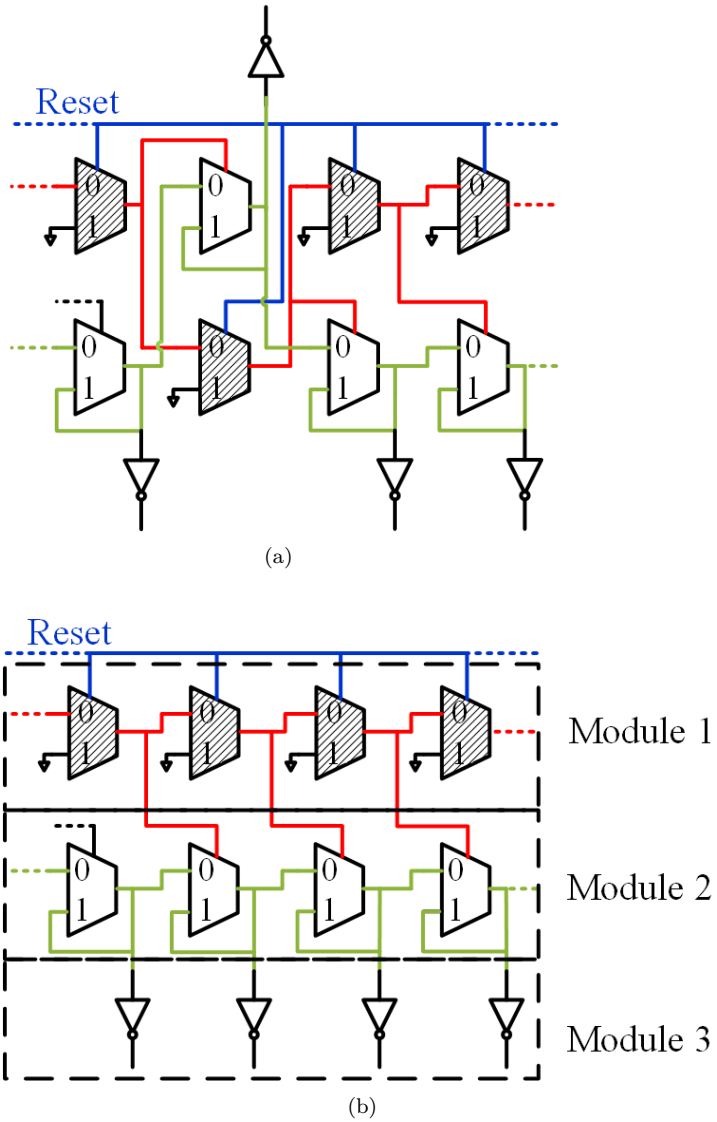


Figure 5.6: Illustration of cell placement with (a) unrestricted P&R (b) modular approach

component of the TDC is the delay line, it is crucial that the delay through each stage of the delay line is exactly the same. If this is not taken care of, then the output TDC code will exhibit non-linear characteristics. In order to maintain linearity it is required that each stage has to drive the same RC load due to the signal routing in layout. Folding of the delay line during layout has to be avoided as some delay stages would have to drive a higher RC load (due to longer routing wires) than others thus contributing to the path delay and also affecting the rise/fall times of the propagating pulses.

Although a fully synthesized TDC has earlier been published in [90] where the TDC is described entirely in an HDL and then placed and routed using an automated tool. The effects of non-linearity introduced by the P&R tool are mitigated by rearranging the delay stages according to measured drive strengths. To remedy the P&R tools randomness [90] had proposed a coarse/fine control of the TDC but the issue of uncertainty in layout remains unsolved [91]. Another problem with the design in [90] is that the accuracy of the TDC cannot be predicted until the design is fully place and routed.

A modular approach can be used to avoid the randomness introduced by P&R tools. Figure 5.6 shows the cell placement using the modular approach and with the unrestricted P&R. The shaded multiplexers belong to the fast delay line and the empty ones belong to the slow delay line. Green and red lines represent the propagating Start and Stop signals respectively. Figure 5.6(a) shows a section of the TDC delay chain placed using the P&R tool without restrictions. As seen from the figure the unit cells for both the delay lines are placed randomly introducing systematic mismatch in the TDC characteristics as the routing lines between the cells of both slow and fast delay lines are non-uniform. In the modular approach, the TDC can be divided into three modules, i.e., the fast delay line, the slow delay line and a chain of load inverters as shown in Figure 5.6(b). Each module is placed and routed independently of the other and then combined later using simple cell alignment. To prevent the random placement of unit cells, the tool is restricted by specifying floor-plan dimensions such that the unit cells are placed in an array structure as specified in the netlist. The pin locations for both the delay lines and load inverters are specified such that when placed vertically the output pins from the fast delay line overlap the select pins of the slow delay line, and the output pins from the slow delay line overlap with the load inverter input. To avoid additional vias the corresponding pins are specified in the same metal layer. Another advantage of the modular approach is that if the TDC resolution or dynamic range need to

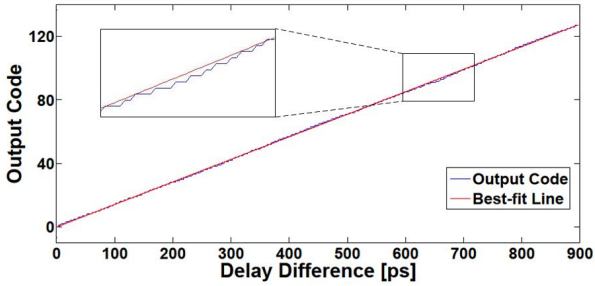


Figure 5.7: TDC transfer function.

be modified, instead of repeating the entire P&R process again only Module 3 i.e., chain of load inverters needs to modified.

The remaining digital blocks like the thermometer encoder can be synthesized using the conventional automatic P&R. Using automated tools the layout time for the synthesized TDC can be significantly reduced from the order of weeks to less than 2 hours.

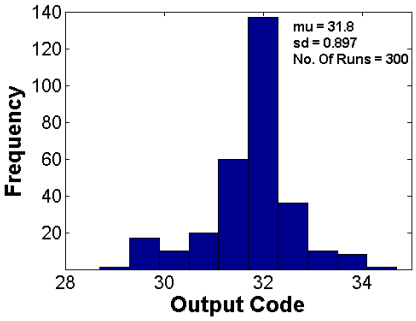
5.4 Experimental Results

The viability of the proposed synthesis approach is demonstrated by using standard cells from an STM 65 nm technology to synthesize a TDC. The place and routed TDC core occupies an area of 9 μm $\times$ 232 μm. The selected process offers transistors and standard cells in the following two types

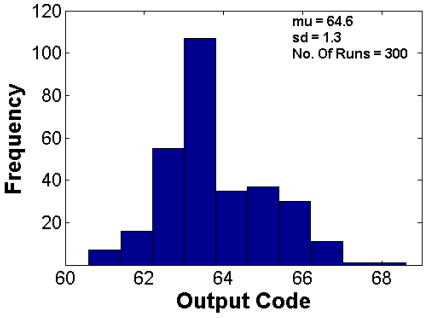
- General Purpose (GP) Devices
- Low Power (LP) Devices

In general the GP devices have a thinner gate oxide layer, operate at slightly lower supply voltages, have higher drive currents and lower threshold voltage V_t as compared to LP devices. For this work, the GP devices were selected due to a smaller variation in the propagation delay over the different process corners. To compensate for the reduced on-state current of GP devices a slightly overdriven supply voltage of 1.2 V instead of the nominal 1.1 V is used.

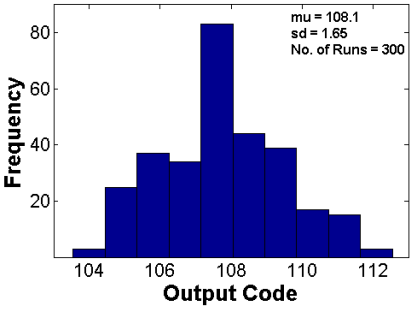
To verify the performance of the synthesized circuit a Spice netlist of the place and routed design, which includes the parasitic resistances and capacitances due to signal routing is exported from SoC Encounter to Spectre [92] and analog



(a)



(b)



(c)

Figure 5.8: Single shot precision of the output codes (a) 32 (b) 64 (c) 108

simulations with conservative accuracy are performed. The TDC is verified to operate at 100 MS/s for all process corners while dissipating 1.66 mW of power. Monte-Carlo simulations for both process and mismatch are performed for a 1.2 V supply at 70° C to model the effects of fabrication. The effect of process variations on the TDC time resolution is shown in Figure 5.9, which is estimated to be around 6.4 ps with a variation of 0.86 ps for 300 runs.

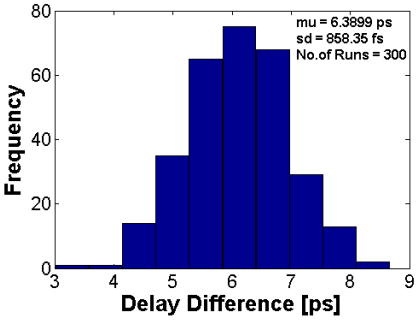


Figure 5.9: Expected TDC resolution with process mismatches.

Single shot precision simulations are performed to capture the effect of jitter accumulation and other noise sources on the synthesized TDC. A single shot simulation observes the output of the TDC corresponding to a fixed time difference between input signals. Histograms for 3 different codes obtained from Monte-Carlo simulations for 300 points are shown in Figure 5.8.

Table 5.1 summarizes the performance of the synthesized TDC. The FOM proposed in [81] is used to evaluate the performance of the synthesized TDC. The FOM takes into consideration the effects of non-linearity and calculates the effective number of linear TDC bits as

$$N_{Linear} = Bits - log_2(INL + 1) \tag{5.3}$$

The FOM is then defined as in (5.4) and also takes into consideration the TDC input sampling rates

$$FOM = \frac{P}{2^{N_{linear}} \times Fs} \tag{5.4}$$

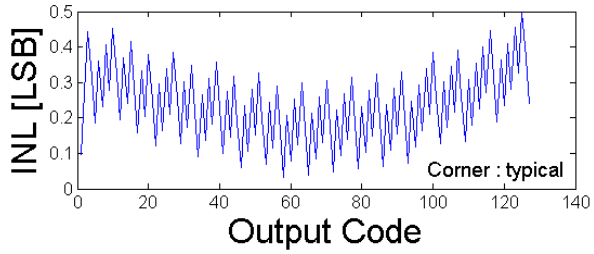
where P is the power consumed by the TDC at a sampling rate of Fs. From the Table 5.1 it can be seen that the synthesized TDC achieves a good performance with significantly reduced design time. The TDC is intended to be used for fully synthesized ADPLLs.

Table 5.1: Performance Comparison

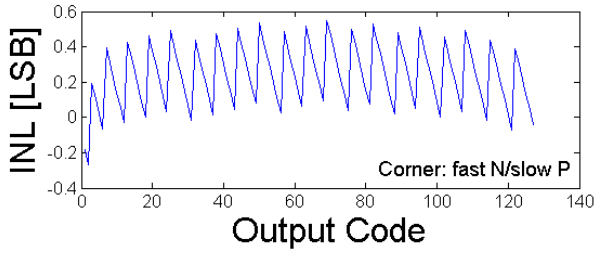
Type	Vernier [89]	This Work
Scheme	Vernier	Vernier
Resolution	5.7 ps	6.4 ps
Bits	7	7
Conversion Rate [MS/s]	100 MS/s	100 MS/s
Range [ns]	0.73	0.8
Power [mW]	1.75	1.62
TDC Core Area [mm^2]	0.001	0.002
Power Supply [V]	1.2	1.2
Synthesizable	No	Yes
Technology [nm]	65	65
FOM [pJ/conv. step]	0.25	0.19
Layout Design Time	6 weeks	$<$ 2 hours

Post P&R simulation of the integral nonlinearity (INL) for three different process corners i.e., typical NMOS/PMOS, fast NMOS/slow PMOS and slow NMOS/fast PMOS are shown in Figure 5.10. Simulated differential nonlinearity (DNL) for the same corners is shown in Figure 5.11. From the simulations it can be observed the linearity of TDC remains stable over the different process corners.

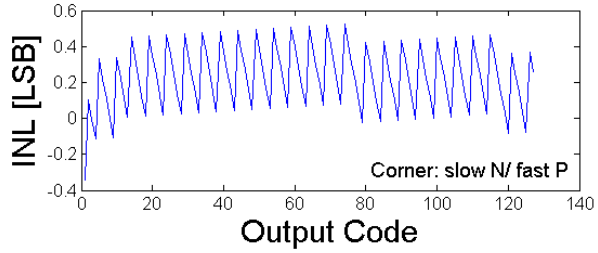
The modular approach presents an interesting alternative to the synthesis of asynchronous circuits like TDCs. Although measurements are necessary to accurately predict the circuit behavior, however, the results predicted by simulations are very encouraging.



(a)

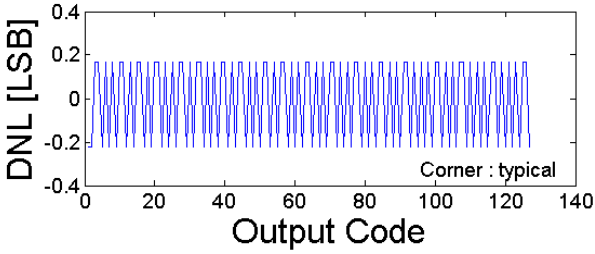


(b)

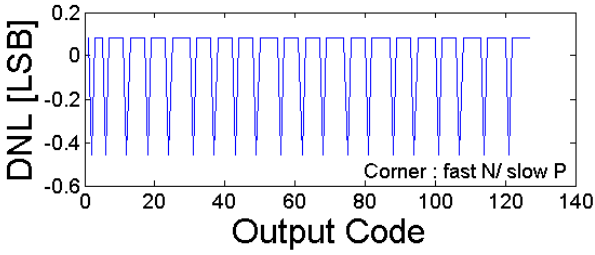


(c)

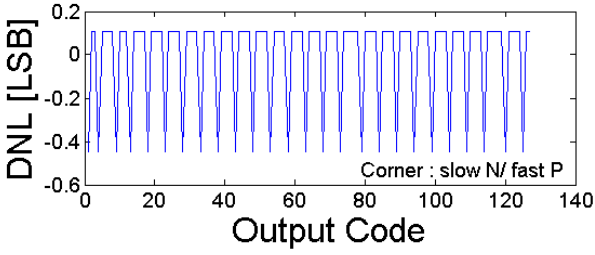
Figure 5.10: DNL simulation for a) typical b) fast N/ slow P and c) slow N/fast P process corners. Time Resolutions are 6.43, 4.614 and 4.51 ps/LSB respectively.



(a)



(b)



(c)

Figure 5.11: DNL simulation for (a) typical (b) fast N/ slow P and (c) slow N/fast P process corners. Time Resolutions are 6.43, 4.614 and 4.51 ps/LSB respectively.

Chapter 6

Summary and Future Trends

The power amplifier (PA) plays an important role in determining the linearity and efficiency of a wireless transmitter. By using switch-mode PAs (SMPAs), the efficiency is improved but to amplify envelope-varying signal SMPAs have to be used together with linearization schemes like pulse-width modulation (PWM). The work presented in this thesis is aimed to enhance the spectral performance of all-digital PWM-based transmitters. Several new transmitter architectures have been presented that reduce the amplitude and phase error in the final transmit signal by compensating for image and aliasing distortions.

In **Paper A** and **B**, a technique to compensate for the amplitude error due to image and aliasing distortions was presented. Improvements of up to 6 dBc in the adjacent channel leakage ratio (ACLR) have been shown. In **Paper C**, the issue of a limited phase resolution in all-digital implementations of baseband PWM transmitters was addressed. By using outphasing the available phase resolution was doubled as compared to the conventional digital PWM transmitter. **Paper E** presented an alternative approach to enhance the spectral performance by using a combination of band-limited PWM and RF-PWM. As compared to **Paper A** and **B**, the transmitter in **Paper E** requires a much smaller silicon area and has a higher efficiency.

As the PWM signal encodes information in the time-domain, it is important to quantify the PWM signals accurately. In **Paper F**, an area efficient time-to-digital converter (TDC) architecture with a 5.4 ps time resolution has been presented. An all-digital implementation of the proposed architecture using automatic place and route has also been explored in Chapter 5. For the future,

the feasibility of an ASIC implementation of the proposed transmitters should be explored. This would be beneficial in overcoming the limitations of FPGA-based implementations and determining the full performance characteristics of the proposed transmitters. The possibility of using a different type of PAs and power combiners to enhance the efficiency should also be explored.

Although not as flexible as ASICs, the processing performance and usage of FPGAs continues to grow as the CMOS technology advances. The possibility of using FPGA-based implementations of wireless transmitters should be explored, especially in application areas with less stringent requirements on power consumption. For example, vehicle to everything (V2X) is an emerging paradigm that aims to use 5G and deep learning-based object recognition to make autonomous driving possible in the near future, all of which can be easily implemented using a modern FPGA.

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Publications

My Contributions

- **Paper A** M. F. U. Haque, M. T. Pasha, and T. Johansson, "Aliasing-Compensated Polar PWM Transmitter," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 8, pp. 912-916, Aug. 2017.
  Contribution: Wrote parts of the manuscript. Set-up and performed measurements in collaboration with the first author.

- **Paper B** M. T. Pasha, M. F. U. Haque, J. Ahmad, and T. Johansson, "A Modified All-Digital Polar PWM Transmitter," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 758-768, Feb. 2018.
  Contribution: Proposed the concept and implementation, and wrote major portions of the manuscript. Collaborated with the second author in setting up and performing the measurements.

- **Paper C** M. T. Pasha, M. F. U. Haque, J. Ahmad, and T. Johansson, "An All-digital PWM Transmitter with Enhanced Phase Resolution," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 11, pp. 1634-1638, Nov. 2018.
  Contribution: Proposed the idea to address the limitations of the implementation in Paper B. Developed the implementation, and wrote major portions of the manuscript. Set-up and performed measurements along with the second author.

- **Paper D** M. F. U. Haque, M. T. Pasha, T. Malik, and T. Johansson, "A Comparison of Polar and Quadrature RF-PWM," presented at NORCAS 2018, Oct. 30-31, Tallin, Estonia.
  Contribution: Setup the simulations and contributed to writing parts of the manuscript.

- **Paper E** M. F. U. Haque, M. T. Pasha, and T. Johansson, "A Power-Efficient Aliasing-Free PWM Transmitter," accepted for publication in IET Circuits, Systems and Devices, Oct. 2018.
  Contribution: Collaborated with the first author in developing the idea. Writing parts of the manuscript, setting up and performing measurements.

- **Paper F** M. T. Pasha, N. U. Andersson, and M. Vesterbacka, "Power-Efficient Time-to-Digital Converter for All-Digital Frequency Locked Loops," presented at ECCTD 2015, Aug. 24-26, Trondheim, Norway.
  Contribution: Intermixed co-work with the second author along with writing parts of the manuscript.

- **Paper G** M. T. Pasha and M. Vesterbacka, "A Modified Switching Scheme for Multiplexer-Based Thermometer-to-Binary Encoders," presented at NORCHIP 2014, Oct. 27-28, Tampere, Finland.
  Contribution: Proposed the concept, performed the simulations, and wrote the manuscript.

Papers

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