CVD growth of SiC for high-power and high- frequency applications

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Cover: Image taken with an optical microscope using a Nomarski prism for contrast. The image is taken from a 4H-SiC homoepitaxial layer grown on on-axis substrate. The image depicts a sample covered in a step-like structure.

During the course of the research underlying this thesis. Robin Karhu was enrolled in Agora Materiae, a multidisciplinary doctoral program at Linköping University, Sweden.

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To my family

ABSTRACT

Silicon Carbide (SiC) is a wide bandgap semiconductor that has attracted a lot of interest for electronic applications due to its high thermal conductivity, high saturation electron drift velocity and high critical electric field strength. In recent years commercial SiC devices have started to make their way into high and medium voltage applications.

Despite the advancements in SiC growth over the years, several issues remain. One of these issues is that the bulk grown SiC wafers are not suitable for electronic applications due to the high background doping and high density of basal plane dislocations (BPD). Due to these problems SiC for electronic devices must be grown by homoepitaxy. The epitaxial growth is performed in chemical vapor deposition (CVD) reactors. In this work, growth has been performed in a horizontal hot-wall CVD (HWCVD) reactor. In these reactors it is possible to produce high-quality SiC epitaxial layers within a wide range of doping, both n- and p-type.

SiC is a well-known example of polytypism, where the different polytypes exist as different stacking sequences of the Si-C bilayers. Polytypism makes polytype stability a problem during growth of SiC. To maintain polytype stability during homoepitaxy of the hexagonal polytypes the substrates are usually cut so that the angle between the surface normal and the c-axis is a few degrees, typically 4 or 8°. The off-cut creates a high density of micro-steps at the surface. These steps allow for the replication of the substrates polytype into the growing epitaxial layer, the growth will take place in a step-flow manner. However, there are some drawbacks with step-flow growth. One is that BPDs can replicate from the substrate into the epitaxial layer. Another problem is that 4H-SiC is often used as a substrate for growth of GaN epitaxial layers. The epitaxial growth of GaN has been developed on on-axis substrates (surface normal coincides with c-axis), so epitaxial 4H-SiC layers grown on off-axis substrates cannot be used as substrates for GaN epitaxial growth.

In efforts to solve the problems with off-axis homoepitaxy of 4H-SiC, on-axis homoepitaxy has been developed. In this work, further development of wafer-scale on-axis homoepitaxy has been made. This development has been made on a Si-face of 4H-SiC substrates. The advances include highly resistive epilayers grown on on-axis substrates. In this thesis the ability to control the surface morphology of epitaxial layers grown on on-axis homoepitaxy is demonstrated. This work also includes growth of isotopically enriched 4H-SiC on on-axis substrates, this has been done to increase the thermal conductivity of the grown epitaxial layers.

In (**paper 1**) on-axis homoepitaxy of 4H-SiC has been developed on 100 mm diameter substrates. This paper also contains comparisons between different precursors. In (**paper 2**) we have further developed on-axis homoepitaxy on 100 mm diameter wafers, by doping the epitaxial layers with vanadium. The vanadium doping of the epitaxial layers makes the layers highly resistive and thus suitable to use as a substrate for III-nitride growth. In (**paper 3**) we developed a method to control the surface morphology and reduce the as-grown surface roughness in samples grown on on-axis substrates. In (**paper 4**) we have increased the thermal conductivity of 4H-SiC epitaxial layers by growing the layers using isotopically enriched

precursors. In (**paper 5**) we have investigated the role chlorine have in homoepitaxial growth of 4H-SiC. In (**paper 6**) we have investigated the charge carrier lifetime in as-grown samples and traced variations in lifetime to structural defects in the substrate. In (**paper 7**) we have investigated the formation mechanism of a morphological defect in homoepitaxial grown 4H-SiC.

POPULÄRVETENSKAPLIG SAMMANFATTNING

Sedan den första transistorn demonstrerades så har den varit av hög betydelse för den teknologiska utvecklingen. Transistorn är en elektrisk komponent som tillsammans med olika typer av dioder är tillverkade av halvledarmaterial. I dag är det vanligaste materialet för tillverkning av dessa komponenter kisel. Kisel som material är inte lämpat för att hantera stora strömmar och spänningar. Så för tillämpningar som kräver hantering av höga strömmar och spänningar så måste man börja se sig om efter andra material. Ett material som har varit av intresse i många år är kiselkarbid (SiC) då detta material har egenskaper som är bättre lämpade för att hantera höga strömmar och spänningar. Detta eftersom att SiC har större bandgap, hög elektronmobilitet, hög värmeledningsförmåga och hög kritisk fältstyrka. Detta betyder att komponenter tillverkade av SiC kan hantera större strömmar utan att bli för varma samt hantera större spänningar utan att kortslutas jämfört med likvärdiga komponenter tillverkade i kisel.

I dag så tillverkas SiC för elektroniska komponenter mestadels genom homoepitaxi med hjälp av chemical vapor deposition (CVD). CVD bygger på att man låter gaser flöda genom en tillväxtkammare där gaserna reagerar med en yta för att bilda det önskade materialet. Homoepitaxi betyder att ytan man låter gaserna reagera på är av samma material som det önskade materialet. I detta fall så betyder det att SiC växer på SiC substrat. Detta kan låta konstigt, men det är på grund av att kommersiella SiC-substrat inte är lämpade för tillverkning av elektriska komponenter.

SiC är ett så kallat polymorfiskt material. Med detta menas att materialet existerar i flera olika varianter fastän de har samma kemiska sammansättning. Detta genom att Si-C lagren kan staplas på olika sätt, de olika staplingsordningarna kallas för polytyper. De vanligaste polytyperna av SiC är 3C-, 4H- och 6H-SiC. Kiselkarbids polytypism leder till problem när det kommer till homoepitaxi, då det är svårt att få den önskade polytypen att växa. För de hexagonala polytyperna, 6H och 4H, så är det vanligaste sättet att bibehålla substratets polytyp i det växande epitaxiella lagret att skära substratet med en liten vinkel. Vinkeln som substraten skärs på är så att yt-normalen och substratets c-axel inte är parallella, typiskt är denna vinkel 4 eller 8°. Detta bildar en hög densitet av steg på substratets yta, dessa steg kan då användas för att bibehålla substratets polytyp i det växande epitaxiella lagret. Dessa substrat kallas för off-axis substrat. Homoepitaxi på off-axis substrat tillåter dislokationer i kristallens basplan att överföras till det epitaxiella lagret. Ett annat problem är att 4H-SiC används som substrat för galliumnitrid (GaN), men denna tillväxten är utvecklad för on-axis (yt-normalen parallell med c-axeln) SiC substrat.

Homoepitaxi av SiC på on-axis substrat har demonstrerats tidigare. I detta arbete så har homoepitaxi av SiC på on-axis substrat utvecklats vidare. Bland annat så har epitaxiella lager med hög resistivitet växts. Den höga resistiviteten har åstadkommits via dopning av lagren med vanadin. Isotopanrikad SiC har också växts på on-axis substrat i ett försök att höja värmeledningsförmågan på SiC. SiC-tillväxt på on-axis substrat har också utvecklats så att det går att kontrollera yt-morfologin på de epitaxiella lagren.

PAPERS INCLUDED IN THE THESIS

Paper 1

J. Ul Hassan, R. Karhu, M. Ghezellou, L. Lilja, E. Janzén

Wafer scale on-axis homoepitaxial growth of 4H-SiC(0001) for high power devices: Comparison of different growth chemistries and growth rate limitations

Submitted

Paper 2

R. Karhu, E. Ö. Sveinbjörnsson, B. Magnusson, I. G. Ivanov, Ö. Danielsson, J. Ul Hassan

CVD growth and properties of on-axis vanadium doped semi-insulating 4H-SiC epilayers

Accepted: Journal of Applied Physics to be published in 2019

Paper 3

R. Karhu, J. Ul Hassan

Control of the growth mechanism and surface morphology of 4H-SiC on-axis homoepitaxial layers

Manuscript

Paper 4

R. Karhu, B. Lundqvist, J. T. Chen, E. Ö. Sveinbjörnsson, B. Magnusson, I. G. Ivanov, O. Kordina, Ö. Danielsson, J. Ul Hassan

Isotopically enriched semi-insulating on-axis 4H-SiC(0001) epilayers: Substrates for III-nitrides based HEMT structure

Manuscript

Paper 5

R. Karhu, I. D. Booker, J. Ul Hassan, I. G. Ivanov, E. Janzén

The role of chlorine during high growth rate epitaxy

Materials Science Forum 821 (2015) 141-144.

Paper 6

R. Karhu, I. D. Booker, I. G. Ivanov, E. Janzén, J. Ul Hassan

Long charge carrier lifetime in as-grown 4H-SiC epilayer

Materials Science Forum 858 (2016) 125-128.

Paper 7

R. Karhu, I. Kamata, M. Ghezellou, J. Ul Hassan

The origin and formation mechanism of an inclined line-like surface morphological defect in 4H-SiC epilayer

Manuscript

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PART 1: INTRODUCTION TO THE FIELD

1. INTRODUCTION

Silicon Carbide (SiC) first attracted interest due to its hardness and is to this day used as an abrasive material. In more recent years the attention has changed to the semiconducting properties of SiC. It is no understatement to say that the discovery of the semiconducting properties of Si has been one of the most important discoveries in the last century, with the discovery of the solid-state transistor and the continuous development of Si technology enabling great progress in microelectronics. But as the Si technology advances and the demand on the devices increase, the limitations of Si as a semiconductor become clear. This becomes especially clear in the case of high-power electronic applications. Researchers have searched for materials that could relieve some of the limitations of Si, so far with success only for niche applications. Some of the problems with other materials have included, difficulties to grow the material, inability to dope the material sufficiently, and so on. One of the materials that could replace Si in high power applications is SiC. This is due to its large bandgap, high electric breakdown field, and high thermal conductivity. SiC also stands out as one of few wide bandgap semiconductors that has successfully been doped, both n- and p-type in wide ranges. Even though the growth process of SiC is very involved and much of this text will discuss the problems that take place during SiC growth, today there exists large scale SiC wafers and epitaxial layers. At the moment of writing this text SiC substrates are commercially available in sizes up to 150 mm in diameter. The substrates can be bought both heavily n-type and semi-insulating, the epitaxial layers can be obtained in various thicknesses and with a wide range of doping, both n- and p-type. Due to the advances in SiC growth it is now possible to obtain commercial SiC electronic devices. SiC has also gained much interest as a substrate for the growth of epitaxial layers of III-nitrides, such as GaN and AlN.

Great progress has been made in both bulk and epitaxial growth, there is however still much work left to be done. A short description of the history of SiC growth will be presented below.

Silicon carbide is rare in nature. The history of SiC starts with a man named Jacob Jöns Berzelius (1779-1848), a Swedish chemist who was the first person to discover the bond between silicon and carbon [1]. The first natural occurrence of silicon carbide was discovered in a meteorite in Cañon Diablo, Arizona, by Henri Moissan (1852-1907). The mineralogical name for SiC is moissanite after Henri Moissan.

In an attempt to grow diamonds Edward Goodrich Acheson heated silica and carbon with some additives (salts and sawdust) in a crucible [2]. This process mainly produced powdered SiC that could be used as an abrasive material for grinding and polishing. As a by-product smaller single crystalline platelets of SiC formed. Although these platelets were not pure enough to be used for electrical applications, they were important for the early understandings of SiC. The furnace used in the Acheson process is a trough with a graphite core that has electrodes mounted at the ends [2]. The trough is filled with a mixture of silica, coke, salts and sawdust. The furnace is heated by passing a large current through the graphite core, to a temperature of 2000-2700 °C. This temperature is kept for a certain amount of time and then gradually reduced. The added sawdust is to keep the mixture porous, allowing for the reaction gases, such as carbon monoxide, to escape.

In an effort to produce high purity SiC Jan Anthony Lely developed a sublimation growth process in 1955 [3]. This development became the first step to investigate SiC as a semiconductor. The Lely method uses the fact that SiC sublimes at high temperature to grow high purity SiC crystals. The growth takes place in a cylindrical graphite crucible with the walls covered with SiC lumps, which could for example be grown using the Acheson process. The graphite crucible is placed in a resistively or inductively heated furnace. The temperature in the furnace is $\sim 2500^\circ\text{C}$ in a protective atmosphere, such as Ar. The crucible is designed so that the top of the crucible is colder than the SiC covered walls. This allows the dissociated species to condense on the colder parts and form SiC platelets. Some of the drawbacks with the Lely method is the lack of control of spontaneous nucleation and a continuous shift in concentration of dissociated species as the SiC source is depleted.

The SiC crystals produced by the Lely method although of high purity have been difficult to use in electronic applications. The main problem with using the crystals from the Lely method comes from the rather small and irregular shapes of the crystals. One of the breakthroughs was when Tairov and Tsvetkov introduced the seeded sublimation growth in 1978 [4]. The seeded sublimation method (sometimes called modified Lely) showed promise already in the first paper published where single polytype crystals ~ 1 cm in diameter were presented. Since the first paper published on seeded sublimation growth a lot of effort has been made to further develop this method [5-16]. The growth procedure is similar to the Lely method but the SiC source material is usually placed at the bottom of the crucible and the seed is placed at the top. The seed is kept at a temperature slightly lower than that of its surrounding.

Epitaxially grown layers are crucial for the fabrication of SiC electronic devices. In the epitaxially grown layers, it is possible to design both doping concentrations and thicknesses of the layers. 4H- and 6H-SiC have a big advantage in that there exist large scale commercially available native substrates. This makes it possible to grow homoepitaxial layers where the only contribution to lattice mismatch is the difference in doping and defect concentrations between the substrate and the epitaxial layer.

In 1987 Matsunami introduced the step-controlled epitaxy to SiC homoepitaxy, this allowed polytype replication from the substrate into the growing epitaxial layer [17, 18]. The step-controlled epitaxy uses substrates that have not been cut along crystal planes, but at a slight angle. This means that the surface normal will create a small angle with respect to the [0001]-direction, this angle is typically 4 or 8° . This creates steps on the surface of the substrates where the kinks of the steps offer unique nucleation sites to replicate the substrate's polytype. Substrates with the surface normal coinciding with the [0001]-direction are called on-axis substrates. If the surface normal is inclined with respect to the [0001]-direction, they are called off-axis substrates. A schematic image of the step structure can be seen in Figure 1. Homoepitaxial growth on off-axis substrates take place in a step-flow manner.

Figure 1: Schematic image of the stacking sequence and surface structure of 4H-SiC. a) on-axis, b) off-axis.

Several different methods can be used to grow epitaxial layers, but for SiC the most successful method has been chemical vapor deposition (CVD). CVD growth of SiC has been used since the 1980's and in 1995 the hot-wall reactor design was adopted [19]. The main advantage of the hot-wall CVD (HWCVD) reactor over its cold-wall reactor counterpart is the more uniform heating.

2. SILICON CARBIDE

2.1. CRYSTAL STRUCTURE

Silicon Carbide is a compound semiconductor with every Si atom being tetrahedrally bound to four C atoms, and every C atom is bound to four Si atoms. The ground state electron configuration for Si and C is:

$$\text{Si: } 1s^2 2s^2 2p^6 3s^2 3p^2$$

$$\text{C: } 1s^2 2s^2 2p^2$$

The Si-C bonds together in a mainly covalent bond by sharing sp^3 -hybrid orbitals. The bond length of Si-C is 1.89 Å and the bond is slightly ionic. Using Pauling's definition of ionicity the bond is 12 % ionic and 88 % covalent. The Si atom of the bond is slightly more positively charged compared to the C atom [2]. The two-atom basis of the SiC crystal makes it polar, with one side terminated by Si-atoms and one side terminated by C-atoms. Due to the slight ionicity of the Si-C bond the two different faces of the SiC crystal have some slightly different properties. The difference between the C-face and Si-face is often attributed to the difference in surface energy. Some of the properties that differ between the faces are polytype stability [8] and doping incorporation [20].

Figure 2: Hard sphere model of the close-packed crystal structure, the three non-equivalent sites are marked as A, B and C.

SiC is a well-known example of polytypism [21, 22]. Polytypism is the phenomenon where a material exists in several different crystal structures, without changing the chemical composition. In the case of SiC this takes place as different stacking sequences of the Si-C bilayers. Each Si-C bilayer has three sites that the bilayer can possibly occupy. The sites are commonly called A, B and C, a schematic of this can be seen in Figure 2. The stacking sequence for 3C-SiC is a repeated stacking in the order ABC. For 4H- and 6H-SiC the stacking sequence is ABCB and ABCACB, respectively. In Ramsdell's notation the different polytypes are characterized by a number and a letter, where the number represent the number of Si-C bilayers in the unit cell, and the letter represent the symmetry of the crystal, C for cubic, H for hexagonal and R for rhombohedral. At times the 3C-SiC polytype is called β -SiC, while all other polytypes are referred to as α -SiC. The polytypes that have attracted the most interest from

research communities have been 3C, 4H and 6H. Even though the different SiC polytypes are chemically the same, their properties vary quite a lot. The structures of some of the common polytypes can be found in Figure 3.

If the nearest neighbor surrounding of an atom is in a cubic structure, this site is called a cubic site (k). If the nearest neighbor surrounding is hexagonal, that site is called a hexagonal site (h). The hexagonality of a polytype is defined as the ratio of hexagonal sites to cubic sites in the polytype's unit cell, this is summarized in Table 1. The hexagonal and cubic sites have different second-nearest neighbors and thus different crystal fields. The different sites lead to different energy levels of dopants, impurities and point defects, this is called the site effect.

Figure 3: Schematic structure of some common SiC polytypes, 3C, 4H and 6H, with unit cell shaded in gray.

Table 1: Basic information about the SiC lattice for different polytypes [23].

Polytype (Ramsdell)	Stacking sequence	Lattice parameters		Hexagonality [%]	Atoms/unit cell
		a [Å]	c [Å]		
3C	ABC	4.359	—	0	6
2H	AB	3.076	5.048	100	4
4H	ABCB	3.073	10.053	50	8
6H	ABCACB	3.080	15.117	33	12
15R	ABCACBCABACBCB	3.079	37.78	40	30

2.2. PHYSICAL PROPERTIES

SiC is a wide bandgap semiconductor with several properties that makes it interesting for high voltage, high frequency and high temperature applications. The bandgap of SiC varies widely between the different polytypes as can be seen in Table 2. All SiC polytypes have indirect bandgap with their valence band maxima located at the Γ -point in the Brillouin zone. The conduction band minima vary with the different polytypes, with X -point for 3C, M -point for 4H and U -point (along the M - L line) for 6H-SiC.

Table 2: Physical properties of some of the most common SiC polytypes and comparisons to other common semiconductors [24-27]. v_{sat} is the electron saturation velocity. μ_e is the electron mobility perpendicular to the c -axis. E_B is the breakdown electric field from material doped to 10^{16} cm^{-3} .

Semiconductor	Bandgap [eV]	v_{sat} [10^7 cm/s]	μ_e [$\text{cm}^2/\text{V}\cdot\text{s}$]	E_B [10^6 V/cm]	Thermal cond. [$\text{W/cm}\cdot\text{K}$]
3C-SiC	2.36	2.0	1000	1.4	3.6 – 4.5
4H-SiC	3.26	2.2	1200	2.8	3.3 – 4.9
6H-SiC	3.02	2.0	380	3.0	4.5 – 4.9
GaN	3.39	2.5	900	3.3	1.3
Si	1.12	1.0	1350	0.3	1.3 – 1.5

The Si-C bond is relatively strong at 4.6 eV and the rather short bond length of 1.89 Å leads to a large energy difference between the bonding and anti-bonding states. This leads to a large bandgap and a high breakdown electric field compared to the smaller bandgap semiconductors, such as Si and GaAs. The large bandgap prevents electrons from being thermally excited from the valence band to the conduction band, leading to low leakage currents and high thermal stability in electrical devices.

SiC first attracted interest for its mechanical properties and was first commercialized as an abrasive material, SiC is one of the hardest known materials. On the Mohs scale of hardness where talc is given the value 1 and diamond 10, SiC has a hardness of 9.3 and Si has 7 [28].

The thermal conductivity of SiC is high, but promising results have been published on increasing the thermal conductivity of semiconductors such as Ge and Si by isotope enrichment [29, 30]. The presence of different isotopes in a material reduces the thermal conductivity. The reduction of the thermal conductivity is due to the difference in mass between the different isotopes acts as a scattering center for phonons. Calculations have been made to estimate the effects of the natural distribution of isotopes on the thermal conductivity compared to isotopically enriched material [31]. For SiC the estimated improvement in thermal conductivity of isotopically enriched SiC compared to natural SiC is 36% [31]. The abundance of the natural occurring isotopes of C and Si can be found in Table 3, and from this table it is clear that the most abundant isotopes are ^{12}C and ^{28}Si .

Table 3: Abundance of the natural occurring isotopes of C and Si [28].

Isotope	Abundance [%]
¹² C	98.93
¹³ C	1.07
²⁸ Si	92.22
²⁹ Si	4.69
³⁰ Si	3.09

2.3. DOPANTS

Doping of a semiconductor is to intentionally introduce defect states into the bandgap of the semiconductor. These defect states will allow for the generation and transport of carriers. For a group IV semiconductor, such as Si or SiC, the dopants are found in the two neighboring groups, group III and group V in the periodic table. The group III elements will have one electron too few to form the tetrahedral bonds and are called acceptors, while the group V elements have one electron too many for the tetrahedral bond and are called donors.

Controlled doping of semiconductors is a key for semiconductor device manufacturing and is one of the reasons for the success of SiC as a wide bandgap semiconductor. Doping of 4H-SiC has been demonstrated for a wide range of doping, both n- and p-type. In the n-type case N doping has been demonstrated in the range of at least $1 \cdot 10^{14} - 2 \cdot 10^{19} \text{ cm}^{-3}$, and in the p-type case Al doping in the range of $2 \cdot 10^{14} - 5 \cdot 10^{20} \text{ cm}^{-3}$ has been achieved.

Doping of SiC has been shown to be sensitive to the C/Si-ratio during growth. This doping dependence on C/Si-ratio has led to the so-called site competition theory [32, 33]. The site competition theory is based on dopants being substitutional defects in SiC, where for example, N occupies the C-site and Al occupies the Si-site. This leads to higher C/Si-ratios suppressing N incorporation. On the other hand, lower C/Si-ratio would suppress Al incorporation [32, 34].

Due to the low diffusivity of SiC the main technique for doping SiC is to introduce dopants during epitaxial growth. It is possible, and advances have been made to introduce local doping via ion implantation. Doping incorporation during epitaxial growth is performed by injecting dopant-containing gases into the reactor during growth. For doping with N this is done by injecting N₂ gas while Al-doping is commonly done by trimethylaluminum (TMA; Al(CH₃)₃). TMA is a liquid at room temperature and is injected via a bubbler system.

The two group III elements that have attracted attention as n-type dopants in 4H-SiC are N and P [33], with N being the most widely used donor. For the group V elements B, Ga and Al have been investigated, with most interest given to Al as a p-type dopant [35-37].

SiC doped with V or Fe shows semi-insulating properties [38, 39]. Of these two dopants V has been studied more extensively. V substitutes Si in the SiC lattice and acts as an amphoteric defect in 4H- and 6H-SiC; this means that the position of the Fermi level determines whether the defect acts as a donor or acceptor. Substitutional V possesses three charge states in 4H-SiC, V⁴⁺ (neutral), V³⁺ (negatively charged) and V⁵⁺ (positively charged). These three charge states enable two charge transition (deep) levels in 4H-SiC, V^{4+/3+} and V^{4+/5+}, which act as

acceptor and donor levels, respectively. The acceptor level is located at $E_C - 0.97$ eV [40, 41] and the donor level is located at $E_C - 1.57$ eV [42]. Bulk SiC material with high resistivity has been demonstrated [39], but rather high V-concentrations have been required to obtain the semi-insulating properties. This is due to the higher background doping obtained during bulk growth of SiC. This high V-concentration has shown to negatively affect device performance [43-45].

2.4. TRANSPORT PROPERTIES

The electron and hole mobilities for 4H- and 6H-SiC are often quoted as the maximum mobility. However, there are many parameters that strongly influence the electron and hole mobilities. This includes doping density and temperature, the mobilities are also anisotropic with the highest mobilities along the c-axis. There exist empirical models to describe the rather complex mobility behavior. One of these models is the Caughey-Thomas model expressed as:

$$\mu(T, N_{imp}) = \mu_{min} + \frac{\mu_{max}(T) - \mu_{min}}{1 + \left[\frac{N_{imp}}{N_{ref}(T)} \right]^{\gamma(T)'}}$$

where μ_{min} and $\mu_{max}(T)$ is the minimum and maximum mobility, respectively. N_{imp} is the impurity concentration that is affecting the mobility, $N_{ref}(T)$ is the reference concentration and $\gamma(T)$ is a fitting parameter. Some papers where a detailed investigation of mobilities has been published can be found in [46-52].

At sufficiently high electric fields the carrier's velocity becomes saturated. The saturation comes from carrier interactions with optical phonons. The saturation drift velocity approximately follows the expression:

$$v_{sat} = \sqrt{\frac{8\hbar\omega_{LO}}{3\pi m^*}}$$

where $\hbar\omega_{LO}$ is the energy of the longitudinal optical phonon and m^* is the effective mass of the carrier.

3. ELECTRONIC DEVICES

SiC has attracted interest as a semiconductor for high power and high-frequency applications. This is due to the large band gap, high thermal conductivity, high breakdown electric field strength and high saturation drift velocity of carriers. SiC also has very good properties for withstanding high temperatures and harsh ambient. The combination of these properties makes SiC an interesting semiconductor for a very wide variety of fields. These fields include power distribution, electric vehicles and sensor devices for corrosive gases.

Today commercial electronic devices made from SiC are available from several different manufacturers.

3.1. UNIPOLAR AND BIPOLAR DEVICES

Microelectronic devices can be grouped into two categories depending on if the current is mainly electrons (unipolar) or a combination of electrons and holes (bipolar). Different types of both unipolar and bipolar devices have been demonstrated in SiC.

3.2. METAL-SEMICONDUCTOR JUNCTION

To discuss the metal-semiconductor junction some quantities related to the electron energies need to be established. The work function of a metal, ϕ_m , is the energy that an electron must absorb in order to escape from the metal. ϕ_m is equal to the difference between the Fermi level, E_F , and the vacuum level (an electron at rest an infinite distance away from the surface). In the same manner the work function of a semiconductor, ϕ_s , can be defined as the difference between the Fermi level and the vacuum level. The electron affinity for the semiconductor, X , is the energy to remove an electron from the bottom of the conduction band, E_C , to the vacuum level. These quantities are defined in Figure 4 a).

Figure 4: Schematics of band diagrams for a metal and a semiconductor with $\phi_m > \phi_s$. a) Band diagram of metal and semiconductor spatially separated. b) Band diagram of metal and semiconductor fused together.

This example is limited to the case of n-type semiconductors. If a metal and a semiconductor with $\phi_m > \phi_s$ are put in contact electrons can move across the structure. Initially the Fermi level is higher in the semiconductor relative to the metal. To equalize the Fermi level across the structure, the Fermi level in the semiconductor will be lowered by diffusion of electrons to the metal. Near the metal-semiconductor junction a region depleted of electrons will form, called a depletion region, W . The positively charged donors will be left in the depletion region creating an electric field with the high concentration of negatively charged electrons in the metal. This electric field will reach its equilibrium contact potential, $V_0 = \phi_m - \phi_s$, preventing further electrons to diffuse to the metal. The potential barrier height, $\phi_B = \phi_m - X$, for electrons to be injected from the metal into the semiconductor is marked in Figure 4 b). The equilibrium contact potential, V_0 , can be manipulated by external electric fields. By applying a positive bias to the metal and a negative bias to the semiconductor the potential barrier is reduced, and this is called forward biased. Reversing the polarity of the applied bias result is an increased potential barrier, and this is called reversed bias. A schematic view of both the forward and reverse bias cases can be seen in Figure 5. The barriers dependence on the polarity of the applied bias leads to nonlinear current vs. voltage (I-V) behavior (Figure 6) of this metal-semiconductor junction. Metal-semiconductor junctions with nonlinear I-V behavior is commonly called Schottky barrier diodes.

Figure 5: Schematic band diagram of a metal-semiconductor junction. a) Forward biased junction. b) Reversed biased junction.

Figure 6: Schematic I-V characteristic of a metal-semiconductor junction.

Another case that can be observed in metal-semiconductor junctions is that $\phi_m < \phi_s$. This example will also be limited to the case of n-type semiconductors. This case will result in a linear I-V behavior due to the barrier being formed between the metal and the semiconductor in this case, these contacts are called Ohmic contacts. It is however rare to find this combination of metal and semiconductor and practically Ohmic contacts are usually produced by placing the contacts on heavily doped regions of the semiconductor.

Metal contacts are very important for electrical devices, and to be able to fabricate useful devices both Schottky and Ohmic contacts are needed. It is also desirable to be able to form both Schottky and Ohmic contacts on both n- and p-type semiconductors. For ideal semiconductors the height of the Schottky barrier would only depend on the work function of the deposited metal. However, for real semiconductors it has been shown that surface states play a very important role in determining the barrier height [53]. Many metals form Schottky contacts on SiC, a detailed review can be found in reference [54]. The formation process of Ohmic contacts on SiC is more involved. For n-type 4H-SiC the common metal to use for Ohmic contacts is Ni annealed at 950 °C, this process forms Ni₂Si that acts as an Ohmic contact [55, 56]. It has been proposed that the formation of the Ni₂Si is not enough to form Ohmic contacts

on n-type 4H-SiC. Reports have been made that carbon vacancies formed during the silicidation play an important role in the formation of Ohmic contacts [57]. On p-type SiC Ohmic contacts are often made from an Al/Ti layered system and annealed at 1000 °C [58]. It has later been suggested that the Ohmic nature of these contacts come from alloying of Ti_3SiC_2 and Al_4C_3 at the contact-semiconductor interface [59].

3.3. UNIPOLAR ELECTRONIC DEVICES

Unipolar devices only inject majority carriers into the active region of the device. Majority carriers are electrons for n-type semiconductors and holes for p-type semiconductors.

A couple of different types of unipolar devices have become very successful and are today commercially available. The most successful kind of devices has been the Schottky barrier diode (SBD) and the metal oxide semiconductor field effect transistor (MOSFET).

3.3.1. SCHOTTKY BARRIER DIODES

SBDs are unipolar device that utilize the metal-semiconductor junction for rectification. The forward current in SBDs consists of majority carriers being injected into the metal from the semiconductor. What makes SBDs attractive to fabricate on SiC is the high breakdown electric field, wide bandgap and high thermal conductivity. The high breakdown electric field leads to larger reverse bias blocking. The wide bandgap together with the high thermal conductivity makes high-temperature operation of SBDs more efficient. The SBD is a two-terminal device with the I-V characteristics of a metal-semiconductor junction shown schematically in Figure 6. SiC SBDs have been studied thoroughly and some studies can be found in [60-62].

3.3.2. METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTORS

One of the greatest successes of Si is the ease of forming and the thermal stability of SiO_2 , this oxide makes it possible to fabricate metal-oxide-semiconductor (MOS) devices. SiC is the only wide bandgap semiconductor that can form SiO_2 through oxidation. During the oxidation of SiC both SiO_2 and CO will form creating charged traps in the interface between the SiO_2 and SiC. The traps detected at the interface have mostly been assigned to oxygen vacancies within the oxide and carbon-related defects at the interface [63]. These charged traps have a negative influence on the MOS channel mobility [63]. Reports have shown that the charged traps can be neutralized to some extent using annealing at high temperatures in nitric oxide [64-66]. The possibility of forming an oxide of high quality, such as SiO_2 , on SiC allows the fabrication of MOS devices also on SiC.

MOS field effect transistors (MOSFET) are three-terminal devices where the current through two terminals (Source, Drain) is controlled by the third terminal (Gate). The gate electrode is placed on the SiO_2 . The source and drain contacts are placed on highly doped regions of opposite polarity of the body of the MOSFET structure. In Figure 7 these are the n^+ regions of the p-type body. If sufficient gate voltage is applied a channel will open up between the source and drain, allowing a current to pass between these electrodes.

Figure 7: Schematic drawing of a MOSFET structure.

3.4. BIPOLAR DEVICES

Bipolar devices inject both majority and minority carriers into the active region of the device. Minority carriers are holes for n-type semiconductors and electrons for p-type semiconductors. Bipolar devices have been demonstrated on SiC but if the device contains a common structural defect (basal plane dislocation) the device will rapidly degrade [67-70].

3.4.1. PIN DIODES

A PiN-diode is a pn-junction where an intrinsic layer (i) has been sandwiched in between. A schematic drawing of a PiN diode can be seen in Figure 8. In real devices the i-layer is not in fact intrinsic but consist of a low doped n^- layer. The addition of the i-layer increases the blocking voltage of the device, but the physical thickness of the i-layer makes it possible for electrons and holes to recombine before completing the travel across this layer. This puts requirements on the minority carrier lifetime to be sufficiently long to achieve conductivity modulation. The drawback with long charge carrier lifetimes is that the switching speed of the device will be limited by the recombination time.

Figure 8: Schematic drawing of a PiN diode structure.

4. GROWTH

There exists no stoichiometric liquid phase of SiC at process relevant temperatures and pressures. This makes it hard to grow SiC from smelt at process relevant pressures. Instead of forming a stoichiometric liquid SiC sublimes at very high temperatures, above 1800-2000 °C. The problem that arises when growth must be made from sublimed species instead of from melt is that the growth takes place at temperatures that are further away from thermal equilibrium. Growth from a seed that is closer to thermal equilibrium with its surrounding allows for adatoms to be reemitted from the seed. This can prevent defects from forming during growth and lowers the number of structural defects in the final crystal. Since bulk SiC crystals must be grown via sublimation methods the SiC bulk material still suffers from a high number of structural defects.

The formation of a crystal is a phase transformation into the solid phase from a solid, liquid or vapor phase. The case with a transformation from a solid state is usually a slow process and not often practical. One such case is diffusion from one crystal to another crystal. The other two cases namely liquid or vapor phase transforming into a solid phase are very common in semiconductor manufacturing. The driving force for the formation of a crystal is the supersaturation, which is defined as:

$$\Delta\mu = \mu_m - \mu_c$$

where μ_m is the chemical potential for the medium (melt, vapor, solution) and μ_c is the chemical potential of the crystalline phase. If $\Delta\mu > 0$ the medium is said to be supersaturated and growth can take place. Whereas if $\Delta\mu < 0$ the medium is undersaturated and dissolution will take place.

Crystal growth preferentially takes place around steps on the surface of the crystal or around dislocations. A detailed description of the theory of growth is detailed in the paper by Burton, Carberera and Frank (so called BCF theory) [71]. The first to adopt and modify this theory for the hexagonal SiC polytypes were Kimoto and Matsunami in [72]. Below follows a brief summary of the theory.

Considering a surface with steps of height h separated by a terrace of length λ as is shown in Figure 9. To this surface there will be a flux of adsorbed and desorbed adatoms. The adatoms can diffuse on the surface and if the adatom diffuse to a step the adatom can be incorporated into the crystal. For high supersaturations the adatoms can coalesce and form a nucleus on a terrace, a schematic illustration can be found in Figure 9. If the nucleation on terraces are neglected the continuity equation for the adatoms can be expressed as [71]:

$$-D_s \frac{d^2 n_s(y)}{dy^2} = J - \frac{n_s(y)}{\tau_s}$$

where $n_s(y)$ is the number of adatoms per unit area on the surface, J is the flux of adsorbed adatoms, τ_s is the mean residence time of adatoms on the surface and D_s is the diffusion coefficient. In this differential equation the incoming flux of adatoms is set equal to the diffusion flux towards steps. A solution to this differential equation can be written as:

$$n_s(y) = J\tau_s + (n_{s0} - J\tau_s) \frac{\cosh(y/\lambda_s)}{\cosh(\lambda/2\lambda_s)},$$

where λ_s is the diffusion length for adatoms along the surface, n_{s0} is the equilibrium adatom concentration.

The adatom surface diffusion length can be expressed using the Einstein relationship as:

$$\lambda_s = \sqrt{D_s\tau_s} = a \exp\left(\frac{E_{des} - E_{diff}}{2k_B T}\right),$$

where a is the jump distance of adatoms, E_{des} , E_{diff} are the activation energies for desorption and surface diffusion, respectively. The flow of adatoms along the y -direction (as defined in Figure 9) can be expressed as:

$$J_s(y) = -D_s \frac{dn_s(y)}{dy} = \lambda_s \left(J - \frac{n_{s0}}{\tau_s} \right) \frac{\sinh(y/\lambda_s)}{\cosh(\lambda/2\lambda_s)}.$$

Coming back to the initial assumption that the steps act as perfect sinks for adatoms, it is possible to express the step velocity, v_{step} , as:

$$v_{step} = 2 \frac{J_s(y)}{n_0} \Big|_{y=\lambda/2} = \frac{2\lambda_s}{n_0} \left(J - \frac{n_{s0}}{\tau_s} \right) \tanh\left(\frac{\lambda}{2\lambda_s}\right),$$

where n_0 is the surface density of adatom sites. Both adatoms arriving to the step from left and right are considered. The growth rate is estimated as the product of the step velocity and $\tan \theta$, where $\theta = h/\lambda$ is the off-angle of the substrate. The final expression for the growth rate then becomes:

$$R = \frac{2h\lambda_s}{n_0\lambda} \left(J - \frac{n_{s0}}{\tau_s} \right) \tanh\left(\frac{\lambda}{2\lambda_s}\right).$$

Figure 9: Schematic representation of the different processes taking place at a surface.

4.1. CHEMICAL VAPOR DEPOSITION

Chemical vapor deposition (CVD) is the most commonly used method for growing epitaxial layers of 4H-SiC. In CVD growth the precursors are supplied in gaseous form to the growth zone where they react with the substrate to form the desired material. The CVD growth equipment is frequently called a reactor since growth takes place from chemical reactions. A reactor is typically a quartz tube with one end connected to a gas mixing system and one end to a pump system. A susceptor with substrates is placed in the quartz tube and is inductively or resistively heated. The basic principle of a CVD reactor is rather simple, but a lot of engineering is needed to make a good CVD reactor. A schematic drawing of the cross-section of a hot-wall CVD (HWCVD) reactor can be seen in Figure 10. In the following section some aspects of CVD growth will be considered. The HWCVD reactor design is commonly used for epitaxial growth of 4H-SiC due to more homogeneous thermal distribution across the substrate. HWCVD was introduced to epitaxial growth of SiC in 1995 [19].

Figure 10: Schematic illustration of a HWCVD reactor.

In order to have control of growth in the reactor, changes in the gas flow into the reactor need to correspond to changes in the ambient inside the reactor. This can be achieved by having a laminar flow through the reactor, laminar flows are usually characterized by the Reynolds number:

$$Re = \frac{d u \rho}{\mu},$$

where d is the diameter of the tube, u the velocity of the gas, ρ is the density of the gas and μ is the gas viscosity. The Reynolds number can be used to estimate if flows will be laminar or turbulent. When gas is dragged against a surface the gas slows down to some degree. This creates a region in the vicinity of the susceptor walls where the gases move with a much lower velocity. This region is called the boundary layer and the thickness of this layer can be estimated by:

$$\delta \sim \sqrt{\frac{\mu x}{\rho U_{\infty}}},$$

where δ is the boundary layer thickness, x is the distance along the surface and U_{∞} is the gas bulk velocity [73]. A schematic drawing of the boundary layer at a flat surface is shown in Figure 11. The gas phase reactants that manages to diffuse through the boundary layer are able to contribute to the growth of the epilayer.

Figure 11: Schematic figure of the boundary layer at a flat surface.

The growth rate of CVD growth can in general be divided into three growth rate limiting regimes dependent on the growth temperature, as illustrated in Figure 12. At low temperatures the growth rate is limited by the slowest reaction taking place in the gas phase or at the surface. Since at these temperatures the growth rate is limited by reaction kinetics it is possible to increase the growth rate by increasing the growth temperature. At a certain temperature the growth rate will no longer be limited by reaction kinetics but will instead start to be limited by the mass transport through the boundary layer. In this regime the growth rate is rather independent of the growth temperature and the growth rate is controlled by the partial pressures of the precursors. This is the regime where CVD reactors are normally operated. At even higher temperatures the growth rate starts to decrease with increasing temperature. At these temperatures the growth rate starts to be limited by thermodynamic processes. These processes can be parasitic reactions in the gas phase, parasitic deposition on susceptor parts and increased desorption from the growing epitaxial layer [74].

Figure 12: Growth limiting regimes dependence on growth temperature.

The method most widely used to maintain polytype stability during homoepitaxy of 4H- and 6H-SiC is to use off-cut substrates. These are substrates cut at an angle so that the surface normal creates an angle with the c-axis, typically 4 or 8°. The cutting is typically done towards the $[11\bar{2}0]$ direction since the $(11\bar{2}0)$ planes have the highest density of atoms. This off-cut leaves the surface of the substrate with a high density of micro-steps that can be used for replication of the substrate's polytype into the growing epilayer in a step-flow manner. The concept of step-flow growth was introduced for SiC by Matsunami [17]. The standard CVD process for homoepitaxial growth is typically performed in the temperature range of 1500-1650 °C using the precursors silane (SiH_4) and a hydrocarbon, typically ethylene (C_2H_4), propane (C_3H_8) or butane (C_4H_{10}). The carrier gas used to dilute the precursors is hydrogen (H_2) or a combination of hydrogen and argon.

4.2. CHLORINATED GROWTH

Using the standard precursors (silane together with a hydrocarbon) limit the growth rate to about 20 $\mu\text{m/h}$. The limitation of the growth rates stems from Si gas phase nucleation at high Si/H₂ ratios. Adding Cl to the gas phase is suppressing the gas phase nucleation of Si. The first attempts at chlorinated SiC growth were for bulk growth of 6H-SiC [75]. The idea of added Cl to the growth was rapidly adopted to CVD growth of SiC epitaxial growth [76, 77]. Using the chlorinated CVD process growth rates of over 100 $\mu\text{m/h}$ have been achieved. Chlorine can be added to the growth process in several different ways. The most common is to either use trichlorosilane (TCS; SiHCl₃) as the Si precursor or to add HCl to the standard growth process. Several other precursor systems containing Cl have been investigated, such as chlorinated C precursors and using a single precursor containing Si, C and Cl [78, 79]. A detailed review of many of the different chlorinated precursors can be found in reference [80].

4.3. ON-AXIS HOMOEPITAXY

One way to avoid the replication of BPDs into the growing epitaxial layer during homoepitaxial growth is to grow on on-axis substrates [81]. However, on-axis substrates lead back to the problem of polytype stability. Homoepitaxial layers grown on on-axis substrates usually have several 3C-SiC domains present in the epitaxial layer [82-84]. Homoepitaxial layers of 4H-SiC without 3C-inclusions have been successfully grown on both the C- and Si-face of 4H-SiC [81, 85]. On-axis homoepitaxy was demonstrated on the C-face earlier than the Si-face due to the higher polytype stability for 4H-SiC on the C-face [8], but the C-face suffers from high incorporation of background doping such as N [20]. Today all device fabrication on 4H-SiC is performed on the Si-face making the development of on-axis homoepitaxy on the Si-face desirable.

To perform on-axis homoepitaxy of 4H-SiC on the Si-face the initial stage of the growth is very important, since the substrates as received from the vendor have a very low density of micro-steps at the surface. The in-situ surface preparation step is crucial to obtain a suitable step-structure on the surface to allow polytype replication from the substrate into the epitaxial layer [81, 86]. It has previously been reported that in-situ surface preparation with a slight addition of silane can create suitable surfaces for homoepitaxial growth [86]. In paper 1 of this thesis the starting conditions for on-axis homoepitaxy of 4H-SiC on Si-face are further explored. In this paper susceptor design, precursors and history of the growth cell is being considered and concluded that all these parameters affect the effective C/Si-ratio in the growth cell and must be considered when choosing the starting conditions. In paper 1 on-axis homoepitaxial growth on 100 mm diameter wafer is demonstrated with no 3C-inclusions excluding the wafer edge. The growth on on-axis substrates takes place as a mixture of step-flow growth and spiral growth, where the step-flow part originates from unintentional steps on the surface from the cutting and polishing of the substrate and the spiral part originate from TSDs intersecting the surface [81]. The mixture of growth modes makes the final surface of the homoepitaxial layer rough. On a 100 μm thick epitaxial layer the surface roughness can be on the order of 5-6 μm . In paper 3 in this thesis the problem with the surface roughness is addressed and a process to significantly reduce the surface roughness of as-grown

homoepitaxial layers are demonstrated. In this paper the surface is transformed from a mainly valley and hillock morphology to a surface covered in large macro-steps. This change in surface morphology is achieved by prolonging the in-situ surface preparation step from 10 minutes to 20 minutes.

5. DEFECTS

5.1. POINT DEFECTS

Point defects are defects created by a single atom. This atom can occupy a lattice site of the crystal and is then called a substitutional defect. It can also be found at a non-lattice site in the crystal, in this case it is an interstitial defect. Both the substitutional and interstitial point defects can be intrinsic or extrinsic atoms. If the defect is intrinsic the defective atom is native to the crystal. If the atom is foreign to the crystal the defect is called extrinsic. If a lattice site is not occupied by an atom this defect is called a vacancy.

Atoms can also occupy the non-equilibrium sites. This can for example be an atom of species A occupying the lattice site of atom species B in a two-atom crystal system. This defect is called anti-site and can occur for both intrinsic and extrinsic atoms.

Point defects can create energy levels inside the SiC bandgap. The most common deep levels in n-type 4H-SiC are $Z_{1/2}$ and $EH_{6/7}$ [87-89]. The $Z_{1/2}$ and $EH_{6/7}$ have shown to originate from the carbon vacancy [90-92]. The two deep levels of $Z_{1/2}$ have been shown to originate from the two different charge states of the carbon monovacancy [92, 93]. $Z_{1/2}$ has been identified as a lifetime killer defect [40]. The $Z_{1/2}$ deep levels are located at $E_C - 60$ eV and $EH_{6/7}$ are located at $E_C - 1.55$ eV [40, 87]. The charge carrier lifetime can be controlled by controlling the concentration of $Z_{1/2}$ deep levels. Since the $Z_{1/2}$ deep levels are related to carbon vacancies the concentration is dependent on C/Si-ratio and temperature during growth [94, 95].

5.2. STRUCTURAL DEFECTS

To describe structural defects the Burgers circuit is often used. A Burgers circuit is an atom-to-atom path drawn in an area of the crystal containing a dislocation and forms a closed loop. This loop is then compared to an identical loop drawn in a dislocation-free part of the crystal. The loop drawn in the dislocation free part of the crystal will not be a closed loop. The vector required to finish the loop is called the Burgers vector, this vector is commonly used to describe dislocations. For edge dislocation the dislocation line is orthogonal to the Burgers vector and for a screw dislocation the dislocation line is parallel to the Burgers vector. Schematic drawings of the Burgers circuits can be seen in Figure 13 and Figure 14 for the edge and screw dislocation, respectively. A dislocation can change its line direction, this can however only happen if the Burgers vector is conserved. It is also impossible for a dislocation to terminate within a crystal, dislocation termination can only happen at crystal surfaces.

Dislocations can easily move inside of a crystal under applied shear stress. The movement of dislocations can take place as one of two different ways: Conservative movement (Glide) when the dislocation moves in the surface which contains both the line and Burgers vector. Non-conservative (Climb) which is when the dislocation moves out of the glide surface (normal to the Burgers vector). The glide of dislocations often results in a slip, which is a common plastic

deformation in crystals. A slip system consists of a slip plane and a slip direction. The slip planes are normally the planes with the highest density of atoms and the slip direction is the direction with the shortest lattice translation vector. In the case of hexagonal close-packed (hcp) crystal systems, such as 4H- and 6H-SiC, the slip plane is the $\{0001\}$ basal plane and the slip direction $\langle 11\bar{2}0 \rangle$. The shortest translational vector in the hcp system is $\frac{1}{3} \langle 11\bar{2}0 \rangle$. At high temperatures dislocations can move by climb, however, climb leaves a trail of point defects in the crystal.

Figure 13: Schematic drawing of Burgers circuits for an edge dislocation. a) Burgers circuit containing an edge dislocation. b) Burgers circuit in a defect-free area. This image is adopted from [96].

Figure 14: Schematic drawing of Burgers circuits for a screw dislocation. a) Burgers circuit containing a screw dislocation. b) Burgers circuit in a defect-free area. This image is adopted from [96].

In 4H-SiC dislocations are very common with some of the most common being the threading edge dislocation (TED), threading screw dislocation (TSD) and the basal plane dislocation (BPD). TSDs have a Burgers vector nc , where c is the lattice parameter and n is an integer. If n is sufficiently large a hollowed-core super-screw dislocation, called a micropipe, will form. The first prediction of hollowed-core screw dislocations was done by Frank [97], the radius of the micropipe is expressed by:

$$r = \frac{\mu |\mathbf{b}|^2}{8\pi^2 \gamma}$$

where μ is the shear modulus and γ is the specific surface energy. This theory put forward by Frank was later shown to agree well with the micropipes in 6H-SiC and 4H-SiC [98, 99]. For 6H-SiC micropipes have a Burgers vector $|\mathbf{b}| \geq 2c$, and for 4H-SiC the Burgers vector is $|\mathbf{b}| \geq 3c$ [99, 100]. The micropipe creates a pinhole in the crystal. Devices located close to micropipes show severely degraded device characteristics [101].

TSD is replicated from the seed crystal into the growing boule and will also replicate into epilayers during homoepitaxial growth. The Burgers vector of TSDs are $\mathbf{b} = nc$, just as for the micropipes discussed previously. The difference is that the integer, n , is under the critical limit for the formation of micropipes. TSDs can also form in pairs during growth of a SiC boule, the Burgers vectors of the two TSDs will be $\mathbf{b} = +c$ and $\mathbf{b} = -c$. These pairs of dislocations have been shown to nucleate at inclusions in the boule [102, 103].

TED and BPD have the same Burgers vector of $\mathbf{a}(<11\bar{2}0>/3)$. The TED and BPD thus have the same origin, the only difference is whether the dislocation extends in the (0001) basal plane (BPD) or along the c-axis (TED). Conversion between TED and BPD is commonly observed [104, 105]. This conversion is in fact one of the major benefits of SiC homoepitaxy, where the conversion rate of BPD to TED can be very high [106, 107]. This is important for device fabrication since the BPD has been shown to degrade bipolar devices during forward biasing [67, 68]. This degradation can thus be mitigated by conversion of BPDs to TEDs during homoepitaxial growth.

A common way to observe dislocations in SiC is to etch the sample in molten KOH. The preferential etching around the dislocations is visible in an optical microscope. The different types of dislocations have characteristically different shapes. TEDs show a small hexagonal etch pit, TSDs show a much larger hexagonal etch pit and BPDs intersect the surface at an angle due to the substrate off-cut, this can be seen in Figure 15.

Figure 15: Optical microscopy image of a 4H-SiC sample etched in molten KOH. The image indicates a BPD, TED and a TSD.

Stacking faults are as the name implies a fault in the stacking sequence of the polytype. Due to the low stacking fault formation energy of SiC stacking faults are common [108]. In heavily N doped 4H-SiC the formation of the so-called double Shockley stacking fault can form during oxidation or annealing in Ar atmosphere at temperatures higher than 1000 °C [109-114].

6. CHARACTERIZATION

Characterization of grown epitaxial layers has been used to establish a feedback loop for further growth experiments. In this chapter a short introduction to the characterization methods used for feedback is presented.

6.1. SURFACE ANALYSIS

6.1.1. OPTICAL MICROSCOPY

Optical microscopy with Nomarski differential interference contrast is a valuable tool for studying as-grown epitaxial layers. Irregularities of the as-grown surface and morphological defects can be easily observed in an optical microscope. If the sample is etched in KOH it is also possible to observe dislocations in the microscope.

Nomarski differential interference contrast is a technique used in optical microscopes to enhance contrasts in unstained, transparent samples. The technique works by spatially separating polarized light into two orthogonal components. This is done by inserting a so-called Nomarski prism in the beam path of the optical microscope. These two light beams will interfere with the sample. On the way back to the eyepiece the beams will merge together and form the image. The contrast in the image comes from differences in lengths of optical path between the two beams. This makes it possible to see even small irregularities of the sample surface.

6.1.2. ATOMIC FORCE MICROSCOPY

Atomic force microscopy (AFM) is a technique that can measure atomic scale irregularities of a surface in standard atmosphere. Since AFM is a very sensitive method it is important to use properly cleaned samples but otherwise no special sample preparation is required.

AFM is a technique in the scanning probe microscopy (SPM) family, these techniques are mainly used for careful studies of surfaces. The common part for all SPM techniques is that a probe with a very pointy tip is scanned across the surface, this generates a signal that can be made into an image. For AFM the signal is composed of the atomic force between the tip and the surface.

In AFM the tip is placed at the end of a cantilever, a laser beam is focused on the end of the cantilever as well. When the cantilever is being deflected the reflected laser beam will also be deflected. This deflection of the reflected laser beam is being detected and recorded as the signal, as seen in Figure 16. The deflection of the cantilever is caused by the forces acting between the sharp tip and the surface of the measured sample. This force can be described by Hooke's law as:

$$F = -kx$$

where k is the spring constant of the cantilever and x is the deflection of the cantilever. The dominant contribution to the force between the tip and the surface is the van der Waals interaction.

An AFM can be operated in several different modes such as non-contact mode, contact mode and tapping mode. For SiC samples the most frequently used mode is the tapping mode, where the cantilever is set to oscillate around its equilibrium position gently tapping the surface. By maintaining a constant amplitude of the oscillations, the forces between the surface and the tip can be detected to form an image of the sample surface.

Figure 16: Schematic illustration of an AFM.

6.2. OPTICAL ANALYSIS

Photoluminescence (PL) is the light emitted from the recombination of electron-hole pairs or the relaxation of electrons. For this process to take place excitation of electrons (holes) is required, this is usually done via laser excitation. There exist several different PL techniques and, in this chapter, low-temperature PL (LTPL) and time-resolved PL (TRPL) will be discussed.

6.2.1. LOW-TEMPERATURE PHOTOLUMINESCENCE (LTPL)

Low-temperature photoluminescence is much as the name implies a PL technique that is performed at low temperatures. The low temperatures are often obtained by submerging the sample in liquid helium, so the temperatures are in the range of 4 K or below. LTPL is a contactless method that can give a lot of information about the sample.

Electron-hole pairs can be created in a semiconductor by illumination with photons with energy, $\hbar\omega > E_g$, where $\hbar$ is the reduced Planck's constant, ω is the photon frequency and E_g is the band gap energy. The excess electrons and holes created will recombine, some of the recombination processes will be radiative, these are the processes of interest for PL studies. There exist recombination processes where the energy is transferred to phonons instead of photons, these processes are called non-radiative.

The most straight forward recombination process is the band-to-band recombination where an electron at the bottom of the conduction band will recombine with a hole at the top of the valence band. The emitted photon will have the energy, $E_{photo} = E_g$, this process is however very unlikely to happen in 4H-SiC due to the indirect band gap.

Radiative recombination can take place between neutral donors and acceptors. The donor-acceptor pair is spatially separated, and the emitted photon energy will be a function of this distance. The photon energy can be described as:

$$\hbar\omega = E_g - E_D^b - E_A^b + \frac{e^2}{4\pi\epsilon_0\epsilon_r R}$$

where e is the electron charge, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the semiconductor, R is the spatial distance between the donor and acceptor, E_D^b and E_A^b is the binding energy of the donor and acceptor, respectively. Since R can only have discrete values the donor-acceptor pairs result in a series of photon energies.

At low temperatures a likely recombination process is free and bound excitons. An exciton is a state formed by Coulomb interaction between an electron and a hole. Excitons are hydrogen-like quasi-particles that can recombine radiatively.

In materials with small dielectric constants the Coulomb interaction between the electron and hole can be rather strong. The strong binding between the electron and hole leads to a small spatial confinement of the exciton, on the same order of size as the unit cell. These excitons are called Frenkel excitons. For the case of semiconductors that usually have rather large dielectric constant the so-called Wannier-Mott exciton is more common. In the Wannier-Mott excitons the binding energy is weaker and results in a larger size (several unit cells) of these excitons compared to the Frenkel excitons.

Free excitons are excitons that are not spatially bound to any defect and can freely move around in the lattice. Bound excitons on the other hand are excitons that are bound via Coulomb interaction to a charged defect. Some common types of bound excitons are the donor-bound exciton and the acceptor-bound exciton. The recombination energy for a free exciton can be described as:

$$\hbar\omega = E_g - E_{FE} - E_{Phono}$$

where E_{FE} is the energy of the free exciton and E_{Phono} is the phonon energy. In the case of bound excitons, the expression is very similar and can be expressed as:

$$\hbar\omega = E_g - E_{FE} - E_{BE} - E_{Phono}$$

where E_{BE} is the binding energy of the bound exciton to the impurity.

SiC is a good example of free and bound excitons. In Figure 17 a LTPL spectrum from a nitrogen doped 4H-SiC sample is presented. The spectrum is recorded at a temperature of 2 K using an excitation source with 351 nm wavelength. In this figure the free excitons are denoted with I_x , the nitrogen bound excitons have been denoted with P_x and Q_x for the hexagonal and cubic site, respectively. The 'x' subscript is used to denote different phonon replicas of the emission line. The 'x' is the approximate energy in meV of involved phonon.

Figure 17: LTPL spectra recorded from a 4H-SiC sample doped with nitrogen. The spectrum is recorded at a temperature of 2 K and with an excitation source with 351 nm wavelength.

Methods for accurately estimating the nitrogen doping concentration in 4H- and 6H-SiC using LTPL spectrums have been developed [115, 116]. The nitrogen concentration can be estimated in the range of $10^{14} \text{ cm}^{-3} - 3 \cdot 10^{16} \text{ cm}^{-3}$ for 4H-SiC and $10^{14} \text{ cm}^{-3} - 10^{17} \text{ cm}^{-3}$ in 6H-SiC. The methods require no contacts and no other sample preparation prior to measurements. These methods use the ratio of the intensities of a nitrogen-bound exciton and the free exciton. The bound and free excitons used for 4H-SiC is the bound exciton zero-phonon line, Q_0 , and the most intensive free exciton phonon line, I_{77} . For 6H-SiC the ratio is calculated from the bound exciton zero-phonon line, R_0 and S_0 , and the most intensive free exciton phonon replica I_{77} .

6.2.2. TIME-RESOLVED PHOTOLUMINESCENCE (TRPL)

In TRPL the near band edge luminescence decay is recorded after a short optical injection pulse. The PL peak intensity is proportional to the excess carrier densities, $\Delta n, \Delta p$, and can be expressed as:

$$I_{PL}(t) = C(n + \Delta n(t))(p + \Delta p(t))$$

where C is a constant and n, p are the equilibrium carrier concentrations. TRPL measurements are usually performed under low-injection conditions, this means that the excess carrier concentration is lower than the equilibrium value. When working with n-type material, this allows us to neglect the $\Delta n(t)$ term.

Several different recombination mechanisms can take place in a semiconductor. In Figure 18 a schematic of some of the common recombination processes are presented. The SRH recombination process was introduced by Shockley, Read and Hall in 1952 [117, 118]. SRH recombination is the electron-hole pair recombination through a recombination center, E_r . Auger recombination requires three carriers, of which two recombine transferring the released energy to the third carrier. This makes Auger recombination unlikely to take place during low concentrations of carriers. Radiative recombination is the direct recombination of

an electron and a hole resulting in the emission of a photon. Direct recombination is rare in SiC due to its indirect bandgap.

Figure 18: A schematic illustration of radiative, Auger and SRH recombination processes.

From the decay curves it is possible to extract the measured lifetime, $\tau_{measured}$, which is the sum of all recombination processes in the semiconductor. The measured lifetime can be expressed as:

$$\frac{1}{\tau_{measured}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{rad}}$$

where τ_{SRH} is the Shockley-Read-Hall (SRH) recombination lifetime, τ_{Auger} is the Auger recombination lifetime and τ_{rad} is the radiative recombination lifetime. Since 4H-SiC is an indirect semiconductor radiative recombination processes are typically not a limiting factor for the excess carrier lifetime. The TRPL experiments are also typically designed with low enough injection of excess carriers to leave the Auger recombination processes irrelevant. This leaves only the non-radiative SRH recombination processes as the determining factor for the measured lifetime.

6.3. ELECTRICAL ANALYSIS

Electrical measurements can be used to estimate a wide variety of properties in semiconductors. These properties include, net carrier concentration, resistivity and concentration of deep levels in the band gap.

6.3.1. CV/IV

Capacitance-voltage (CV) techniques can be used to extract the net carrier concentration in a semiconductor. CV techniques use the fact that the space charge region of a metal-semiconductor junction device depends on applied voltage. These metal-semiconductor junction devices are usually consisting of two contacts placed on the semiconductor, one ohmic and one Schottky contact. Liquid contacts are commonly used, for research purposes, so that no solid contacts need to be evaporated onto the epilayer. A frequently used liquid

contact is mercury (Hg) which is a liquid metal at room temperature and easy to remove from epilayers.

A reverse-biased Schottky junction will produce a space-charge region of width W . The capacitance of the space-charge region can be approximated with a parallel plate capacitor:

$$C = \frac{\epsilon_r \epsilon_0 A}{W}$$

where A is the area of the parallel plates. In the case of a semiconductor doped with acceptors the expression for the doping concentration will be:

$$N_A(W) = -\frac{C^3}{q\epsilon_r\epsilon_0 A^2 dC/dV}$$

A detailed derivation of the doping expression can be found in [119].

6.3.2. DLTS

Deep level transient spectroscopy (DLTS) is a capacitance-time (C-t) measurement technique. This technique uses reverse-biased Schottky junctions that are periodically being forward-biased for a short time. This forward-bias pulse will create a capacitance transient that can be recorded. DLTS was first introduced by Lang [120] and builds on C-t and current-time (I-t) techniques [121, 122].

DLTS uses a rate-window (for example box-car or lock-in) on the capacitance transients to generate a spectrum as a function of temperature. From this spectrum it is possible to find out where deep levels are located inside the bandgap, the capture cross section and concentration of deep levels. For some deep levels, such as the $Z_{1/2}$, it is possible to correlate the concentration to the concentration of point defects in the crystal. In the case of $Z_{1/2}$ this would be the carbon vacancy in 4H-SiC.

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SUMMARY OF PAPERS

Paper 1

In this paper homoepitaxial growth of 4H-SiC has been developed on the Si-face of on-axis substrates of up to 100 mm in diameter with no 3C-inclusions excluding wafer edges. The growth process presented in this paper is stable and could produce homoepitaxial layers with thicknesses of $>100\mu\text{m}$. The influence of different growth ambient, susceptor design and growth history is studied. The paper also includes a study of the effect of using chlorinated precursors for growth on on-axis substrates. The growth rate is still limited to $<10\mu\text{m/h}$ and attempts to increase the growth rate resulted in the formation of 3C-inclusions. The largest impact of the growth rate was to increase the growth temperature indicating that the growth rate is limited by surface kinetics.

Paper 2

In this paper the effect of vanadium doping on homoepitaxial growth of 4H-SiC on the Si-face of on-axis substrates was investigated. The vanadium doping is introduced as vanadium tetrachloride during the growth. Due to the narrow growth window on on-axis substrates the highest concentration of V-doping that could be incorporated into the epitaxial layer without causing 3C-inclusions was $2\times 10^{16}\text{ cm}^{-3}$. In this paper epitaxial layers with V-doping between $1\times 10^{15} - 2\times 10^{16}\text{ cm}^{-3}$ have been investigated. For the samples grown with higher V-concentrations the shallow dopants were almost completely compensated. At the higher V-concentrations the epitaxial layers demonstrated very high resistivity in the range of $3\text{-}5\times 10^9\Omega\text{-cm}$ as measured at 150°C . In the epitaxial layers with lower V-concentrations it was possible to measure the resistivity at room temperature and resistivities in the range $2\text{-}6\times 10^5\Omega\text{-cm}$ were obtained.

Paper 3

In this paper the high roughness of homoepitaxial layers of 4H-SiC grown on the Si-face of on-axis substrates is improved. The growth on on-axis substrates takes place as a mixture of step-flow and spiral growth. This leaves the final surface rough with a valley and hillock morphology, in $120\mu\text{m}$ thick epitaxial layers the surface roughness can exceed $6\mu\text{m}$. By adjusting the time of the in-situ surface preparation it was possible to change the morphology to a macro-step morphology. This change in surface morphology significantly lowers the surface roughness, a $120\mu\text{m}$ thick epitaxial layer grown with the macro-step morphology has a surface roughness of $0.5\mu\text{m}$.

Paper 4

In this paper isotopically enriched V-doped 4H-SiC was grown on the Si-face of on-axis substrates. The isotopically enriched homoepitaxial layers were $90\mu\text{m}$ thick grown on 100 mm diameter wafers. The growth is performed using isotopically enriched methane and trichlorosilane. Secondary ion mass spectroscopy measurements show that the final epitaxial layer consisted of 99.85% ^{28}Si and 99.98% ^{12}C . The isotopically enriched 4H-SiC epitaxial layers showed increases in the thermal conductivity compared to epitaxial layers grown using

precursors with natural distribution of isotopes. The V-doping resulted in homoepitaxial layers with high resistivity and the epitaxial layers were in turn used as substrates for growth of GaN based HEMT structures.

Paper 5 In this paper 4H-SiC homoepitaxial layers are grown on off-axis substrates using chlorinated precursors. The natural Cl/Si-ratio is 3 when using trichlorosilane as the Si precursors. In this paper higher Cl/Si-ratios are investigated by adding HCl during the growth. Two series of samples were grown, one at $\sim 50 \mu\text{m/h}$ and one at $\sim 100 \mu\text{m/h}$. It is demonstrated that excess amounts of chlorine can affect the growth rate negatively and that excess chlorine can limit the availability of Si for the growth.

Paper 6

In this paper a sample with a long charge carrier lifetime is investigated, the charge carrier lifetime in this sample is very non-uniform. The non-uniformity was studied using DLTS, LTPL and KOH etching. It is shown from the DLTS measurements that the long charge carrier lifetime is due to a low concentration of $Z_{1/2}$ defects related to carbon vacancies. From the KOH etching it was clear that the non-uniformity was related to structural defects. Later the epitaxial layer was lapped away which showed that the structural defects originated from the substrate.

Paper 7

In this paper a morphological defect that occurs during homoepitaxial growth of 4H-SiC on off-axis substrates is studied. The morphological defect can appear in two different directions, from KOH etching it was clear that the all these morphological defects originates from a TSD. Using x-ray topography, it was possible to correlate the direction of the morphological defect to the sign of the Burgers vector of the TSD, so that all morphological defects in one direction originated from TSDs with the same sign of the Burgers vector. It is proposed that the morphological defects form due to the interaction between the step-flow growth and the spiral growth taking place at the TSDs.

MY CONTRIBUTION TO THE PAPERS

I have planned and performed most of the CVD growth experiments and material characterization for all papers except for the Paper 1 where I have contributed through some of the growth experiments and for paper 7 where X-ray topography was performed by a co-author in collaboration. I have written the first version of the manuscripts of paper 2-7.

Papers

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