16 GS/s Continuous-Time $\Sigma\Delta$ Modulator in a 22 nm SOI Process
a Simulation and Feasibility Study

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Declaration of authorship

We, Eric Öberg and Gustav Kindeskog, declare that this thesis titled, “16 GS/s Continuous-Time ΣΔ Modulator in a 22 nm SOI Process - a Simulation and Feasibility Study”, and the work presented in it is our own. We confirm that this work submitted for assessment is our own and is expressed in our own words. Any uses made within it of the works of other authors in any form (e.g. ideas, equations, figures, text, tables, programs) are properly acknowledged at any point of their use. A list of the references employed is included.

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Abstract

With a reference specification model in terms of 8 GS/s Sigma Delta Modulator in a 28 nm CMOS process consuming 890 mW, the purpose with this thesis is to construct a similar and simpler model but with higher specification demands. In a 22 nm SOI process with an input signal bandwidth of 500 MHz sampled at 16 GS/s with a power consumption below 2 W, the objective is to design a Continuous-Time Sigma Delta Modulator with verified simulated functionality on a transistor level basis. This specification is accomplished - with a power consumption in total of 75 mW.

The design methodology is divided into an integrator part along with a quantizer and feedback DAC part. A top-down strategy is carried out starting with an ideal high level Verilog-A model for the complete system, followed by a hardware implementation on transistor level.
Acknowledgements

We would like to thank the staff at Ericsson for their accommodating attitude and pleasant working environment. A special thanks to our supervisor Håkan Bengtsson for his helpfulness and dedication to this thesis. We also want to thank our examiner J Jacob Wikner for his support at the university.
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<th>Full Form</th>
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<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>ADC, A/D</td>
<td>Analog-to-digital converter</td>
</tr>
<tr>
<td>BOI</td>
<td>Band of interest</td>
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<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>CT</td>
<td>Continuous-time</td>
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<tr>
<td>DAC</td>
<td>Digital-to-analog converter</td>
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<td>DC</td>
<td>Direct current</td>
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<td>DFF</td>
<td>D-type flip-flop</td>
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<tr>
<td>DFT</td>
<td>Discrete Fourier transform</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
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<tr>
<td>DSP</td>
<td>Digital signal processing</td>
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<tr>
<td>ELD</td>
<td>Excess loop delay</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
</tr>
<tr>
<td>HDL</td>
<td>Hardware description language</td>
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<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-pass filter</td>
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<td>MASH</td>
<td>Multi stage noise shaping</td>
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<tr>
<td>MOSFET</td>
<td>Metal oxide semiconductor field effect transistor</td>
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<tr>
<td>NMOS</td>
<td>N-channel MOSFET</td>
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<tr>
<td>OSR</td>
<td>Oversampling ratio</td>
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<tr>
<td>OTA</td>
<td>Operational transconductance amplifier</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-channel MOSFET</td>
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<tr>
<td>QNF</td>
<td>Quantization noise floor</td>
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<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>SAR</td>
<td>Successive approximation register</td>
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<tr>
<td>SDM</td>
<td>Sigma delta modulator</td>
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<tr>
<td>SE</td>
<td>Single-ended</td>
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<tr>
<td>SFDR</td>
<td>Spurious free dynamic range</td>
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<tr>
<td>SNDR</td>
<td>Signal to noise and distortion ratio</td>
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<tr>
<td>SNR</td>
<td>Signal to noise ratio</td>
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<tr>
<td>SOI</td>
<td>System on insulator</td>
</tr>
<tr>
<td>SQNR</td>
<td>Signal to quantization noise ratio</td>
</tr>
<tr>
<td>VCVS</td>
<td>Voltage-controlled voltage source</td>
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<td>VGA</td>
<td>Variable gain amplifier</td>
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## Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
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<tbody>
<tr>
<td>Δ</td>
<td>Delta</td>
</tr>
<tr>
<td>Σ</td>
<td>Sigma</td>
</tr>
<tr>
<td>τ</td>
<td>Tau</td>
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Chapter 1 - Introduction

In an radio frequency (RF) receiver an analog-to-digital converter (ADC) is necessary to integrate into the system in order to process the incoming analog signal from the antenna into sequences of digital data, to further on decode this data which is useful for various applications. For telecommunication purposes, the sigma delta modulator (SDM) is a suitable option of an ADC and is to be constructed and evaluated in this thesis.

1.1 Motivation

In today’s technical society ADCs are used to a huge extent. The reason for this being that many modern systems uses various kinds of digital signal processing (DSP) units due to their ease of use, flexibility and ruggedness to manage data collected from peripheral devices. However, large quantities of the collected data comes in form of analog signals from sensors and other analog devices. In order for a DSP to be able to interpret these analog signals they have to be digitized. This is the primary objective of an ADC, to translate analog signals into digital bits that can be utilized by a computing unit.

Choosing the correct ADC for a specific application can be quite a challenge. There are many different types of ADCs currently used in various applications depending on the requirements for each specific application. To mention a few there are for example the successive-approximation register (SAR) ADC, direct-conversion (Flash) ADC and ramp-compare (Slope) ADC. The SAR ADC can be designed to consume a very small amount of power while achieving decent performance with fairly high resolution (typically 8 to 16 bits) and conversion speeds of kilo- to mega samples per second.

Where very high speeds are required and not necessarily a high resolution the Flash ADC is a good choice. It is considered to be the fastest ADC structure. However, the speed comes at a cost in terms of high power consumption and limited resolution, generally eight bits or below.

The simplest ADC is the Slope ADC which uses timing of a ramped signal (integration of the input signal) and compares that to a reference voltage. A DSP unit is used to determine how much time has elapsed before the comparator changes state and generates a bit pattern proportional to that time. Although being relatively easy to implement it is difficult to achieve good linearity with a Slope ADC.

A sigma delta modulator (SDM) oversamples the input while also pushing noise outside the signal band using an integrating low-pass filter, a quantizer, a digital-to-analog converter (DAC) and a feedback loop to generate an output signal with a high dynamic range (DR). This translates into an increase in the effective number of bits (ENOB) which is a way of quantifying the output resolution. The Continuous-Time (CT) SDM has potential of high speed and power efficiency and is therefore suitable for wide band high speed ADCs. These attributes makes it attractive to implement in a receiver for telecommunication purposes and
also because of its outstanding robustness to noise along with its high potential of output resolution.

1.2 Problem statements

With an objective of constructing a sigma delta modulator for RF purposes with followed up measurements; the main challenge is to find suitable circuit architectures for this type of ADC that cooperates and functions in a complete system at very high frequencies.

A typical problem regarding the CT SDM is the excess loop delay (ELD) that mainly occurs over the quantizer and the feedback DAC. An investigation of how problematic this becomes at high sampling speeds is to be analyzed towards final conclusions.

1.3 Project limitations

The design is limited to schematic level with simulations verifying functionality, i.e, layout level with continuous tape out is off limits.

The initial design was supposed to be a third order 1-1-1 multi-stage noise shaping (MASH) structure but was changed to a first order structure without MASH in order to have a reasonable level of complexity of the construction for this thesis.

1.4 Layout of report

The report begins with a chapter of background presenting an article which the report is based on. This is followed by a chapter where all relevant theory is stated as a background to the sequent part where the methodology is presented. This part is divided into two chapters, i.e two subsystems of the design, where one handles the integration and summation part, and where the other handles the quantization and feedback DAC part. The methodology is followed by chapters with results, discussions, future work, bibliography and finally appendices.
Chapter 2 - Background

This thesis is based on the IEEE article “A 72 dB-DR 465 MHz-BW Continuous-Time 1-2 MASH ADC in 28 nm CMOS”. The article is focused on the analog-to-digital conversion signal processing part at an IF-sampling base station receiver. A radio frequency (RF) input signal from the antenna is amplified, filtered and downconverted to an intermediate frequency (IF) by a mixer. Further on, the IF signal is amplified by variable-gain amplifiers (VGA) and finally filtered before the signal is sampled by the ADC. The DR of the receiver is optimized since the gain of the VGA is adjusted with a fast digital loop.

To allow practical thermal management due to maximum allowed temperatures on a board the power consumption is restricted to a maximum of 2.5 W of the ADC chip. If a dual-ADC chip is applied on the board, the power of one single ADC should be less than 1 W. The authors of the article have accomplished a power consumption of 890 mW which in their case is an accepted power efficiency considering the specification. Other results are as described in the title; a dynamic range of 72 dB over a signal of 465 MHz. Also, a CT 2-1 MASH topology is implemented.

An implementation of a sigma delta ADC in this system structure of a receiver with not too different specification requirements is the aim with this thesis.
Chapter 3 - Theory

The following subsections present theory about sigma delta modulator fundamentals and how this modulator can be extended towards better performance with higher levels of complexity. Further on the Silicon on Insulator (SOI) process is explained and a project specification is listed along with methods of measurements to obtain final results. Background theory about the modulator building blocks is finally presented.

3.1 Sigma delta modulator fundamentals

The main reason to use a sigma delta modulator (SDM) instead of other types of ADCs is that the SDM is fast, relatively inexpensive and the performance can be changed somewhat by the user even if the product is already produced. By altering the sampling frequency $f_s$ the properties of the SDM are changed.

The most basic variant is a first order SDM consists of one adder, integrator, quantizer, DAC and a feedback amplifier (if necessary). Such a system is illustrated in figure 3.1.

![Figure 3.1: A system overview of a first order sigma delta modulator.](image)

3.1.1 Oversampling

A SDM utilizes oversampling to achieve a better dynamic range (DR) at the output compared to simply following the Nyquist sampling theorem. The reason for this is that if more samples are taken there is more material to work with in order to represent the signal which implies that a more accurate average value can be obtained [8].

When the signal is digitized most of the excess samples are removed by decimation, generating a digital sequence with a better and more accurate average signal value. The oversampling ratio (OSR) describes how much oversampling that is used [8].

3.1.2 Noise floor

The noise floor for the digitized signal is referred to as quantization noise floor (QNF) and depends on the sampling frequency and the resolution of the quantizer. For a given quantizer the noise floor is of a fixed amount and evenly distributed across the frequency range. However, if a higher sampling frequency is used, that is the OSR is increased, the noise floor
will still be of the same amount, although distributed across a larger frequency range. This results in an improved signal-to-quantization-noise ratio (SQNR). The SQNR increases by 3 dB for every 2x oversampling which corresponds to an improvement in ENOB of half a bit [8].

The QNF can be affected by the OSR and with an increased OSR the QNF is spread out over a larger frequency band which decreases the noise level. The amount of noise is unchanged but when a wider frequency band is used the noise is spread out over that frequency band instead of being forced into a smaller frequency band, increasing the noise level. By oversampling and filtering out the frequency range that is not of interest reduces the noise in the band of interest (BOI). Depending on the OSR factor more or less of the noise floor can be attenuated [8].

3.1.3 Process noise and signal in parallel

Instead of employing a high order external low-pass filter before the ADC to prevent signals around multiples of the output sampling rate from aliasing down in band, the CT SDM features an inherent filtering effect. The modulator samples at the output of the forward loop filter, and the signal is first low-pass filtered by the loop before sampling, which attenuates signals around the modulator loop sampling rate that can alias down in band. These aliased signals are then injected at the input of the quantizer, they are noise shaped by the loop in the same manner quantization noise is shaped. These effects reduces requirements of additional external filtering which reduces systems complexity, cost and power [9].

In figure 3.2, an image demonstrates how SNR increases when oversampling and noise-shaping the input signal. From the figure it can be understood that the noise floor lowers significantly and results in a higher SNR [8].

![Figure 3.2: Illustration of how oversampling with frequency f_s along with noise shaping affects the noise within the signal frequency band of f_B, where the bandwidth of f_R is finally being cut off.](image)

3.1.4 Integration

By integrating the input signal, that is amplifying the low frequencies and reduce the high frequency noise, the overall noise quantity is reduced. With a single integrator a first order SDM can be designed. Similarly, an Nth order SDM can be designed using N integrators connected in series. By adding more integrators the performance of a SDM can be
significantly improved without the need to use too much oversampling. A second order SDM is illustrated in figure 3.3.

With increased SDM order the signal amplitude will decrease at a much faster pace with increased frequency, ideally with $\frac{N \cdot 20 \text{dB}}{\text{decade}}$. This is illustrated in figure 3.4.

However, when using two integrators or more in series stability issues may occur. One way to mitigate this problem is to make the subsystem with the shortest feedback path the most dominant by setting the amplification factor $k_n$ of the amplifiers after the DAC to $k_N > k_{N-1} > k_{N-2} (\ldots)$. In the case of the second order SDM in figure 3.3, this method would give $k_2 > k_1$ and result in a second order SDM with better stability.
3.1.5 Multi-stage noise shaping

A long chain of more than two individual integrators connected in series may cause system instability. One way to prevent this is by assigning one integrator to be dominant, thus attenuating the effect of other integrators. Another solution is to use a multi-stage noise shaping (MASH) structure, which contributes with several additional benefits such as increasing the system stability and attenuating the noise in the band of interest by pushing it to higher frequencies. This approach to lower the system instability comes with the cost of high accuracy within the integrators to minimize the quantization error due to analog to digital filtering mismatches [12].

3.1.6 Non-idealities of a sigma delta modulator

There are two main disadvantages with the CT SDM, namely the two non-idealities referred as excess loop delay and clock jitter.

Clock jitter can be explained as statistical variations of clock edges and affects the clocks controlling the quantizer and the DAC respectively. Clock jitter occurs in forms of delay clock jitter and pulse-width clock jitter which can degrade the SNR of the modulator in terms of white noise spread out over the frequency band [10]. However, since ideal clock signal generators are used in this system clock jitter is chosen to be neglected as a non-ideality.

Ideally, the sigma delta modulator expects the DAC to respond immediately at the clock edge from the quantizer and produce valid analog outputs. In reality, there is a delay between these states mostly due to switching times of the transistors among the comparators and also due to propagation time across the integrator and the DAC. This delay is referred as the excess loop delay [1].

The ELD becomes a problem in the CT Modulator, since the timing errors of output current from the DAC are continuously accumulated in the loop filter. In figure 3.5, the step response of the non-ideal DAC is illustrated where $t_d$ refers to the reaction time delay until the DAC pulse can be set high [1].

![Figure 3.5: The excess loop delay $t_d$ of a non ideal digital-to-analog converter pulse](image)

The loop delay can ideally be modeled with equation 3.1a.

$$DAC_{ideal} = \frac{1-e^{-\frac{t}{\tau}}}{\tau}$$ (3.1a)
Further on, the problematic non-ideal delay is shown in equation 3.1b, where the time constant $\tau$ is the rise time for the DAC pulse.

$$DAC_{\text{nonideal}} = DAC_{\text{ideal}} \frac{e^{\frac{-r}{\tau S}}}{1+\frac{r}{\tau S}}$$

(3.1b)

According to these equations, it is understood that the non-ideal unpredictable delay can modify the input-output relationship shown in equation 3.1b. This can increase the system order of the feedback open loop by one. Added system order and feedback loop delay can cause instability to the system and degradation to the performance of the modulator, such as SNR. The SNR does not significantly worsen with small delays, but after a certain delay, it can degrade significantly [1].

If this loop delay becomes a problem, there are some existing methods of reducing the problem, for instance by coefficient tuning and by adding an extra delay in the feedback [1].

### 3.2 SOI process

Instead of using a conventional CMOS process - the transistor circuits are designed in an SOI process. The silicon substrates among the transistors are replaced with silicon-insulator-silicon layers to reduce parasitic device capacitances. The silicon junction is above an electrical insulator of a material suitable for the system. Sapphire is typically used as an insulator for high-performance RF applications. The silicon-insulator-silicon layer increases system performance with lower parasitic capacitances, lower leakage currents and less power consumption with isolation from the bulk silicon. The process is also useful at low VDD operations.

The standard bulk CMOS process technology holds the P-type body of the NMOS to ground, while the N-well body of the PMOS is held to VDD because of a metal contact to the N-well. Since the drain, source and body regions of a MOSFET are insulated from the substrate in an SOI process technology, the body of the MOSFET is left unconnected which results in a floating body, which can get freely charged or discharged at the switching activities. The bulk nodes among all the MOSFETs are connected to ground in the entire system for this project.

### 3.3 Specifications

Since this project is supposed to be a refinement of an existing SDM the goal is partially to achieve the same performance figures or better or to explain why the goals could not be met. In table 3.1 the specifications/requirements/goals are listed.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Priority</th>
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<tbody>
<tr>
<td>Total power consumption</td>
<td>$&lt; 2$ W</td>
<td>High</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>16 GHz</td>
<td>High</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>5 bits</td>
<td>High</td>
</tr>
</tbody>
</table>
Output ENOB | > 10 bits | High
---|---|---
MASH structure | 2-1 | Medium
Bandwidth | 500 MHz | High

*Table 3.1: Performance specification of the sigma delta modulator.*

### 3.3.1 Relevant measurements

#### 3.3.1.1 Signal and noise

Noise is a fundamental factor of error in analog design, and limits the signal level to what a circuit can process with acceptable quality. It is typically a central topic because it trades with speed, linearity and power dissipation [2].

For an intelligible output signal, its power needs to be higher than the power of its noise. SNR is the power of the signal divided by the integrated power of the noise within the band and can be calculated according to equation 3.2 [2].

\[ SNR = \frac{P_{signal}}{P_{noise}} \]  
\[ (3.2) \]

The total average power of noise is the area integrated to its spectrum according to equation 3.3 [2].

\[ P_{noise} = \int_{-\infty}^{\infty} S_{noise}(f) df \]  
\[ (3.3) \]

This implies that the noise power can be very large if \( S_{noise}(f) \) extends a wide range of frequency [2].

SFDR is in the ADC designer’s interest to measure since it is desired to have as clean spurious free sinusoidal waves as possible. Ideally, all signal power is concentrated at the applied frequency, but because of spuriouses due to noise and non ideal components this is not true in real world. SFDR can be set as the range between the signal power and the highest spurious power within the desired band. It can be calculated according to equation 3.4 [3].

\[ SFDR = \text{Amplitude of Fundamental}(dB) - \text{Amplitude of Largest Spur}(dB) \]  
\[ (3.4) \]

The effective number of bits (ENOB) is a measurement of an A/D resolution performance and is possible to obtain from a calculated SNR (or SNDR) according to equation 3.5 [7].

\[ ENOB = \frac{SNR-1.76}{6.02} \]  
\[ (3.5) \]
3.3.1.2 Mismatch
In each step of the manufacturing process there are uncertainties resulting in mismatches of the MOSFETs. For instance, there are random microscopic variations at the gate dimensions introducing mismatches at lengths and widths between two identically specified MOSFETs. There are also voltage threshold variations among MOSFETs because of varying doping levels in channels and gates. It is of interest to analyze the mismatches since they may affect DC offsets (further explained under the subheading “Comparators”), finite even-order distortion which is a degradation of symmetry of the design, and since it may also lower the common-mode rejection - the change in the differential output divided by the change in the input common-mode level [2].

3.4 Modulator building blocks
The actual system that is implemented and tested is illustrated in figure 3.6.

![Figure 3.6: A system overview of a sigma delta modulator.](image)

3.4.1 Integrator
A fundamental block of the ΣΔ modulator is the integrator. An ideal integrator can be described as a LPF (low-pass filter) with infinite DC gain which amplifies or attenuates a signal below or above a certain unity gain frequency $f_{ug}$ respectively. However, in reality, infinite DC gain is not possible which implies that the integrator will behave like a LPF. The goal is to design an integrator with as much DC gain as possible in order to preserve the characteristics of an ideal integrator and maintain stability and to suppress the noise within the band of interest.

3.4.2 Quantizer
The following subsections explains the Flash ADC quantizer, presents different approaches to the subcomponents. Also, considerations regarding performance and evaluation methods are discussed.
3.4.2.1 Flash ADC

An ADC follows the integrator where a noise filtered input signal is converted into $2^M - 1$ levels, where $M$ is the number of bits [11]. In a sigma delta modulator it is practical to use a flash ADC which is fast and simple. A lot of hardware is typically required when designing a flash ADC with high resolution, but since the modulator uses relatively few bits to generate a significantly higher number of bits, the amount of hardware required is not a problem. Although an arbitrary number of bits can theoretically be implemented, eight bits is generally considered the upper limit for a flash ADC for practical reasons. An example of this type of converter with a specification of 2 bits and 4 levels of resolution is illustrated in figure 3.7 where three thermometer encoded levels are generated which can further on be converted into 2 bits of binary code.

Figure 3.7: An illustration of a flash analog-to-digital converter that generates 3 thermometer encoded bits which further on can be converted into 2 bits of binary code.

The input signal is being compared with reference voltages generated by voltage dividing in a resistor ladder. Each comparator is having a certain reference voltage to compare the input
signal with, and will output a "1" if the input signal is higher and "0" if the reference signal is higher. The output is represented in thermometer code. A certain amount of comparator outputs from the flash ADC will be high similar to a thermometer bar depending on what value the input signal is having at a certain sample, and the comparator with the highest reference input that outputs "1" will be the most significant bit.

3.4.2.2 Comparators

Important parameters considering design of comparators are accuracy and power consumption which are being discussed in this section, along with some final standard comparator circuits in single ended modes for simplicity.

Accuracy comprises offset, metastability, resolution, overdrive recovery and noise. Offset is a significant issue concerning comparators and can be expressed as static offset and dynamic offset. The static mismatch refers to mismatch in cross coupled pairs and on signal inputs, while the dynamic mismatch concerns imbalanced load capacitance as well as imbalanced charge injection and clock feed through. Usually there is only static offset in the pre-amplifier in terms of threshold voltages, widths and lengths of the transistors. The DC-offset refers to mismatch in the input transistors. A circuit having an input set to zero that generates an output that is not zero suffers from output referred offset and is a mismatch between input transistors. The input referred offset is the input level required to force the output voltage to zero. Offset limits performance and makes the system nonlinear. The phenomena limits the precision of which signals can be measured which applies to an amplifier making decisions whether an input signal is higher or less than a certain reference signal. The input referred offset causes a lower bound on the minimum Vin-Vref that can be detected with precision according to figure 3.8 [2].

![Figure 3.8: Model of the input referred offset among comparators that causes a lower bound on the minimum Vin-Vref that can be accurately detected.](image)

Metastability is a problem that occurs when the input signal level is near the decision point and the output is to be regenerated to one or zero. This highly affects the resolution since it is
the comparators ability of making a correct decision and produce valid results within half a clock cycle. If the comparator fails within this time the metastability is too high [4].

Overdrive recovery is the ability to prevent the memory effect. The comparator shall be able to output a valid one or a zero regardlessly of what the previous output value was. If the recovery time to discharge the previous state takes to long there will be an output error. An overdrive recovery test can be performed by comparing to different inputs directly after each other without generating output errors [5].

Kickback noise is a phenomena described as disturbances at the comparator inputs due to large voltage variations in the latch part of the comparator. This may affect the input signals in a way that incorrect latch decisions are taken resulting in a misrepresented digital output [6].

Further on, a higher immunity to environmental noise is possible with a differential comparator. For instance, considering a sensitive signal distributed as two equal and opposite phases over two adjacent lines in a circuit; there will be an equal amount of transition disturbances over the differential phases leaving the difference intact. The common-mode level of the two phases is disturbed but the differential output is however not corrupted which implies that the common-mode noise is rejected. Common-mode rejection with a differential arrangement also applies to noisy supply voltages, as the noise on VDD affects the single-ended outputs separately, but not the differential output. Other benefits with a differential configuration besides robustness to noise is the increase of maximum achievable voltage swings, easier biasing and higher linearity. The drawback with twice as size of area occupation is a minor issue compared to the several advantages of a differential operation. [2]

Power consumption is a standard parameter to be aware of and is obviously in the designer’s interest to analyze.

There are usually three types of comparator circuit variants, namely static latched comparators, Class-AB latched comparators and dynamic latched comparators. An example of a static latched comparator is shown in figure 3.9 below.
A preamplifier stage of an NMOS differential pair with output currents mirrored through diode connected PMOS transistors is connected to the PMOS inputs of the latch. When the clock goes high the latch turns into reset mode and the latched outputs are forced to ground. When the clock goes low, the latch enters regeneration mode and $V_{on}$ or $V_{op}$ is set to $VDD/VSS$ depending on the differential input.

The preamplifier constantly feeds current in both of the operation modes, thus this comparator is not very power efficient. It also suffers from a rather slow regeneration process, but has low kickback noise because of the input PMOS transistors of the latch isolating the aggressive voltage variations from the inputs [6].

Further on, a Class-AB latched comparator is illustrated in figure 3.10.
The inputs are connected to a preamplifier stage of a differential pair of NMOS, and these outputs are connected directly to the inputs/outputs of the latch stage. When the clock goes low, the comparator enters reset mode and the outputs of the latch are shorted and charged to VDD through the open PMOS. When the clock goes high, the regeneration mode is initiated and the back-to-back connected CMOS inverters regenerates the smaller differential input voltages into full levels of VDD and VSS.

Current only flows through the latch stage when clock is high and the drains of the NMOS transistors are connected to ground, and the speed is improved with current increasing momentarily with the cross-coupled CMOS inverters. Also, the latch reacts quickly to input voltage variations by connecting the preamplifier outputs directly to the regeneration nodes of the latch, however, this increases kickback noise connected capacitively across the gate and drain nodes at the input differential NMOS pair. To sum up, the comparator is faster and more power efficient, but suffers from kickback noise [6].

Finally a dynamic latched comparator is shown in figure 3.11.
In the reset phase, the output nodes as well as the drains of the input NMOS pair are charged to VDD and current flow is blocked with the cut-off NMOS. As the clock goes high the PMOS transistors operate in cut-off region and the current flows through the open NMOS to ground. The NMOS with highest input voltage will let through most current to the cross-coupled CMOS inverter which will regenerate a low latched output voltage. After the regeneration, there is zero voltage potential at the drains of the input differential pair, and no current is flowing during the rest of the regeneration phase.

Since current only flows through the comparator during the actual regeneration process, this prototype is very power efficient. However, the differential input NMOS pair will change operating regions during the reset phase and the regeneration phase, causing disturbing voltage variations at the input signals along with kickback noise from the cross-coupled CMOS inverters [6].

### 3.4.3 Feedback DAC

The digitized signal is sent for digital signal processing but in order for the loop filter to work an analog feedback signal representing the digitized signal is required to be sent back to the integrators. Since the DAC is of a fixed resolution the output signal, it is going to be
somewhat square shaped. This introduces an error as the difference between the integrator output and the feedback signals [7].

Different variants of DACs are presented and explained in the following paragraphs.

A simple approach to a DAC is demonstrated in figure 3.12, where the output thermometer code is being divided over resistors to generate currents that accumulates at the output, with corresponding levels according to number of active ones in the thermometer sequence. Design simplicity and equally large output impedances are major advantages with this DAC.

![Figure 3.12: An example of a simple current summation digital-to-analog converter.](image)

Another approach is to implement the R-2R ladder DAC which inputs a bit pattern and divides the voltage over resistors where and the number of high bits will determine the output level of current. Current sources assumed to have infinite impedance feeds switches controlled by the input pattern, and the input impedance is always 2R, since the leftmost section is constituted by two resistors in series. This also applies for the next section with two resistors in parallel with the two series R resistors. This type of DAC circuit is shown below in figure 3.13 [7].

![Figure 3.13: A variant of the R-2R ladder digital-to-analog converter.](image)

A disadvantage of this type of DAC is that the resistors are more or less nonlinear with signal-dependent capacitances, which is a source of distortion. There are also glitches due to the switches, and the current sources will have different terminal voltages since the internal voltages varies resulting in non linearity and distortion [7].
The previously discussed R-2R DAC has a similar variant where a voltage-mode encoded DAC is realized with one resistor for each input bit. Voltage division is performed with a reference voltage feeding a resistor ladder and each voltage level $V_m$ can be modelled with the following equation.

$$V_m = \frac{m \cdot R}{R_{ref}} \cdot V_{ref} = \frac{m}{2^n - 1} \cdot V_{ref} \quad (3.6)$$

This voltage dividing resistor string DAC is shown in figure 3.14.

As the number of input bits increases the required number of elements increases, which makes this approach appropriate for a low resolution. Matching of the resistors in the string is crucial for the DAC accuracy, and RC-timing through the switches limits the bandwidth [7].

Current DAC’s are generally faster but at the cost of higher sensitivity to glitches. An additional current DAC variant is to use current cells receiving input digital ones and zeros, that outputs a positive or a negative current depending on a high or a low input. These cells can consist of cascaded connected transistors acting as current sources, and a switching pair of transistors that receives the input signal [7]. An example of a schematic for this approach is illustrated in figure 3.15 where a single PMOS cascode with input bias voltages acts as a current source to a differential input switch generating output currents at nodes $I_+$ and $I_-$. 

$$\text{Figure 3.14: Example of a resistor string digital-to-analog converter.}$$

$$\text{Figure 3.15: Example of a cascode current DAC.}$$
Figure 3.15: A proposed current cell in a current-steering digital-to-analog converter with a differential input switch driven by a cascode connected PMOS current source.
Chapter 4 - Method - Integrator

Chapter four consists of the design approach used for the integrator, summer and the amplifier highlighted in figure 4.1. Some of the problems encountered during the design will be discussed and whether or not these problems were solved.

![Figure 4.1: System overview of a first order sigma delta modulator with the components discussed in this section highlighted. These are the summer, integrator and the amplifier.](image)

The design of the ΣΔ modulator was divided into three main parts. First, a high abstraction level was carried out using hardware description language (HDL) to create a functional system that behaved as the modulator was intended to. This was followed by a step down in abstraction level where ideal components the HDL blocks were exchanged for ideal components. This system was intended to have the same behavior as the HDL system. The final abstraction level is where the ideal components and HDL parts were replaced by transistor models containing built-in parasitics in order to achieve a more realistic system.

4.1 HDL level

The purpose of designing a system in HDL is to make sure that the behavior of the system satisfies the required specifications. This should be followed by a mix of Verilog-A code and ideal components. The ideal components should later be replaced by non-ideal components (transistor level). Testbenches were also created where both the ideal and non-ideal transistor systems later could be tested in order to verify a correct behavior.

4.1.1 Verilog-A

The structure was intended to resemble a schematic view that could be used later in the transistor level. All components and blocks that the Verilog-A code was supposed to describe were divided into separate parts where each part described one component or block. These different parts to be described were an integrator, summer, ADC and DAC. The integrator and summer were merged into one block since that is how the system really will work.
4.1.1.1 Open-loop SDM (Integrator characteristics)

During simulations the integrator block did not function as first expected. When a signal was applied on the input, the output consisted of an amplified version of the input signal added by a slope. That is, the output signal DC level changed continuously according to a linear function. In order to fix this problem the system feedback loop had to be broken. This allowed the integrator block to be characterized without interference of a feedback signal. Mathematically the integrator function for one output becomes

\[ V_{on} = A \int V_{in} dt = A \int (\sin(\omega t) + V_{CM}) dt = A \left( \frac{1}{\omega_0} (-\cos(\omega t)) + tV_{CM} + C \right) \]  

for a first order system where \( C \) is a constant. In figure 4.2 the behavior of equation 4.1 is graphically illustrated.

![Figure 4.2: Behaviour of a Verilog-A integrator.](image)

Although the output signal behavior is mathematically correct according to equation 4.1 it is not desirable due to \( V_{CM} \) and the \( C \) term. The output signals \( V_{on} \) and \( V_{op} \) are \(-\cos\) and \( \cos\) functions respectively and they should be at the same DC level as \( V_{in} \) and \( V_{ip} \). However, if no adjustments are made to the input signals, both output signals will start at \( V_{out} = 0 \) at \( t = 0 \) according to figure 4.2. Due to this they will never cross, one will always be on top of the other. This created a problem which meant that it was not possible to perform tests and
simulations on this system since the output signal did not have a constant DC level. In short, the ideal Verilog-A integrator was too ideal. The other blocks (ADC and DAC) worked as expected.

In an attempt to rectify the problem to be able to get a usable system out of this, some modifications to the Verilog-A code had to be made. First, the slope needed to be eliminated. What causes it is the $V_{CM}$ off 600 mV. By subtracting $V_{CM}$ from $V_{in}$ and $V_{ip}$ before the integration, and add it again after the integration, the slope will no longer be present. The expression then becomes

$$V_{on, V_{cm \text{ correction}}} = A \cdot \int (\sin(\omega t) + V_{CM} - V_{CM}) \, dt + V_{CM} =$$

$$= A \cdot \left( \frac{1}{\omega} \cdot (-\cos(\omega t)) \right) + V_{CM} \quad (4.2)$$

and results in a slope and $V_{CM}$ correction illustrated in figure 4.3.

![Figure 4.3: Verilog-A integrator with slope and $V_{CM}$ correction.](image)

Next, the $C$ term must be eliminated. The $C$ term causes the output curves to never overlap which would imply more errors, although small in comparison to the DC offset but still significant. One small problem here is that depending on what sign the input signals have initially results in the output signal curves to shift location along the $y$-axis. For example, a positive sine function at the input will result in a negative cosine function at the output. A negative cosine function with its origin at $y = 0$ will always stay above the $y$-axis and just touch $y = 0$ once every period. The exact opposite is true for a negative sine function applied at the input. This is visible in figure 4.3 where $V_{CM} \leq V_{on} \leq \frac{A}{\omega}$ and $-\frac{A}{\omega} \leq V_{op} \leq V_{CM}$ and as a result, the sign of the input signal needs to be accounted for when correcting the $C$ term. In the case of the positive sine input signal, the output signal (negative cosine) needed to be
subtracted by half its amplitude, that is \( \frac{A}{2\omega} \). The opposite is true in the case of the negative sine input, where \( \frac{A}{2\omega} \) needs to be added to the output signal. Thus, \( C = \pm \frac{A}{2\omega} \) depending on the input signal. This is further clarified in equation 4.3 and 4.4.

\[
V_{on, \text{C correction}} = V_{on} - \frac{A}{2\omega} = \frac{A}{\omega} \cdot (\cos(\omega t)) + V_{CM} \tag{4.3}
\]

\[
V_{op, \text{C correction}} = V_{op} + \frac{A}{2\omega} = \frac{A}{\omega} \cdot (\cos(\omega t)) + V_{CM} \tag{4.4}
\]

When \( C \) was corrected the behaviour of the outputs became as illustrated in figure 4.4.

*Figure 4.4: Verilog-A integrator with slope, \( V_{CM} \) and constant correction.*

One thing to mention is that the slope and offset corrections could have been ignored if the DC offset of both the input and output signals was supposed to be 0 V.

Now, the Verilog-A integrator behaves as desired. In figure 4.5 an AC analysis for the Verilog-A integrator is displayed.
In order to increase the unity gain frequency $f_{ug}$ the output gain of the integrator must increase. Also, figure 4.2 through 4.5 illustrates the functionality of the integrator alone with no feedback applied according to figure 4.1.

### 4.1.1.2 Closed loop SDM

With a working integrator and a closed loop system simulations were carried out for a first order Verilog-A SDM. The input signal frequency $f_{in}$ was changed to 500 MHz according to the bandwidth limitation in order to make sure that the system worked according to the specifications. Also, the differential signal amplitude was reduced to 200 mV\textsubscript{peak-peak} from 400 mV\textsubscript{peak-peak} to reduce the risk of distortion to occur on the signals. This will be clarified more later.

In figure 4.6 the initial behaviour of a first order Verilog-A SDM with feedback is illustrated.
Looking at the first four nanoseconds of a two microsecond simulation shows how the Verilog-A SDM acts at startup. It only takes around 0.2 ns for the system to settle and stabilize. Moreover, \( V_{\text{out}} \) follows \( V_{\text{in}} \) which indicates that the loop is locked and the system is stable. There is a very small amount of ELD (excess loop delay). In later simulations of the complete transistor system, the ELD will be a limiting factor.

By looking at an AC analysis of the system is shown in figure 4.7, it is visible that the gain of the integrator is moving towards infinity as \( f_m \to 0 \). In reality however the amplification will saturate at some frequency and remain constant below that frequency. This will make the integrator act as a LP filter with noise suppression in the passband. It is therefore desired to push the dominant pole far down in frequency to achieve as much DC gain as possible without sacrificing bandwidth.
Figure 4.7: AC analysis of a Verilog-A integrator. Since this is a first order system, the amplification attenuates with a factor of 10 per decade (20 dB/dec). fug is placed at 2.5 GHz in this simulation. The result illustrates the open loop gain.

Another way to measure performance for a SDM is to perform a DFT (discrete fourier transform) measurement. A DFT clearly shows the DR (dynamic range) over a large frequency range and how the noise floor is suppressed within, or pushed out from, the band of interest. This is illustrated in figure 4.8.
Figure 4.8: A discrete Fourier transform analysis of a first order Verilog-A sigma delta modulator.

The characteristics of the DFT analysis in figure 4.8 is typical for a SDM where the noise floor is suppressed within the band of interest and pushed out of it. However, the look of this particular DFT analysis is not as clear as it should be. There appears to be a noise floor in the -150 dB to -160 dB region, starting to ramp up at around 20 MHz which can be considered normal. There also appears to be quite a lot of spurs with the first being around -130 dB at 20 MHz followed by another spur around -115 dB at 100 MHz and so on. These spurs are not desired and the reason for them being present in this plot is unknown. One reason could be the accuracy of the simulator itself which may introduce some errors, showing up as spurs in the plot. Despite the spurs, this SDM is performing really well. The DR within the band of interest is overall very high which indicates a large amount of loop gain. This loop gain is one of several critical parameters that directly affect the performance of a SDM.

With a working principle of a first order SDM carried out using Verilog-A the integrator block could now be exchanged for another block utilizing ideal components instead with the goal being to achieve similar results as for the Verilog-A SDM.

**4.1.2 Ideal components**

The next step in abstraction was to replace the Verilog-A blocks for the integrator with ideal analog components, voltage sources and ideal amplifiers with variable gain. The idea being that this would be one step towards a more realistic design with the working principle of a
transistor schematic but using ideal components. In figure 4.9 a schematic of the integrator is shown.

![Figure 4.9: Schematic of an integrator circuit consisting of ideal components.](image)

The amplifiers $A_{\text{diff}}$ and $A_{\text{Vcm}}$ are ideal voltage-controlled voltage sources (VCVS) which amplifies the input voltage difference by an amplification factor $A$ and sends it to the output. In this case $A_{\text{diff}} = A_{\text{Vcm}} = 1000$ to keep $A$ somewhat realistic. $V_{\text{in}}$ and $V_{\text{fbn}}$ (and $V_{\text{CM,fb}}$) are summed up at the common node after the resistors (voltage addition). $V_{\text{in}}$ and $V_{\text{fbn}}$ are AC signals and $V_{\text{CM,fb}}$ is a DC signal derived from the output common mode voltage signal $V_{\text{CM,out}}$ which is compared to $V_{\text{CM}}$. $A_{\text{Vcm}}$ amplifies the difference and the resulted signal is $V_{\text{CM,fb}}$ that is supposed to make sure that $V_{\text{on}}$ and $V_{\text{op}}$ have the correct $V_{\text{CM,out}}$. The summation resistors $R_N$ and $R_P$ are paralleled with capacitors $C_N$ and $C_P$ which filters out any potential transients and smoothes out $V_{\text{CM,out}}$ to provide a stable DC signal to $A_{\text{Vcm}}$. The values for all components in figure 4.9 are listed in table 4.1 below.

<table>
<thead>
<tr>
<th>Component</th>
<th>$R_{\text{in,p}}$</th>
<th>$R_{\text{fbn,p}}$</th>
<th>$R_{\text{CMn,p}}$</th>
<th>$R_{\text{integ,p}}$</th>
<th>$R_{\text{N,P}}$</th>
<th>$C_{\text{integ,p}}$</th>
<th>$C_{\text{N,P}}$</th>
<th>$A_{\text{diff}}$</th>
<th>$A_{\text{Vcm}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>300 Ω</td>
<td>300 Ω</td>
<td>1k Ω</td>
<td>1M Ω</td>
<td>1M Ω</td>
<td>200f F</td>
<td>100f F</td>
<td>1000</td>
<td>1000</td>
</tr>
</tbody>
</table>

Table 4.1: Component values for an ideal integrator.

The theoretical unity gain frequency $f_{ug}$ with these values are determined by $R_{\text{in}}$ and $C_{\text{integ}}$ according to the formula given in equation 4.5

$$f_{ug} = \frac{1}{2\pi R_{\text{in}} C_{\text{integ}}}$$

and yields $f_{ug} \approx 2.65 \text{ GHz}$. This is illustrated in the AC analysis in figure 4.10.

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Note that the integrator now behaves more like a LPF compared to the Verilog-A integrator. For frequencies around 2 MHz and below $A$ is more or less constant, and for frequencies around 10 MHz and above $A$ decreases with a factor of 10 per decade, thus behaving like a LPF with integrator characteristics at high frequencies.

In figure 4.11 and figure 4.12 the transient analysis for a first order ideal SDM is illustrated where the first shows the characteristics of the SDM at $t = 0$ and the second at $t = 2 \text{ us}$. 
Figure 4.12: Transient analysis for an ideal first order sigma delta modulator at 1.996 µs to 2.0 µs.

As illustrated in figure 4.11 the settling time is almost non-existing, the signals are stable at $V_{CM}$ after only a couple of picoseconds. The system is stable and the signals are locked to each other.

Although both the transient analysis and AC analysis yields good results the corresponding DFT shown in figure 4.13 did not.
Several simulations were made in an attempt to achieve a better DFT but without success. The overall behavior of the SDM is still somewhat intact, that is the noise suppression in the passband and the slope characteristic. However, the sample values can be mostly ignored since a passband noise floor of -220 dB is not really feasible.

Simulations were also carried out for a second order ideal SDM according to the system displayed in figure 3.3. To ensure system stability the shortest feedback loop must be dominant. This is controlled by the constants $k_1$ and $k_2$, where $k_2 = 1.5k_1$. This results in a gain increase for the feedback signal applied to the short-loop integrator. A schematic of this system is displayed in figure 4.14.
The first integrator (Ideal 1) and the second integrator (Ideal 2) are identical except for the $R_{\text{fb},p}$ values. From table 4.1, $R_{\text{fb},p} = 300 \, \Omega$ for Ideal 1 while for Ideal 2, $R_{\text{fb},p} = 200 \, \Omega$. This has to do with the previously mentioned $k$-factor which is supposed to be 1.5 times larger for Ideal 2 compared to Ideal 1. By selecting a lower $R_{\text{fb},p}$ value the feedback gain will increase since the feedback gain is given by $A_{\text{feedback}} = \frac{k_{\text{factor}}}{R_{\text{fb},p}}$. Thus, lowering $R_{\text{fb},p}$ for Ideal 2 by a factor of 1.5 should increase the feedback gain by a factor of 1.5. Although this method provides more stability to the system it also limits the input signal range since $V_{\text{mid},p}$ increases by the same factor 1.5 as shown in figure 4.15. Because of this $V_{\text{in},p}$ was lowered from 400 mV to 200 mV to prevent distortion from occurring at $V_{\text{mid},p}$ as previously mentioned.

![Figure 4.14: Schematic of an ideal second order sigma delta modulator.](image)

![Figure 4.15: Transient analysis for an ideal second order sigma delta modulator showing how the signals settle in.](image)
Another thing worth mentioning is that now the system needs some time to settle in. The input signals are not hovering around $V_{CM}$ at startup as for the first order system. Instead, $V_{in,p}$ starts at roughly 670 mV, as seen in figure 4.16 where the first 4 ns are zoomed in, before finally reaching their $V_{CM}$ value after around 50 ns.

This is due to the common-mode feedback signal $V_{CM,fb}$ that is supposed to keep $V_{in,p}$ at 600 mV. In this case, that requires $V_{in,p}$ to be slightly higher at startup. Since $V_{in,p}$ is not fixed at a certain DC level it can move somewhat depending on the values of $V_{fb,n,p}$ and $V_{CM,n,p}$. After approximately 50 ns $V_{in,p}$ is practically stable at 600 mV and at two µs it is very stable as seen in figure 4.17.
For a second order SDM with two identical integrators $f_{ug}$ is the same for both. This is visible in the AC-analysis plot shown in figure 4.18.

If figure 4.18 is compared to figure 4.10 the light blue curve is the same. For the second order SDM an additional integrator with the same gain has been added which increases the overall gain for the loop filter from $A$ to $A^2$. This would improve the DR in the passband section. Unfortunately, this is not clearly visible in figure 4.19 since it can not be compared with the DFT for the first order ideal SDM due to the simulation mishap.
Even though not all simulations gave expected results it was decided to move on to the transistor level. The desired behaviour of both a first order and a second order SDM is at this point relatively well known.

4.2 Transistor level

During the design of the transistor level system several variations of integrator designs were tested and simulated.

4.2.1 Introduction

A test circuit consisting of an inverter with a capacitive load was designed to characterize the properties of the SOI transistors for different sizes and transistor models. Since there are a couple of different SOI transistor models with different threshold voltages ($V_T$) one test circuit was designed for each model. In total three test circuits were made, one for lvt (low $V_T$), one for slvt (super low $V_T$) and the last for elvt (extreme low $V_T$). These test circuits are displayed in figure 4.20.
Figure 4.20: Inverter test circuits, each with an equal capacitive load. P0 and N0 are lvt transistors while P1 and N1 are slvt transistors and finally P2 and N2 are elvt transistors.

A quick side note, to make the subsequent schematics a bit less cluttered the bulk connector and the parameter text for the components will be left out. If there is a need to mention the specific parameters for some of the components that will be mentioned in the text.

With the test circuits set up simulations were performed with different transistor sizes. The smallest size of a SOI transistor is a width of 300 nm and a length of 22 nm ($W/L = 300/22$). However, since the amplifiers in the integrator needs to be able to drive the output capacitance the size needs to be enlarged. The length of the transistors will remain at 22 nm but the width will have to be increased to allow more current to pass through. Also, in order to achieve as much linearity as possible, minimize the risk of mismatch between the transistors, increase the driveability and to simplify the design, it was decided to use a unity transistor size. This unity transistor size could then be multiplied (multiple unity transistors connected in parallel) with an arbitrary integer to allow for more current flow. The unity transistor size was set to have the parameters listed in table 4.2.

<table>
<thead>
<tr>
<th>Total width</th>
<th>Finger width</th>
<th>Fingers</th>
<th>Length</th>
<th>Multiplier ($M$)</th>
<th>Other parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 um</td>
<td>300 nm</td>
<td>20</td>
<td>22 nm</td>
<td>Integer</td>
<td>Untouched/standard</td>
</tr>
</tbody>
</table>

*Table 4.2: Unity transistor parameters. To achieve as much linearity as possible and minimize mismatch the size of the transistor will be set by the multiplier alone.*

With this setup only the multiplier $M$ will have to be changed to alter the current flow through the transistor. This results in an easier design procedure since only one parameter will have to be changed for each transistor. In figure 4.21 the difference between the different transistor types (lvt, slvt and elvt) regarding charging and discharging a capacitive load is displayed.
In figure 4.21 the transistor type with the most symmetrical charge and discharge characteristics is the slvt with a rise and fall settling time of around 400 ps for the unity transistor size with a capacitive load of 200 fF. The lvt was considered too slow and although the elvt was a bit faster than the slvt it was not symmetrical regarding rise and fall times. Therefore the transistor type of choice throughout the integrator part was the slvt. The voltage spikes at the transition moments are due to the fast rise and fall times at $V_{in}$.

Although the rise and fall times for the slvt are sufficient enough for a clock frequency of 1 GHz, as seen in figure 4.21, it is not enough for higher clock frequencies. For the system to be nearly fast enough for a clock frequency of 16 GHz the transistor size must be increased by the same factor. $M$ will therefore be set to 16. However, as shown in figure 4.22 and 4.23, the performance of the transistor does not scale linearly according to the clock speed.
Figure 4.22: Characteristics of an inverter with slvt transistors at a clock frequency of 16 GHz with a 200 fF capacitive load.

Figure 4.23: Same as figure 4.22 but zoomed in at 2.5 ns.

It is clear that the rise and fall time at the output of the inverter is not fast enough. However, this is an extreme scenario. If the inverter were treated as an amplifier instead and the input was a sinusoidal signal with a lower frequency, the amplifier would be strong enough to amplify the signal as can be seen in figure 4.24.
Figure 4.24: Inverter used as an amplifier. Input is a sinusoidal signal with an amplitude of 100 mV at a frequency of 1 GHz.

Although the amplifier works as an amplifier, the gain is very limited at high frequencies, around two times the input voltage for a 1 GHz signal. For lower frequencies the gain will increase as shown in figure 4.25.

Figure 4.25: Inverter used as an amplifier. Input is a sinusoidal signal with an amplitude of 10 mV at a frequency of 100 MHz.

This setup can also be considered a transconductance-capacitance filter (or gmC filter) with a low-pass filtering characteristic. A gmC filter is comparable to an active RC filter with the absence of resistors as a part of the filter. Instead of resistors the internal resistance, or transconductance, of the transistors in association with the external capacitor will give the filter its characteristics. Since gmC filters has a tendency of poor having linearity active RC
filters were opted for instead. Moreover, active RC filters are easier to manage since the resistors can be used to control the amplification of the active filter whereas for a gmC filter the transistors themselves or the external capacitor needs to be altered to achieve the same effect. Active RC filters are also considered to have better linearity than their gmC filter counterparts.

With the transistor characteristics relatively well known and the preferred filter type selected the design of the integrator itself could begin.

4.2.2 Integrator

Two main types of integrator structures were created, one in single-ended (SE) topology and the other in fully differential topology. The goal from the beginning was that the system should be fully differential. The reason for starting with a SE system is that it is slightly easier to start with and understand in general. Later, when satisfactory results were received in SE, the design of the fully differential system began using the knowledge obtained from the simulations in SE.

4.2.2.1 Single-ended amplifier configuration

One of the most simple amplifier circuits consists of two transistors connected in an inverter configuration, as already proven. However, as mentioned previously, the gain of such an amplifier is very limited. To solve the gain issue more amplifiers can be connected in series, but this approach results in unwanted effects such as oscillation and DC offset issues. This DC offset effect can be seen in figure 4.24 and 4.25 where the output signal is close to a 300 mV DC level compared to the 400 mV DC level of the input signal.

One way of solving this has already been used in the ideal integrator where \( V_{CM,\text{out}} \) is compared to \( V_{CM} \) and the difference is amplified and fed back to the input which results in the \( V_{CM,\text{in}} \) matching \( V_{CM,\text{out}} \) by the time the system has settled in (see figure 4.9).

Another theoretical solution would be to size the transistors so they keep the desired DC level throughout the chain of amplifiers. However, this is like sending a space shuttle into orbit without the ability to control the behaviour of the space shuttle once it has been launched. The smallest deviation in wind speed or a momentary misfire in one of the rocket boosters would be enough to alter the course of the space shuttle, either sending it out into space or having it come back to earth resulting in a crash. The probability of reaching a steady orbit without the ability to control the space shuttle after it has been launched is almost zero. Some kind of active control system is needed. Similarly for the transistor amplifier a small difference in temperature or process variation would result in a DC level either too high or too low.

A third option will be described in the section of the fully differential amplifier. It is similar to the control system used in the ideal integrator, but instead of sending the feedback signal to
the input it controls one of the bias transistors. As will be seen and discussed further on this system proves to be better than the input referred feedback system.

For this SE integrator a control system based on the input referred feedback will be used. The control system is displayed in figure 4.26.

![Figure 4.26: Common-mode voltage regulator for input referred signal feedback.](image)

The integrator setup used is also based on the ideal system with all the resistors and capacitors kept the same. The difference is the amplifier which will be consisting of the already discussed inverter style circuits. However, since one amplifier will not provide enough gain a chain of three amplifiers will be used to increase the gain. In figure 4.27 both a single stage amplifier and a three stage amplifier are displayed.

![Figure 4.27a: A simple single-amplifier integrator.](image)  ![Figure 4.27b: An integrator circuit consisting of three amplifiers connected in an inverter configuration.](image)

While there are several benefits with using an integrator consisting of only one amplifier such as good stability and a large output drive ability (depending on transistor size) there are also
some drawbacks. The biggest being poor gain which limits the field of use quite significantly. Adding two more amplifiers will result in a much better gain, but at the cost of stability. Three inverter connected amplifiers can theoretically achieve a phase shift of 270° at $f \to \infty$. However, a phase shift of 180° is much more likely to happen within the band of interest which will cause instability due to oscillation. If the two amplifier designs are combined into a single 3+1 design illustrated in figure 4.28, the best properties of the two will be utilized. That is stability and drive ability from the single stage along with the improved gain from the three stage amplifier. By tweaking the transistor size ratio of the amplifier stages by enlarging the transistors in the single stage compared to the ones connected in series the properties of the 3+1 amplifier can be adjusted in favor of higher gain or better driveability and stability.

**Figure 4.28: Design of one integrator in single-ended topology.**

The transistor sizes used are $M = 4$ for the series connected amplifier transistors and $M = 16$ for the single stage amplifier transistors. The other component values are the same as listed in table 4.1. In order to obtain a complete SDM two of the circuits shown in figure 4.28 are needed in addition to the control circuit in figure 4.26. With the two integrators and the control circuit in one common block the schematic for the first order SDM becomes as displayed in figure 4.29.
In figure 4.30 the result for the transient analysis for this integrator setup is shown.

![Figure 4.30: Transient analysis for a first order transistor sigma delta modulator in single-ended setup.](image)

Now with non ideal amplifiers made out of transistors instead of voltage controlled voltage sources it is expected that the system needs some time to settle in. From the graphs in figure 4.30 the settling time, the time it takes for $V_{in}$ and $V_{out}$ to reach $V_{CM}$ is around 500 ns. In figure 4.31 the first four nanoseconds are displayed.
As can be seen in figure 4.31 $V_{in}$ and $V_{out}$ lock on to each other very quickly which proves that the system is stable and fully functional, although $V_{out}$ is a little distorted initially. As can be seen in figure 4.32 the distortion is no longer as severe when the system has settled in properly.

Because of the $V_{CM}$ control feedback applied to the input the signal strength is decreased which results in a loss in open loop gain as can be seen in figure 4.33 where the AC analysis for this setup is displayed.
When comparing figure 4.33 to figure 4.10 one can see that the loss in open loop gain for low frequencies is quite large, an amplification factor decrease from 400 to 230. This means that the transistor system does not match the ideal system perfectly. However, that outcome was to be expected since the amplification factor of the VCVSs used in the ideal system was set to 1000 which was believed to be much more than the transistor amplifier would be able to achieve. Reaching an open loop gain of slightly more than half that of the ideal system will simply have to be considered good enough. The last analysis for the SE system that needs to be good enough before moving on to a fully differential setup is the DFT analysis displayed in figure 4.34.
Figure 4.34: Discrete Fourier transform analysis of a first order transistor sigma delta modulator in single-ended setup.

From figure 4.34 the SFDR can be measured to be roughly 70 dB. Comparing this result with previous DFT analysis for the Verilog-A (figure 4.8) and ideal systems (figure 4.13 for first order and figure 4.19 for second order) the difference is around 20 dB. The noise floors differs too, around -140 dB for the transistor design versus -160 to -150 dB for the others (excluding figure 4.13). Since the behaviour is the same as for previous results and the differences are not as important since the SE system is more a proof of concept and a test to make sure that the amplification achieved by the transistors is sufficient enough it was decided to move on to a fully differential setup.

4.2.2.2 Differential amplifier configuration

Designing a differential amplifier from a SE system is in theory not particularly difficult. Instead of connecting the source terminals of the corresponding amplifier transistors to $V_{DD}$ and $V_{SS}$ respectively (as in figure 4.28) they are connected to the drain terminals of a PMOS and NMOS bias transistor respectively. Such a setup is illustrated in figure 4.35.
By suspending the amplifier in this way between two bias transistors which acts as current limiters (basically two variable resistors) the properties of the amplifier regarding DC operating point and maximum allowed $V_{out}$ swing can be controlled. However, the biggest advantage is that this setup is much more resilient to a non-ideal voltage source or accidental voltage spikes (transients) that may occur which would damage the transistors if no precautions were taken. The maximum voltage allowed over the amplifier transistors is 0.8 V and $V_{DD}$ in the differential setup is 1.2 V. This means that a total of at least 0.4 V must be absorbed by the bias transistors. Also, $V_{CM}$ should be at around $\frac{V_{DD}}{2}$ V which means that the bias transistors should absorb 0.2 V each.

With this differential amplifier setup the desired DC offset level could be achieved in a different way compared to the ideal integrator and the SE system. A different control system method where one of the bias transistors would be controlled instead of using the input referred DC offset feedback system was previously mentioned and will be further explained. In a suspended differential setup the $V_{CM}$ can be manipulated and self regulating. This is achieved by controlling the current through the bias transistors instead of sending a feedback signal ($V_{CMfb}$) to the input as in the case of the ideal SDM and the SE system.

**4.2.2.3 Bias transistor regulators**

Two different approaches were used to manage the current limiting transistors in the differential amplifier circuits. In the first approach a mix of current mirroring and voltage division is used. A set of four transistors connected in a cross-cascode semi-diode configuration generates a fixed $V_{bias,N}$ which is fed to the NMOS bias transistors. This setup is
illustrated in figure 4.36a. At a $V_{DD}$ of 1.2 V a fixed current is obtained through the transistors which in turn generates a specific voltage drop over each transistor. In order to obtain a voltage drop of 200 mV over the NMOS bias transistors a gate voltage of close to 500 mV is required. With the specific type of transistor used in the regulator (slvt) an output voltage of 487 mV is achieved which is close enough to the 500 mV target. A few millivolts off target does not affect the system in a significant way. In this case where $V_{bias,N}$ is slightly smaller than 500 mV. The result will be an insignificant increase in voltage drop over the NMOS bias transistors, somewhere up towards 210 mV instead of 200 mV.

In the second approach illustrated in figure 4.36b feedback is used to compare $V_{CM,out}$ with $V_{CM}$. This is done with an OTA circuit which amplifies the difference between $V_{CM,out}$ and $V_{CM}$. The amplified signal $V_{bias,P}$ is fed to the gates of the corresponding bias transistors, PMOS in this case. Note that the same kind of filtering circuit and amplifier was used in the SE system apart from the bias transistors. However, in the SE system the corresponding feedback signal $V_{CM,fb}$ was connected to the input through a resistor $R_{CM}$ as can be seen in figure 4.26 and figure 4.28.

This system is self regulating and makes sure that the output $V_{CM}$ for each integrator circuit is stable and close to the input common mode voltage. If the $V_{CM,out}$ was about to drop, i.e. the equivalent resistance of the PMOS bias transistors would increase, then $V_{bias,P}$ would also drop at a much faster rate. This would affect the PMOS bias transistors and open them more.
which implies that their equivalent resistances would decrease, thus restoring the $V_{CM,\text{out}}$ to the desired voltage level.

4.2.2.4 Complete integrator using fully differential amplifiers

A total system schematic is displayed in figure 4.37. The same schematic is also found in Appendix G with better resolution.

![Figure 4.37: Schematic of one complete integrator circuit in differential setup with common mode voltage regulation.](image)

All the transistors in this system are the same size of $M = 4$ except for the single stage differential amplifier where the transistors are $M = 16$, the same ratios as for the SE system. All the other component values was the same as for the ideal integrator system. Since these component values generated good enough results for the SE system it was safe to assume that the results would not be worse when using the same values for the fully differential system. In figure 4.38 a transient analysis for this system is displayed.
According to figure 4.38 the settling time for the SDM with a fully differential integrator is close to 400 ns, around 100 ns better than for the SE system. In figure 4.39 a close up of the first 4 ns is displayed.

As can be seen it takes about 0.4 ns for $V_{out}$ to lock on to $V_{in}$ which is a ever so slightly faster than for the SE system. The big difference is that $V_{out}$ is not distorted whatsoever. $V_{CM}$ is a bit low in the beginning but stabilizes after around 400 ns according to figure 4.38. In figure 4.40 the final 4 ns are displayed.
Figure 4.40: Same as figure 4.38 but only the last four nanoseconds.

For the SE system the open loop gain dropped to a factor around 230 compared to the ideal system which open loop gain was around 400 times. This also resulted in worse noise reduction within the passband as already discussed. However, for the differential system the open loop gain was improved to an amplification factor of 300 since the $V_{CM}$ control system no longer affect the input signals which for the SE system affected the loop gain in a negative way. The AC analysis which illustrates the open loop gain for the differential system is displayed in figure 4.41.

Figure 4.41: AC analysis for the fully differential system. The result illustrates the open loop gain.

In figure 4.42 the DFT analysis for the differential system is displayed.
Figure 4.42: Discrete Fourier transform analysis for the fully differential system.

The noise floor in the passband is between -170 dB to -150 dB which is an improvement compared to the SE system. This is a consequence of the larger loop gain. Another improvement is the SFDR which for the SE system was around 70 dB compared to around 90 dB as can be seen in figure 4.41.
Chapter 5 - Method - Quantizer and DAC

5.1 System overview

The main blocks of the subsystem are highlighted in figure 5.1 and can be described as a differential flash ADC and a feedback current DAC.

The subsystem receives two inputs from the integrator subsystem of which one input is simply inverted to generate a differential input.

The VDD of the modulator is set to 1.2 V with a DC operating point at 0.6 V, and with rail-to-rail limits at 0.2 V and 1.0 V for the quantizer and DAC. This gives an operating voltage range of 0.8 V. The differential input signals from the integrator are specified with the range of 0.4-0.8 V. They are quantized through a flash ADC which outputs are connected back to the integrator through a feedback DAC, as well as to a digital block outside the modulator.

5.2 Implementation strategy

Top schematic is formed with blocks and connections that is used throughout the design process. The idea with this model is to get an overview of the system, and to verify the complete ideal functionality to use as a reference in the actual design. These blocks are designed to be configurable, so that the user can change between an ideal Verilog-A view and a completely analog transistor view.
5.3 Subsystem design

The following sections will demonstrate each block's functionality and how this is implemented in circuits with non-ideal components.

5.3.1 Flash ADC

The flash ADC consists of 31 comparators where each one is deciding whether the input signal or differential signal is the highest. 31 levels of resolution also requires 31 resistors in a ladder structure providing the reference signals according to a 5 bits flash structure. These reference voltages as well as the input signal has a range between 0.4-0.8 V. Figure 5.2 shows a part the flash ADC where two quantization levels are shown as two differential comparators.

Figure 5.2: 2 out of 31 comparators of the flash analog-to-digital converter generating two quantization levels.

5.3.2 Signal path for one quantization level

To generate one level of quantization the signal is as previously mentioned compared to a reference voltage in a synchronous comparator to further on produce a one or a zero. Moreover, this comparator output is sampled by a DFF to hold the output high for an entire clock period, and is finally analog converted through a feedback DAC as well as sent through a digital block to output a pure digital one/zero. The signal path is demonstrated in figure 5.3.

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5.3.3 Comparator

An ideal differential comparator is designed with simple Verilog-A code to compare signals, which can be found in Appendix B.

Figure 5.4 below shows the comparator in transistor schematic view containing a fully differential preamplifier and a latch.

The chosen preamplifier and latches are explained in the following two subsections where the circuit voltage levels are adjusted with DC voltage sources from 1.2 V of VDD to 1.0 V, and from 0 V of ground to a 0.2 V potential. This is shown in the circuit figures and is necessary.
in order to produce output comparator voltages of 0.8 V (full operating voltage range) with a
common-mode operating point at 0.6 V as earlier explained in 5.1. These voltage supply
adjustments are also applied at 5.3.4.

5.3.3.1 Preamplifier

The preamplifier has four inputs as earlier explained and the purpose with this subblock is to
amplify the difference between the incoming input signals and reference voltages.

The designed and evaluated prototype is illustrated in figure 5.5, where the inputs are fed to
NMOS and PMOS differential pairs that generate outputs connected through current mirrors
that are finally summed at the two output nodes \( V_{op} \) and \( V_{on} \). NMOS transistors are used
at reference input voltages above the common mode DC level which is 0.6 V, and PMOS
transistors are used at reference input voltages below 0.6 V. With this arrangement, at least
one transistor always conducts current in the differential input pair regardless what the
voltage level of the input sinusoidal is and a complete cut-off input can be avoided, to secure
a stable current flow through the circuit.

In order to provide stable DC currents, both of the current mirrors that supply the input
differential pair transistors operate in saturation. All of the input transistors are sized rather
large to obtain some gain and to reduce noise at the cost of more capacitance. They also have
low thresholds to support the current bias MOSFETs N7, N4, P6 and P8 into the saturation
region. These MOSFETs are further on dimensioned to have a drain to source voltage as low
as possible to achieve a wide operating voltage range for the amplifier, and also to fulfill the
saturation criteriums and to provide about the same currents for both of the input stages. The
sizing strategy for the rest of the preamplifier is to optimize the settling time of the
comparator. The current source is set to 200 uA which is a suitable level for this design in
order to provide enough current to drive the load and to generate fast switching times along
with the latches, and it is not too high to increase the power consumption to an unnecessarily
high level.
Figure 5.5: The preamplifier schematic integrated in the comparator with complementary NMOS and PMOS stages driven by mirrored current sources.

5.3.3.2 Latch

Two latches are being implemented and evaluated in the system, namely a semi-dynamic latch and a dynamic latch.

The semi-dynamic latch receives inputs at PMOS transistors P24 and P25 connected between voltage supply and the outputs. During the evaluation phase the clock is high and the circuit is conducting current since the lower NMOS N0 is open. The differential input voltages are regenerated into full levels VDD and VSS through the back-to-back connected CMOS
inverters and are further amplified at final CMOS stages generating the latched rail-to-rail outputs. In the reset phase, the outputs are shorted and therefore high since the connected PMOS P3 between nodes $V_{on}$ and $V_{op}$ will be open when the clock is low. The NMOS N0 is simultaneously closed so that no current is flowing through the circuit. A schematic of this latch is shown below in figure 5.6.

Figure 5.6: The semi-dynamic latch schematic integrated in the comparator.

The dynamic latch receives signals $V_{ip}$ and $V_{in}$ at its differential pair of NMOS N5 and N8 that amplifies the signal when enabled as the clock is high in evaluation mode and N0 starts to conduct current. The signal is further amplified through the back-to-back positive feedback connected CMOS inverters that also generates fast switching times. Current flows through the latch until the regeneration is complete. As in the case of the semi-dynamic latch, the outputs are generated across final CMOS stages. During the reset mode when the clock is low, both of the nodes $V_{on}$ and $V_{op}$ are pre-charged to voltage supply since the PMOS transistors P28 and P27 will conduct current, and the NMOS N0 will simultaneously be cut-off preventing current flow to VSS.

A shorted NMOS transistor is connected between both of the input NMOS drains in order to maintain correct output levels despite changes at the input signals. For instance, if $V_{on}$ is forced low when the clock is high and the input signal changes state $V_{on}$ becomes floating and sensitive to leakage current from the PMOS P21 that may result in a wrong output - when N1 is not connected. As N1 is shorted, the leakage current from the PMOS will flow through
this NMOS instead to VSS across the conducting N6. A schematic of this latch is shown in figure 5.7.

![Schematic of the dynamic latch integrated in the comparator](image)

**Figure 5.7: The dynamic latch schematic integrated in the comparator.**

The following subsections evaluates performance attributes of a comparator where the discussed preamplifier connected to the semi-dynamic latch is referred as comparator 1, and where the preamplifier connected to the dynamic latch is referred as comparator 2.

**5.3.3.3 Accuracy**

Accuracy of a comparator is as earlier mentioned equivalent to offset, metastability, resolution and noise. The offset is approximated by letting the differential inputs run between 0 mV to a maximum distance of 50 mV to their reference voltages, to verify the lowest possible distance level where the comparator can generate a valid output. The test is performed nominally as well as with 200 Monte Carlo iterations to include process and mismatch manufacturing variations. The simulation setup is presented in figure 5.8, followed by simulations of the two comparator prototypes.
Figure 5.8: Setup of the offset simulation. Differential ramped inputs with a maximum of 50 mV distance from the reference signals, sampled at the high clock rate of 16 GHz over 25 ns.
Figure 5.9: The nominally estimated offset for comparator 1 where the output is settled high within half a clock cycle. The top graph shows the clock signal, the middle graph shows the input and reference signals, and the lower graph finally shows the differential output.
Figure 5.10: 200 Monte Carlo iterations implies that a minimum distance of approximately 44 mV is required for all of the iterations to generate settled VDD outputs within half a clock cycle for comparator 2. The top graph shows the clock signal, the middle graph shows the input and reference signals, and the lower graph finally shows the differential output.

From figure 5.10, it is understood that a minimum voltage of 44 mV is required to generate a valid VDD output for all of the Monte Carlo iterations, i.e., an offset compensation of 44 mV can be used.

The result of the same test carried out for comparator model 2 is presented below in figures 5.11-5.12.
Figure 5.11: The nominally estimated offset for comparator 2 where the output is settled high within half a clock cycle. The top graph shows the clock signal, the middle graph shows the input and reference signals, and the lower graph finally shows the differential output.
Figure 5.12: 200 Monte Carlo iterations implies that a minimum distance of approximately 37 mV is required for all of the iterations to generate fully high VDD outputs within half a clock cycle for comparator 2. The top graph shows the clock signal, the middle graph shows the input and reference signals, and the lower graph finally shows the differential output.

From figure 5.12, it is in this case understood that a minimum voltage of 37 mV is required to generate a valid VDD output for all of the Monte Carlo iterations, i.e., an offset compensation of 37 mV can be used.

An input voltage range of 0.4 V with 32 levels of accuracy requires a resolution of 12.5 mV for each comparator and this is verified in an overdrive recovery test where the differential inputs are changed with 25 mV across the reference signals to check the output switching time of the comparators. This is measured in figures 5.13-5.14.
Figure 5.13: Switching time of about 21.6 ps for comparator 1, with differential opposite inputs plotted across reference voltages in the highest two windows, followed by differential outputs and a sampling clock in the two lower windows.
Figure 5.14: Switching time of about 20.9 ps for comparator 2, with differential opposite inputs plotted across reference voltages in the highest two windows, followed by differential outputs and a sampling clock in the two lower windows.

Implementation of comparators in the subsystem increases the switching times of the comparators according to figures 5.15-5.16.
Figure 5.15: Switching time of comparator 1 when implemented in subsystem, with differential opposite inputs plotted across reference voltages in the highest two windows, followed by differential outputs and a sampling clock in the two lower windows.
Figure 5.16: Switching time of comparator 2 when implemented in subsystem, with differential opposite inputs plotted across reference voltages in the highest two windows, followed by differential outputs and a sampling clock in the two lower windows.

Regarding noise, the input NMOS and PMOS transistors of the preamplifier are sized rather large for robustness. Further on, because of the preamplifier the kick-back noise from the latches does not significantly affect the input signals. However, this type of noise affects the preamplifier outputs that can possibly generate a wrong decision at the latch. The two comparator models have latches with different resistance to kick-back noise. As stated in the theory chapter, this dynamic latch prototype is fast and power efficient, but is weak concerning the kick-back noise. Demonstrating simulations are shown below in figures 5.17-5.18 of how the latches of the comparator prototypes handles kick-back noise indicated on the preamplifier outputs, where sinusoidal waves and constant reference levels act as inputs.
Figure 5.17: Kickback noise simulation with comparator 1 where clock, inputs, differentially amplified outputs and latched outputs from the top are plotted.
Moreover, simulations are shown below in figures 5.19-5.20 of how the latches of the comparator prototypes handles kickback noise indicated on the preamplifier outputs, with an overdrive recovery test.
Figure 5.19: Kickback noise simulation at an overdrive recovery test with comparator model 1 where the clock in the top row is followed by two rows of differential inputs to the comparator that further on generates amplified differential outputs and final latched outputs shown in the lowest two rows.
5.3.3.4 Power consumption

Comparator model 1 consumes an average of 1.009 mW, with 962.3 µW over the preamplifier and 46.67 µW over the semi-dynamic latch. The second prototype is slightly less power efficient with an average power consumption of 1.065 mW distributed with 962.5 µW over the preamplifier and with 102.2 µW over the dynamic latch.

A power consumption of approximately 1 mW for both of the comparators is considered as a fair result since the total limit of power consumption of the sigma delta is set to 2 W.

5.3.4 DFF

The latched output signals are being processed and sampled through DFFs in order to generate sequences of data and to further on perform an analog current summation in the feedback loop. An ideal Verilog-A model of the DFF can be found in Appendix F, and the transistor schematic is shown in figure 5.21.
When the clock is low the DFF inputs latched signals, and when the clock is high the current latched value gets locked so that new inputs are blocked. The locked value is constantly updated as a high ‘1’ or a low ‘0’ with the activated feedback path. When the clock goes low again the value is locked locked at the last stage with its value constantly updated through the feedback path. Also, new input latched values are let through at the first stage ready to be sampled when the clock once again goes high. Sampled values as well as inverted sampled values are available at the output.

All the transistors have minimum size to make the DFF as fast as possible.

### 5.3.5 Current DAC

A Verilog-A model of a current DAC is found in Appendix D, and resistors are connected to VSS at the ideal block’s differential output to terminate the current.

The analog DAC is constituted by 31 resistors in parallel connected at the DFF outputs.
A simple approach is chosen with 31 parallel connected resistors at the comparator outputs demonstrated in figure 5.22.

Figure 5.22: 31 resistors in parallel performing current summations for digital-to-analog conversion.

5.3.6 Digital output processing

The quantized sequences of bits are being sent to the feedback DAC as well as to digital Verilog-A blocks to output the quantized digital converted signal of the analog input sinusoidal. Simple Verilog-A code for these two blocks can be found in Appendix C and in Appendix D. The block schematic of the digital processing is shown in figure 5.23.

Figure 5.23: Digital processing block outside the modulator that regenerates fully digital outputs of the quantized outputs from the modulator.
5.3.7 Thermometer-to-Binary Decoder

The thermometer coded output from the comparators is translated into binary coded sequences with an ideal Verilog-A block outside the modulator. This code can be found in Appendix E.

5.3.8 Complete subsystem schematic

The top level of the subsystem is presented in figure 5.24, where two types of flash ADCs are evaluated, namely, flash 1 and flash 2. These are constituted by the first and the second comparator prototype respectively.

![Complete subsystem schematic](image)

*Figure 5.24: Complete subsystem with a flash analog-to-digital converter, sampling D-type flip-flops, resistor feedback digital-to-analog converter and finally digital Verilog-A blocks to digitize the sampled outputs, as well as to obtain the output binary sequence and a digital quantized representation of the input analog sinusoidal signal.*

Simulation of the complete subsystem with a sinusoidal differential input of 500 MHz sampled at 16 GHz is shown in figure 5.25-5.26 below, where flash 1 is used in figure 5.25 and where flash 2 is used in figure 5.26.
Figure 5.25: Subsystem simulation using flash 1 where the differential input and output has been plotted along with the highlighted digital output.
Moreover, a simulated timing diagram of the sampling process for one comparator is presented in figure 5.27 with signals marked next to the y-axis. In this case, the comparator 2 prototype is used.
Verification of the thermometer decoding of the flash ADC as well as the followed up binary decoding is presented in figure 5.28, where an input ramp with a frequency of 10 MHz has been used for visual clarification.
5.3.9 Subsystem measurements

A DFT simulation across the analog differential feedback is presented in figure 5.29, with a pre-layout simulation where capacitances have been added to the circuit to obtain a more realistic view of the plot on a potential layout level. As seen in the plot the inband spuriouses have low power while the spuriouses are significantly higher outside the signal band above 500 MHz.

Figure 5.28: The digital binary translation verified with an input ramp signal of 10 MHz.
Figure 5.29: Discrete Fourier transform plot across the analog differential feedback.

A DFT simulation with 80 Monte Carlo iterations is presented in figure 5.30, where a lower SNR performance is reached.
Figure 5.30: Discrete Fourier transform plot at the differential analog output with 80 Monte Carlo iterations.
Chapter 6 - Results

The block schematic of the modulator is shown in figure 6.1 below.

![Block schematic of the modulator](image)

**Figure 6.1: The complete sigma delta modulator.**

A complete test simulation of the modulator is carried out where mismatch errors due to process variations are also included to get a realistic picture of the design functionality.

Mismatches during the manufacturing process can be simulated with a Monte Carlo analysis. This type of simulation evaluates a large number of combinations of errors in the manufacturing process. Mismatch errors and process variations are simulated with a Monte Carlo test in a pre-layout configuration, so that capacitances are added to simulate these disturbances that appear in a layout level. Both process variations and mismatch variations are covered in a test that includes thirty iterations.

To measure the signal’s relation to spuriouses, a DFT is plotted. Frequencies up to 500 MHz are of interest and frequencies above are considered to be filtered out. To verify the functionality of the modulator a shaped noise slope shall appear within this band, where the Signal-to-Noise ratio can be calculated by dividing the signal power by the integrated noise floor. SFDR, i.e the distance between the signal tone and the nearest highest tone within the signal band can be obtained directly from the plot.

A complete pre-nominal simulation is performed in figures 6.2-6.4 below, with input signal frequencies of 500 MHz, 250 MHz and 100 MHz sampled at 16 GHz.
Figure 6.2: Pre-layout nominal simulation with an input signal frequency of 500 MHz sampled at 16 GHz. The first window shows the differential input to the modulator followed by the output signals from the feedback digital-to-analog converter in the second window and the integrator output signals in the third window. Finally, the completely digital output is shown in the fourth window.
Figure 6.3: Pre-layout nominal simulation with an input signal frequency of 250 MHz sampled at 16 GHz. The first window shows the differential input to the modulator followed by the output signals from the feedback digital-to-analog converter in the second window and the integrator output signals in the third window. Finally, the completely digital output is shown in the fourth window.
Figure 6.4: Pre-layout nominal simulation with an input signal frequency of 100 MHz sampled at 16 GHz. The first window shows the differential input to the modulator followed by the output signals from the feedback digital-to-analog converter in the second window and the integrator output signals in the third window. Finally, the completely digital output is shown in the fourth window.

A DFT plot of the pre-nominal simulation at the digital output signal of the modulator is presented in figure 6.5, where an SNDR within the signal band of approximately 50 dB is achieved.
Figure 6.5: A pre-layout nominal simulation at the digital output of the quantizer with a plotted discrete Fourier transform having an input signal frequency of 500 MHz sampled at 16 GHz.

The same simulation as in previous figure at the feedback analog differential signal is presented below in figure 6.6 where an SNDR within the signal band of approximately 62 dB is achieved.
In figure 6.7 below, a DFT plot of a Monte Carlo simulation at the digital output of the modulator is shown with 30 iterations.
Figure 6.7: A Monte Carlo simulation with 30 iterations at the digital output of the quantizer with a plotted discrete Fourier transform having an input signal frequency of 500 MHz sampled at 16 GHz.

In figure 6.8, a DFT of a Monte Carlo simulation at the analog differential feedback of the modulator is shown with 30 iterations.
Figure 6.8: A Monte Carlo simulation with 30 iterations at the differential analog output of the digital-to-analog converter with a plotted discrete Fourier transform having an input signal frequency of 500 MHz sampled at 16 GHz.

The Monte Carlo simulations in figures 6.7-6.8 shows that the SNDR has decreased in performance with a higher noise floor resulting in SNDRs within the band of interest of approximately 38 dB in figure 6.7 and 41 dB in figure 6.8.

A total average power consumption of 75 mW is achieved for the complete modulator, with the following distribution in figure 6.9:
Figure 6.9: The total average power consumption of 75 mW distributed over the system as 46.5% across the quantizer and 53.5% across the integrator.
Chapter 7 - Discussion

7.1 Methodologies

The top-down strategy of construction gives a clear picture of the architecture of the system starting with blocks of simple code. However, the real job effort obviously lies on the hardware design. Instead of having more or less guaranteed solutions to implement this has been an exploring experimental task. By reason around different design methods where some have been tried out with different levels of descent results, a functioning complete system was finally reached.

In Chapter 4 an inverter style amplifier structure was chosen for the integrator. The reasoning behind that choice was that speed is more important than gain. If the amplifier has too much delay the ELD will be worse resulting in a SDM that does not fulfill the required sampling speed of 16 GS/s. Other amplifier structures such as an operational transconductance amplifier (OTA) were considered but during simulation of a 3+1 OTA integrator the intermediate DC levels became a serious problem resulting in very poor gain. Couple that with the extra complexity of the circuit it was decided to use inverter style amplifiers exclusively for the integrator.

A second order SDM using two equal fully differential integrator circuits (one resistor value was changed as described in the ideal integrator section) was attempted. Although it worked and yielded quite good results when using Verilog-A quantizer and DAC the results will be left out since a first order SDM gave satisfactory results. When running at 16 GHz the ELD became a limiting factor when implementing a second order SDM in the complete system setup with non ideal quantizer and DAC circuits. If the system could be running at a lower clock frequency the second order SDM would have worked since the only problem holding it back was the ELD.

Challenges with the quantizer includes finding a suitable architecture for a this sigma delta modulator. The architecture of the double differential preamplifier was not obvious because of the range of input voltages. Also, a feedback common-mode regulator was considered but was not included in the final design. By excluding a common-mode feedback regulator some power and area were saved.

The design of the latch resulted in a semi-dynamic class AB latch and a dynamic latch, hence two comparator prototypes. The dynamic latch comparator was used in the final system simulations because of its faster rise and fall time and because its lower contribution of distortion in the modulator loop comparing to the semi-dynamic latch comparator. Measuring the power consumption reveals that the comparators consume about the same amount of
power which probably depends on the very high sampling clock frequencies. At some lower frequencies the dynamic latch has superior power efficiency.

The prior was focused on the quantizing part and to maintain some simplicity to be able to finish and put together an entire sigma delta modulator, hence, a very simple DAC solution of resistors in parallel was realized as a feedback path. Aside from its simplicity, the output impedance is held constantly equal and a longer propagation delay across switches and control logic can be avoided. The voltage output swing from the DAC between 0.2-1 V is matched to the feedback input swing at the integrator of 0.4-0.8 V by sizing the value of the DAC resistors twice as high to obtain same currents.

7.2 Results

The complete simulations of the modulator gave expected results with a regenerated quantized output of the input sinusoidal wave. The input signal is set to half of the specified swing in order to keep the system stable. As mentioned in Chapter 4, the reason for this is that the results for a first and second order SDM should be comparable. Since the intermediate integrator differential signal for a second order system (the signal between the two integrators) became 1.5 times the amplitude of the input signal, because of the k-factor described in Chapter 4, the amplitude of the signal needed to be reduced in order to prevent distortion. The distortion would occur because of the reduced \( V_{DS} \) over the amplifier transistors which requires a voltage drop at least 200 mV of \( V_{DS} \) to work properly. This intermediate signal amplification is visible in figure 4.17. If the input signal amplitude would be set to full swing (400 mV peak-peak) the intermediate signal would be 600 mV peak-peak which would result in a \( V_{DS} \) of only 100 mV for each amplifier transistor since they work in a 800 mV span. With the input signal set to 200 mV peak-peak there was room for the intermediate integrator signal.

At higher input frequencies the signal is distorted which may partly depend on excess loop delay. Using an ideal ADC and DAC where a delay is intentionally set at the quantizer results in the very same distorted pattern as in the case of a complete non-ideal transistor modulator. Figures 6.2-6.4 shows the distortion upon the signal at three levels of input frequencies.

DFT plots demonstrating the signal’s relation to spurious are more or less accurate depending on the resolution of the simulator which affects performance numbers such as SNDR and ENOB. An estimation of ENOB across the differential output of the DAC can be set to 10 effective number of bits at nominal conditions according to figure 6.6.

The remarkably lower power consumption of 75 mW compared to 890 mW in the reference specification may depend on the fact that no MASH structure nor higher modulator order were implemented in this ADC, and because of no layout was realized with additional chip frames. Anyhow, the final complete power consumption is considered low.
7.3 Ethics

Modern high technological RFIC devices contributes to faster communication possibilities for IoT products, mobile phones and even for medical equipments. This particular technological field only covers a small working area of electrical engineering, which is one of the reasons to why this is an important occupation for today’s society. Moreover, this profession shall be applied to companies with healthy and open ethical stands where no irregularities are even possible as that may have a large impact on our society.

Regarding the SDM developed during this thesis, it is a universal tool designed to be implementable in a wide variety of products. Where or in what type of products it may end up being implemented is beyond the responsibility of the authors, no matter if it ends up in constructive or destructive applications.

7.4 Source criticism

Material for this thesis has been collected from dissertations and master thesis with some of them suggested by Ericsson. Also, a lot of information is referred to a well recognized book within this area “Design of Analog CMOS Integrated Circuits” by Behzad Razavi [2]. Finally some smaller amount of information was retrieved from National Instruments. Well cited sources have been used to the largest extent possible.

Sources have been chosen from their truthfulness and relevance to the subject. This thesis has involved a lot of practical work with Cadence as a reliable IC design tool with accurate simulations taking non idealities into account.

7.5 Future work

Although problems with DC offset was much more profound when using OTA amplifiers in the integrator compared to inverter style amplifiers there is room for improvement. Perhaps if a different DC control system was used the OTA amplifier would work with possibly even better gain which would result in even better performance from the SDM.

An offset compensation at the comparators of the quantizer can be implemented to generate even more accurate decisions, as well as a common-mode feedback regulator to ensure a fixed common-mode level and non-varying gain independent of the input voltage levels.

As previously explained, a functioning modulator of a second or third order gives a higher SNR and output resolution and can for that matter be considered as a continuation of the construction. A MASH structure can also be implemented to push out noise out of the signal band with more efficiency and to make the system even more stable. A decimation block outside the modulator has not been included in this system and is necessary to implement in order to have practical use of this ADC at reasonable frequencies in an RF receiver.
Because of some distorting excess loop delay in the modulator, there are some improvement possibilities to consider in a future work scenario. Firstly, the delay time over the quantizer and feedback path may be shorter by moving the DFF outside the modulator. By implementing an interleaving arrangement using two flash quantizers in parallel receiving one differential input each, there is no longer a dependency on the reset signal between each new input sample slowing down the system, and half the sampling speed would be used resulting in less sensitivity to distortion because of excess loop delay.

Finally, the resistance at the integrator feedback input causes different voltage drops depending on the current of the analog signal which results in non-linearities at the feedback integrator input. Therefore, these resistors can be removed while sizing the DAC resistors to a higher value instead to match the current.
Chapter 8 - Bibliography

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Chapter 9 - Appendices

In order to provide better understanding for the reader the content of the Verilog-A files are provided in appendix A through F. A complete schematic of an integrator circuit is also displayed in appendix G.

9.1 Appendix A: Verilog-A code for the integrator sub system

```verbatim
// Verilog-A for Integrator, verilog_integrator_2, Verilog-A

`include "constants.vams"
`include "disciplines.vams"

module verilog_integrator_2(vin, vip, von, vop, vcm, vdd, vss, fbn, fbp);
    input vin, vip, fbn, fbp;
    inout vdd, vcm, vss;
    output von, vop;
    electrical vin, vip, von, vop, vdd, vcm, vss, fbn, fbp;

    parameter real nn0 = 1;
    parameter real nd0 = 0;
    parameter real nd1 = 1;
    parameter real ngain = 1;
    parameter real pn0 = 1;
    parameter real pd0 = 0;
    parameter real pd1 = 1;
    parameter real pgain = 1;
    //parameter real vcm = 0; //Set to input signal DC offset (Vcm)
    parameter real AC_ampl = 0;
    parameter real AC_freq = 0;
    parameter integer vout_two_PI_correction = 0 from [0:1];
    parameter integer C_correction = 1 from [-1:1];
    parameter integer vcm_correction = 1 from [0:1];
    parameter real fb_gain = 1;

    real ngain_i = ngain*(`M_TWO_PI**vout_two_PI_correction);
    real pgain_i = pgain*(`M_TWO_PI**vout_two_PI_correction);
    real vin_i, vip_i;
    analog begin
        vin_i = (V(vin) - vcm_correction*V(vcm)) - fb_gain*(V(fbn) - vcm_correction*V(vcm));
        vip_i = (V(vip) - vcm_correction*V(vcm)) - fb_gain*(V(fbp) - vcm_correction*V(vcm));

        V(von) <+ (ngain_i*laplace_nd (vin_i, [nn0], [nd0, nd1]) - C_correction*ngain_i*(AC_ampl/(2*`M_TWO_PI*AC_freq)) + vcm_correction*V(vcm));
        V(vop) <+ (pgain_i*laplace_nd (vip_i, [pn0], [pd0, pd1]) +
```
```
\[ \text{C} \_\text{correction} \* \text{pgain} \_i \* (\text{AC} \_\text{ampl}/(2 \* \text{M} \_\text{TWO} \_\text{PI} \* \text{AC} \_\text{freq}) \) + \text{vcm} \_\text{correction} \* \text{V}(\text{vcm}); \]

9.2 Appendix B: Verilog-A code for the ideal comparator block

// Verilog-A for ADC_DAC, comparator2, Verilog-A

`include "constants.vams"
`include "disciplines.vams"

module comparator2(Von_rail2rail, Vop_rail2rail, vdd, vss, Vin, Vip, clk, vref_neg, vref_pos);

inout vdd;
inout vss;
input Vin, vref_pos, Vip, vref_neg, clk;
output Von_rail2rail, Vop_rail2rail;

electrical Vin, vref_pos, Vip, vref_neg, clk, Von_rail2rail, Vop_rail2rail,
vdd, vss;

parameter real vlogic_high=1;
parameter real vlogic_low=0.2;
parameter real vtrans_clk=0.6;
parameter real vtrans = 0.6;
parameter real tdel = 1p; //tdel = 36.5, 26.5
parameter real trise = 1p;
parameter real tfall = 1p;

real result_pos;
real result_neg;

analog begin
 @((\text{cross}(\text{V}(\text{clk}) - \text{vtrans_clk}, +1 )) begin
  if (\text{V}(\text{Vip}) >= \text{V}(\text{vref_pos})) begin
   result_pos = \text{V}(\text{vdd});
   result_neg = \text{V}(\text{vss});
  end
  else begin
   result_pos = \text{V}(\text{vss});
   result_neg = \text{V}(\text{vdd});
  end

  \text{V}(\text{Vop_rail2rail}) \leftrightarrow \text{transition}(\text{result_pos, tdel, trise, tfall});
  //result, delay, ttime

  end

endmodule
\( V(\text{Von_rail2rail}) \leftrightarrow \text{transition}(\text{result}_\text{neg}, \text{tdel}, \text{trise}, \text{tfall}) \);

//result, delay, ttime

end

dendum

9.3 Appendix C: Verilog-A code for the digital regeneration block

// Verilog-A for ADC_DAC, digital_output, Verilog-A

'include "constants.vams"
'include "disciplines.vams"

module digital_output(vdd, vss, analog_sampled, clk, digital_sampled);

inout vdd;
inout vss;
input clk;
input analog_sampled;
output digital_sampled;

electrical vdd, vss, clk;
electrical analog_sampled;
electrical digital_sampled;

parameter real vlogic_high=1;
parameter real vlogic_low=0.2;
parameter real vtrans_clk=0.6;
parameter real vtrans = 0.6;
parameter real tdel = 1p;
parameter real trise = 1p;
parameter real tfall = 1p;

real result = 0.2;
real analog_sampled_tmp;

analog begin
  @(cross(V(clk) - vtrans_clk, +1 )) begin
    analog_sampled_tmp = V(analog_sampled);
    if (analog_sampled_tmp > vtrans)
      result = V(vdd);
    else
      result = V(vss);
  end
V(digital_sampled) <+ transition(result, tdel, trise, tfall);
end

dendum
9.4 Appendix D: Verilog-A code for the ideal DAC block

`include "constants.vams"
`include "disciplines.vams"

module idealDAC(vop_analog, vop_sampled);
output vop_analog;
electrical vop_analog;
input vop_sampled;
electrical vop_sampled;

parameter real vtrans_clk = 0.6;
parameter real vtrans = 0.6;
parameter real tdel = 1p;
parameter real trise = 1p;
parameter real tfall = 1p;
parameter real Ibias=0;

real tmp;

analog begin
    if(V(vop_sampled) > vtrans) begin
        tmp = 0.8;
    end
    if (V(vop_sampled) < vtrans) begin
        tmp = 0;
    end
    I(vop_analog) <+ -Ibias * transition(tmp, tdel, trise, tfall);
end
endmodule

9.5 Appendix E: Verilog-A code for the thermometer-to-binary decoder block

`include "constants.vams"
`include "disciplines.vams"

module verilog_therm_to_bin_31_levels (vi31, vi30, vi29, vi28, vi27, vi26, vi25, vi24, vi23, vi22, vi21, vi20, vi19, vi18, vi17, vi16, vi15, vi14, vi13, vi12, vi11, vi10, vi09, vi08, vi07, vi06, vi05, vi04, vi03, vi02, vi01, vo4, vo3, vo2, vo1, vo0);
input vi31, vi30, vi29, vi28, vi27, vi26, vi25, vi24, vi23, vi22, vi21, vi20, vi19, vi18, vi17, vi16, vi15, vi14, vi13, vi12, vi11, vi10, vi09, vi08, vi07, vi06, vi05, vi04, vi03, vi02, vi01;
output vo4, vo3, vo2, vo1, vo0;
electrical vi31, vi30, vi29, vi28, vi27, vi26, vi25, vi24, vi23, vi22, vi21, vi20, vi19, vi18, vi17, vi16, vi15, vi14, vi13, vi12, vi11, vi10, vi09, vi08, vi07, vi06, vi05, vi04, vi03, vi02, vi01, vo4, vo3, vo2, vo1, vo0;

parameter real vtrans = 0.6;
parameter real vlogic_high = 1;
parameter real vlogic_low = 0.2;
real vo4int, vo3int, vo2int, vo1int, vo0int;

analog begin
  if (vtrans < V(vi31)) begin
    vo4int = vlogic_high;
    vo3int = vlogic_high;
    vo2int = vlogic_high;
    vo1int = vlogic_high;
    vo0int = vlogic_high;
  end
  else if (vtrans < V(vi30)) begin
    vo4int = vlogic_high;
    vo3int = vlogic_high;
    vo2int = vlogic_high;
    vo1int = vlogic_high;
    vo0int = vlogic_low;
  end
  else if (vtrans < V(vi29)) begin
    vo4int = vlogic_high;
    vo3int = vlogic_high;
    vo2int = vlogic_high;
    vo1int = vlogic_low;
    vo0int = vlogic_high;
  end
  else if (vtrans < V(vi28)) begin
    vo4int = vlogic_high;
    vo3int = vlogic_high;
    vo2int = vlogic_high;
    vo1int = vlogic_low;
    vo0int = vlogic_low;
  end
  else if (vtrans < V(vi27)) begin
    vo4int = vlogic_high;
    vo3int = vlogic_high;
    vo2int = vlogic_low;
    vo1int = vlogic_high;
    vo0int = vlogic_high;
  end
  else if (vtrans < V(vi26)) begin
  end
end
else if (vtrans < V(vi26)) begin
vo4int = vlogic_high;
vo3int = vlogic_high;
vo2int = vlogic_low;
vo1int = vlogic_high;
vo0int = vlogic_low;
end
else if (vtrans < V(vi25)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_high;
  vo2int = vlogic_low;
  vo1int = vlogic_low;
  vo0int = vlogic_high;
end
else if (vtrans < V(vi24)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_high;
  vo2int = vlogic_low;
  vo1int = vlogic_low;
  vo0int = vlogic_low;
end
else if (vtrans < V(vi23)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_low;
  vo2int = vlogic_high;
  vo1int = vlogic_high;
  vo0int = vlogic_high;
end
else if (vtrans < V(vi22)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_low;
  vo2int = vlogic_high;
  vo1int = vlogic_high;
  vo0int = vlogic_low;
end
else if (vtrans < V(vi21)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_low;
  vo2int = vlogic_high;
  vo1int = vlogic_low;
  vo0int = vlogic_high;
end
else if (vtrans < V(vi20)) begin
  vo4int = vlogic_high;
  vo3int = vlogic_low;
  vo2int = vlogic_high;
  vo1int = vlogic_low;
  vo0int = vlogic_low;
end
else if (vtrans < V(vi19)) begin
  vo4int = vlogic_high;

vo3int = vlogic_low;
vo2int = vlogic_low;
vo1int = vlogic_high;
vo0int = vlogic_high;
end
else if (vtrans < V(vi18)) begin
vo4int = vlogic_high;
vo3int = vlogic_low;
vo2int = vlogic_low;
vo1int = vlogic_high;
vo0int = vlogic_low;
end
else if (vtrans < V(vi17)) begin
vo4int = vlogic_high;
vo3int = vlogic_low;
vo2int = vlogic_low;
vo1int = vlogic_low;
vo0int = vlogic_high;
end
else if (vtrans < V(vi16)) begin
vo4int = vlogic_high;
vo3int = vlogic_low;
vo2int = vlogic_low;
vo1int = vlogic_low;
vo0int = vlogic_low;
end
else if (vtrans < V(vi15)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_high;
vo1int = vlogic_high;
vo0int = vlogic_high;
end
else if (vtrans < V(vi14)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_high;
vo1int = vlogic_high;
vo0int = vlogic_high;
end
else if (vtrans < V(vi13)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_high;
vo1int = vlogic_low;
vo0int = vlogic_high;
end
else if (vtrans < V(vi12)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_high;
vo1int = vlogic_high;
vo0int = vlogic_low;
end
vo2int = vlogic_high;
vo1int = vlogic_low;
vo0int = vlogic_low;
end
else if (vtrans < V(vi11)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_low;
vo1int = vlogic_high;
vo0int = vlogic_high;
end
else if (vtrans < V(vi10)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_low;
vo1int = vlogic_high;
vo0int = vlogic_low;
end
else if (vtrans < V(vi09)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_low;
vo1int = vlogic_low;
vo0int = vlogic_high;
end
else if (vtrans < V(vi08)) begin
vo4int = vlogic_low;
vo3int = vlogic_high;
vo2int = vlogic_low;
vo1int = vlogic_low;
vo0int = vlogic_low;
end
else if (vtrans < V(vi07)) begin
vo4int = vlogic_low;
vo3int = vlogic_low;
vo2int = vlogic_high;
vo1int = vlogic_high;
vo0int = vlogic_high;
end
else if (vtrans < V(vi06)) begin
vo4int = vlogic_low;
vo3int = vlogic_low;
vo2int = vlogic_high;
vo1int = vlogic_high;
vo0int = vlogic_low;
end
else if (vtrans < V(vi05)) begin
vo4int = vlogic_low;
vo3int = vlogic_low;
vo2int = vlogic_high;
end
volint = vlogic_low;
vo0int = vlogic_high;
end
else if (vtrans < V(vi04)) begin
  vo4int = vlogic_low;
  vo3int = vlogic_low;
  vo2int = vlogic_high;
  vo1int = vlogic_low;
  vo0int = vlogic_low;
end
else if (vtrans < V(vi03)) begin
  vo4int = vlogic_low;
  vo3int = vlogic_low;
  vo2int = vlogic_low;
  vo1int = vlogic_high;
  vo0int = vlogic_high;
end
else if (vtrans < V(vi02)) begin
  vo4int = vlogic_low;
  vo3int = vlogic_low;
  vo2int = vlogic_low;
  vo1int = vlogic_high;
  vo0int = vlogic_low;
end
else if (vtrans < V(vi01)) begin
  vo4int = vlogic_low;
  vo3int = vlogic_low;
  vo2int = vlogic_low;
  vo1int = vlogic_low;
  vo0int = vlogic_high;
end
else begin
  vo4int = vlogic_low;
  vo3int = vlogic_low;
  vo2int = vlogic_low;
  vo1int = vlogic_low;
  vo0int = vlogic_low;
end

V(vo4) <+ vo4int;
V(vo3) <+ vo3int;
V(vo2) <+ vo2int;
V(vo1) <+ vo1int;
V(vo0) <+ vo0int;
end
endmodule
9.6 Appendix F: Verilog-A code for the thermometer-to-binary decoder block

// Verilog-A for ADC_DAC, DFF_master_slave, Verilog-A

`include "constants.vams"
`include "disciplines.vams"

module DFF_master_slave(Q, D, clk, vdd, vss);
output Q;
electrical Q;
input D;
electrical D;
input clk;
electrical clk;
input vdd;
electrical vdd;
input vss;
electrical vss;

parameter real vlogic_high = 1;
parameter real vlogic_low = 0.2;
parameter real vtrans_clk = 0.6;
parameter real vtrans = 0.6;
parameter real tdel = 1p;
parameter real trise = 1p;
parameter real tfall = 1p;

integer x;

analog begin
  @ (cross( V(clk) - vtrans_clk, +1 ))
  x = (V(D) > vtrans);
  V(Q) <+ transition( vlogic_high*x + vlogic_low!*x,
                      tdel, trise, tfall );
end

endmodule
9.7 Appendix G: Schematic of the fully differential integrator