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Stress-induced Charge Trapping and Electrical Properties of Atomic-Layer-Deposited HfAlO/Ga₂O₃ MOS capacitors

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Abstract: Electrical properties and trapping characteristics of atomic layer deposited Al-rich HfAlO/ β -Ga₂O₃ capacitor were evaluated via constant-voltage stress (CVS), capacitance-voltage (C-V), and current-voltage (I-V) measurements. The magnitude of the stress-induced charge trapping increases with increasing voltage and time. The effective charges (N_{eff}) including the “border” traps located in near-interface oxide, interface traps (D_{it}) of HfAlO/ β -Ga₂O₃ interface, and fixed charges contribute significantly to the observed charge trapping, and it is found that interface traps contribute more under large stress bias, compared with “border” traps. In addition, the effective charge density is increased with stress time, implying that the contribution of negative effect defect during CVS process could not be negligible. Measurements of high permittivity (10.74), great interface quality ($D_{it} \sim 1 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$), and small gate leakage ($1.18 \times 10^{-5} \text{ A/cm}^2$ at +10 V) has been extracted, suggesting the great electrical properties of Al-rich HfAlO/ β -Ga₂O₃ MOSCAP. According to the above analysis, Al-rich HfAlO is an attractive candidate for normally off Ga₂O₃ transistors.

Keywords

Gallium Oxide, HfAlO/Ga₂O₃ MOSCAP, Oxide traps, constant-voltage stress.

1. Introduction

Gallium oxide (Ga₂O₃) is one of the promising wide bandgap materials for the next generation power electronics due to its ultra-wide bandgap (E_g) of 4.6-4.9 eV, high theoretical breakdown field (E_{br}) of 8 MV/cm, and high Baliga's Figure of Merit (BFOM) compared with the current research hotspot materials such as SiC and GaN.^[1-3] Besides excellent material properties, the simple, low-cost, and mature melt-growth methods for large-area Ga₂O₃ wafers offers Ga₂O₃ an economic advantage over other ultra-wide bandgap semiconductors such as AlN and diamond.^[2-3] Recently, metal-oxide-semiconductor field-effect transistors (MOSFET) and Schottky barrier diodes (SBD) based on β -phase Ga₂O₃ have been intensively investigated^[4-11] for power application. For instances, A. J. Green *et al.* measured an average E_{br} of 3.8 MV/cm in β -Ga₂O₃ MOSFETs, which surpasses the theoretical limits of GaN and SiC^[4], K. Zeng *et al.* achieved their Ga₂O₃ MOSFETs using composite field-plate design with an average E_{br} of 2.2 MV/cm and breakdown voltage (V_{br}) of 1.85 kV^[5], Mg-ion implantation has been systematically investigated with first-principle simulation^[6] and experiment^[7], and applied to achieve a record vertical Ga₂O₃ MOSFETs^[8] by M. H. Wong *et al.*; and Z. Hu, H. Zhou *et al.* produced β -Ga₂O₃ SBDs on sapphire substrate via transferring β -Ga₂O₃ nano-membrane channel with record V_{br} of 3 kV^[9]. In general, gate stack quality and field plate design are crucial to the performance of Ga₂O₃-based devices including MOSFET and SBD with field plate design, meanwhile, charge trapping in the gate dielectric affects critical device parameters, such as mobility, gate leakage, gate-oxide quality, etc.

To our knowledge, Al_2O_3 or SiO_2 gate dielectric^[4,5,8,10,11] have been widely used for Ga_2O_3 MOS devices for the sufficient conduction band offset (ΔE_c) of $\text{Al}_2\text{O}_3/\text{Ga}_2\text{O}_3$ (1.5-1.7 eV)^[12,13] and $\text{SiO}_2/\text{Ga}_2\text{O}_3$ (3.6 eV)^[14]. Compared with Al_2O_3 , SiO_2 , various high- k materials (such as HfO_2 , ZrO_2 , and La_2O_3) with large permittivity (12~24), good thermodynamic stabilities, and high crystallization temperature could be also used as gate oxide of Ga_2O_3 power device for achieving lower effective oxide thickness (EOT) and high critical electric field. In our previous work^[15,16], Hf-based high- k materials (HfO_2 , and HfAlO with different Hf:Al ratio) are prove to be attractive gate oxide candidate for Ga_2O_3 power device. Furthermore, we had found that Al-rich HfAlO ^[15] dielectric possess sufficient band offsets with $\beta\text{-Ga}_2\text{O}_3$ substrate, and owns reported higher crystallization temperature^[17,18] in HfAlO/SiC structure, making it suitable for prospective Ga_2O_3 -based MOS devices. In this study, the further analyzes of Al-rich $\text{HfAlO}/\beta\text{-Ga}_2\text{O}_3$ capacitor are provided, including electrical properties and charge trapping on $\text{HfAlO}/\beta\text{-Ga}_2\text{O}_3(-201)$ interface.

Understanding the electrical properties of the oxide- Ga_2O_3 interfaces under either normal condition or constant voltage stress is important for developing Ga_2O_3 MOS devices, which impact critical parameters such as threshold voltage, channel mobility, and device stability. Analyses of the interface state density at the interface between $\beta\text{-Ga}_2\text{O}_3$ and atomic layer deposition (ALD) or Low-Pressure Chemical Vapor Deposition (LPCVD) SiO_2 ^[19,20], ALD Al_2O_3 ^[13,19,21], and ALD HfO_2 ^[16,22] dielectrics have been reported recently, particularly, there are already many systematical works^[13,19,21] about the electrical properties, interface trap, and stress-induced charge trapping of the $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ MOS structures, but only a few work^[21] focus on stress-induced reliability of the $\beta\text{-Ga}_2\text{O}_3$ MOS capacitor. In this work, $\beta\text{-Ga}_2\text{O}_3$ MOS capacitors (MOSCAP) with ALD-derived HfAlO dielectric were fabricated, and the responses to constant voltage stress (CVS) of $\text{HfAlO}/\text{Ga}_2\text{O}_3$ MOS structure were evaluated via capacitance-voltage (C-V) and current-voltage (I-V) methods. The results exhibit that Al-rich $\text{HfAlO}/\text{Ga}_2\text{O}_3$ MOS has attractive characteristics, which are a low gate leakage, high effective breakdown field, and proper dielectric constant of gate oxide film. Then, constant voltage stress measurements show that electron-trap densities are increased for increasing positive stress voltages, and stress-induced traps are found to be located primarily in HfAlO gate dielectric layer and $\text{HfAlO}/\text{Ga}_2\text{O}_3$ interface, and to be distributed broadly with the stress time and/or the stress bias. Further analyze reflects the effective oxide charges (N_{eff}) including the “border” traps, fixed charges, and interface traps (D_{it}) contribute significantly to the observed charge trapping, which is different with previous report in $\text{Al}_2\text{O}_3/\beta\text{-Ga}_2\text{O}_3$ interface^[21].

2.Devices and experiments

2-inch $\beta\text{-Ga}_2\text{O}_3$ wafer (680 μm thick, unintentionally-doped (UID) n-type doping concentration (N_d) of $\sim 2.60 \times 10^{17} \text{ cm}^{-3}$, extracted from the slope of $1/C^2$ versus V ^[14,23]) with a polished surface were used to fabricate Al-rich $\text{HfAlO}/\text{Ga}_2\text{O}_3$ MOS structure. Before gate dielectric deposition, the substrate were diced into small pieces (5 mm $\times$ 5 mm), then solvent clean (acetone/isopropanol/deionized water) was carried out followed by Piranha pretreatment (98% H_2SO_4 + 30% H_2O_2 1:1) for 2 min. Piranha pretreatment^[19] has been consider as effective pretreatment on $\text{Al}_2\text{O}_3/\text{Ga}_2\text{O}_3$ or $\text{SiO}_2/\text{Ga}_2\text{O}_3$ interface. The deposition of ALD HfAlO layer was performed by depositing alternating cycles of HfO_2 and Al_2O_3 at 250 $^\circ\text{C}$ with a Beneq TFS200 ALD System. The thickness of HfAlO film (30.71 nm) was measured on a Si monitor wafer by spectroscopic ellipsometry (SE) with an error of 0.4~2%. The precursors $\text{Hf}(\text{NCH}_3(\text{C}_2\text{H}_5))_4$ (TEMAH) and H_2O were used for ALD- Al_2O_3 film, and ALD- HfO_2 films were deposited using $[(\text{CH}_3)_3\text{Al}]_2(\text{TMA})$ and H_2O precursors, the ALD cycle ratio of $\text{HfO}_2/\text{Al}_2\text{O}_3$ was 1:4. Prior to ALD process, the backside Ti (40 nm)/Au (200

nm) ohmic contacts were deposited followed by rapid thermal annealing at N₂ atmosphere (500°C, 3min) to decrease the ohmic contact resistance^[1516]. Following ALD deposition, Ni (20 nm)/Au (230 nm)/Ni (20 nm) circular gate electrodes^[12] (electrode area: $4.9 \times 10^{-3} \text{ cm}^2$.) were formed by physical vapor deposition (PVD).

The capacitance-voltage (C-V), current-voltage (I-V) measurements and constant-voltage stress characteristics of MOSCAPs were measured using Agilent 1500A semiconductor parameter analyzer with Cascade Probe Station. It is worth mentioned that all the above measurements were implemented at room temperature in a shield dark box to isolate the ambient noise as much as possible. In addition, material characterization like the X-Ray Photoelectron Spectroscopy (XPS), Atomic force microscopy (AFM), and X-ray diffraction (XRD) measurement were widely used to characterize material properties and Surface morphology^[12-14,24-25]. In our experiment, AFM and XRD were used to characterize $\beta\text{-Ga}_2\text{O}_3$ (-201) crystals and HfAlO films. The XRD analysis was conducted in a Bruker D8 Advance diffractometer system with $K\alpha$ radiation at 40 kV and 40 mA. It was observed from Fig. 1(a-b) that the surface roughness (rms=0.25 nm, 0.41 nm, respectively) values of Ga₂O₃ wafers and HfAlO films were both relatively small, indicating the smooth surface of $\beta\text{-Ga}_2\text{O}_3$ and HfAlO. For XRD characterization, as shown in Fig. 1(c), two sharp peaks (locate at 18.78°, 38.24°) are represent (-201) and (-402) orientation, corresponding to (-201)-oriented β -phase of Ga₂O₃.

FIG. 1. AFM measurement of the surface roughness before ALD HfAlO on $\beta\text{-Ga}_2\text{O}_3$ substrate (a), AFM measurement of the surface roughness after ALD HfAlO on $\beta\text{-Ga}_2\text{O}_3$ substrate (b), and (c) XRD pattern of bulk $\beta\text{-Ga}_2\text{O}_3$.

3.Result and discussion

3.1Electrical properties of MOS sample

Figure 2 shows the electrical properties of the HfAlO/Ga₂O₃ MOS capacitor, including C-V and I-V characteristics. For C-V characteristic, the MOS device was swept from accumulation to depletion then back to accumulation at high-low frequency (1 MHz, 1 kHz, respectively), and the inset in Fig. 2(a) shows $1/C^2$ versus V , using to extract N_d via equation (4). As shown in Fig. 2(a), both typical C-V hysteresis and negligible frequency dispersion is

observed in the pre-stress C-V curve, implying the great interface quality of HfAlO/Ga₂O₃. First of all, the relative dielectric constant (ϵ) of HfAlO film is extracted from accumulation capacitance (C_{ox}); that value of ϵ (10.74) is higher than either SiO₂ (3.9) or Al₂O₃ (8.9). The higher ϵ enables a thinner EOT (11.15 nm) of the as-deposited film, and the value of ϵ is in between the previous reported ALD-Al₂O₃ (8.9) [12] and ALD-HfO₂ values (14) [22] on β -Ga₂O₃ (-201). The factors including excessive Al percentage in oxide film and any residual impurities from the ALD process [22], are likely responsible for the lower dielectric constant than various high- k materials (12~24). Pre-deposition process (like UV/O₃ exposure) and Post-deposition annealing may be expected to increase the dielectric constant [13,22], which needs further investigate in HfAlO/Ga₂O₃ MOS structure.

FIG. 2. (a) measured high and low frequency (1 MHz and 1 kHz) C-V characteristic of β -Ga₂O₃ MOS capacitor with the inset of (a) shows $1/C^2$ vs. V plot, and (b) leakage current density vs. voltage of β -Ga₂O₃ MOS.

Table. I. Relevant parameters extracted from the C-V curve of pre-stress sample.

	MOS Sample	Theoretical/Reported value
EOT (nm)	11.15	8.55-13.31
ϵ	10.74	8.9-14 ^[12,22]
Hysteresis (V)	0.92	-
V_{FB} (V)	3.60-4.52	1.03
N_{eff} ($\times 10^{12}$ cm ⁻²)	5.42	-
N_{bt} ($\times 10^{12}$ cm ⁻²)	5.87	-
N_d ($\times 10^{17}$ cm ⁻³)	2.57	-
D_{it} ($\times 10^{12}$ eV ⁻¹ .cm ⁻²)	1.16	-

Table I lists the relevant parameter calculated from high frequency C-V curve, including flat-band voltage (V_{FB}), hysteresis voltage (V_{hy}), dielectric constant ϵ , UID n-type doping concentration N_d , and various effective defect. Usually, at insulator-Ga₂O₃ MOS structure, different types of charges coexist^[19], including “border” trap (N_{bt}), interface trap (D_{it}), fixed oxide trapped charges, and deep traps. “Border” traps are located in the near-interface oxide, that typically interact with the semiconductor by tunneling to and from states in the conduction band (E_c), resulting in longer capture

and emission time constants, depending on their energy level as well as their proximity from the interface^[19]. Normally, N_{bt} and D_{it} mainly change charge occupancy as the surface Fermi level changes. As shown in Table 1, the extracted flat-band voltage (V_{FB}) (3.60 V) is much larger than the ideal value (1.03 V), which suggests the presence of negative effective defect or interface trap in the insulator film and/or at the HfAlO/Ga₂O₃ interface. However, the interface state density close to $1 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ combined with hysteresis lower than 1V implies the large positive flat-band shift is more likely attributed to the negative effective defects, compared with interface trap. The extracted effective oxide charge density ($N_{eff}=5.42 \times 10^{12} \text{ cm}^{-2}$, by equation (1)^[14,23]) and the calculated interface state density ($D_{it} = 1.16 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$, using the single frequency method^[26], by equation (3)) of HfAlO/Ga₂O₃ interface approve the above speculation. Between SiO₂/Ga₂O₃^[27], Al₂O₃/Ga₂O₃^[13], and HfO₂/Ga₂O₃^[16,22] interface, a large number of fixed sheet charges were also found, and the calculated N_{eff} on the HfAlO/Ga₂O₃ interface is close to reported values (SiO₂/Ga₂O₃: $5.5 \times 10^{12} \text{ cm}^{-2}$ ^[27], Al₂O₃/Ga₂O₃: $3.6 \times 10^{12} \text{ cm}^{-2}$ ^[13], respectively). We speculate that the interface traps may possible act as acceptor states during the formation of negative fixed charges, similar with HfO₂/Ga₂O₃^[16]. In addition, using equation (2), equation (4), and equation (5), we estimate the density of “border” trap located in the near-interface oxide ($N_{bt}= 5.87 \times 10^{12} \text{ cm}^{-2}$ by equation (2)), UID n-type doping concentration of Ga₂O₃ substrate ($N_d=2.57 \times 10^{17} \text{ cm}^{-3}$, by equation (4)^[14,23]), and theoretical flat band voltage ($V_{FB}^{ideal} = 1.03 \text{ V}$, by equation (5)). Following, gate leakage properties of the MOS sample are also provided and analyzed. As shown in Fig. 2 (b), the forward I-V characteristics indicate that the HfAlO dielectric supported an effective electric field strength is up to 5.87 MV/cm (+10 V), and gate leakage current density of $1.18 \times 10^{-5} \text{ A/cm}^2$ at gate voltage of 10 V has been obtained. The effective electric field (E_{eff}) is calculated using $E_{eff}=(V-V_{fb})/EOT$, taking into account the physical thickness, ε and V_{fb} extracted from C-V curve. It worth mentioned that the potential contribution of mobile charges in HfAlO/ β -Ga₂O₃ MOS structure has been neglected in chapter 3, as it's hard to detect by room temperature electrical measurement.

The extracted V_{FB} values were used to obtained “border” trap density (N_{bt})^[19,29,30] and the effective oxide charge density (N_{eff})^[19,29,30] which represents the sum of “border” traps, fixed oxide trapped charges, and all deep traps. Next, interface state density is extracted using single frequency method^[26] by equation (3), UID n-type doping concentration ($N_d=2.57 \times 10^{17} \text{ cm}^{-3}$) can be estimated using equation (4)^[14,23], and the ideal flat-band voltage can be obtained using equation (5)^[28]. The above parameter is extracted using following equation:

$$N_{eff} = \frac{C_{ox} |\omega_{MS} - V_{FB}|}{qA} \quad (1),$$

$$N_{bt} = \frac{C_{ox} * \Delta V_{FB}}{qA} \quad (2),$$

$$D_{it} = \frac{2}{qA} \frac{G_{m,max} / \omega}{(\frac{G_{m,max}}{\omega C_{ox}})^2 + (1 - \frac{C_m}{C_{ox}})^2} \quad (3),$$

$$N_d = \frac{2}{A^2 q \varepsilon_o \varepsilon} \frac{d(1/C^2)}{dV} \quad (4),$$

$$V_{FB}^{ideal} = \Phi_m - \chi - E_g / 2 + (K T / q) \ln(N_d / n_i) \quad (5),$$

where C_{ox} , A , q , ω_{MS} , and ΔV_{FB} are accumulation capacitance, gate area, electron charge, metal-semiconductor work function difference, and flat-band voltage shift. The variables $G_{m,max}$, C_m , ω , ϵ_0 , ϵ are the maximum conductance, the capacitance corresponding to $G_{m,max}$, the angular frequency, the vacuum permittivity and relative dielectric constant of Ga_2O_3 (10^{12}). In addition, the variables Φ_m , χ , and n_i in equation (5) are the metal work function (5.15 eV^[31]), electron affinity of Ga_2O_3 (4.00 ± 0.05 eV^[12,13,32]), and intrinsic carrier concentration of $\beta\text{-Ga}_2\text{O}_3$.

3.2 Constant voltage stress of MOS sample

The constant-voltage stress (CVS) measurement on Al-rich HfAlO/ $\beta\text{-Ga}_2\text{O}_3$ MOS devices are provided and analyzed. Figure 3(a) shows high frequency C-V curves of HfAlO/ $\beta\text{-Ga}_2\text{O}_3$ MOS capacitors with specific stress bias (6V) and stress time range (from 10s to 1000s), and Fig. 3(b) shows the extracted ΔV_{FB} as a function of applied positive stress voltage and stress time. Positive shifts of C-V curves are observed in Fig. 3(a), consistent with increasing negative charge trapping in HfAlO oxide film. These observed positive shifts may be attributed to charge trapping in the oxide film and/or associated with interface traps at the HfAlO/ Ga_2O_3 interface. As shown in Fig. 3(b), the positive shifts of ΔV_{FB} with increasing stress time (from 10 s to 1000 s) are observed for different stress voltages (from 0 V to 8V). These results illustrate that charge trapping increases with stress time, while more negative effective charges are formed or filled at positive stress bias. Next, it has found that the flat-band voltage shifts are increased for larger positive stress voltages, which implies the presence and increment of stress-induced traps in the HfAlO film and/or at the HfAlO/ Ga_2O_3 interface bias at larger constant-voltage stress. It also reflects that after same stress time, the larger stress bias results in the increment of negative effective charges in HfAlO oxide film. These CVS characteristics observed in HfAlO/ $\beta\text{-Ga}_2\text{O}_3$ MOSCAP may be attribute to a typically broad distribution^[21,33] of capture cross section and tunneling distances between the $\beta\text{-Ga}_2\text{O}_3$ and traps in the HfAlO dielectric.

FIG. 3. (a) High-frequency (1 MHz) C-V curves vs. stress time for $\beta\text{-Ga}_2\text{O}_3$ MOS biased at 6 V and (b) the extracted ΔV_{FB} vs. stress voltage and time.

To further investigate the contributions of “border” traps, fast interface traps, or fixed charges in these CVS measurement for HfAlO/ Ga_2O_3 MOSCAPs, the parameters including D_{it} , N_{bt} , and N_{eff} are extracted from C-V curves, as shown in Fig. 4(a-c). As shown in Fig. 4(a-b), most of “Border” trap density (N_{bt}) and interface state density (D_{it}) decrease with increasing stress time; the lowest N_{bt} is achieved at stress voltages of 4 V; and the lowest D_{it} is obtained

under larger stress biases (8 V). It is found that the minimum values of N_{bt} ($5.53 \times 10^{11} \text{ cm}^{-2}$) and D_{it} ($2.10 \times 10^{11} \text{ eV}^{-1} \cdot \text{cm}^{-2}$) are observed at different stress biases, implying that the contribution of interface traps and “border” traps is disparate under different stress bias ranges. Under large stress voltage range, the fast interface traps (D_{it}) mainly contribute to the observed stress-induced charge trapping and positive flat-band voltage shift, while, under medium stress voltage range, compared with D_{it} , N_{bt} contribute more to the observed flat-band shift. Then, Fig. 4(c) show a column chart of N_{eff} derived from the C-V curves in Fig. 3(a), which represents the sum of “border” traps, fixed oxide trapped charges, and all deep traps. At stress time 10-200s range, the effective charge density increases with stress time, and the value reach saturation after longer stress time ranges. Meanwhile, it has found that the value of N_{eff} under different stress voltages is different, implying that the except for “border” traps and all deep traps, the contribution of negative fixed sheet charge may not be negligible and the increased fixed sheet charge during constant voltage stress process may also contributes the positive shift of ΔV_{FB} increased with increasing stress time.

FIG. 4. (a) N_{bt} vs. stress voltage and time, (b) D_{it} vs. stress voltage and time, (c) N_{eff} vs. stress voltage and time.

FIG. 5. D_{it} versus energy level from the conduction band ($E_c - E_t$) based on Hi-Lo C-V measurements under different stress biases (4 V (a), 8 V (b)) and times.

To further make verification to the contribution of fast interface trap, the D_{it} was also extracted using the Hi-Lo method proposed by M. Kuhn^[34], where the difference between high frequency (HF) capacitance (1 MHz) and low frequency (Lo, 1 kHz) capacitance at each stress bias determines these D_{it} values, which is given by:

$$D_{it} = \frac{C_{ox}}{qA^2} \left(\frac{C_{lo} / C_{ox}}{1 - C_{lo} / C_{ox}} - \frac{C_{HF} / C_{ox}}{1 - C_{HF} / C_{ox}} \right) \quad (6),$$

where C_{lo} , and C_{HF} are the low frequency and the high frequency measured capacitances, respectively, and other parameters have been mentioned above. The calculated D_{it} by Hi-Lo method is accurate in a limited energy range from 0.2 to 0.6 eV below the conduction band (E_c) of Ga₂O₃.^[19-21] In this range, the trapped charges are emitted from the states to the majority carrier band, in response to the perturbations of the surface Fermi level in the DC (direct current) bias as well as the small AC (alternating current) signal. The extracted D_{it} profiles (Fig. 5(a-b)) show the D_{it} vs. energy level from conduction band (E_c-E_t) based on Hi-Lo C-V measurements (bias at 4 V (a), 8 V (b)), which verifies the similar trend with Fig. 4(b). For pre-stress sample, the interface state density of HfAlO/Ga₂O₃ is calculated to be $1.43 \times 10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ at 0.3 eV below the conduction band (E_c). The average D_{it} is evaluated to be $\sim 4.56 \times 10^{11} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ (stress time & bias: 400 s, 8 V) and $\sim 3.05 \times 10^{11} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ (stress time & bias: 800 s, 8 V), respectively. Post-deposition annealing^[13,21] may expected to decrease defect density in HfAlO/ β -Ga₂O₃ MOSCAPs.

4. Conclusion

In conclusion, negative charge primarily appear in gate dielectrics of HfAlO/ β -Ga₂O₃ MOS capacitors during positive stress bias, which is mainly attributed to the effective oxide charge in the HfAlO/Ga₂O₃ MOS structure including “border” traps, fast interface traps, fixed charges, and all deep traps. The magnitude of the stress-induced charge trapping increases with increasing bias and time, and contribution of “border” traps and interface traps is relatively uniformly with increasing stress time. Moreover, it has found that the “border” traps locate in the near-interface oxide layer contributes more significantly to ΔV_{FB} shift at medium stress bias (4 V), and interface state generation possess more influence on ΔV_{FB} shift the at large stress bias (8 V). In addition, an increasing negative fixed sheet charge density is induced at the HfAlO/ β -Ga₂O₃ interface and/or in the oxide film when stress time increased, which may also contribute the observed positive flat-band shift. Moreover, for the electrical characteristics of pre-stress ALD HfAlO/ β -Ga₂O₃ capacitor, the positive shift of ΔV_{FB} shows that negative effective defect or interface trap exists in that MOS structure. The large number of negative sheet charge density induced in the HfAlO/Ga₂O₃ MOS structure results in the interface traps in part, which also play important roles as acceptor states during the formation of negative fixed charges. Next, the forward I-V characteristics indicate that the HfAlO could supported an effective electric field strength is up to 5.87 MV/cm (+10 V) which make it suitable to exploit device parameters of β -Ga₂O₃ MOS device. These results suggest that a HfAlO/ β -Ga₂O₃ interface could be favorable for power electronic applications in future integration with β -Ga₂O₃ MOS transistors, and illustrate the strong role of “border” traps, fast interface traps, and fixed oxide trapped charges on the stress-induced charge trapping in Al-rich HfAlO/ β -Ga₂O₃ MOS devices.

Additional Information

Competing financial interests: The authors declare no competing financial interests.

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