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A Fully Integrated Multilevel Synchronized-Switch-Harvesting-on-Capacitors Interface for generic PEHs

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Abstract—This paper presents a novel architecture for realizing the synchronized-switch-harvesting-on-capacitors (SSHC) technique used for enhanced energy extraction from piezoelectric transducers. The proposed architecture allows full integration by utilizing the storage capacitor already present in most energy harvesting systems. A promising circuit implementation of the technique, named *multilevel synchronized-switch harvesting on capacitors (ML-SSHC)*, is proposed as well, and its performance is analyzed theoretically. On the basis of that, a fully integrated and power-efficient transistor-level design in 0.18- μm CMOS is presented and fabricated in a prototype chip. When operating at a mechanical excitation frequency of 22 Hz and delivering between 1.51 μW and 4.82 μW , the measured increase in extracted power is $7.01\times$ and $6.71\times$, respectively, relative to an ideal full-bridge rectifier. While the performance is comparable to the state-of-the-art, this is the first implementation allowing full integration at such low frequencies without posing special requirements on the piezoelectric harvester.

Index Terms—Piezoelectric, energy harvesting, bias flipping, ML-SSHC, SSHI, SSHC, self-powered, implant, low power, adiabatic, switched capacitor

I. INTRODUCTION

Energy harvesting from mechanical vibrations using piezoelectric harvesters (PEHs) has the potential to make self-powered medical implants a reality [1]–[3]. It is particularly suitable for providing power for leadless pacemakers implanted within the heart and harvesting energy from the heartbeats. While being generally applicable, the research presented in this paper is done in this context.

The PEHs are usually arranged as cantilevered beams of piezoelectric material with a seismic mass attached at the free end. In the case of harvesting from human heartbeats, a suitable natural frequency for this arrangement is in the vicinity of 20 Hz. Due to their construction, PEHs present several challenges for extracting the energy they transduce: they exhibit large internal resistance and capacitance, and their output current direction is alternating. The combination of these three factors means that, while possible, the use of a full-bridge rectifier (FBR) would yield rather poor performance. In order to achieve high energy extraction efficacy, the capacitive impedance of the PEHs has to be complex-conjugate matched by the harvesting interface. A successful approach to achieve this is the bias flipping method (also known as SSHI(C)), [4], [5], in which the capacitance of the PEH

is resonated with a relatively small inductor, however, at a much higher frequency, see Section II.

Recently, the idea of bias flipping has been developed further and several solutions omitting the bulky inductor have been reported. They utilize a switched-capacitor (SC) network to mimic the behavior of the inductance-based interfaces, and are thus collectively called SSHC. While these solutions are either not fully integrated, [6], [7], or are special cases, [1], [8], they are an important step towards full miniaturization. Furthermore, their performance often exceeds that of their inductance-based SSHI counterparts.

We propose a new switched-capacitor (SC) implementation of the bias flipping method which is fundamentally different from those previously reported, and thus, can be fully integrated. The difference lies in the fact that, at any given time, it only stores a small fraction of the bias flipping energy on its SC network. To achieve this it utilizes the main energy storage of the harvesting system—the smoothing capacitor C_{storage} following the rectifier. This capacitor is anyway required to maintain the rectified voltage. Measurement results from a prototype chip show a seven-fold increase in extracted power, compared to a theoretical zero-dropout FBR, while consuming 233 nW and delivering 1.51 μW to the load; and a 6.71-fold increase when delivering 4.85 μW and consuming 665 nW. We expect that, with a miniature PEH like the one we used, similar power levels would be possible to extract from a human heart. This power can be used to extend the battery life of a pacemaker or to even continuously power one with low activity.

The remainder of this paper is organized as follows: In Section II we provide an overview of the bias flipping technique and generalize the novel aspects of our approach; In Section III a system-level implementation is proposed; In section IV the ultimate theoretical performance is derived; In section V we present the design of the fabricated test chip; and finally, in Section VI show the experimentally obtained performance and compare it to that of previously reported solutions; Conclusions are provided in Section VII.

II. BACKGROUND ON BIAS FLIPPING

The core concept of the SSHI(C) techniques is to quickly reverse (bias flip) the polarity of the voltage on the PEH parasitic capacitance (V_{C_p}) every time the piezoelectric current (I_P) reverses direction. This has the effect that I_P is always working against a high voltage of the same polarity, and is, therefore, delivering higher power. Ideally, after flipping, the magnitude of V_{C_p} should remain the same, as any drop

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would result in a reduction of the average power at which the PEH operates, and therefore, in a reduction of the extraction efficacy.

In order to reverse the polarity of V_{C_P} a bias flipping interface first discharges the PEH parasitic capacitance (C_P) and then recharges it in the opposite sense. Crucially, when discharging, the previously known interfaces temporarily store the energy in an energy reservoir, and then reuse that same stored energy to restore the charge on C_P . Fig. 1 illustrates this principle. Three components are utilized: an active rectifier; a temporary energy storage reservoir; and an energy transport circuit to move charge between C_P and the energy reservoir.

Since an inductor can readily transport energy from a capacitor in an adiabatic process, many of the previously proposed interfaces utilize it to implement the energy reservoir, [4], [5], [9]. Therefore, the additional circuitry they need is of a relatively low complexity. Nevertheless, inductors of the required size (several millihenry) are bulky and not economically viable to integrate. Therefore, several successful attempts to replace them with capacitors have recently been demonstrated in [1], [6]–[8]. In terms of efficacy, these solutions can compete and, in many cases, even outperform the inductance-based interfaces. However, in order for the voltages on their capacitors to remain manageable, their capacitance has to be comparable to that of the PEH (tens of nanofarads). Still, such a large amount of capacitance is impractical, and in most cases impossible, to integrate. The solutions in [6] and [7] utilize four and, respectively eight, external capacitors, each as large as C_P . They require off-chip area as well as bonding pads and package pins, all driving the system volume and cost up. In the special cases of [1] and [8], the capacitors could be fully integrated. However, the former operates in the kilohertz range with a PEH exhibiting very small C_P (78 pF), while the latter requires a special multi-electrode PEH.

III. PROPOSED ARCHITECTURE

To avoid the use of external components, we propose an SSHC concept in which, instead of using a dedicated reservoir for the bias flipping energy, we utilize one that is already present in practically any power supply system, namely the smoothing capacitor $C_{storage}$ (and/or battery) following the rectifier. This is illustrated in Fig. 2 where the energy transport component from Fig. 1 is now a bi-directional multilevel (that is, variable ratio) DC/DC converter inserted between the PEH and the smoothing capacitor. At the beginning of the bias flipping the DC/DC converter discharges C_P and deposits its charge on $C_{storage}$ by boosting its voltage to the rectified voltage (V_{rect}). This continues until the PEH is as discharged as possible, at which point it is shorted to dissipate any remaining charge. Then, the rectifier exchanges the polarity of the PEH terminals, and the DC/DC converter is configured to buck the voltage of $C_{storage}$ (V_{rect}) to that of C_P , charging it back to V_{rect} .

Crucially, since at any point in time, the DC/DC converter has to store only a small fraction of the total bias flip energy, it is possible to implement it using only small capacitors; thus, making full integration of the system economically feasible.

Fig. 1. Generalization of the previously reported techniques using a hard to integrate dedicated energy storage element.

Fig. 2. Generalization of the proposed technique. The rectifier smoothing capacitor $C_{storage}$ is utilized to temporarily store the bias flipping energy and a dedicated energy reservoir is no longer needed.

We implemented the proposed technique with a circuit generalized as shown in Fig. 3, where the shaded part on the right corresponds to the DC/DC converter, and the one on the left – to the rectifier. The various circuit configurations and the associated sketched waveforms are shown in Fig. 4. This circuit implements an N -ratio DC/DC converter providing $N + 2$ equally spaced voltage levels (ground, $V_{level,1} \dots N$ and V_{rect}) to which the PEH is successively connected to adiabatically discharge and charge it to perform bias flipping. We call this a *multilevel synchronized-switch harvesting on capacitors (ML-SSHC) interface*. The stability of this class of circuits, and the spontaneous generation of the level voltages, are discussed in-depth in [10].

Fig. 3. Generalized circuit of the proposed multilevel bias flipping rectifier.

A. Level voltage generation

To understand the functionality of the ML-SSHC interface let us first examine the operation of the part implementing

Fig. 4. Sketched waveforms generated during operation of the proposed technique, top left, and the various circuit configurations generating them – Level voltage generation (flyby and charge redistribution cycles), top right; Multilevel bias flip rectification, bottom.

the DC/DC converter and how it divides V_{rect} into N equally spaced voltages $V_{level,1...N}$. Assume that, in Fig. 3 the PEH and the load are disconnected and that all capacitors are charged to arbitrary voltages. The timing of the circuit starts and C_{fly} is connected between each two neighbouring voltage levels, initially, it is connected between V_{rect} and $V_{level,N}$, then – between $V_{level,N}$ and $V_{level,N-1}$, and so on, until finally, it is connected between $V_{level,1}$ and ground. After that the cycle restarts and C_{fly} is again connected between V_{rect} and $V_{level,N}$. This cycle is shown in detail in Fig. 4 top right.

When C_{fly} is connected between two new levels P and $P-1$ (from 12 o'clock to 3 o'clock in Fig. 4), for which the condition $V_{level,P} - V_{level,P-1} \neq V_{C_{fly}}$ is true, charge is transferred between C_{fly} , $C_{L,P}$ and $C_{L,P-1}$ such that $V_{level,P} - V_{level,P-1}$ becomes closer to what $V_{C_{fly}}$ was before the connection. After the insertion, C_{fly} holds the voltage difference $V_{level,P} - V_{level,P-1}$. Therefore, in the next step, when $V_{C_{fly}}$ is connected between the next pair of level capacitors (3 o'clock to 6 o'clock in Fig. 4), their voltage difference ($V_{level,P-1} - V_{level,P-2}$) is forced closer to the voltage difference of the previous pair ($V_{level,P} - V_{level,P-1}$). Thus, as the cycle is repeated, charge is transferred between

all capacitors such that $V_{level,P+1} - V_{level,P} \rightarrow V_{level,P} - V_{level,P-1}$, for any P . Furthermore, since at the bottommost level ($P = 1$) there is no capacitor $C_{L,0}$ we only have $V_{level,1} \rightarrow V_{level,P+1} - V_{level,P}$ (9 o'clock in Fig. 4). Thus, after many repetitions of the cycle, charge is distributed such that $V_{level,P} - V_{level,P-1} = V_{level,1}$ for any P .

In conclusion, repeating the cycle shown in Fig. 4 top right, divides the topmost voltage $V_{level,N+1}$ (which is V_{rect}) and generates $N+1$ equally spaced voltages V_{rect} and $V_{level,1...N}$. Let us call one cycle on C_{fly} a *flyby cycle*; and the repetition of flyby cycles a *charge redistribution cycle*. The charge redistribution cycle creates a ringing voltage on C_{fly} as illustrated in Fig. 4, the amplitude of this ringing represents the charge unbalance between the levels.

B. Bias flipping and rectification

To harvest the energy transduced by the PEH, the multipositional switch S_{multi} is in position $N+1$ connecting the PEH to $C_{storage}$ and to the rectifier output. The bias flipping begins by connecting the PEH to $V_{level,N}$, see bottom of Fig. 4. Since the level capacitors (C_L) are much smaller than C_P , the voltage $V_{level,N}$ becomes equal to V_{rect} , this is represented

by a corresponding bump of $V_{level,3}$ in Fig. 4 top left. In this state, charge redistribution is performed until all voltage levels become equally spaced, Fig. 4 top left. When this happens, the PEH is connected to $V_{level,N-1}$ and charge redistribution is performed again. This process is repeated until the PEH is at $V_{level,1}$, after which it is shorted to ground to fully discharge it, which concludes the discharge phase of the bias flipping. Notice that, since $C_{storage}$ is charged to the highest voltage and is much larger than all of C_L and C_{fly} , it absorbs essentially all of the charge redistributed from C_P . The charge transferred from C_P creates a small increase in V_{rect} as illustrated in Fig. 4.

Once the PEH is fully discharged, the connection of its terminals is swapped by the active rectifier and it is charged back to V_{rect} by performing the reverse procedure from above. The charge that was previously deposited on $C_{storage}$ is now returned to C_P . The bias flipping process completes after the charge redistribution at level $V_{level,N}$. At this point, the PEH can either be connected to V_{rect} or it could be left unconnected letting I_P charge it to V_{rect} (See section IV-C).

At first glance, the solutions in [6]–[8] are similar to what we propose, particularly, due to the use of switched capacitor circuits and the stepwise charging of C_P . However, as was highlighted by Figs. 1 and 2, [6]–[8] store the bias flipping energy on dedicated capacitors while we utilize $C_{storage}$ for that purpose. Consequently, the creation of the voltages for the stepwise charging is done differently – we utilize a multilevel DC/DC converter, while [6]–[8] rearrange the connections of the storage elements themselves.

IV. PERFORMANCE ANALYSIS

The loss of charge during bias flipping, that is, the ability of the interface to restore the magnitude of the voltage on C_P , is the main limitation for the power extraction efficacy of an SSHL(C) interface. Here, we analyze the performance and quantify the voltage flipping coefficient, that is, the ratio of the final to the initial voltage on C_P . There are two sources of charge loss in the proposed bias flipping process: shorting of C_P at the end of the discharge phase; and shorting of the C_{fly} bottom plate parasitic (C_{bot}) at the end of each flyby.

A. Voltage flipping coefficient

The charge on C_P before shorting it at the end of the discharge phase is $Q_{C_P} = C_P V_{rect,1} / (N + 1)$, where $V_{rect,1}$ is the rectified voltage after charge redistribution at level $V_{level,1}$. Since the level capacitors (C_L), C_{fly} and C_P are at least three orders of magnitude smaller than $C_{storage}$ we can ignore their charge. If $V_{rect,init}$ is the rectified voltage before bias flipping, the rectified voltage at level 1 is $V_{rect,1} = V_{rect,init} \left(1 + \frac{N}{N+1} \frac{C_P}{C_{storage}}\right)$, and the charge on C_P is:

$$Q_{C_P,1} \approx C_P V_{rect,init} \frac{1}{N+1}. \quad (1)$$

This will be the charge removed from the system at the end of the bias flipping. Therefore, the final voltage on C_P when connected to the topmost level (N) would be $V_{C_P,N} = V_{rect} \frac{N}{N+1}$,

and the voltage flipping coefficient for the ML-SSHC can be written as:

$$k_{ML-SSHC} = \frac{V_{C_P,final}}{V_{C_P,init}} = \frac{V_{C_P,N}}{V_{rect}} = \frac{N}{N+1}. \quad (2)$$

Crucially, for this first order result, the flipping coefficient is independent of the capacitor sizes, and they can be made small enough to allow full integration of the proposed technique.

A commonly used figure-of-merit for harvesting from PEHs is the maximum output power increase ratio (MOPIR) [4], defined as the ratio between the power extracted by a given interface and that by a theoretical, zero-dropout full-bridge rectifier (FBR). Using the voltage flipping coefficient, the MOPIR can be expressed as $MOPIR_{ML-SSHC} = \frac{2}{1-k_{ML-SSHC}}$, [1], [4], which using (2) becomes:

$$MOPIR_{ML-SSHC} = 2(N+1). \quad (3)$$

This suggests that the power increase ratio can be set arbitrarily high by using a large number of levels N . In practice however, for large N , the power consumption of the control circuitry needed to perform the flipping would eventually negate any further gain.

B. Charge loss due to the bottom plate parasitic capacitance

The bottom plate parasitic capacitance (C_{bot}) of C_{fly} is connected between ground and the negative electrode of C_{fly} . Therefore, for each flyby, it is shorted when C_{fly} is between $V_{level,1}$ and ground. Before this, C_{fly} has been connected between $V_{level,2}$ and $V_{level,1}$, the voltage on C_{bot} has been $V_{C_{fly}} = V_{level,1} = \frac{V_{rect}}{N+1}$, and the charge lost by shorting it is:

$$Q_{loss,flyby} = V_{rect} \frac{1}{N+1} C_{bot}. \quad (4)$$

The above means that to achieve high efficiency C_{bot} should be kept as small as possible, while the charge transported per flyby—as much as possible. As the charge redistribution progresses, a point is reached when the charge lost through C_{bot} per flyby equals the charge transferred between C_P and $C_{storage}$. This must be detected and used to stop the redistribution, followed by either a change of level, shorting and exchange of the PEH terminals, or termination of the flipping.

C. Active diode—power gain vs. consumption

After flipping, the PEH should eventually be connected to V_{rect} . One alternative is to do that as soon as the last charge redistribution completes. Let us call this the No-Wait (NW) method. It would use charge from $C_{storage}$ to restore V_{PEH} to V_{rect} forcing I_P to immediately start working against a higher voltage and deliver more energy. However, this exact same amount of extra energy was dissipated by the closing of the switch that connected the PEH to V_{rect} , totaling in zero energy gain. Another, previously employed approach, is to use an active diode to detect when $|V_{PEH}| = V_{rect}$ and then connect the two, [1], [4]–[8], [11]. Let us call this the Diode-Wait (DW) method. This prevents the transfer of charge from $C_{storage}$, however, energy is nevertheless used to run the active diode. We, therefore, assess which method is worth

implementing by comparing them in quantitative terms. We assume the following: steady-state operation, V_{rect} does not change across the bias flipping cycles; V_{rect} is fixed for both methods, that is, the load current changes to compensate; The active diode in the DW case starts conducting at time t_x after bias flipping is complete, Fig. 4.

First, consider a PEH model without damping, that is, only a current source in parallel with C_P . The total charge delivered by I_P for each half-cycle is fixed irrespective of which method is used. However, the root-mean-square voltage, and therefore power, at which this happens, is different. For the DW method, before the diode starts conducting, V_{rect} droops due to the load current. While, for the NW method, V_{rect} drops with a step when C_P is charged from $C_{storage}$. Since after t_x the two cases are topologically indistinguishable, and since to ensure steady-state, the final conditions must be the same, any difference in load current must be due to the difference of $\Delta V_{rect} = V_{rect,DW} - V_{rect,NW}$ before t_x . The peak ΔV_{rect} occurs just after the end of the flipping and is $\max(\Delta V_{rect}) = (1 - k_{ML-SSHC}) V_{rect,init} \frac{C_P}{C_P + C_{storage}}$. For values matching our implementation ($C_P = 6 \text{ nF}$, $C_{storage} = 2.1 \mu\text{F}$, $k_{ML-SSHC} = 0.75$ ($N = 3$), $V_{rect} = 5 \text{ V}$ and $R_L = 1.66 \text{ M}\Omega$), the peak instantaneous difference in load current is $\max(\Delta V_{rect})/R_L = 2.1 \text{ nA}$.

The approach above is also valid for a more realistic PEH model with parallel-connected damping resistance R_P , however, the energy it dissipates should be accounted for. Before time t_x the voltage on R_P is lower for the DW case, initially the difference is $(1 - k_{ML-SSHC}) V_{rect,init}$, and it diminishes following a cosine function becoming zero at t_x . We can integrate along the difference in V_{PEH} for both cases to obtain the difference in I_{R_P} and therefore in load current:

$$\begin{aligned} \Delta I_{R_P} &= \frac{\omega}{\pi R_P} \int_0^{t_x} V_{rect} - V_{PEH,DW} dt \\ &= \frac{\omega}{\pi R_P} \left(t_x V_{rect} (1 - k_{ML-SSHC}) - \frac{\hat{I}_P}{\omega C_P} \left(t_x - \frac{\sin(\omega t_x)}{\omega} \right) \right) \end{aligned} \quad (5)$$

where ω is the excitation frequency, $\hat{I}_P$ is the amplitude of I_P and $t_x = (1/\omega) \cos^{-1}(1 - V_{rect}(1 - k_{ML-SSHC})\omega C_P/\hat{I}_P)$. A detailed derivation is provided in [12]. With $\omega = 138 \text{ rad/s}$, $\hat{I}_P = 1.95 \mu\text{A}$, $R_P = 3.5 \text{ M}\Omega$ and the example values above, for the DW case we obtain an additional current of $\Delta I_{R_P} = 81 \text{ nA}$. This represents the highest gain combination of the operating conditions we present in Section VI. It places a bound on the power we can allocate for the active diode of the Diode-Wait method. Active diodes are usually based on a latched comparator, [11], [13]. The diode in [13] consumes 40 nA , while that in [11]—at least 30 nA . Furthermore, such low bias currents lead to low bandwidth and large input offset (due to poor sub-threshold matching) which could jeopardize the DW method.

The above can be interpreted in terms of maximum power point tracking. The DW case is more efficient since V_{PEH} rises slower, better matching the rise of I_P . Notice that, this can be extended to the entire bias flipping duration where, for maximum power transfer, the rate of change of V_{PEH} must

track that of I_P . This is the same conclusion reached and demonstrated in [9].

Due to the additional complexity and risk, and the small expected power gain of the Diode-Wait method, for our test chip, we employed the No-Wait approach. Notice that, if a passive diode is used it would cause even more power to be dissipated by R_P .

V. CIRCUIT IMPLEMENTATION

Fig. 5 shows a detailed top-level circuit implementing the proposed technique with five ($N = 3$) voltage levels. On the left side is the front-end, which corresponds to the rectifier and the bias flipping DC/DC converter; and on the right—is the control circuitry, which coordinates the operation of the front-end. Timing is provided by the timing generator shown in Fig. 6. Two power supply domains are used, as indicated by the vertical dashed line in Fig. 5. The circuits to the left of the line are powered from V_{rect} , which is the highest voltage in the system, while the circuits to the right—by a one-volt supply domain $V_{pwr,1V}$ derived from V_{rect} . To keep the power consumption low, the architecture and the individual circuits are designed to avoid the need for low-to-high level-shifters. In order to quickly absorb the charge from C_{fly} and to prevent ringing in the bondwires and the PCB traces for V_{rect} , we utilized the available space in our test chip for an on-chip capacitor (900 pF) and connected it in parallel to $C_{storage}$.

A. Front-end

The switches $S_{LP,1...4}$, $S_{LN,1...4}$, $S_{L,0}$, $S_{rect,P}$ and $S_{rect,N}$ perform the active rectification and level selection, they correspond to S_{multi} in Fig. 3. Their state is controlled according to the state diagram shown in Fig. 5. Switches $S_{LP,3...4}$, $S_{LN,3...4}$ are PMOS transistors, switches $S_{LP,2}$, $S_{LN,2}$ are transmission gates, while the rest are NMOS transistors.

The DC/DC converter functionality is implemented by the level capacitors $C_{L,1...3}$ (150 pF each), the flying capacitor C_{fly} (150 pF) and the switches $S_{R,0...3}$. To allow high clock rate for charge redistribution, the switches not connected to V_{rect} or ground are bootstrapped from the top plate of C_{fly} . Furthermore, since both terminals of C_{fly} are switched at the same time, $S_{R,1...2}$ are double switches sharing bootstrapping circuitry, gate node, and control signals.

Since the flying capacitor is implemented as a MiM structure on the CMOS chip, we created a diode connected in series with C_{bot} by placing an nwell covering the area under C_{fly} . By letting the nwell, which is the cathode of the diode, float during the bias flipping we reduced the effective C_{bot} from 1.12 pF to 0.91 pF . To reverse-bias the diode, the nwell is connected to V_{rect} when the bias flipping is not running.

B. Charge-redistribution-end detector

As indicated in Section IV-B, we need to detect when the charge redistribution has settled to the point that the charge loss through C_{bot} is greater than the charge transferred from/to $C_{storage}$. Due to the small quantities involved, it is impractical, if at all possible, to measure this relationship directly.

Fig. 5. Detailed schematic of the proposed technique for $N = 3$. To the left is the multilevel bias flipping rectifier, to the right—the control circuitry.

Therefore, to obtain an assessment of the charge transferred per flyby, we use the peak-to-peak amplitude of the voltage on C_{fly} ($V_{p-p, C_{fly}}$). Initially, $V_{p-p, C_{fly}}$ is relatively large, approximately $2V_{rect}/(N+1)$, and it decays toward a small constant as the redistribution settles, see top right of Fig. 4. Since the charge loss due to C_{bot} remains approximately constant, we can compare $V_{p-p, C_{fly}}$ to a constant to detect the settling. The circuit performing this is shown inside the blue box in Fig. 5, we call it a *charge-redistribution-end detector*.

The detector consists of two parts: a sample-and-hold circuit; and a comparator with an adjustable built-in offset. First, the sample-and-hold is driven so as to sample the min and max peaks of $V_{C_{fly}}$ on two capacitors. Then, it is rearranged such that the difference of the sampled voltages, that is, $V_{p-p, C_{fly}}$, is fed to the comparator input. When $V_{p-p, C_{fly}}$ drops below the comparator offset, it triggers, indicating that the charge redistribution is complete. The offset is tuned to represent the rate of charge loss through C_{bot} . The sampling capacitors' size is much smaller than that of C_{fly} , (~ 300 fF vs. 150 pF), therefore the bias flipping is not affected by the sampling.

This sampling scheme removes the DC component of $V_{C_{fly}}$ which, combined with a voltage limiter, allows the comparator to be powered by the low-voltage domain $V_{pwr, 1V}$ and to be built using short-channel thin-oxide devices, which together keep its power consumption low. Furthermore, the comparator is of a dynamic type, consuming power only when clocked.

C. Active rectifier state machine

The rectifier is controlled by a state machine implemented as a traveling-one shift register, Fig. 5 bottom right. It operates according to the state diagram shown in Fig. 5 top right.

After reset it enters state “flip complete” and waits for a rising edge on *startFlipping*. When that occurs the state machine starts the timing generator, which activates the charge redistribution and the end detector, and it moves the PEH between the different voltage levels, keeping it connected to a particular level until the end detector triggers.

To prevent short-circuit currents, the state machine operates the switches of the rectifier in a break-before-make fashion. This is achieved by sizing the relevant pull-up/down networks of the gates of the state machine and the drivers at its output, such that the propagation delay for the transitions that turn the switches off is shorter than for those turning them on.

D. Timing generation

The timing generator drives the bootstrapped switches performing the charge redistribution. In addition to turning them on and off, it also coordinates the precharging of their bootstrapping capacitor. It guarantees non-overlapping signals to ensure that the precharging is stopped before the switches are turned on, and that no unintended connections of C_{fly} are made. The timing generator also runs the sampling circuit and the comparator of the charge-redistribution-end detector which should be in sync with the converter timing, as well as with the rectifier level states. The latter is required in order to sample the peaks of $V_{C_{fly}}$ whose position within the flyby cycle depends on the level the PEH is connected to. A timing diagram, as well as a detailed schematic of the generator and its connections to the bootstrapped switches, are shown in Fig. 6.

Since the timing generator drives many signals with high switching activity, and has to be operated for many cycles

Fig. 6. Detailed circuit of the timing generator for the charge redistribution.

for each bias flipping, special consideration has been put on its power efficiency. Therefore, we developed the timing generator which we first presented in a generalized form in [14] and is shown, tailored for the current needs, in Fig. 6. It is based on a differential ring oscillator whose internal states $P_{osc,0...3}$ (Fig. 6 top right) are translated into timing signals (Fig. 6 middle right) using differential-input XOR gates. Thus, it generates the one-hot sequence $R_{0...3}$ which directly drives the $S_{R,0...3}$ switches. The power efficiency of this timing generator stems from the low fan-in/out of its internal signals. Each state transition of the oscillator is always translated to a transition of a control signal. Furthermore, no state transition is fed to a gate whose output will not transition as well.

The XOR gate produces a high- and a low-voltage version of its output, R_{HV} and R_{LV} , derived from V_{rect} and $V_{pwr,1V}$ respectively. R_{LV} is level-shifted down from R_{HV} . In order to guarantee that the converter switches are never turned on at the same time, a switch in series with the XOR gate pull-up network blocks the low-to-high transition of R_{HV} and R_{LV} until the corresponding bootstrapped switch has signaled that it has turned off. This forms an active guard feedback as shown with a dashed line in Fig. 6. The dependence between the individual transitions is shown inside the zoom-in box.

Due to the information richness of the ring oscillator states, very little circuitry is required to also generate the end detector timing signals. The `evalSamp` is an AND-ed version of $P_{osc,0}$ and $P_{osc,2}$, while `evalRedist` is a copy of $R_{LV,2}$. The `samplePos` and `sampleNeg` are derived from $R_{LV,0...3}$ by gating them with the rectifier level-select signals $L_{1...3}$ and `chargeDir`, which is generated by the rectifier state machine and indicates the direction in which the PEH is being charged.

E. Bootstrapped switch

The schematic of the bootstrapped switch is shown in Fig. 7. It is a version of a widely used circuit, [15]–[17], modified in two critical ways to achieve low power consumption.

As was initially proposed in [15], separate signals and paths are used to turn the switch off from those used to enable precharging of the bootstrapping capacitor. The traditional approach, to start precharging simultaneously with turning the switch off, creates a temporary short-circuit path between supply and ground, causing shoot-through current to flow. By splitting the paths and using two non-overlapping control signals, the associated power consumption is avoided by precharging only after the switch has been fully turned off. Shoot-through current can also flow during the transition to the off state. We prevent this by turning off in two stages. Initially, the main switch transistors are turned off by $OnOff_{LV}$ going low. Then, one of $Off_{HV,0...2}$, goes low to also disable the bootstrapping circuit. To reduce the required number of control signals, three of $R_{HV,0...3}$ are wire-ORed by transistors $M_{P,1...3}$ to produce the internal `turnOff` signal.

Fig. 7. Transistor-level circuit of the bootstrapped switch.

The state of the main switch transistor is monitored using $M_{\text{monP},1\dots 2}$ and $M_{\text{monN},1\dots 2}$, which derive the `turnedOff` output. It is used to form the non-overlap guard feedback loop in the timing generator. The power consumption of this circuit is kept low by utilizing a break-before-make scheme. Whenever OnOff_{LV} changes logic level the `turnedOff` output first enters a high-impedance state, after which it is switched by the bootstrapped transistor gate.

It should be noted that, even though the bootstrapped switch is for voltages reaching V_{rect} , all of its control signals, except $\text{Off}_{\text{HV},0\dots 2}$, are driven from $V_{\text{pwr},1\text{V}}$, thus, saving power. Furthermore, since none of the control inputs are sensitive to the transition times of the signals driving them, to keep the consumption low, we could use minimum-size drivers in the timing generator while not causing any shoot-through current.

F. XOR gate and ring oscillator delay cell

Fig. 8 shows the transistor-level implementation of the delay cell of the ring oscillator. This circuit was proposed in [18] where its suitability for building low-power ring oscillators was explored and demonstrated. It saves power by exploiting the break-before-make switching scheme, which prevents shoot-through currents. Furthermore, contrary to the traditional current-starved delay cells, the output signal of this cell spends very little time close to the conduction region of both P- and NMOS transistors, therefore the ring oscillator can directly drive the XOR gates without causing them to consume shoot-through current. A sketch of the transitions at the output of the delay cell is shown in Fig. 8. The current source transistors are biased to provide 5 nA and no extra capacitance was added to the output.

Fig. 8. Transistor-level implementation of the delay cells of the ring oscillator.

VI. EXPERIMENTAL RESULTS

A prototype chip implementing five voltage levels ($N = 3$) was fabricated in a standard 180-nm CMOS process offering 1.8 V and 5 V devices, as well as MiM capacitors. Fig. 9 shows a micrograph of the chip. The circuitry occupies an active area of 1 mm^2 ($1288 \times 746 \mu\text{m}$), dominated by MiM capacitors. The used custom PEH from Vernon S.A has a length of 15 mm, width of 4 mm, clamped capacitance of 6 nF and seismic mass of 1.4 g, and was excited by a shaker table at its resonant frequency of 22 Hz. It is expected that this frequency would yield good performance when energy is harvested from a human heart.

Fig. 9. A micrograph of the prototype chip. Other circuits are cropped away. We acknowledge the help from Dr. Andreas Ehliar producing the photo.

Fig. 10. Measured waveforms—cold start-up and bias flipping details.

Fig. 11. Performance for various operating conditions. Peak power limited by the maximum PEH deflection. The peak FoM at high $V_{\text{PEH},oc}$ is limited by the breakdown voltage of the chip.

TABLE I
COMPARISON TO STATE-OF-THE-ART INTERFACES.

	This work	[8]	[1]	[6]	[7]	[5]	[9]
Technology	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.35 μm	0.35 μm	0.18 μm
Extraction technique	Multilevel synchronized-switch harvesting on capacitors ML-SSHC	Split-electrode SE-SSHC	Flipping-capacitor rectifier FCR	Split-phase flipping-capacitor SPFCR	SSH on capacitor SSHC	Parallel-SSHI	Sense and set SaS
PEH model	Vernon S.A. VH1504C-2	Multielectrode MEMS	Piezo Systems P5A4E	Mide PPA-1021	Mide V21BL	Mide V21B & V22B	Mide PPA-1022
C_P	6 nF	1.94/0.155 nF	78.4 pF	22 nF	45 nF	27.5/20.8/9.6 nF	8 nF
Key Component	On-chip MIM capacitors (Ctot = 600 pF)	On-chip MIM capacitors (Ctot = 4 nF)	On-chip MIM capacitors (Ctot = 1.44 nF)	Four off-chip capacitors (Ctot = 272 nF)	Eight off-chip capacitors (Ctot = 360 nF)	Off-chip inductor (L = 3.4 mH)	Off-chip inductor & capacitor (L=1 mH, C=10 nF)
Chip size	1 mm ²	5.38 mm ²	1.7 mm ²	0.2 mm ²	2.9 mm ²	1.17 mm ²	0.47 mm ²
Output power	1.5-5.3 μW	186 μW	50.2 μW	0.5-64 μW	161.8 μW	408 μW	16 μW
Frequency	22 Hz	219 Hz	110 kHz	200 Hz	92 Hz	135.6-229.6 Hz	85 Hz
Voltage flipping coefficient	0.75	0.69 ^b	0.85	0.83 ^d	0.8	0.94-0.89	N/A
FoM ^a	7.01 $\times$	5.87 $\times$ ^c	4.83 $\times$	9.30 $\times$	6.30 $\times$ ^c	6.81 $\times$ ^e 4.93 $\times$ ^f	5.56 $\times$

^a $FoM = \frac{P_{measured}}{C_P f_P V_{oc}^2}$; ^bFrom graph in [8]; ^cCalculated from reported $V_{PEH,oc}$; ^dFrom graph in [6] ^eOff resonance; ^fAt resonance.

We used a microcontroller (ATmega328, consuming ~ 4.5 mW from an external supply) to align the phase of the bias flipping with the zero-crossing of the piezoelectric current I_p . The output power was calculated by forcing a fixed voltage on V_{rect} and measuring the current. In order to prevent device breakdown, the excitation and load resistance were limited such that $V_{rect} < 5$ V. In order to reduce the ripple on V_{rect} , we used a relatively large value for $C_{storage}$, 2.1 μF .

Fig. 10 shows a cold start of the harvesting system, as well as details of the bias flipping operation. Cold start is achieved by a full-bridge rectifier (FBR) connected in parallel with the SSHC interface. Once V_{rect} reaches ~ 1 V, sufficient to run all active circuitry, the bias flipping is activated and active harvesting begins. This is evidenced by the increase of V_{rect} and the square wave-like shape of V_{PEH} . A close inspection of V_{rect} during bias flipping (bottom of Fig. 10) reveals that the charge from C_P is indeed temporarily transferred to $C_{storage}$ and then back to C_P . The voltage on the PEH is restored to $\sim 60\%$ without consuming any additional energy, and at the cost of a 1.5 mV drop on V_{rect} ($C_{storage} = 2.1 \mu\text{F}$), it is restored to $\sim 75\%$ of its initial value, as predicted by (2). This voltage drop is due to the losses from C_{bot} as well as the total system power consumption.

A close-up of V_{PEH} for several flybys during charge redistribution is shown in the zoom box in Fig. 10. It is seen that the charge on C_P is depleted with a step every eight microseconds. The time needed for one flipping is ~ 1.8 ms, hence, the number of flybys per charge redistribution is ~ 38 .

Table II shows a breakdown of the current consumption of the system components when harvesting energy at peak performance (max FoM) at $V_{rect}=2.95$ V, as well as, at peak power at $V_{rect}=5$ V. The peak power was limited by the maximum deflection of the PEH, while the peak FoM (MOPIR) at high $V_{PEH,oc}$ was limited by the breakdown voltage of the transistors – for $V_{PEH,oc}=2.34$ V, the maximum power point occurs at $V_{rect}>5$ V. The 1 V power supply $V_{pwr,1V}$ was

derived from V_{rect} using an off-chip linear regulator, sourcing the current for $V_{pwr,1V}$ from V_{rect} without transformation. The quiescent current of the regulator was provided externally.

TABLE II
MEASURED POWER CONSUMPTION BREAKDOWN.

Block/Power domain	Current/Power [nA]/[nW]	
	$V_{rect} = 5$ V	$V_{rect} = 2.95$ V [†]
Bootstrapped switches	38 / 190	14 / 41
End detector	12 / 60	8 / 24
Timing incl. bias	43 / 215	19 / 56
Total from $V_{pwr,1V}$	40 [‡] / 40	38 [‡] / 38
Total from V_{rect}	133 / 665	79[‡] / 233

[†] Peak performance. [‡] Sourced from V_{rect}

We tuned the offset of the comparator of the charge-redistribution-end detector to correspond to the energy losses and, therefore, terminate the bias flipping such that the efficiency is maximized. We also tuned the speed at which the ring oscillator of the timing generator runs. This allowed us to optimize the trade-off between the conduction losses in the switches and the conduction angle of the rectifier.

Measurements shows that the implemented multilevel rectifier is able to extract 7.01-6.13 $\times$ more power than a theoretical, zero-drop-out full-bridge rectifier (FBR), Fig. 11. We used several mechanical excitation levels covering the full voltage-range of $V_{rect} - 1.5$ -5 V. While the system can operate below 1.5 V, it was selected to allow a regulator for $V_{pwr,1V}$ to operate reliably.

It can be seen in Fig. 11 that V_{rect} at peak power is approximately proportional to $V_{PEH,oc}$ (which in turn is proportional to the piezoelectric current), while the optimal load resistance remains mostly independent of $V_{PEH,oc}$. The variation of the load resistance is due to the flipping efficiency which changes with V_{rect} .

Since the PEH is the only source of energy, we can validate our measured and theoretical results by adding the power

consumed by the active circuitry (233 nW) to the output power at peak performance (1.5 μ W) to obtain the total extracted power (1.733 μ W), which gives a power extraction ratio of $8.05\times$. This is a close match to the value of eight predicted by (3) for $N = 3$. A comparison to the state-of-the-art is shown in Table I.

Even though our circuitry was designed for the power levels provided by the used PEH, we tested at a higher power with a different PEH. This revealed a small shortcoming of the implementation of the end detector. At higher powers, I_P is still relatively large when C_P is being discharged at $V_{level,3}$. It deposits charge on C_P against the DC/DC converter which is removing charge from it. This causes the end detector to trigger later. It is possible to compensate this by adjusting the threshold of the comparator, however a threshold setting suitable for Level 3 is not suitable for Level 1. This is because by the time the PEH reaches the lower voltage levels, I_P has become much smaller. The same phenomenon occurs during the charging phase. In that case, however, the end detector triggers relatively earlier at $V_{level,3}$. A solution to allow operation at higher power is to include a separate threshold setting for each voltage level in each direction – six in total.

VII. CONCLUSION

This paper proposed a new fully integrated, capacitance-based technique to perform bias flipping of the synchronized-switch method for energy harvesting from piezoelectric transducers. A promising implementation was shown along with analysis, transistor-level realization, and experimental validation. The technique is fundamentally different from the previously explored in that it utilizes the rectifier smoothing capacitor to store the PEH energy during bias flipping. The analysis showed that a high power extraction efficacy can be obtained by only using small on-chip capacitors. Careful circuit design allowed high efficacy to be obtained from a prototype chip. The predicted flipping voltage coefficient and, the (compensated for the quiescent power) predicted figure-of-merit (MOPIR) were experimentally validated. The results show an FoM of $7.01\text{--}6.13\times$ and a power efficiency of 87–88% for output power of as little as 1.51–4.85 μ W. To the best of our knowledge, this is the first fully-integrated interface for standard PEHs capable of such performance at a frequency as low as 22 Hz. With this work, it should be possible to reduce the harvesting circuits volume enough to make self-powered implants viable in the near future. Furthermore, it should be possible to apply the core principles of the proposed architecture and utilize the smoothing capacitor to reduce the size of the inductor needed for inductance-based interfaces.

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