Designing Inverters Based on Screen Printed Organic Electrochemical Transistors Targeting Low-Voltage and High-Frequency Operation

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Low-voltage operating organic electronic circuits with long-term stability characteristics are receiving increasing attention because of the growing demands for power efficient electronics in Internet of Things applications. To realize such circuits, inverters, the fundamental constituents of many circuits, with stable transfer characteristics should be designed to provide low-power consumption. Here, a rational inverter design, based on fully screen printed p-type organic electrochemical transistors with a channel size of 150 x 80 µm², is explored for driving conditions with input voltage levels that differs of about 1 V. Further, three different inverter circuits are explored, including resistor ladders with resistor values ranging from tens of kΩ to a few MΩ. The performance of single inverters, 3-stage cascaded inverters and 3-stage ring oscillators are characterized with respect to output voltage levels, propagation delay, static power consumption, voltage gain, and operational frequency window. Depending on the application, the key performance parameters of the inverter can be optimized by the specific combination of the input voltage levels and the resistor ladder values. A few of the inverters are in fact fully functional up to 30 Hz, even when using input voltage levels as low as (0 V, 1 V).

1. Introduction


Organic electrochemical transistors (OECTs)[16,18–27] is currently one of the most studied organic electronic devices and is explored in various applications, such as in fully printed logic circuits,[16,26] active matrix addressed displays,[17] display driver circuits,[19] sensors,[22,23,27–29] neuromorphics,[24] just to name a few. OECTs can be manufactured via cost-effective protocols using different printing techniques, such as screen printing,[19,21]

3D printing,[30] inkjet printing,[14] and other processes,[35,36] OECT-based logic gates and circuits have also been investigated broadly,[35,37–40] where inverters as the elementary components of any combinational logic circuit play a key role. By employing OECT-based inverters[16,26,35] as the essential components of advanced circuits, various forms of OECT-based digital circuits[16,24,35] can be realized.

In organic electronics, by considering the targeted final applications, circuits operating at low voltages and at low power consumption are utterly desired. By lowering the operational voltage margins for circuits, the voltage strain and the risk of degradation can be minimized.[16] This then allows for prolonged operational lifetime, easy integration with other technology platforms and connectivity to communication infrastructure. For example, in Internet of Things (IoT) applications, in order to lower the overall power consumption of systems utilizing a large number of electronic components in a compact circuitry, efficient employment of individual logic components is demanded to expand the IoT ecosystem. To realize such circuitry, the operating voltage levels of the system elements must be reduced. As inverters are the crucial elements of logic circuits, the operating voltage range of the final circuits can be lowered to a large extent.

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by optimizing the inverter designs. Therefore, inverter circuits that operate at low voltages will have an extended lifetime and enable easier integration and connectivity. However, for circuits relying on organic materials, proper operation upon applying low voltage levels is challenging, due to larger threshold voltage alteration of the transistors.[36] To overcome this challenge, transistors and inverters need to be designed properly.

The performance of OECT-based inverters depends to a large extent on the switching voltage and on the ON/OFF current ratio of the OECT. Further, in an OECT there are structural parameters such as channel area (ACh)[13] the area of the carbon source and drain electrodes exposed to the electrolyte (ACD)[15] and the gate electrode area (AC) that impact the overall OECT performance. Subsequently, to design OECT-based inverters, the OECT structure along with other crucial parameters of the resulting inverter circuit, such as the resistor chain, supply voltage, and input voltage levels are equally important. Although previous reports have addressed OECT-based inverters,[1,15,36] the prior works have not focused on the low-voltage operation aspects capable of obtaining rail-to-rail input and output levels along with extended operational lifetime.

In this work, fully screen printed depletion mode OECTs and discrete resistors were configured on a breadboard to assemble inverters, an approach that allows us to easily investigate different resistor ladders. The inverter structures as well as ring oscillators have been comprehensively studied by evaluating how various resistor ladders, input voltage levels, and switching frequencies are affecting the inverter performance including voltage strain, voltage gain, propagation delay, and operational lifetime. To the best of our knowledge, this is the first time an OECT-based inverter in terms of resistor ladder design (Rs) has been comprehensively studied by evaluating how various resistor ladders. The inverter structures as well as ring oscillators have been comprehensively studied by evaluating how various resistor ladders, input voltage levels, and switching frequencies are affecting the inverter performance including voltage strain, voltage gain, propagation delay, and operational lifetime. To the best of our knowledge, this is the first time an OECT-based inverter in terms of resistor ladder design (Rs) has been comprehensively studied.

2. Results and Discussion

2.1. Printed OECTs and Inverter Design

In this study, three sets of p-type depletion mode OECTs were screen printed, where the areas of ACh and AC were ≈50 000 µm² and ≈95 000 µm², respectively, but with different ACD. For these three different OECTs, the channel areas defined by the width (W) and length (L) were 150 × 80, 150 × 100, and 200 × 100 µm². A transistor operating within an inverter structure defines different drain-source voltage (VDS) levels depending on the selection of resistor values, supply voltages, and input levels. For any logic circuit, the input voltage (VIN) levels corresponding to logic “0” (VINL) and logic “1” (VINH) are fundamental parameters for proper operation. The input levels of the inverter can be empirically estimated based on the behavior of the OECT at sufficiently high VDS values. That is, carrying out I–V (drain current vs gate voltage, transfer characteristics) measurements under high VDS levels is one approach to estimate the effective switching voltage and ON/OFF ratio of OECTs. In this work, the I–V measurements were performed for the printed OECTs with VDS equal to −1.5 and −1.7 V, while the gate-source voltage (VG) was swept between 0 to 1.5 V with a step size of 10 mV. Figure 1 illustrates the layers of the printed OECTs, the measured I–V characteristics for the three OECT designs, the circuit schematic of the inverter and the simulated logic output of the inverter in terms of resistor ladder design (R).
Figure 1c schematically depicts an inverter as a voltage divider structure including three resistors (denoted as $R_1$, $R_2$, and $R_3$) and an OECT. The inverter is powered by $V_+$ and $V_-$ as the supply voltage levels. The voltage applied to the gate electrode of the OECT (commonly denoted $V_G$, $V_{IN}$, or control signal) together with the supply voltages and the three resistor values define the output voltage ($V_{OUT}$) levels of the resulting inverter. In an inverter, when $V_{IN,L}$ is applied to the gate electrode, $V_{OUT}$ is determined by $V_+$, $R_1$, $R_2$, and the ON-state channel resistance. Instead, when $V_{IN,H}$ is applied to the gate electrode, the OECT channel switches to high impedance and the $V_{OUT}$ signal is then defined by $V_+$, $V_-$, $R_1$, $R_2$, and $R_3$. Therefore, by choosing the right supply voltages and resistor values, the $V_{OUT}$ signal switches between the $V_{IN,L}$ and $V_{IN,H}$ values. According to the $I$–$V$ measurements of the OECT, with $A_{CS} = 150 \times 80 \mu m^2$ (cf. Figure 1b), the typical ON resistance ($R_{ON}$) and OFF resistance ($R_{OFF}$) of the OECT channel was $\approx 2 \, k\Omega$ and $\approx 50 \, M\Omega$, respectively. These values are estimated from the forward sweeps of the $I$–$V$ measurements for ten OECTs ($A_{CS} = 150 \times 80 \mu m^2$), see Figure S1, Supporting Information. The $R_{ON}$ values, taken at $V_{DS} = -0.1 \, V$ and $V_G = 0 \, V$ to simulate the situation of $V_{IN,L}$, varies between 1.73 and 2.06 k$\Omega$, with a mean value of 1.89 k$\Omega$ and a standard deviation of 0.12 k$\Omega$. The $R_{OFF}$ values, obtained at $V_{DS} = -1.5 \, V$ and $V_G = 1.2 \, V$ to simulate the $V_{IN,H}$ state, varies between 18.1 and 160.9 M$\Omega$, with a mean value of 62.6 M$\Omega$ and standard deviation of 50 M$\Omega$. By observing the $I$–$V$ characteristics of the OECT in Figure 1b, similar ON current values are found for both $V_G = 0$ and $0.1 \, V$, hence, the $V_{IN,L}$ level for this study is set to 0.1 V. To turn the transistor off, a $V_{IN,H}$ value between 1.1 and 1.3 V is sufficient and any further increase in $V_{IN,H}$ will result in higher leakage currents (see the transfer curves). In this work, the effect of $V_{IN}$
levels on the overall performance of an inverter is investigated by using $V_{IN} = (0.1/1.1)$ V, $V_{IN} = (0.1/1.2)$ V and $V_{IN} = (0.1/1.3)$ V. As mentioned earlier, the use of heterogeneous manufactured and configured inverters is motivated by that it gives us the possibility to easily study the effect of different resistor ladders ($R_1$, $R_2$, $R_3$). In the resistor ladder, $R_3$ plays the key role to enable the inverter function since the channel resistance of the OECT in the ON and OFF states strongly defines the value of $R_3$. Ideally, $R_3$ is formulated as $R_3 = \sqrt{R_{ON} \times R_{OFF}}$ for a well-balanced design, where $R_{ON}$ and $R_{OFF}$ is the channel resistance in the ON and OFF state of the OECT, respectively. However, the inverter performance can be optimized depending on the targeted application, for example, either toward fast switching or low power consumption. A rule of thumb is that $R_3$ needs to be at least 20 times higher than $R_{ON}$ and at most one-twentieth of $R_{OFF}$.[16] The $V_{OUT}$ levels of the inverter as a function of $R_3$, achieved from MATLAB simulations, are shown in Figure 1d. The $R_{ON}$ and $R_{OFF}$ value in the simulation is 2 kΩ and 50 MΩ, respectively. For the lowest value of $R_3$, 500 Ω, $V_{OUT}$ does not even exceed 0.26 V, which is far too low to be used in an inverter. When $R_3$ reaches 41 kΩ, the $V_{OUT}$ level increases to an acceptable $V_{OUT}$ level of 1.16 V. When $R_3$ is equal to 316 kΩ, given by the equation $R_3 = \sqrt{R_{ON} \times R_{OFF}}$, the $V_{OUT}$ level is 1.23 V, while the $V_{OUT}$ remains at a sufficiently low level (0.11 V). By further increasing $R_3$ to 2.5 MΩ, $V_{OUT}$ reaches 1.27 V, but at the same time $V_{OUT}$ tends to deviate from the target value (0.22 vs 0.1 V). The ratio between $R_2$ and $R_3$ determines the maximal voltage difference between the gate and the drain ($V_{GD}$), which is crucial for the lifetime and for long-term stability, and an optimized value of this ratio is $0.46$.[16] The resistance of $R_3$ is approximately the sum of $R_2$ and $R_3$, which gives a ratio of $R_2/R_3 = 1.4$ in this work. Therefore, three resistor ladders were chosen to allow for a comparative study of the performance while implemented into inverters established with screen printed PEDOT:PSS-based OECTs. Table 1 presents the three resistor ladders used in this work, named as Low R, Mid R, and High R, where $R_3$ originates from the simulations in Figure 1d.

The selection of the resistor values, supply voltage, and input voltage levels defines the $V_{DS}$ values being applied to the drain side of the transistor in the inverter structure. The three sets of resistor ladders have identical resistor matching, hence, each combination of $V_{IN}$ levels gives that the identical supply voltages can be used for all cases. Thereby, for $V_{IN} = (0.1/1.1)$ V, $V_{IN} = (0.1/1.2)$ V and $V_{IN} = (0.1/1.3)$ V the supply voltage set ($V_i/V_j$) corresponds to $+4.43/-4.42$, $+4.83/-4.84$, and $+5.23/-5.26$ V, respectively, independent of the resistor ladder being chosen. These values imply that the OECTs of the inverters will experience $V_{DS}$ levels of $-1.33$, $-1.46$ and $-1.60$ V for $V_{IN} = (0.1/1.1)$ V, $V_{IN} = (0.1/1.2)$ V, and $V_{IN} = (0.1/1.3)$ V, respectively. Note that the initially chosen $V_{DS}$ values ($-1.5$ and $-1.7$ V), shown in Figure 1b, are reasonable.

In the following, several aspects of the switching behavior have been investigated for single inverters, 3-stage cascade-coupled inverters and 3-stage ring oscillators. The inverter performance is described in terms of output voltage levels with respect to input voltage levels, voltage gain, propagation delay, switching time and/or frequency of oscillation, static power consumption, lifetime stability, and performance at different frequencies of the input signal.

### 2.2. Inverter Output Voltage Levels

The performances of the inverters have been examined for all three resistor ladders along with the three sets of $V_{IN}$ levels, where each set is alternating between $V_{IN,H}$ and $V_{IN,L}$ as square wave pulses at two different frequencies; 0.25 and 1 Hz. The measured switching behavior in terms of $V_{OUT}$ levels is summarized in Figure 2.

According to Figure 2, at 0.25 Hz, all $V_{OUT}$ signals follow a typical square-wave shaped behavior for both the low-to-high and high-to-low voltage transitions. Typically, the propagation delay of an inverter can be extracted from the rise or fall transition times of the $V_{OUT}$ signal with respect to the half-value of the $V_{IN}$ signal span. Then, the average of the rise and fall transition times can represent the overall propagation delay of an inverter. Based on Figure 2, almost independent of the $V_{IN}$ levels, the propagation delay is $\approx$14, $\approx$26, and $\approx$110 ms for the Low R, Mid R, and High R ladder, respectively, at both 0.25 and 1 Hz. As the inverter performance in Figure 2 shows, each of the three different resistor ladders, regardless of the $V_{IN}$ levels, results in distinct trends for both the $V_{OUT}$ levels and the $V_{OUT}$ signal shapes. This behavior, which is more pronounced when using a 1 Hz input voltage signal, is explained in detail in the Supporting Information.

### 2.3. Switching Frequency

The inverter performance for a few frequencies higher than 1 Hz (3, 5, 7, and 10 Hz) is shown in Figure 3. The duration of each measurement is 40 s, but in order to get a clearer view of the $V_{OUT}$ signals at the increased frequencies, only the data from a few hundred milliseconds are shown. However, the $V_{OUT}$ levels during the entire measurements are as stable as those presented in Figure 3. Only the results of $V_{IN} = (0.1/1.2)$ V are shown in Figure 3, while the results of $V_{IN} = (0.1/1.1)$ V and $V_{IN} = (0.1/1.3)$ V can be found in Figure S2, Supporting Information.

#### 2.3.1. Low R Ladder

As shown in Figure 3a, the $V_{OUT}$ signal is only able to switch between 0.1 and 0.16 V when using the Low R ladder at a

<p>| Table 1. Specifications of the three resistor ladders used in OECT-based inverters connected on a breadboard. |</p>
<table>
<thead>
<tr>
<th>resistor ladder</th>
<th>Resistor values</th>
<th>$R_1/R_3$</th>
<th>$R_2/R_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low R ($R_3&gt;20R_{ON}$)</td>
<td>$R_1=57.6$ [kΩ]</td>
<td>1.40</td>
<td>0.46</td>
</tr>
<tr>
<td></td>
<td>$R_2=19$ [kΩ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_3=41$ [kΩ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mid R ($R_3=\sqrt{R_{ON} \times R_{OFF}}$)</td>
<td>$R_1=442$ [kΩ]</td>
<td>1.40</td>
<td>0.46</td>
</tr>
<tr>
<td></td>
<td>$R_2=146$ [kΩ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_3=316$ [kΩ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High R ($R_3&lt;R_{OFF}/20$)</td>
<td>$R_1=3.5$ [MΩ]</td>
<td>1.40</td>
<td>0.46</td>
</tr>
<tr>
<td></td>
<td>$R_2=1.16$ [MΩ]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_3=2.5$ [MΩ]</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
switching frequency of 3 Hz, that is, only ≈5% of the \( V_{\text{IN}} \) window is achieved at the \( V_{\text{OUT}} \) measurement node. This further proves that the OECT channel is easily switched to its OFF state when using the Low \( R_l \) ladder, whereas switching the channel to its ON state is a slow process that cannot be achieved at 3 Hz. Hence, for the inverter based on the Low \( R_l \) ladder, 1 Hz is approximately the upper limit for the operating frequency. Because of this, the Low \( R_l \) ladder inverters have not been characterized at frequencies above 3 Hz.

### 2.3.2. Mid \( R_l \) Ladder

For the inverters based on the Mid \( R_l \) ladder, the on and off switching times are better matched, which means that higher operation frequencies are possible. This is evident in Figure 3b–d where the inverter switches at 5, 7, and 10 Hz, with \( V_{\text{OUT}} \) levels matching >99% of the \( V_{\text{IN}} \) levels. With such a negligible voltage decay, a safe voltage propagation is guaranteed when implementing logic circuits through cascade-coupling of several inverters.

### 2.3.3. High \( R_l \) Ladder

The voltage spikes observed in the \( V_{\text{OUTL}} \) signal for the High \( R_l \) ladder (red curves in Figure 3a,b) can be related to the capacitive effect stemming from charge accumulation in the load capacitance. That is, by using high resistances in the resistor ladder of the inverter, the transition from a charged state (at \( V_{\text{IN,H}} \)) to a discharged state (at \( V_{\text{IN,L}} \)) is prolonged by the RC component, which in turn results in the voltage spikes. By neglecting the voltage spikes, it can be observed that the \( V_{\text{OUT}} \) signal switches between 0.23 and 1.2 V in Figure 3a, that is, ≈88% of the \( V_{\text{IN}} \) window is reached by the \( V_{\text{OUT}} \) levels. By comparing the behavior at 0.25 Hz (Figure 2c), 1 Hz (Figure 2f), 3 Hz (Figure 3a), and 5 Hz (Figure 3b), it is obvious that the slow ON-to-OFF switching of the OECT when using the High \( R_l \) ladder prevents the inverter to operate at frequencies higher than ≈0.25 Hz, simply because the targeted \( V_{\text{OUTL}} \) level is not reached before the opposite switching is initiated.

### 2.4. Lifetime Stability of the Inverter

Voltage strain (\( V_{\text{GD}} \)) is defined as the voltage between the gate and drain electrodes of the OECT inside the inverter circuit. The \( V_{\text{GD}} \) is equal to the sum of the \( V_{\text{IN}} \) being applied and the highest \( V_{\text{DS}} \) value that the OECT experiences (depending on the selected supply voltages, the resistor values and the logic state of the inverter) during the inverting process. The highest \( V_{\text{GD}} \) is obtained upon applying \( V_{\text{IN,H}} \), since this also implies a high \( V_{\text{DS}} \) in the inverter circuit, the inverter design and targeted voltage levels are therefore critical in order to lower the probability of OECT degradation. As described in conjunction with Figure 1b, the OFF current level of the OECT is increasing...
upon elevating $V_{IN}$ and/or $V_{DS}$ beyond their critical values. Therefore, the $V_{IN}$ and $V_{DS}$ values are directly influencing the performance and lifetime of the OECT. Hence, to prolong the operational lifetime in an OECT-based inverter, or other logic circuits, it is of critical importance to minimize $V_{GD}$.

Each specific $V_{IN}$ window results in identical $V_{DS}$ values for the three different resistor ladders used herein, since they are relying on identical resistor matching. However, for a given $V_{DS}$, different $V_{GD}$ values can be obtained by varying the $V_{IN, H}$ level. For instance, for any of these three resistor ladders, the $V_{IN}$ signal specified by $V_{IN} = (0.1/1.1)$ V leads to $V_{GD} = 2.43$ V. The lifetime stability of inverters based on Mid $R$ ladders in terms of different $V_{GD}$ levels is illustrated in Figure 4, where $V_{GD} = 2.43$ V, $V_{GD} = 2.66$ V, and $V_{GD} = 2.90$ V corresponds to $V_{IN} = (0.1/1.1)$ V, $V_{IN} = (0.1/1.2)$ V and $V_{IN} = (0.1/1.3)$ V, respectively. Hence, the recorded values of $V_{OUT, H}$ and $V_{OUT, L}$ as a function of time give an indication of how performance and lifetime of inverters based on the Mid $R$ ladder, in this case switched at 1 Hz, are affected for various $V_{IN}$ windows.

It can be observed from Figure 4 that the operational lifetime is inversely proportional to the overall voltage strain on the inverter. The degradation of the inverter is illustrated by a gradual decrease of the $V_{OUT, H}$ level, which occurs due to a gradual increase of $R_{ON}$ in the OECT channel during the measurement. Hence, a higher $V_{GD}$ value results in faster device degradation. It can also be observed that the $V_{OUT, L}$ levels are very stable over time, for all $V_{IN}$ windows, which indicates that the OECT channels always can be switched to their OFF states upon applying $V_{G}$. For $V_{GD} = 2.90$ V (corresponding to $V_{IN} = (0.1/1.3)$ V), the $V_{OUT, H}$ graph starts to decline after ≈1.5 h of constant switching at 1 Hz, whereas for $V_{GD} = 2.43$ V, the $V_{OUT, H}$ graph starts dropping after ≈3.5 h. Hence, the operational lifetime of the inverter is at least doubled upon decreasing $V_{GD}$ from 2.90 to 2.43 V. The inverters were not able to recover after several days of resting, which is an evidence of permanent OECT degradation. Thus, minimizing $V_{GD}$ is advantageous for the OECT operational lifetime.

2.5. Propagation Delay

In an inverter, it takes time for the voltage signal to propagate from the input to the output, which is defined as the propagation delay ($t_p$). The propagation delay occurs due to the load (switching) capacitance in the OECT, which is charged and discharged during the signal transitions. A smaller load capacitance leads to a shorter propagation delay. The propagation delay is a key parameter dictating the switching frequency of logic circuits. In the following, the propagation delay is investigated by cascade coupling of three OECT-based inverters, as well as by connecting three inverters into 3-stage ring oscillators. The results are summarized in Figure 5 for $V_{IN} = (0.1/1.2)$ V.
whereas the results for $V_{IN} = (0.1/1.1)$ V and $V_{IN} = (0.1/1.3)$ V are found in Figures S3 and S4, Supporting Information, respectively. All measurements were performed for 12 s, but to get a clearer view of the $V_{OUT}$ signals, only a few seconds from each measurement are shown. The $V_{OUT}$ levels were stable during the entire measurements.

### 2.5.1. Cascade-Coupled Inverters

In Figure 5a–c, the $V_{IN}$ and $V_{OUT}$ signals of single inverters and 3-stage cascade-coupled inverters are shown for the three different resistor ladders. A cascade-coupled inverter circuit consists of several inverters connected in series, such that the $V_{IN}$ signal is applied at the gate electrode of the first inverter, the $V_{OUT}$ signal of the first inverter is connected to the gate electrode of the second inverter, and so on for an arbitrary number of inverters, and the $V_{OUT}$ signal is finally recorded at the measurement node of the last inverter. Thus, each inverter contributes to the total propagation delay, that is, the total propagation delay increases with the number of inverters (stages). The propagation delay of a single inverter can be assessed based on the low-to-high and high-to-low transitions of the $V_{OUT}$ signal. The propagation delay when the $V_{OUT}$ signal transits from the low to high state, and reaches 50% of the $V_{IN}$ voltage window, is denoted by $t_{pLH}$, while $t_{pHL}$ is the propagation delay when $V_{OUT}$ transits from the high to low state. The $t_{pLH}$ and $t_{pHL}$ show approximately similar values and the propagation delay of the inverter is here defined by the average of these two values. According to Figure 5a–c, the signal propagation delay per stage for the Low $R$, Mid $R$, and High $R$ ladders is...
The oscillation frequency (or period) of ring oscillators depends on the propagation delay $t_p$, causing the oscillation. The oscillation frequency (or period) gets inverted, due to the odd number of inverters, thereby leads to an increased oscillation frequency. In these measurements the supply voltages of the inverters were set to mimic the reference values. Hence, no external input signal is required in the ring oscillator circuit, and in these measurements the supply voltages of the inverters were set to mimic the case of using $V_{IN} = (0.1/1.2)$ V. The $V_{OUT}$ at the last stage gets inverted, due to the odd number of inverters, thereby causing the oscillation. The oscillation frequency (or period time) of ring oscillators depends on the propagation delay $t_p$ of each inverter. In a ring oscillator with $N$ stages, the propagation delay can be calculated as $t_p = (2 \cdot N \cdot f_0)^{-1}$, where $f_0$ is the oscillation frequency. Naturally, a short propagation delay leads to an increased oscillation frequency. In these measurements the $V_{OUT}$ signals are recorded in one of the inverters of the 3-stage ring oscillator circuits. Based on the self-oscillations shown in Figure 5d–f, the $V_{OUT}$ signals oscillate at $\approx 22.6$ Hz, $\approx 74$ Hz, and $\approx 1$ Hz for the Low $R$, Mid $R$ and High $R$ ladder, which corresponds to an inverter propagation delay of $7$, $22.5$, and $166.5$ ms, respectively. Thus, the measurement results of the ring oscillators are matching relatively well with the measured and simulated results of the cascade-coupled inverters described in the previous section, and the trend is that the oscillation frequency decreases with increased resistances in the resistor ladder. The propagation delays obtained from the ring oscillators are slightly longer than those obtained from the 3-stage cascade-coupled inverters, this is probably due to that the latter are driven by an external $V_{IN}$, whereas the input signal in the ring oscillator is provided by the feedback loop. Note that when using the Low $R$, Mid $R$, and High $R$ ladder in the ring oscillators, the $V_{OUT}$ signals oscillate between 0.26 and 1.07 V, 0.18 and 1.14 V, and 0.31 and 1.14 V, respectively. This corresponds to $\approx 73\%$, $\approx 87\%$, and $\approx 75\%$ of the targeted $V_{IN}$ levels, which indicates that ring oscillators based on the Mid $R$ ladder is the most stable alternative. A detailed summary of the self-oscillating $V_{OUT}$ levels for the three resistor ladders, when mimicking $V_{IN} = (0.1/1.1)$ V, $V_{IN} = (0.1/1.2)$ V and $V_{IN} = (0.1/1.3)$ V, is presented in Table S2, Supporting Information.

2.5.2. Ring Oscillators

Figure 6a compares the relationship between oscillation frequency and supply voltage of the ring oscillators (based on the Low $R$ ladder) in this work versus the organic-based ring oscillators (manufactured by printing and hybrid techniques) reported in the literature. Among the OECT-based ring oscillators so far reported in the literature, the ring oscillator in this work achieved the fastest signal propagation, to the best of our knowledge.

2.6. Voltage Gain and Static Power Consumption

Voltage gain, defined as the ratio of the $V_{OUT}$ to the $V_{IN}$ signal, is the ability of an electronic component to amplify a voltage signal from its input to the output. Here, the voltage gain values are extracted from the forward sweeps of the voltage transfer characteristics of the inverters, where the $V_{IN}$ is swept from 0 to 1.4 V with a step size of 10 mV. For the inverter
voltage transfer measurements, and similarly to the operation of the ring oscillators, different \( V_{IN} \) signals can be mimicked by tuning the supply voltages. By mimicking \( V_{IN} = (0.1/1.2) \) V, a voltage gain of \( \approx 6.4, \approx 13.9, \) and \( \approx 17 \) is achieved for the Low \( R \), Mid \( R \), and High \( R \) ladder, respectively. The voltage gain tends to increase by increased \( V_{IN,R} \) level. For example, by mimicking \( V_{IN} = (0.1/1.3) \) V, voltage gain values of \( \approx 7.1, \approx 14.2, \) and \( \approx 18 \) are measured for the respective resistor ladder. Table S3 and Figure S5, Supporting Information, present the voltage gain values for the three resistor ladders when mimicking different sets of \( V_{IN} \) signals.

For an inverter, static power \( (P) \) is a combination of leakage and standby power. The leakage part arises from the reverse bias current in an OECT switched to its OFF state, while the standby part is due to constant current flow from the positive supply voltage \( (V_s) \) to the ground in an OECT switched to its ON state. Therefore, the power consumption depends on the OECT state (ON or OFF), and the total power is calculated from either of the two following equations:

\[
P = \frac{(V_s)^2}{(R_s + R_s + R_{ON})} + \frac{(V_s)^2}{(R_s)} \quad (1)
\]

\[
P = \frac{(V_s - V_{OUT})^2}{(R_s + R_s + R_s)} + \frac{(V_{OUT})^2}{(R_{OFF})} \quad (2)
\]

Since the OECT consumes very little power compared to the resistor ladder, the two equations above give almost the same result. Thus, an inverter that is in one state (ON or OFF) during most of its operational time will consume approximately the same amount of power as an OECT that is ON during 50% and OFF during 50% of its operational time. Therefore, the total static power consumption is approximated by using the average result of the two equations above. Here, the ranges of the static power consumption for the inverters based on the Low \( R \), Mid \( R \), and High \( R \) ladders are 690–990, 90–130, and 10–16 \( \mu W \), respectively, where the exact value depends on the \( V_{IN} \) voltages used. As expected, the required static power decreases when the resistances in the resistor ladder are increased. The power consumption of the inverter based on the Low \( R \) ladder is \( \approx 65 \) times higher as compared to the High \( R \) ladder. This is explained by that \( R_s \) when employing the Low \( R \) ladder, is comparable to \( R_{ON} \) of the OECT, and relatively high current flows through \( R_s \) when the OECT is in its ON state. On the other hand, when using the High \( R \) ladder, \( R_s \) of the inverter has much higher resistance than \( R_{ON} \) of the OECT, and therefore the leakage current through \( R_s \) and its corresponding power consumption become negligible when the OECT is ON. The detailed values of the static power consumption, calculated for the three resistor ladders mimicking different input voltage levels, are presented in Table S3, Supporting Information. Figure S6b summarizes the static power consumption, voltage gain, and oscillation frequency corresponding to the three resistor ladders. This figure can serve as a guide for selecting the resistor ladder with the lowest power consumption that still meets the requirements of a particular application in terms of voltage gain and oscillation frequency.

According to Figure 6, regardless of the selected \( V_{IN} \) signal, the High \( R \) ladder provides an inverter with low power consumption at the cost of oscillation frequency, while the Low \( R \) ladder results in inverters with faster oscillations, but high power consumption. The Mid \( R \) ladder gives an intermediate performance in terms of all the parameters. Therefore, we conclude that the Mid \( R \) ladder offers a good balance for general applications.

**Table 2** summarizes key parameters for the performance of the organic-based inverters reported in earlier studies and in this work. The table compares the effect on the inverter performance with respect to the transistor type, the organic material used in the channel and the transistor channel area \( (A_{CH}) \). To the best of our knowledge, this work reports on the lifetime stability of organic-based inverters for the first time.

### 2.7. Inverters with 1 V Input Voltage Window

Minor misalignment between the layers is likely to occur in screen printed OECTs, especially when considering that these devices are multi-layered and have relatively small dimensions. The effect of trivial misalignments can introduce minor changes in performance, including the OECT switching voltage. In this work, the majority of the printed OECTs guarantee full switching of the inverters for \( V_{IN,HI} > 1 \) V, therefore, the results presented so far have focused on \( V_{IN} = (0.1/1.1) \) V, \( V_{IN} = (0.1/1.2) \) V and \( V_{IN} = (0.1/1.3) \) V. However, the printed OECTs with highest performance are also fully switching with \( V_{IN} = (0/1) \) V, resulting in an even lower voltage strain \( (V_{GD} = 2.33 \) V), which consequently results in prolonged operational lifetime along with properly defined \( V_{OUT} \) levels also at higher frequencies. Figure 7 shows the switching behavior of an inverter based on one of the best OECTs and the Mid \( R \) ladder, when using a 1 V input voltage window of \( V_{IN} = (0/1) \) V at 10 and 30 Hz.

As shown in Figure 7, the inverter is operational at 10 Hz since the \( V_{OUT} \) signal levels are matching well with the input

---

**Table 2:** Literature overview on key parameters in organic-based inverters.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Technology</th>
<th>Channel material</th>
<th>( A_{CH} = W \times L ) [( \mu \text{m}^2 )]</th>
<th>( V_{IN} ) levels [V]</th>
<th>( V_{OUT} ) levels [V]</th>
<th>Supply voltages [V]</th>
<th>Voltage gain</th>
<th>Lifetime stability [h]</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work (Mid ( R ) ladder)</td>
<td>OECT</td>
<td>PEDOT:PSS</td>
<td>150 × 80</td>
<td>0.1/1.2</td>
<td>(-0.1/1.2)</td>
<td>(+4.83/\sim 4.84)</td>
<td>13.93</td>
<td>(\gtrsim 3)</td>
</tr>
<tr>
<td>[1]</td>
<td>OECT</td>
<td>PEDOT:PSS</td>
<td>320 000</td>
<td>0/1</td>
<td>(=0/1)</td>
<td>(+4/\sim 4)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>[16]</td>
<td>OECT</td>
<td>PEDOT:PSS</td>
<td>150 × 100</td>
<td>0/1.3</td>
<td>(=0/1.3)</td>
<td>(+5/\sim 5)</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>[26]</td>
<td>OECT</td>
<td>PEDOT:PSS</td>
<td>500 × 1000</td>
<td>0/1.5</td>
<td>(0.02/1.25)</td>
<td>(+3.5/\sim 3.5)</td>
<td>3.3</td>
<td>—</td>
</tr>
<tr>
<td>[39]</td>
<td>Complementary</td>
<td>p-type: P(Tp Tp Tp</td>
<td>15 000 × 2.5</td>
<td>0/1</td>
<td>(=0/1)</td>
<td>(+1/0)</td>
<td>17.5</td>
<td>—</td>
</tr>
</tbody>
</table>
voltage levels. Furthermore, this inverter performs even up to 30 Hz, where the \( V_{\text{OUT}} \) signal is reaching \( \approx 70-90\% \) of the \( V_{\text{IN}} \) voltage window. This is an important observation for screen printed OECT-based inverters, since they are routinely considered for operation at very low frequencies.\[^{[16,26]}\] Here, for the \( V_{\text{IN}} \) voltage window of 1 V, a voltage strain of \( V_{\text{GD}} = 2.33 \) V is obtained. That is, shifting the \( V_{\text{IN,H}} \) level from 1.1 to 1 V results in 100 mV lower \( V_{\text{GD}} \), which is advantageous for the lifetime stability, and concurrently well-defined \( V_{\text{OUT}} \) levels of the inverter are accessible at least up to 10 Hz.

### 3. Conclusions

An inverter design based on screen printed p-type depletion mode OECTs with a small channel size (150 \( \times \) 80 \( \mu \)m\(^2\)) was explored for operation with a \( \approx 1 \) V input voltage window. Three different resistor ladders (with resistance values on the order of tens of k\( \Omega \) (Low R), few hundreds of k\( \Omega \) (Mid R), and a few M\( \Omega \) (High R)) were also applied and evaluated in the inverter circuits. The performance was investigated in terms of output voltage levels, propagation delay, static power consumption, voltage gain, and oscillation frequency for single inverters, 3-stage cascade-coupled inverters and 3-stage ring oscillators.

The screen printed OECTs with best performances result in inverters with output voltage levels reaching \( \approx 70-90\% \) of the input voltage levels \( V_{\text{IN}} = (0/1) \) V at a switching frequency of 30 Hz. However, for the majority of the OECTs, a slight increase of the input voltages is required, that is, \( V_{\text{IN}} = (0.1/1.1) \) V, \( V_{\text{IN}} = (0.1/1.2) \) V, or \( V_{\text{IN}} = (0.1/1.3) \) V is needed in order to give consistent results in terms of complete switching of the output voltage levels (ranging from \( \approx 93\% \) to \( \approx 99\% \) of the input voltage levels). For the three sets of input voltage levels, it was shown that the inverters, based on the three different resistor ladders, have low output voltage decays when switched at low frequencies (0.25 and 1 Hz). However, upon increasing the switching frequency to 7 or 10 Hz, only the inverter with the Mid R ladder performs properly in terms of acceptable output voltage levels. This implies that the inverter based on the Mid R ladder enables cascade coupling and reliable signal propagation in more advanced logic circuits.

The propagation delay of the inverter is prolonged by increasing the resistor values of the ladder. Among the three resistor ladders here evaluated, the Low R ladder results in the shortest propagation delay for a single stage inverter; \( \approx 12 \) ms. This was also confirmed by evaluating self-oscillations in the inverters by configuring a 3-stage ring oscillator based on the Low R ladder, which shows an oscillation frequency of \( \approx 22.6 \) Hz, corresponding to a propagation delay of \( \approx 7 \) ms. To the best of our knowledge, this is the fastest signal propagation observed for screen printed OECT-based ring oscillators.

The inverters based on the High R ladder, on the other hand, show the highest amplification performance, but clearly also the longest propagation delay characteristics.

It was shown that the operational lifetime of the inverters is inversely proportional to the overall voltage strain applied to the inverter. When employing too high \( V_{\text{IN}} \) levels, in combination with a high voltage between the drain and source electrodes, the OECT suffers from parasitic electrochemical reactions that results in shortened operational lifetime. A combination of \( V_{\text{IN}} = (0.1/1.2) \) V and the Mid R ladder gives a good compromise between operational lifetime, low output voltage decay, propagation delay, power consumption, and voltage gain. These attributes make this inverter a good candidate for many generic logic applications, we believe. Discrete resistors were here used to simplify the reconfiguration of the resistor ladders in circuits, but monolithic OECT-based inverter circuits are also possible to manufacture using screen printing on flexible substrates, as previously reported.

### 4. Experimental Section

**Fabrication of OECTs:** First the OECTs were designed by using the Clewin software (WieWeb Software Inc., Netherlands). The resulting OECT designs were manufactured by using screen printing. The printing was done with a screen printer (DEK Horizon 03IX) using polyester meshes. The following layers were printed on a polyethylene terephthalate (PET) plastic substrate, and upon printing the thicknesses were estimated with an optical profilometer (Sensofar Plu neox). Silver (Ag 5000 purchased from DuPont) was printed as the first layer, to create the probe pads at a thickness of \( \approx 11 \) \( \mu \)m. PEDOT:PSS (Clevios S V4 purchased from Heraeus) was printed as the second layer, at a thickness of \( \approx 0.5 \) \( \mu \)m, to provide the OECT channel, followed by \( \approx 9 \) \( \mu \)m thick.
carbon (7102 conducting screen printing paste purchased from DuPont) pads as the source and drain electrodes. Each one of these three layers were thermally treated at 120 °C for 5 min. Next, an insulating (5018 purchased from DuPont) layer with a thickness of 15 μm was screen printed and cured with UV light irradiation. The area defined by the insulating layer was covered by a screen printed 13 μm thick electrolyte material (AF1 VV009 provided by RISE), followed by UV-curing. Finally, another layer of PEDOT:PSS (with a thickness of 0.5 μm), serving as the gate electrode, was printed on top of the electrolyte layer.

Characterization and Measurements: The printed OECTs were stored at a temperature of -20 °C and a relative humidity of ~50%RH, and all measurements were carried out under the same conditions. For the OECT characterization, the transfer measurements (I-V) were performed using a semiconductor parameter analyzer (HP/Agilent 4155B). Inverters were constructed using the screen printed OECTs, passive resistors, and a breadboard. For the characterization of the inverters, the semiconductor parameter analyzer and a function generator (Agilent 33120 A) were used.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

inverters, organic electrochemical transistors, organic electronics, printed electronics, PEDOT:PSS

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