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Hybrid Coupler for LMBA Input Match using an Active Inductor.

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Abstract

With the increase in demand for compact and high data rate communication systems, there is a need for high efficiency with modulated signals (PAPR 5-10 dB) for base-station power amplifiers. One of the famous architectures used to achieve this is Doherty architecture. The architecture has recently been extended to the Load Modulated Balanced Amplifier (LMBA) concept, where a separate integrated amplifier generates the control signal for load modulation. Almost all published studies are concerned with discrete "PCB-based" solutions for LMBA. In a recent study [1], the potential of designing an integrated LMBA in 0.18 μm CMOS has been evaluated. The main limitation concerning losses and area comes from the quadrature couplers, consisting of either two or four inductors. Using active inductors in the coupler design may be possible to obtain a more cost-effective solution. However, several aspects must be taken into consideration. One is that the power consumption of the active inductor should not exceed the power loss of the passive inductor. Another one is the ability to handle high power signals (high voltage swing), corresponding to 10-15 dBm at the input of the amplifier. The main objective of this thesis is to implement a hybrid coupler using an active inductor based on the theory of gyrators. The circuits were implemented using TSMC 0.18 μm process. The coupler and the active inductor are designed to operate at 2 GHz centre frequency. The active inductor implemented is considerably linear up to 12 dBm. The coupler has an input reflection coefficient (S11) of -26 dB, the transmission coefficient (S21) of -4.4 dB, and a coupling coefficient (S31) of -2.4 dB. The coupler shows good coupling and isolation characteristics. The phase difference between the through-port and the coupled-port of the coupler is 92°. As a result, when used as a power divider at the input of the power amplifiers, a PAE (Power Added Efficiency) of 63% and output power of 23 dBm is obtained at an input power of 12 dBm.

Keywords: LMBA, gyrator-c, active inductor, hybrid coupler, TSMC 0.18 μm.

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-Karthik Doddanna

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Abbreviations

LMBA- Load Modulated Balanced Amplifier
RFIC- Radio Frequency Integrated Circuit
CMOS- Complementary metal-oxide-semiconductor
PA- Power Amplifier
GaAs- Gallium Arsenide
PCB- Printed Circuit Board
TSMC- Taiwan Semiconductor Manufacturing Company
VHF- Very High Frequency
DC- Direct Current
AC- Alternating Current
AI- Active Inductor
THD- Total Harmonic Distortion
DLM- Dynamic Load Modulation
CA- Control Amplifier
PAE- Power Added Efficiency
ADS- Advanced Design System

1

Introduction

1.1 Motivation

With the recent advancements in wireless communication technology, there is a high demand for low-cost, low-power, and small-size multifunctional radio frequency front-end circuits [2]. Radio Frequency Integrated Circuits (RFIC) technology have been pushed to extremes to meet the increased need in data capacity and decreased size and power consumption [3]. Power amplifiers are a vital part of the transmitter. Modern wireless communication systems' energy efficiency and linearity are mainly dominated by the transmitter's Power Amplifier (PA) performance [1]. There are several PA efficiency enhancement techniques proposed [4]. In contrast, some of the popular efficiency enhancement techniques like Doherty PA have several drawbacks. The Doherty PA has a larger footprint and narrow bandwidth due to quarter-wave inverters and impedance transformers [5]. Methods to maximize efficiency, linearity, and bandwidth enlargement have been discussed using on-chip transformers and lumped elements [6].

Load Modulated Balanced Amplifier (LMBA) and its variants are discussed in recent studies, employing load modulation techniques to achieve good efficiency [7] [8] [9] [10] [11]. Even though LMBA has the advantage over Doherty architecture, the proposed solutions are Printed Circuit Board (PCB)-based solutions. Which still occupies a more significant footprint. In a recent study, the potential of designing an integrated LMBA in 0.18 μm Complementary metal-oxide-semiconductor (CMOS) has been evaluated [1]. This also involved replacing the discrete couplers and matching networks with their lumped counterparts. The primary limitations

concerning the losses and area come from the quadrature couplers, which use four to two on-chip passive inductors [1].

Couplers are essential components in radio frequency and microwave applications, such as balanced amplifiers, phase shifter modulators, microwave mixers, and filters. Conventional couplers have traditionally had been designed using transmission line technology with insulating substrates such as gallium arsenide (GaAs). The coupler design based on transmission lines is bulky, especially at lower frequencies like below 10GHz, thus making on-chip integration very challenging [12]. To achieve a small footprint, traditional transmission line couplers are replaced by lumped couplers which consist of spiral inductors and capacitors for on chip applications. However, these passive components still pose disadvantages.

CMOS spiral inductors have found a wide range of applications in high-speed communication. These applications include impedance matching, frequency selection, bandwidth enhancements, to name a few. However, the effectiveness of the spiral inductors is affected by several limitations, such as occupies a large silicon area, a low self-resonant frequency, a low or medium quality factor, sensitivity to temperature variations, and non-tuneable inductance [13].

To overcome these problems, in some cases, active inductors are preferred. CMOS active inductors are active networks that consists mainly of MOS transistors. The underlying idea of an active inductor comes from the theory of gyrators, which consists of two back-to-back connected positive and negative trans-conductors [13]. These inductors have some advantages, such as good quality factor, small footprint, and low fabrication costs compared to spiral inductors [14].

Hence an attempt has been made to overcome the drawbacks in CMOS LMBA design concerning the significant area occupied by a lumped coupler. To design a hybrid coupler using active inductors that can replace the lumped coupler at the input and still maintain good performance, is the main drive behind the motivation of this thesis work.

1.2 Aim

This thesis aims to explore the possibility of replacing lumped coupler with a hybrid coupler using an active inductor. It involves designing an active inductor that could be integrated into a coupler design. The design is done using the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18µm process and followed by integrating this hybrid coupler with the CMOS LMBA design. However, several aspects must be considered. One is that the power consumption of the active inductor should not exceed the power loss of the passive inductor. Another one is the ability to handle high power signals (high voltage swing), corresponding to 10-15 dBm at the input of the amplifier.

1.3 Problem statements

This thesis is based on below important research questions.

- Can the active inductor be linear up to 15dBm to handle the high-power swings at the input?
- Does the power consumption of the AI significantly influence the PAE of the full amplifier?
- To what extent is the performance degradation in PA, when integrated with a hybrid coupler using active inductors?

1.4 Limitations

One of the research limitations is concerning the selection of coupler architecture based on the use of floating active inductor or single-ended active inductor. Another limitation is the linearity of the active inductors. Linearity is an important issue regarding the use of active inductors. When the active inductors are driven with large signals, the operating points of the devices vary with the signal amplitude. Hence, small-signal models are not valid.

1.5 Report Structure

This report is divided into six chapters. Chapter 1 gives a general introduction of the thesis work, and the research questions that led to this thesis are explained. Chapter 2 gives the theory of the active inductors and general models of an active inductor, the coupler, its mathematical explanation, and Load Modulated Balanced Amplifier (LMBA). In Chapter 3, the active inductor implementation with CMOS 0.18um is explained, and the design of a hybrid coupler using this active inductor is given. From the obtained simulations, the results are discussed in Chapter 4. In Chapter 5, a discussion and justification of the results are made. In Chapter 6, future work and optimization of the current design are discussed.

2

Theory

This chapter explains the fundamental theory of the couplers, inductors, and their applications in RF systems. The metrics that determine the performance of the coupler and inductor have been discussed. Also, the concept of Load Modulated Balanced Amplifier (LMBA) and the uses of coupler in LMBA is presented in this chapter.

2.1 Directional Coupler

The communication systems often experience issues regarding splitting signals into multiple paths with a well-defined phase shift. This problem is usually solved by using a general class of circuits called directional couplers [15]. A directional coupler is a four-port network that split the signal into two paths with a relative phase difference of 90° or 180°. A directional coupler has a wide range of applications in RF and microwave circuits, such as a balanced amplifier [16], Doherty amplifiers [5], phase shifter modulators, beamforming networks for antennas [17], microwave mixers [18], and filters [19].

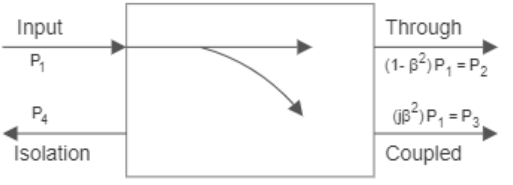

Figure 2-1: Block diagram representation of directional coupler.

A basic block diagram of a directional coupler, as shown in Figure 2-1, consists of four ports, input-port, through-port, coupled-port, and isolation-port. The input power applied at port one is coupled to port three with coupling factor β^2, and at port two, the power applied at port one is output with the coefficient $\alpha^2 = 1 - \beta^2$. However, any port can be defined as the input port, thus switching the through-port, coupled-port, and isolation-port appropriately. There are three broad categories of directional couplers based on the relative position of the isolated-port to the input-port that is contra-directional, co-directional, and trans-directional couplers [20]. In contra directional coupler, as shown in Figure 2-2(a), port one is the input-port, and the output ports are port two and port four, and port three is the isolated port. Figure 2-2(b) shows a codirectional coupler, and it is the most used coupler where port one is the input, and the output ports are port two and port three, and port four is the isolated port. The last category of a coupler is trans-directional, in which port one is the input, and the output ports are port three and port four, and port two is the isolated port is shown in Figure 2-2(c). In this thesis, a codirectional couple has been implemented.

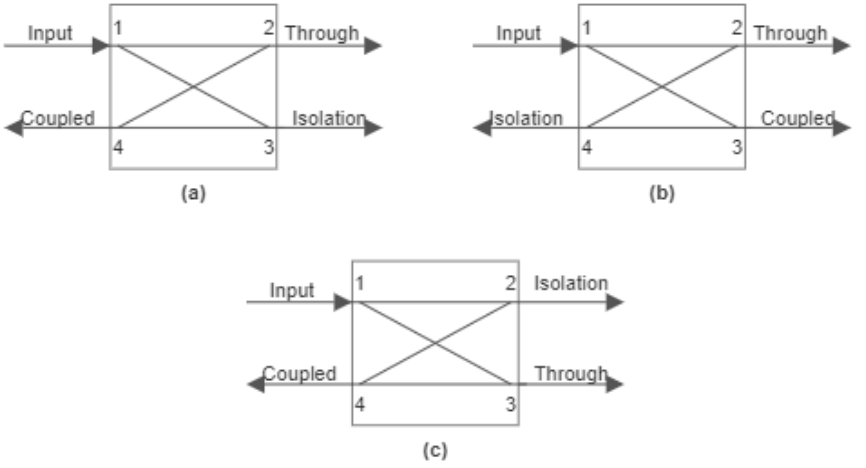

Figure 2-2: Block diagram of directional coupler based on the relative location of the ports, (a) Contra-directional, (b) Co-directional, (c) Trans-directional.

The scattering of a four-port network matched at all ports is shown below [21]:

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} & S_{14} \\ S_{12} & 0 & S_{23} & S_{24} \\ S_{13} & S_{23} & 0 & S_{34} \\ S_{14} & S_{24} & S_{34} & 0 \end{bmatrix} \quad 2.1$$

Multiplication of row 1 and row 2, and multiplication of row 4 and row 3, gives.

$$S_{13}^{*}\, S_{23} + S_{14}^{*}\, S_{24} = 0 \quad 2.2$$

$$S_{14}^{*}\, S_{13} + S_{24}^{*}\, S_{23} = 0 \quad 2.3$$

Multiplying equation 2.2 by S_{24}^{*}, and equation 2.3 by S_{13}^{*}, and the results are subtracted to obtain the following equation,

$$S_{14}^{*}(|S_{13}|^2 - |S_{24}|^2) = 0 \quad 2.4$$

Multiplication of row 1 and row 3, and multiplication of row 4 and row 2 gives.

$$S_{12}^{*}\, S_{23} + S_{14}^{*}\, S_{34} = 0 \quad 2.5$$

$$S_{14}^{*}\, S_{12} + S_{34}^{*}\, S_{23} = 0 \quad 2.6$$

Multiplying equation 2.5 by S_{12}, and equation 2.6 by S_{34}, and the results are subtracted to obtain,

$$S_{23}(|S_{12}|^2 - |S_{34}|^2) = 0 \quad 2.7$$

The equations 2.4 and 2.7 are satisfied if $S_{14} = S_{23} = 0$, which results in a directional coupler. The self-product of the rows of the unitary scattering matrix

2.1 gives the following equations.

$$|S_{12}|^2 + |S_{13}|^2 = 1 \quad 2.8$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \quad 2.9$$

$$|S_{13}|^2 + |S_{34}|^2 = 1 \quad 2.10$$

$$|S_{24}|^2 + |S_{34}|^2 = 1 \quad 2.11$$

From the equations it can be implied that, $|S_{13}| = |S_{24}|$ and $|S_{12}| = |S_{34}|$.

Simplification is made by giving phase reference to the three of the four ports such that, $S_{12} = S_{34} = \alpha$, $S_{13} = \beta e^{j\theta}$, and $S_{24} = \beta e^{j\emptyset}$. Where, α and β are real and $\emptyset$ and θ are the phase constants. The dot products of row 2 and 3 gives,

$$S_{12}^* S_{13} + S_{24}^* S_{34} = 0 \quad 2.12$$

This yields the relation between the phase constants as,

$$\theta + \emptyset = \pi \pm 2n\pi \quad 2.13$$

There are two choices that occur when we ignore the integer multiples 2π.

1. A Symmetric Coupler: $\theta = \emptyset = {}^{\pi}/_{2}$. The scattering matrix has the following form,

$$[S] = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix} \quad 2.14$$

2. An Antisymmetric Coupler: $\theta = 0$, $\emptyset = \pi$. The scattering matrix has the following form,

$$[S] = \begin{bmatrix} 0 & \alpha & \beta & 0 \\ \alpha & 0 & 0 & -\beta \\ \beta & 0 & 0 & \alpha \\ 0 & -\beta & \alpha & 0 \end{bmatrix} \quad 2.15$$

The performance of the directional coupler can be measured using the following parameters [21]:

Coupling Factor (C):

The coupling factor of a directional coupler is the ratio of input power to the coupled power, measured in dB. It indicates the fraction of input power coupled to port three

$$C = 10\,log\frac{P_1}{P_2} = -20\,log\,\beta\ \ dB. \quad 2.16$$

Directivity (D):

The directivity of a directional coupler is the ratio of coupled power to the power at the isolation port, measured in dB. The directivity says how well the coupler manages to isolate backward and forward waves

$$D = 10\,log\frac{P_3}{P_4} = 20\,log\frac{\beta}{|S_{14}|}\ dB. \quad 2.17$$

Isolation (I):

The isolation of the directional coupler is the ratio of input power to the power at the isolation port, measured in dB. It provides the fraction of power delivered to the isolation port

$$I = 10\,log\frac{P_1}{P_4} = -20\,log|S_{14}|\ dB. \quad 2.18$$

Insertion loss (L):

The insertion loss of the directional coupler is the ratio of input power to the power at through port, measured in dB. It accounts for the power delivered to through port due to the influence of power at the coupled and isolated port

$$L = 10\,log\frac{P_1}{P_2} = -20\,log|S_{12}|\ dB. \tag{2.19}$$

The relation between these quantities is given as,

$$I = D + C\ dB \tag{2.20}$$

2.1.1 Branch Line Coupler

The branch line coupler is a quadrature hybrid four-port device. These types of couplers are usually implemented in microstrip lines or strip lines, as shown in Figure 2-3. In a branch line coupler, the power entering port one is ideally evenly divided between port two and port three, with 90° phase shift between these ports, and no power is coupled to the isolation port. The scattering matrix of the branch line coupler has the following form [21]:

$$[S] = \frac{-1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{2.21}$$

The scattering matrix shows that the branch line coupler has a high level of symmetry, as any port can be used as an input port. The even and odd mode analysis can be used for symmetrical networks such as branch-line couplers. This method makes it possible to determine the signals at four ports and how they vary in phase and amplitude, depending on frequency [22].

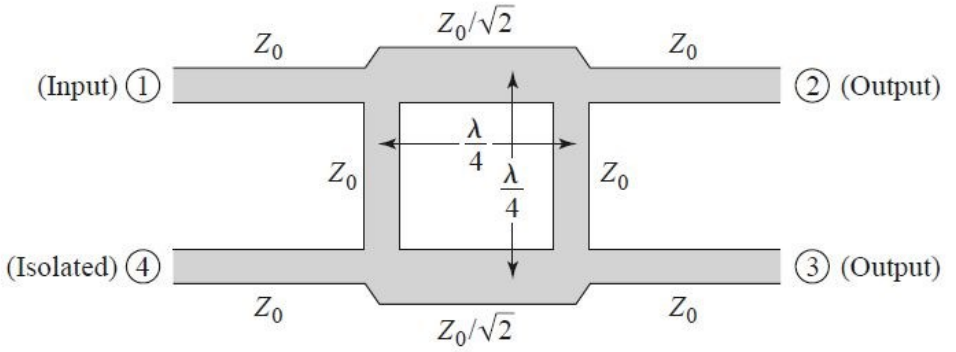

Figure 2-3: The schematic of a branch line coupler *[21]*.

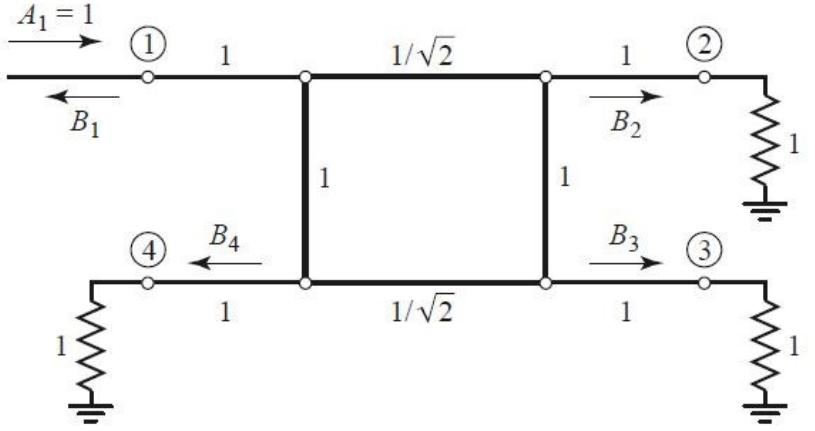

Figure 2-4: Normalized form of branch-line coupler *[21]*.

For even and odd mode, the normalized form of the coupler is considered, as shown in Figure 2-4. In Figure 2-4, each line represents a transmission line with an impedance of Z_0. For this analysis, we believe the signal incident at port one has a unit amplitude. The coupler can be decomposed into even-mode and odd-mode excitation as shown in Figure 2-5. As a result, the four-port network is converted into a set of two decoupled two-port networks [22]. By superimposing the two sets of excitation produces

the original excitation of Figure 2-4.. As the incident signal at port one was considered unity, thus for even and odd mode excitations, the resulting amplitude is $\pm\frac{1}{2}$. The emerging signals at each port of the coupler can be represented as follows [21]:

$$B_1 = \frac{1}{2}\Gamma_e + \frac{1}{2}\Gamma_0 \quad 2.22$$

$$B_2 = \frac{1}{2}T_e + \frac{1}{2}T_0 \quad 2.23$$

$$B_3 = \frac{1}{2}T_e - \frac{1}{2}T_0 \quad 2.24$$

$$B_4 = \frac{1}{2}\Gamma_e - \frac{1}{2}\Gamma_0 \quad 2.25$$

Were $\Gamma_{e,0}$ is the even mode reflection coefficient and $T_{e,0}$ is the odd mode reflection coefficient. The coefficients of even and odd mode excitation are best calculated by multiplying the ABCD matrices of each component in that circuit. The individual ABCD matrices for each component can be found in table 4.1 of [21]. The ABCD parameters can be converted to the S parameter, equal to the reflection and transmission coefficient, considering the ports to be matched.

$$\Gamma = \frac{A + B - C - D}{A + B + C + D} \quad 2.26$$

$$T = \frac{2}{A + B + C + D} \quad 2.27$$

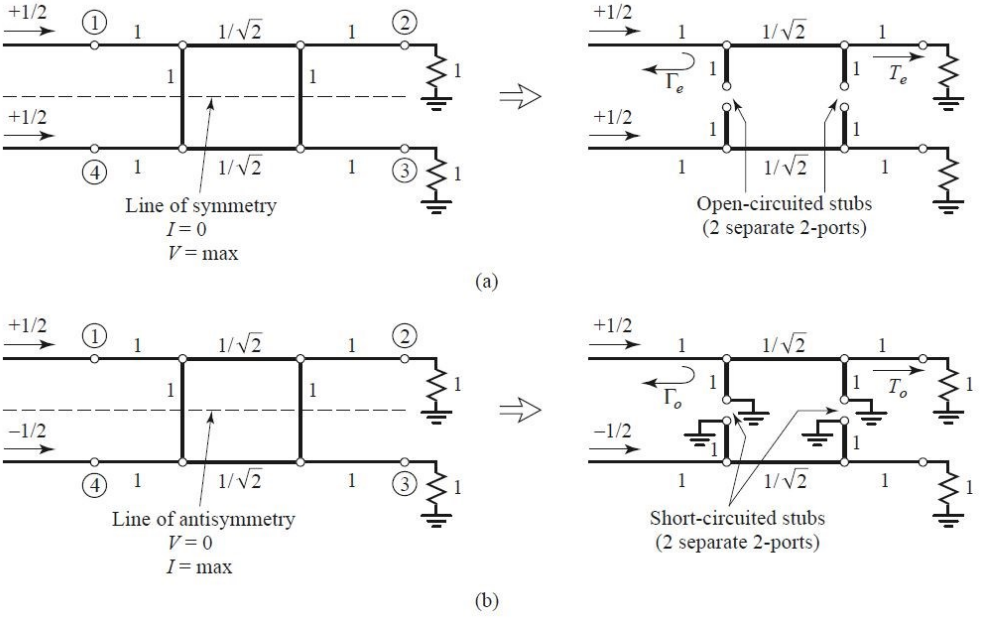

Figure 2-5: Even and odd mode excitation of branch-line coupler.

(a) Even mode (e), (b) Odd mode (o) *[21]*.

ADCD matrix for even mode analysis for Figure 2-5(a) is as follows,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_e = \begin{bmatrix} 1 & 0 \\ j & 1 \end{bmatrix} \begin{bmatrix} 0 & j/\sqrt{2} \\ j/\sqrt{2} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j & 1 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} -1 & j \\ j & -1 \end{bmatrix} \quad 2.28$$

From the equations 2.26, 2.27, and 2.28. The reflection coefficient and transmission coefficient for even mode is given as,

$$\Gamma_e = \frac{A+B-C-D}{A+B+C+D} = \frac{(-1+j-j+1)/\sqrt{2}}{(-1+j+j-1)/\sqrt{2}} = 0 \tag{2.29}$$

$$T_e = \frac{2}{A+B+C+D} = \frac{2}{(-1+j+j-1)/\sqrt{2}} = \frac{-1}{\sqrt{2}}(1+j) \tag{2.30}$$

ADCD matrix for odd mode analysis for Figure 2-5(b) is as follows,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_0 = \begin{bmatrix} 1 & 0 \\ -j & 1 \end{bmatrix} \begin{bmatrix} 0 & j/\sqrt{2} \\ j/\sqrt{2} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -j & 1 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & j \\ j & 1 \end{bmatrix} \tag{2.31}$$

From the equations 2.26, 2.27, and 2.31. Similarly, as above the reflection coefficient and transmission coefficient for odd mode is given as,

$$\Gamma_0 = 0 \tag{2.32}$$

$$T_0 = \frac{1}{\sqrt{2}}(1+j) \tag{2.33}$$

By substituting the obtained reflection and transmission coefficients for even and odd mode analysis in equations 2.22 - 2.25 , the following results is obtained:

$$B_1 = 0 \tag{2.34}$$

$$B_2 = -\frac{j}{\sqrt{2}} \tag{2.35}$$

$$B_3 = -\frac{1}{\sqrt{2}} \quad (2.36)$$

$$B_4 = 0 \quad (2.37)$$

These results show that the port one is matched, and no power is coupled at port four. Half power is delivered to port two and port three with a -90° phase shift from port one to port two and a -180° phase shift from port one to port three [21].

2.1.2 Coupled-Line Coupler

The coupled-line coupler is one of the configurations of the directional coupler. The coupled-line coupler is a four-port network that consists of two unshielded transmission lines placed close to each other, as shown in

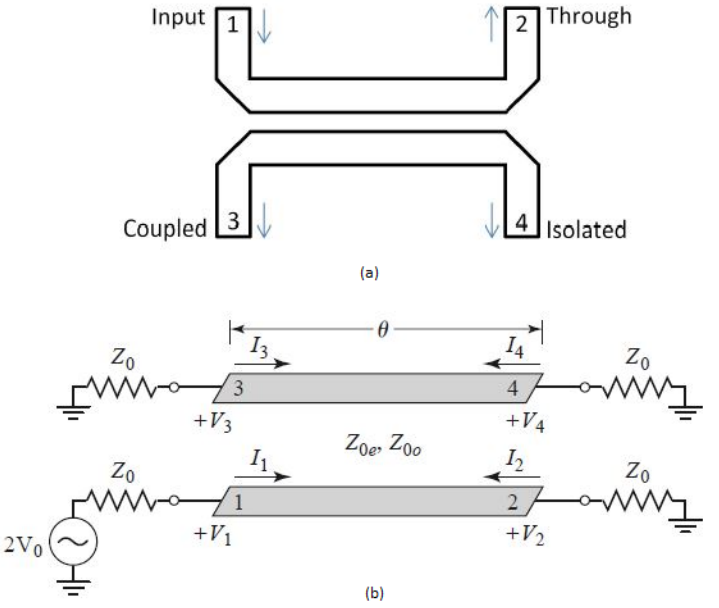

Figure 2-6: Coupled-line coupler. (a) Basic geometry, (b) The schematic.

Figure 2-6. Because of this close proximity, the electromagnetic field of each line interacts with each other, and the power is coupled from one line to the other. Such transmission lines are referred to as coupled transmission lines. Coupled transmission lines support two propagations modes, and this feature can be used to implement directional couplers, hybrids, and filters [23].

There are three ways to couple the transmission lines: broadside coupled, edge coupled, and end coupled. Only the first two are appropriate for quadrature coupler. The various coupled transmission line geometries are shown in Figure 2-7 [21].The coupled-line coupler can achieve better bandwidth than the branch-line coupler, but the electrical length of the coupler also limits it. However, bandwidth can be increased by cascading several sections together with different degrees of coupling between them [24].

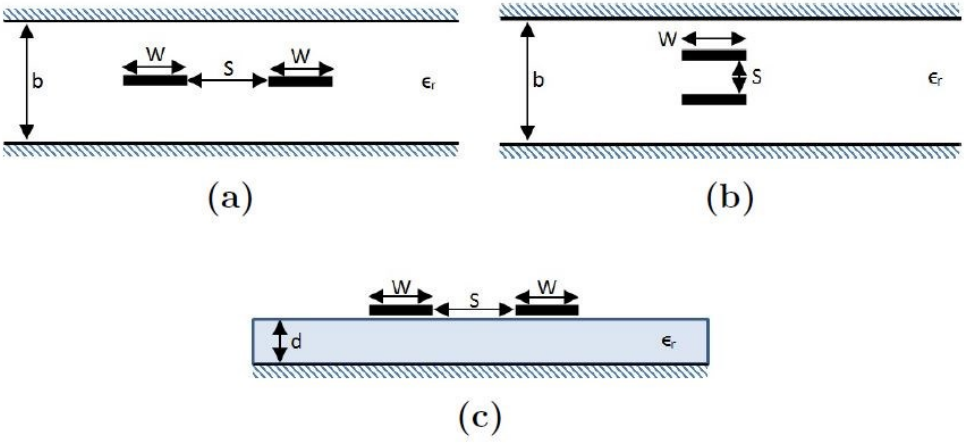

Figure 2-7: Coupled transmission line geometries. (a) Edge coupled strip line, (b) Broadside coupled strip line, (c) Edge coupled microstrip.

There are two modes of current flow in coupled line in an electromagnetic situation. The first one is, current in the strip conductors is equal in amplitude and in the same direction, known as an even mode of excitation. The second one is, current in the strip conductors is equal in amplitude but in the opposite direction, known as the odd mode of excitation.

The even and odd mode characteristics imped can be calculated by using

the equations 2.38 and 2.39, respectively [25]:

$$Z_{0e} = Z_0 \sqrt{\frac{1+C}{1-C}} \quad 2.38$$

$$Z_{0o} = Z_0 \sqrt{\frac{1-C}{1+C}} \quad 2.39$$

Where Z_0 is the characteristic impedance and C < 1 is the voltage coupling coefficient of the coupler.

2.1.3 Lange Coupler

The coupling is too low in the coupled-line coupler to achieve a 3- or 6-dB coupling factor. To solve this problem broadside coupler could be used, but the implementation of a broadside coupler is complex using microstrip technology. These are solutions proposed to solve this problem, and one of them is the Lange Coupler [26]. The basic layout of the Lange coupler is shown in Figure 2-8.

Using several lines parallel to each other, one can use the fringing field at both edges for the coupling instead of just one like in the standard couple-line coupler. With this design, the coupler can easily achieve a 3 dB coupling ratio with a wide bandwidth. This design compensates for different even and odd mode phase velocities, which in turn improves bandwidth. There is a 90-degree phase difference between output lines in the Lange coupler, so the Lange coupler is a type of quadrature hybrid.

The main disadvantage of the Lange coupler is its interdigitated geometry. As the lines in the coupler design are very narrow and close together, thus bounding wire across the lines is required, which increases the design's complexity and makes it challenging to fabricate. However, this circuit is

used for filter circuits and applications which require a high coupling ratio [21].

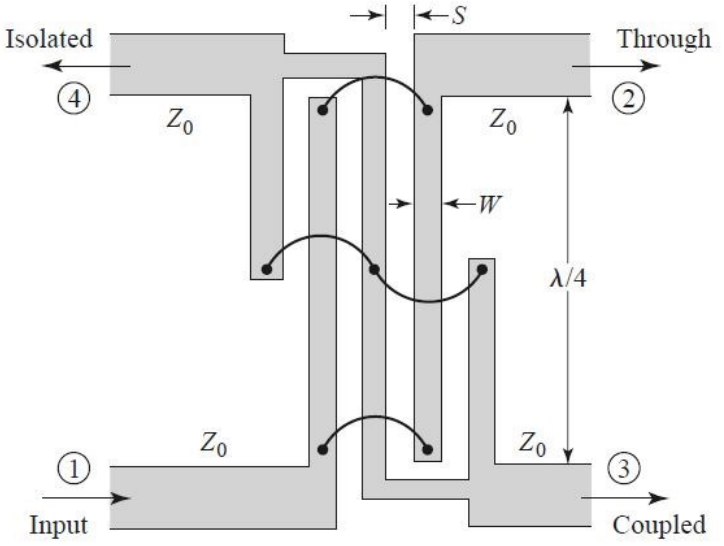

Figure 2-8: The basic layout of the Lange coupler *[21]*.

2.1.4 Lumped Element Quadrature Hybrids

The previously described directional couplers have a wide range of RF and microwave applications. However, these circuits become unacceptably large at low frequencies. It is desirable to use lumped element design for frequencies around a very high frequency (VHF) down to an even radio frequency range. Am equivalent lumped element implementation of directional coupler is compact and has the potential to be cost-effective [27]. However, the lumped element couplers exhibit a restricted bandwidth. Its performance parameters such as isolation, insertion loss, and phase balance all degrade on either side of its centre frequency. This design is developed by implementing the transmission lines with their equivalent lumped elements [28]. To be precise, each transmission lines component will be represented as an equivalent Pi or T network, as shown in Figure 2-9, by equating the ABCD matrix for transmission line segment to the ABCD matrix elements for the lumped network at the design

frequency. The matrix operations for the lossless transmission line with characteristic impedance Z_o and length L are shown below [29].

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos \beta L & jZ_o \sin \beta L \\ jY_o \sin \beta L & \cos \beta L \end{bmatrix} \quad 2.40$$

For $\beta L = 90°$,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & jZ_o \\ jY_o & 0 \end{bmatrix} \quad 2.41$$

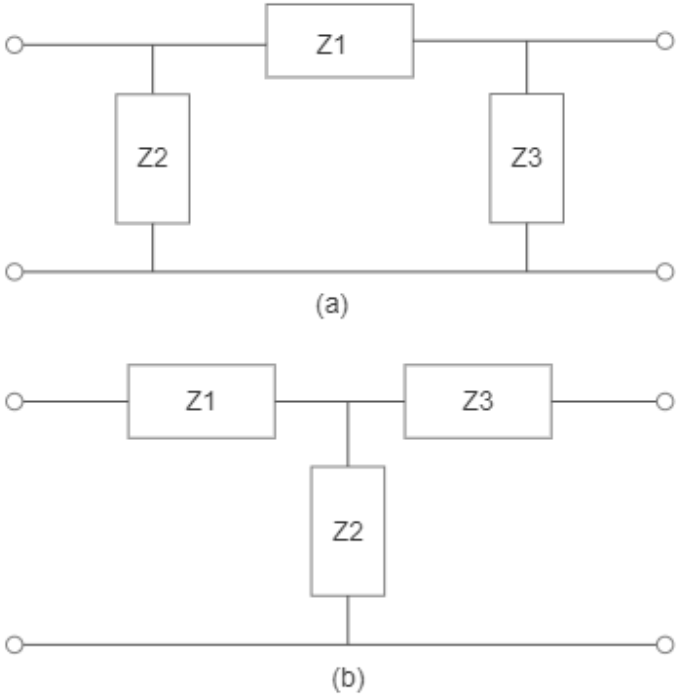

Figure 2-9: Pi and T network configuration.

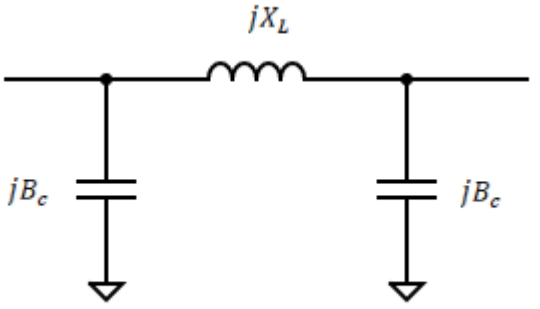

Figure 2-10: Lumped equivalent circuit for the Pi network.

The transmission line can be represented as a low-pass Pi network as shown in Figure 2-10, where the shunt admittance and series element impedance are given as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jB_c & 1 \end{bmatrix} \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jB_c & 1 \end{bmatrix} \quad 2.42$$

$$= \begin{bmatrix} 1 - X_L B_c & jX_L \\ jB_c(2 - X_L B_c) & 1 - X_L B_c \end{bmatrix} \quad 2.43$$

By equating the matrix elements of the transmission line segment to the matrix element of the Pi networks yield the following results:

$$X_L B_c = 1 \; and \; X_L = Z_o \quad 2.44$$

Therefore, $B_c = Y_o$.

The transmission line can be represented as a high-pass T network as shown in Figure 2-11, where the shunt admittance and series element impedance are given as,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & -jX_c \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -jB_L & 1 \end{bmatrix} \begin{bmatrix} 1 & -jX_c \\ 0 & 1 \end{bmatrix} \quad 2.45$$

$$= \begin{bmatrix} 1 - B_L X_c & -jX_c(2 - B_L X_c) \\ -jB_L & 1 - B_L X_c \end{bmatrix} \quad 2.46$$

By equating the matrix elements of the transmission line segment to the matrix element of the T networks yield the following results:

$$B_L X = 1 \; and \; B_L = Y_o \quad 2.47$$

Therefore, $X_c = Y_o$.

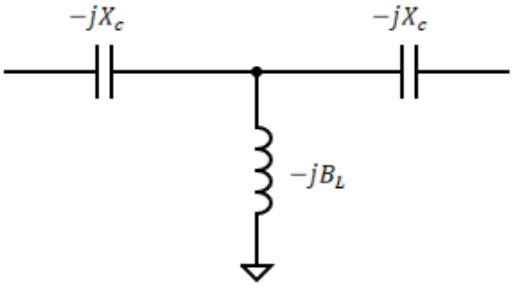

Figure 2-11: Lumped equivalent circuit for the T network.

A low-pass Pi network is preferred over a low-pass T network since fewer inductors are in a low-pass Pi network. The high-pass T network provides better matching of the ABC matrix, and therefore it has fewer inductors than the high-pass Pi network [29].

There are four conventional lumped element topologies of the quadrature hybrid: Type LLC, Type CCL, Type LCC, and Type CCL, and their schematic is shown in Figure 2-12 [30].

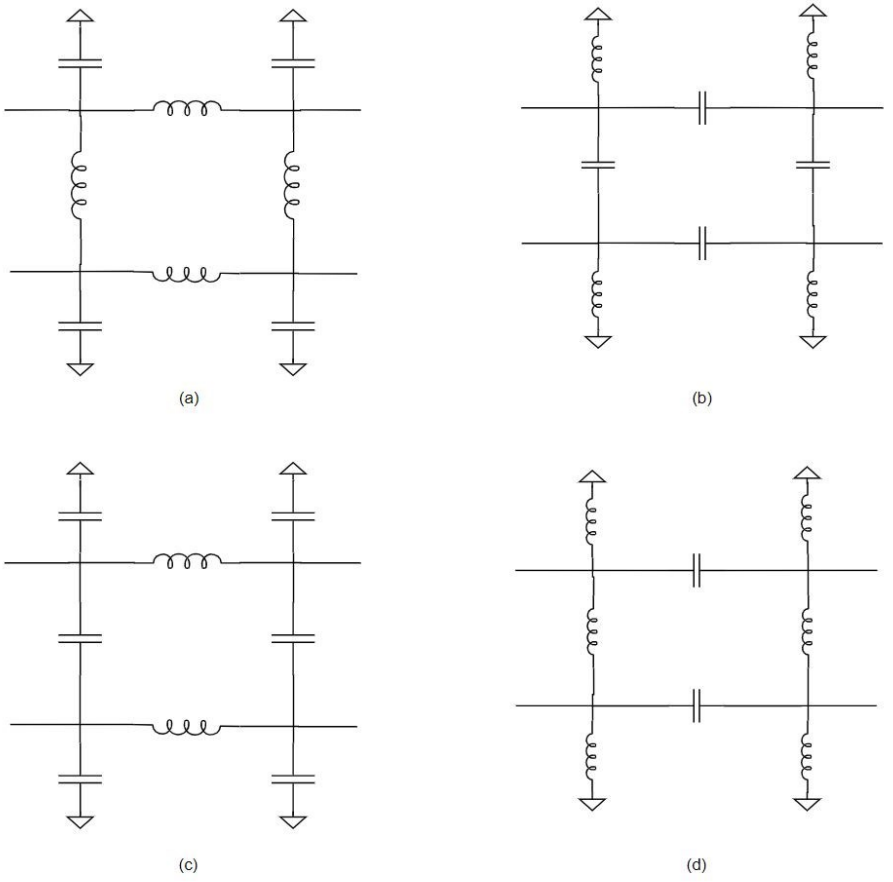

Figure 2-12: Different lumped element topologies of quadrature coupler. (a) LLC type, (b) CCL type, (c) LCC type, (d) CLL type.

2.2 Spiral Inductor

The monolithic on-chip inductors are known as spiral inductors due to the way in which these inductors are laid out. There are three types of on-chip inductors. The circular-shaped inductors are more efficient and can yield better performance, but the availability of the fabrication process often limits the inductor's shape. However, the most used are the planar spiral inductor and square-shaped spiral inductors [31]. Due to very low Q

values, the on-chip inductors are among the most challenging components to design. Inductors have parasitic components and resistances and inductance and are less resistive to DC and highly resistive to AC. The quality of the spiral inductors is described by their Q-factor, effective inductance, and Self Resonating Frequency (SRF) [13].

2.2.1 Planar Spiral Inductor

The typical geometry of a planar spiral inductor is shown in the Figure 2-13 and the lumped equivalent circuit is shown in Figure 2-14. Where L is the inductance, R_s represents the series resistance, C_s accounts for capacitance due to the overlap of spiral and centre-tap, C_{ox} is the capacitance between the spiral and the substrate, C_b and R_b is the capacitance and resistance of the substrate, respectively. The modern CMOS technology consists of multiple metal layers, but only the top layer is used to construct the planar spiral inductors. The main drawback of a planar spiral inductor is its low inductance [13].

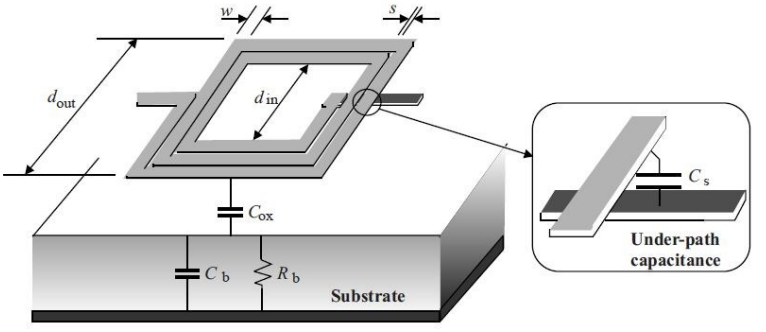

Figure 2-13: Square shaped planar spiral inductor *[13]*.

2.2.2 Stacked Spiral Inductor

One way to increase the inductance of a spiral inductor is by using a stacked configuration, as shown in Figure 2-15. However, this method increases the

spiral-substrate capacitance because the lower metals are used to construct stacked spiral inductors. The inductance of stacked spiral inductor with two spiral layers is,

$$L_{total} = L_1 + L_2 + 2M$$

Where L_1 and L_2 are the self-inductance of spirals one and two and M is the mutual inductance. The inductance of stacked spiral inductors increases linearly with the number of spiral layers in the inductor construction [13].

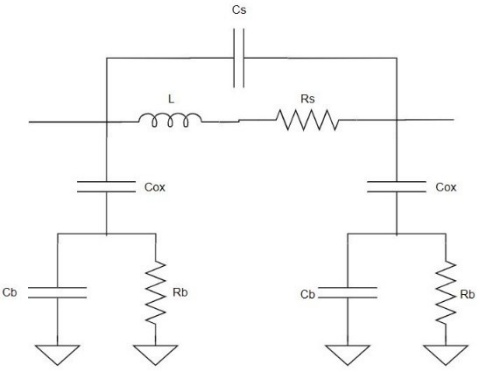

Figure 2-14: Equivalent lumped model of planar spiral inductor.

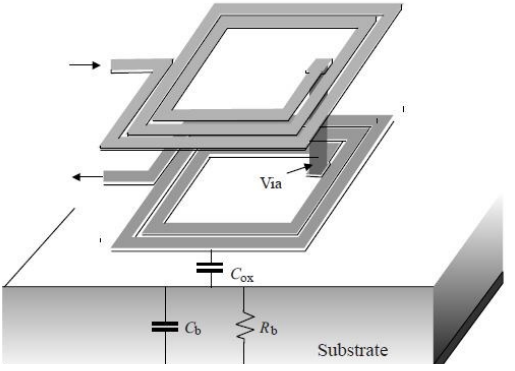

Figure 2-15: Square shaped stacked spiral inductor *[13]*.

2.2.3 Disadvantages of spiral inductors

Low-quality factor: The ohmic loss of the spiral gradually increases with temperature which limits the quality factor of the spiral inductors. The two sources that contribute to the ohmic losses in the spiral inductors are the skin-effect induced resistance of the spiral and the resistance induced by the eddy currents in the substrate.

Low self-resonant frequency: The resonance of the LC tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spirals and the substrate, and the underpass capacitance constitutes the self-resonance of the spiral inductor. The low self-resonant frequency of the spiral inductor is mainly due to the large metal are occupied by the spirals.

Low and fixed inductance: The inductance of the spiral inductor is fixed once the area of the spiral is set and the equivalent inductance is low. The only way to increase the inductance of the spiral inductor is to either increase the number of turns which in turn increases the area of metal or use a stacked configuration topology. The increase in the turns of the spirals increases the area, and the stacked configuration increases the spiral-substrate capacitance.

Large silicon area: The spiral inductors have low inductance. The fact that inductance of the spiral inductors is directly proportional to the number of turns of the spiral of the inductor. Thus, the silicon area required for routing the spiral inductors is large.

2.3 Active Inductor

The active inductors are used to design tuneable and compact radio frequency integrated circuits. CMOS active inductors are active networks that consist mainly of MOS transistors. The active inductors are designed for required operating frequency bands. There are two approaches to implement the active inductors.

1. Operational amplifier-based approach
2. Gyrator-C based approach.

A passive inductor can be replaced by a circuit consisting of a capacitor, operational amplifiers (op-amps) or transistors, and resistors. Figure 2-16 shows the simulated inductor circuit with op-amps. For the op-amp-based

approach, the inductance is a function of operating frequency, and the value of inductance decreases with an increase in frequency. It is used for moderate frequency applications (up to about 100MHz). Also, op-amp-based active inductors suffer from large chip area and nonlinearity [32]. The following section will describe the principles of the gyrator-C-based active inductor.

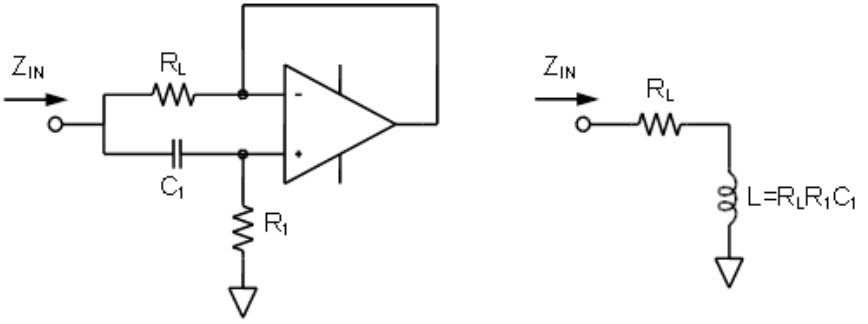

Figure 2-16: Operational amplifier-based active inductor [40].

2.3.1 Lossless single-ended/grounded Gyrator-C Active Inductor

The gyrator-C consists of two transconductors, one positive and negative connected back-to-back with one end connected to the capacitor. This network is lossless when both the input and output impedances of the transconductors are infinite, and the transconductances of the transconductors are constant. The schematic of a lossless grounded gyrator-C active inductor is shown in Figure 2-17.

For the network shown in Figure 2-17, the admittance into port 2 is calculated as:

$$Y = \frac{I_{in}}{V_2} = \frac{1}{s\left(\frac{C}{G_{m1}\,G_{m2}}\right)} \qquad 2.48$$

The equation 2.48 indicates that port 2 of the network behaves as a grounded lossless inductor with its inductance given as,

$$L = \frac{C}{G_{m1}\, G_{m2}} \qquad 2.49$$

Thus, the gyrator-C can be used to synthesize inductors. These inductors are known as gyrator-C active inductors. The equation 2.49 conveys that the inductance is directly proportional to the load capacitance C and inversely proportional to the product of the transconductances of the trans conductors of the gyrators. This topology makes the network inductive over the entire frequency spectrum. Figure 2-18 shows various schematics of the trans conductors widely used in the configuration of the gyrator-C active inductor, such as common-gate, common-drain, differential-pain, and the common source trans conductors [13].

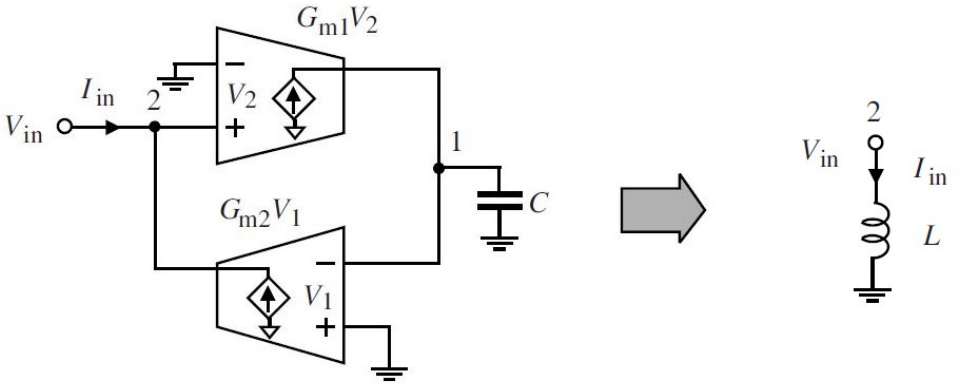

Figure 2-17: Schematic of a lossless grounded gyrator-C active inductor *[13]*.

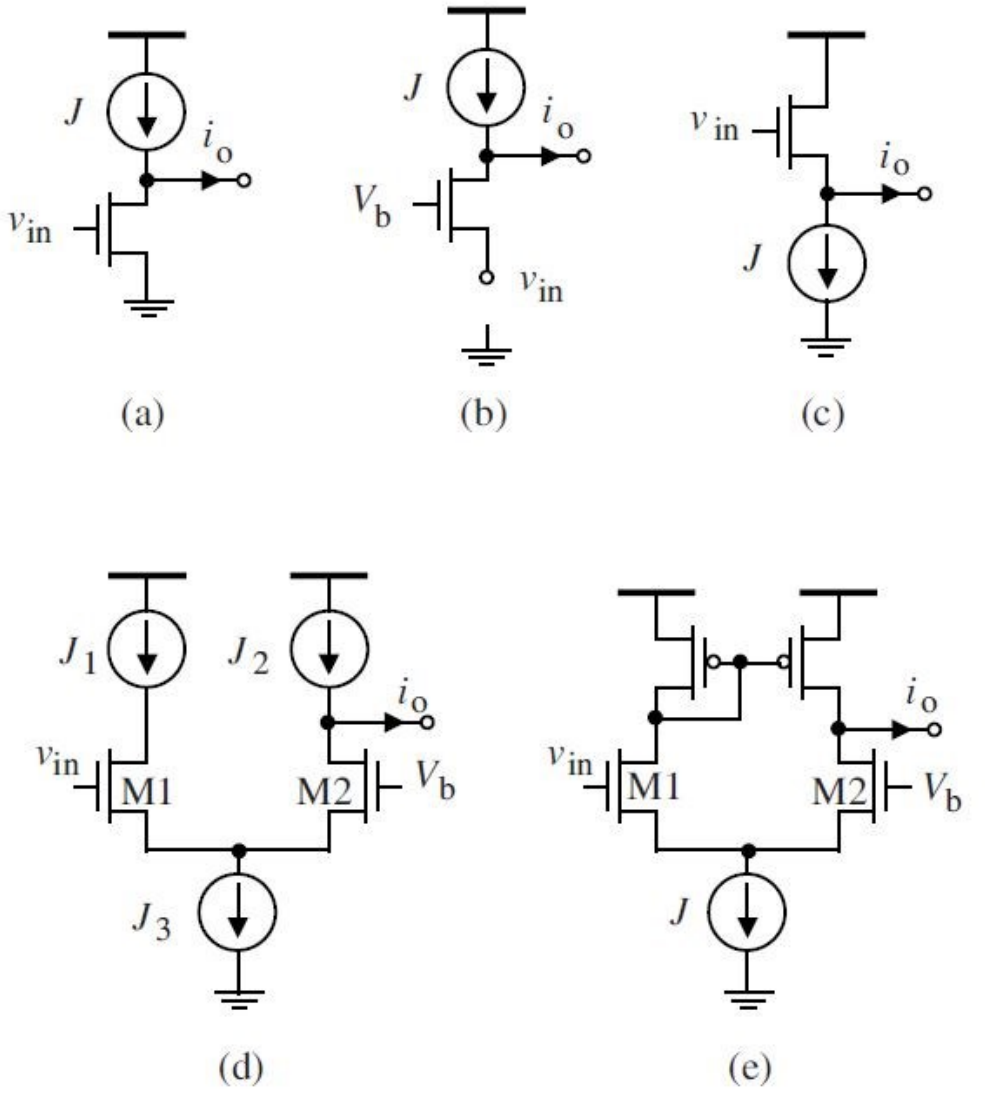

Figure 2-18: Schematics of trans-conductors used in gyrator-C active inductors. (a) Common-source trans-conductor, (b) Common-gate trans-conductor, (c) Common-drain trans-conductor, (d, e) Differential-pair trans-conductors *[13]*.

2.3.2 Lossless Floating Gyrator-C Active Inductor

An active inductor is floating if both ports one and two are not connected to the ground or power supply of the network or circuit containing it. The floating gyrator-C active inductor is constructed by differentially configured trans-conductors, as shown in Figure 2-19 [13].

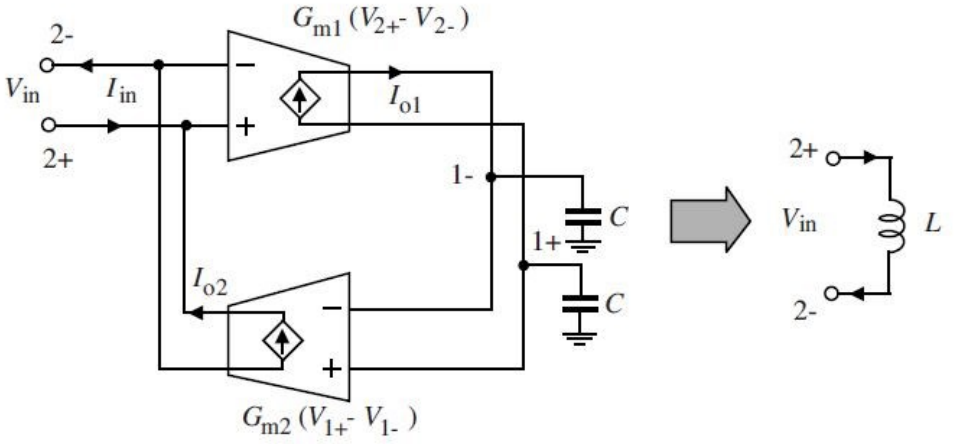

Figure 2-19: Schematic of lossless floating gyrator-C active inductor *[13]*.

From Figure 2-19 we have,

$$V_{in1}^{+} = -\frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \quad 2.50$$

$$V_{in1}^{-} = \frac{g_{m1}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \quad 2.51$$

$$I_{02} = g_{m2}\,(V_{in1}^{+} - V_{in1}^{-}) \quad 2.52$$

Equating equation 2.50, 2.51, and 2.52, we have

$$I_{02} = -\frac{2g_{m1}g_{m2}}{sC}(V_{in2}^{+} - V_{in2}^{-}) \quad 2.53$$

Thus, the admittance into port two is given by,

$$Y = \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}} = \frac{1}{s\left(\frac{2C}{g_{m1}g_{m2}}\right)} \quad 2.54$$

Thus, the equation 2.54 shows that the gyrator-C active inductor in Figure 2-19 behaves as a floating inductor and its inductance is given by,

$$L = \frac{2C}{g_{m1}g_{m2}} \quad 2.55$$

The floating gyrator-C active inductor (AI) has some advantages over the single-ended/grounded gyrator-C active inductor [13]:

1. The differential configuration of flotation gyrator-C AI rejects the common-mode disturbances in the network, making it suitable for both analog and digital circuit applications.
2. The level of voltage swing of floating gyrator-C AI is twice that of single-end AI.

2.3.3 Lossy single-ended/grounded Gyrator-C Active Inductor

The grounded gyrator-C AI is no longer lossless when either the input or the output impedances of the trans-conductors are finite. In practice, the AI does not have inductive behaviour in all frequency spectrums due to their parasitic components in input/output nodes. Figure 2-20 shows lossy grounded gyrator-C AI, where G_{o1} and C_1 and G_{o2} and C_2 are the parasitic conductance and capacitance at nodes one and two, respectively.

Assuming the transconductance as constant, the admittance into port two is given as,

$$Y = \frac{I_{in}}{V_2} = sC_2 + G_{o2} + \frac{1}{s\left(\frac{C_1}{G_{m1}G_{m2}}\right) + \frac{G_{o1}}{G_{m1}G_{m2}}} \quad 2.56$$

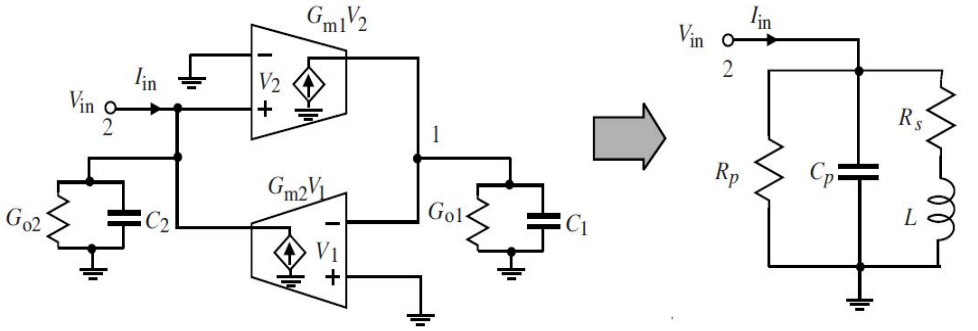

Figure 2-20: Schematic of lossy single-ended/grounded gyrator-C active inductor [13].

From the equation 2.56 the active inductor can be represented as RCL network as shown in Figure 2-20, and its parameters are given by,

$$R_p = \frac{1}{G_{02}} \quad 2.57$$

$$C_p = C_2 \quad 2.58$$

$$R_s = \frac{G_{o1}}{G_{m1}G_{m2}} \quad 2.59$$

$$L = \frac{C_1}{G_{m1}G_{m2}} \quad 2.60$$

The gyrator-c network behaves as a lossy inductor with parasitic parallel resistance R_p, parallel capacitance C_p, and series resistance R_s. The parallel resistance R_p should be maximized, and series resistance R_s should be minimized to have low ohmic losses in the AI. However, the finite input and output impedances of the trans-conductors do not affect the inductance of the AI and result in a limited quality factor. For applications such as band-pass filters, AI should have a large quality factor. For these applications, quality factor enhancement techniques can be used to boost the quality factor. The resonant frequency of the RCL network is given by,

$$\omega_o = \frac{1}{LC_p} = \sqrt{\frac{G_{m1}}{C_1}\frac{G_{m2}}{C_2}} \tag{2.61}$$

w_o is the self-resonant frequency of the active inductor and it defines the maximum frequency at which the active inductor operates [13].

2.3.4 Lossy Floating Gyrator-C Active Inductor

Lossy floating gyrator-C active inductors are analysed similarly to lossy grounded gyrator-C active inductors in section 3.3.3. Figure 2-21 shows the schematic of the lossy floating gyrator-C active inductor and its passive equivalent model. The admittance into port two of the AI is given as [13]:

$$Y = \frac{I_{in}}{V_2^+ - V_2^-} = s\frac{C_2}{2} + \frac{G_{o2}}{2} + \frac{1}{s\left(\frac{C_1}{2G_{m1}G_{m2}}\right) + \frac{G_{o1}}{2G_{m1}G_{m2}}} \tag{2.62}$$

From the equation 2.62 the active inductor can be represented as RCL network as shown in Figure 2-21, and its parameters are given by,

$$R_p = \frac{2}{G_{02}} \tag{2.63}$$

$$C_p = \frac{C_2}{2} \tag{2.64}$$

$$R_s = \frac{G_{o1}/_2}{G_{m1}G_{m2}} \tag{2.65}$$

$$L = \frac{C_1/_2}{G_{m1}G_{m2}} \tag{2.66}$$

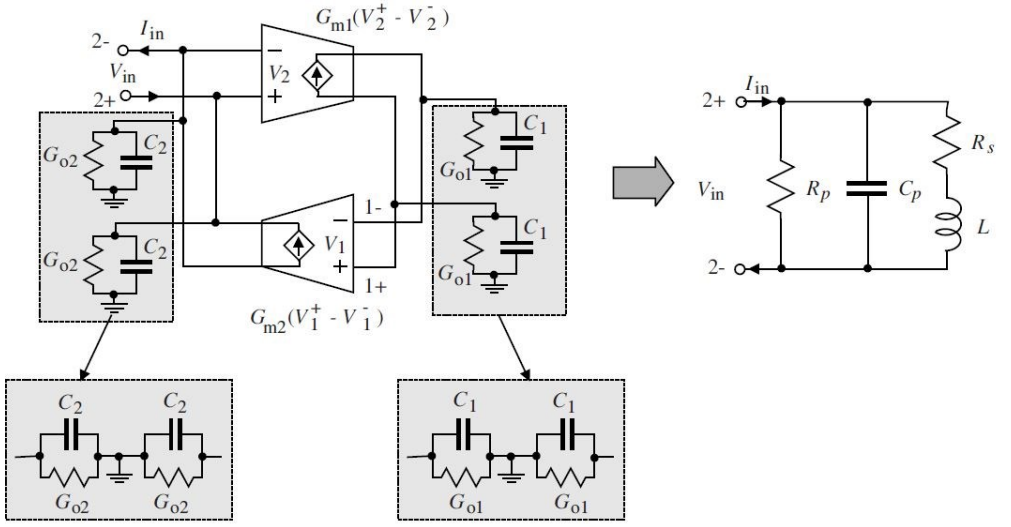

Figure 2-21: Schematic of lossy floating gyrator-C active inductor [13].

2.4 Properties of an Active Inductor

The properties that describe the performance of an active inductor are discussed in this section, such as frequency range, inductive tunability, quality factor, noise, stability, and power consumption [13].

2.4.1 Frequency Range

The lossy gyrator-C active inductor exhibits inductive characteristics only over a specific frequency range, and this frequency range can be obtained from the RLC equivalent circuit.

$$Z = \left(\frac{R_s}{C_p L}\right) \frac{s\frac{L}{R_s} + 1}{s^2 + s\left(\frac{1}{R_p C_p} + \frac{R_s}{L}\right) + \frac{R_p + R_s}{R_p C_p L}} \tag{2.67}$$

When complex conjugate poles are encountered, the pole resonant frequency of Z is given by,

$$\omega_p = \sqrt{\frac{R_p + R_s}{R_p C_p L}} \tag{2.68}$$

Since $R_p \gg R_s$, the equation 2.68 is simplified to,

$$\omega_p = \sqrt{\frac{1}{L C_p}} = \omega_o \tag{2.69}$$

Where w_o is the self-resonant frequency of the active inductor and the Z has a zero at frequency,

$$\omega_z = \frac{R_s}{L} = \frac{G_{o1}}{C_1} \tag{2.70}$$

The Bode plot sketch of Z is shown in Figure 2-22. It is evident that the gyrator-C network is resistive when $\omega < \omega_z$, inductive when $\omega_z < \omega < \omega_o$, and capacitive when $\omega > \omega_o$. The frequency range in which the AI is inductive is lower-bounded by ω_z and upper-bounded by ω_o. The parallel resistance R_p does not affect the frequency range of the inductor. However, the series resistance R_s affects the lower bound of the frequency range. A maximum frequency range can be achieved by minimizing both R_s and C_p in an active inductor of a given L.

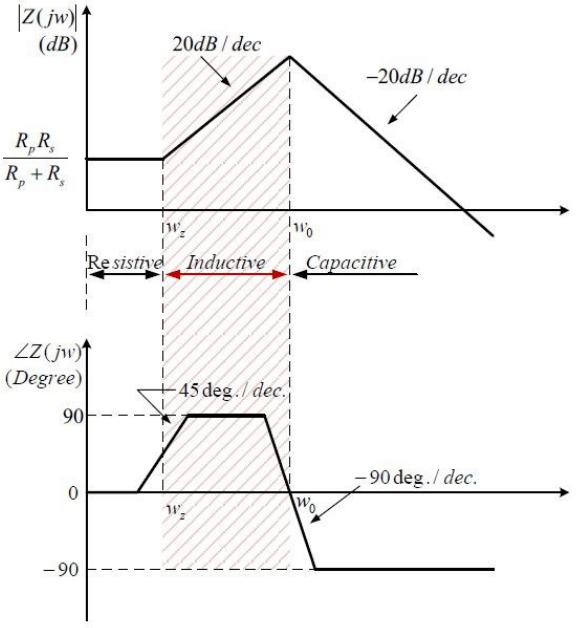

Figure 2-22: Impedance bode plot of lossy gyrator-C active inductor.

2.4.2 Inductance Tunability

A tuneable inductor with a large inductance tuning range is essential in various applications such as filters, voltage, current-controlled oscillators, and phase-locked loops. Figure 2-23 shows a tuneable active inductor where the inductance of the active inductor is tuned either by changing the

load of the capacitance or by varying the transconductances of the trans-conductors of the active inductors.

The capacitance tuning in standard CMOS technologies is usually done by using varactors. There are two types of varactors, namely pn-junction varactors and MOS transistors.

Conductance tuning is carried out by varying the dc operating point of the trans-conductors. This technique offers a large conductance tuning range, subsequently a large inductance tuning range. Conductance tuning can be used for the coarse tuning of the inductance, while capacitance tuning can be used for fine-tuning the inductance of the active inductors.

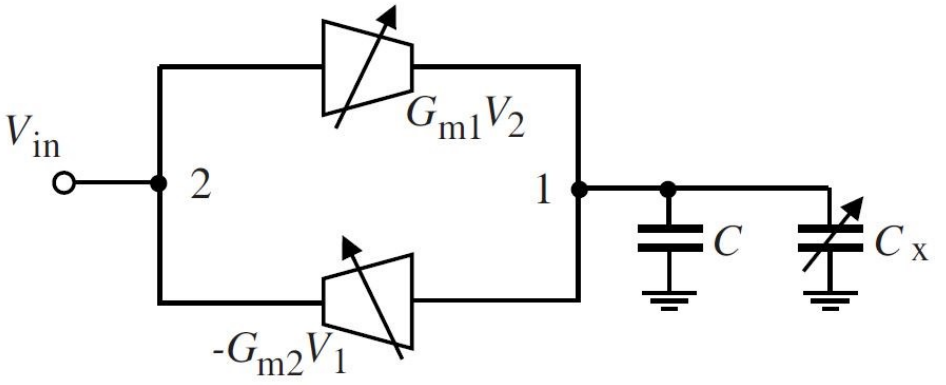

Figure 2-23: Tuneable active inductor *[13]*.

2.4.3 Quality Factor

High quality factor is the most prominent feature of active inductors in contrast with spiral inductors. The quality factor of spiral inductors is independent of the voltage/current of the inductance, and the quality factor of an active inductor is dependent on the voltage/current of the inductance. The quality factor Q of an active inductor quantifies the ratio of the net magnetic energy stored in the inductors to its ohmic loss in one oscillation cycle. Equation 2.71 represents a convenient way to quantify the quality factor of linear inductors, including active inductors.

$$Q = \frac{Im[Z]}{Re[Z]} \tag{2.71}$$

Active inductors are linear when the swing of the voltages/currents of inductors are small, and all transistors of the active inductors are appropriately biased. The quality factor of a lossy gyrator-C active inductor is given as,

$$Q = \left(\frac{\omega L}{R_s}\right) \frac{R_p}{R_p + R_s\left[1 + \left(\frac{\omega L}{R_s}\right)^2\right]} \left[1 - \frac{R_s^2 C_p}{L} - \omega^2 L C_p\right] \tag{2.72}$$

It is clear from the equation 2.72 that the quality factor is dependent on R_s and R_p and it is seen that the first term $\left(\frac{\omega L}{R_s}\right)$ is a dominant part of quality factor in the active inductor. Thus, R_s must be considered when boosting the quality factor. Several approaches that can be considered to reduce the series resistance of active inductor are:

1. Advanced circuit techniques such as cascoding can be used to lower the conductance at node one in Figure 2-21 and Figure 2-23.
2. By increasing the transconductance of trans-conductors.
3. Using negative resistance circuits.

2.4.4 Noise

The main drawback of an active inductor compared with spiral inductors is the high level of noise. As an active inductor is made up of active components, it suffers from internal noise. The prominent noises can be listed as thermal noise, flicker noise, and noise due to the distributed substrate used in transistors. To analyse the noise of a gyrator-C active inductor, the power of the input-referred noise-voltage and noise-current of the trans-conductors should be considered. Through the equivalent noise model of the active inductor circuit, we can analyse it.

2.4.5 Linearity

In an ideal gyrator-C active inductor, all the transistors of the circuit must be in saturation region over the entire tuning range of the inductor. But in lossy gyrator-C active inductors, few transistors switch from saturation to triode region. The transconductance of the trans-conductors that constituting the inductors varies from saturation to triode region. As a result, the inductance value also changes, which adds nonlinearity in the active inductor working. Active inductor linearity can be characterized in two different ways, total harmonic distortion (THD) and 1 dB inductance compression L_{-1dB}. The total harmonic distortion exhibits total unwanted harmonic current to fundamental current when a fundamental ac input signal has been injected into the active inductor. The increase in input current amplitude by 1 dB than its small-signal value gives L_{-1dB}.

2.4.6 Power Consumption

The gyrator-C active inductors consume dc power, mainly due to the dc biasing currents of their trans-conductors. The power consumption by gyrator-C active inductors is usually not a critical concern as the inductance of the active inductors is inversely proportional to the transconductances of the trans-conductors constituting the inductors. Usually, Gm1 and Gm2 are made small to have large inductance. This is typically achieved by lowering the dc biasing currents of the trans-conductors. The replica-biasing network used for reducing the effect of supply voltage fluctuation increases the power consumption of the active inductor. Furthermore, the power consumption is increased when negative resistors are added to the active inductor circuit to boost the quality factor. Often the power consumption by the active inductor is set by that of its replica-biasing and negative resistor networks.

2.5 Load Modulated Balanced Amplifier

The load modulated balanced amplifier (LMBA) is a quadrature-balanced amplifier with a control signal injected into the isolation port of the output combiner. The two transistors can be presented with any load by

controlling the phase and magnitude of the injected signal. This signal eliminates or reduces the need for an output matching network by providing active matching and dynamic load modulation (DLM). As a result, efficiency over a wide output power range is achieved [1].

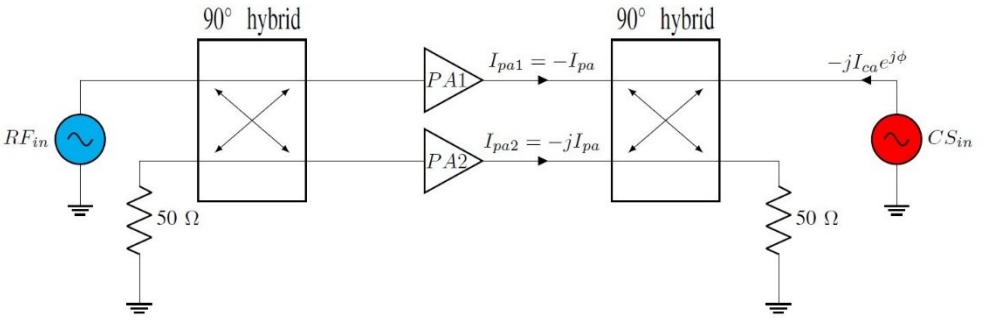

Figure 2-24: Schematic representation of LMBA *[1]*.

The schematic representation of LMBA architecture is shown in Figure 2-24. the control signal CS_{in} used to modulate the load is injected at the isolation port of the output coupler. The modulation is the same for both the amplifiers, which have the same architecture and are biased in the same PA class [1]. The impedance is modulated according to the equation 2.73,

$$Z_{PA1} = Z_{PA2} = Z_0\left(1 - \sqrt{\frac{I_{cs}e^{j\emptyset}}{I_{ba}}}\right) \qquad 2.73$$

Here Z_0 is the impedance of the coupler, $I_{cs}e^{j\emptyset}$ is the amplitude and phase of the control signal, and I_{ba} is the current of power amplifier.

In LMBA, using the load modulation capabilities, a new variant [33] was proposed, which emulates the Doherty amplifier. Figure 2-25 shows a schematic representation of Doherty-like LMBA where a power divider is used to split the input signal into two paths instead of using a separate source for load modulation. A balanced amplifier biased in Class AB or B is

connected to one of the output ports of the power divider. The other output port is connected to the control amplifier (CA), which is usually biased in class C. A variable phase shifter is used to modulate the complex impedance presented to the main amplifier [1].

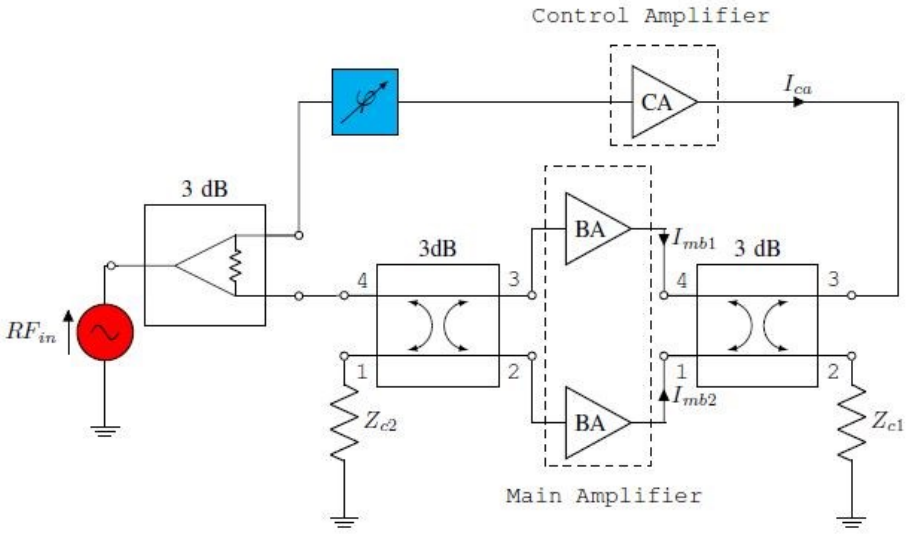

Figure 2-25: Schematic of Doherty-like LMBA *[1]*.

3
Methodology

The main objective of the thesis was to design and implement a hybrid coupler using an active inductor, which could be used for LMBA input matching. The coupler is designed for an operating frequency of 2GHz. In this thesis, TSMC 0.18nm process is used for the implementation of the design. For circuit designing and simulation Cadence Virtuoso, and Keysight Advanced Design Systems tools are used.
This project consists of three parts—the first part consists of designing the active inductor and testing the active inductor for large-signal performance. The second part is developing a hybrid coupler using an active inductor, and the last part is testing the performance of LMBA using the hybrid coupler.

3.1 Active Inductor Design

To minimize on-chip area, lumped couplers are used instead of transmission line couplers. An inductor is one of the main components of a lumped coupler [34] [35]. Small chip area and tunability can be achieved using an active inductor [14]. A single-ended active inductor has been realized in this work using Gyrator C topology, which converts intrinsic capacitance to inductive behaviour [13]. The Gyrator C topology exhibits several disadvantages, such as low-inductance value and narrow frequency range for high Q value [36]. Cascode grounded topology was introduced to overcome these limitations [37]. Three models of an active inductor were realized and studied in this work.

3.1.1 Circuit Design Description.

In this section, the working principle of an active inductor in Figure 3-1 will been discussed. The active inductor is based on the theory of Gyrator-C, with two back-to-back connected transconductance. Additional elements are added along the feedback path to increase the performance and tunability of the active inductor. Figure 3-1 shows the circuit diagram of the active inductor with the transistor current source.

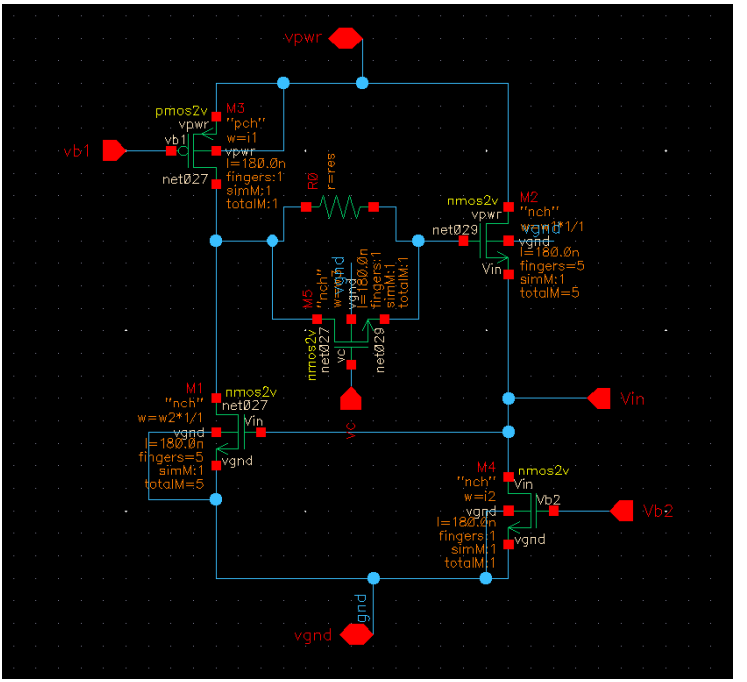

Figure 3-1:Schematic of an active inductor with transistor current source.

In Figure 3-1 the transistors M1 and M2 form the gyrator. The transistors M1 and M2 are normal thin oxide nmos 1.8 V transistors with a total W/L ratio of 50 µm/0.18 µm with 5 gate fingers. Multiple fingers were used to reduce the gate resistance. While the transistors M3 and M4 are used as current source, which are normal thin oxide nmos 1.8 V transistors with

total W/L ratio of 20 µm/0.18 µm and 25 µm/0.18 µm. The V_{b1} and V_{b2} are the biasing voltages (V_{b1} = 0.98 V and V_{b2} = 0.72 V) used to set the current condition for transistors M3 and M4. Figure 3-2 shows the active inductor equivalent circuit. To improve the tenability and enhance inductance and the quality of an active inductor resistor R0 (1.1kΩ) and transistor M5 (22.5 µm/0.18 µm) has been used along the feedback which together forms a tuneable resistor R_f [38]. The feedback resistor reduces the equivalent resistance and increases the equivalent inductance, thus enhancing the active inductor's quality factor. Considering R_t and g_t as the net resistance and conductance of the composite of the resistor R0 and transistor M5. The effective conductance of the composite of the R0 and M5 is increased by tuning V_c. Fine tuning of the active inductor can be achieved by varying the biasing voltage V_c of the transistor M5 along the feedback.

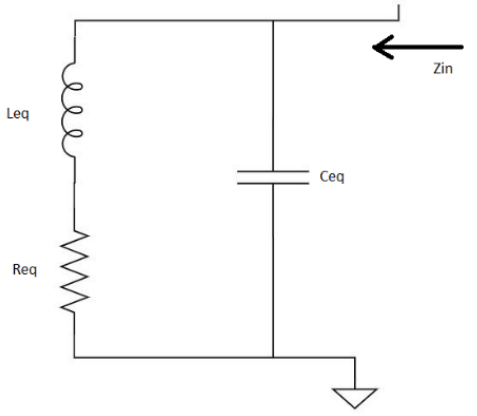

Figure 3-2: Active inductor equivalent circuit.

The impedance for Figure 3-2 can be written as

$$Z_{in} = \frac{sL_{eq} + R_{eq}}{s^2 C_{eq} L_{eq} + sC_{eq} R_{eq} + 1} \qquad 3.1$$

However, the self-resonating frequency and the frequency of operation of

the active inductor at which the quality factor is maximum, is decided by choice of the resistance R_f. The equivalent inductance L_{eq}, quality factor, and the operation frequency is be tuned independently of each other. The small-signal circuit of the schematic given in Figure 3-1 is shown in Figure 3-1. The transconductance and gate-source capacitance of the transistor M1 and M2 are given by g_{m1}, g_{m2}, C_{gs1}, and C_{gs2}, respectively. Whereas g_{dp} and g_{nd} are the drain conductance of transistors M3 and M4, and R_v and g_v are the resistance and conductance of the R0 resistor and M5 transistor. The equivalent resistance and inductance is given by,

$$R_{eq} = g_{dp}/(g_{m2}g_{m1} + g_{m2dn}g_{dp}) \qquad 3.2$$

$$L_{eq} = g_{vdp}C_{gs2}/(g_{m2}g_v g_{m1} + g_{m2nd}g_{dp}g_v) \qquad 3.3$$

In equation 3.2 and 3.3, $g_{vdp} = (g_v + g_{dp})$, $C_{gs12} = (C_{gs2} + C_{gs1})$, and $g_{m2dn} = (g_{m2} + g_{dn})$.

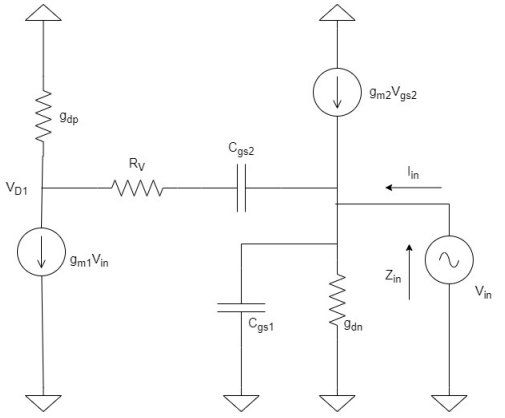

Figure 3-3: Small-signal equivalent model of the active inductor in Figure 3-1

In the previous topology shown in Figure 3-1, the DC flowing through the feedback transistor M2 is regulated by a current source. However, when

the active inductor is excited by a higher order of input power, the DC component of the drain current of M2 increases due to the second-order component resulting from the excitation.

The current I_d of the transistor M2 is fixed by the current from the transistor current source M4. With higher input power, the V_{gs} of the transistor is reduced along with the decrease in its gm. From equation 3.3, we can see that with the reduction in the gain of the transistor M2, the equivalent inductance increases. Thus, inductance values increase with larger input power, and the performance of the active inductor deviates from the small-signal performance. This change in inductance value limits the use of this topology for higher power applications. To overcome this limitation, the transistor M7 is placed in shunt with the feedback trans-conductor M5 as shown in Figure 3-4. The active inductor circuit in Figure 3-4 is implemented with pmos current mirror which acts as a current source, as current mirror provides good biasing stability. The pmos current source sources current from the positive supply, which provides well-controlled output current, and the supplied current does not depend on the output voltage.

This enhances the large signal behaviour of the active inductor. The linearity of the active inductor was further increased by using voltage shifter along the transistor M7 and M5. This reduced the biasing voltage to the transistor M7 which regulated the feedback transistor M5.

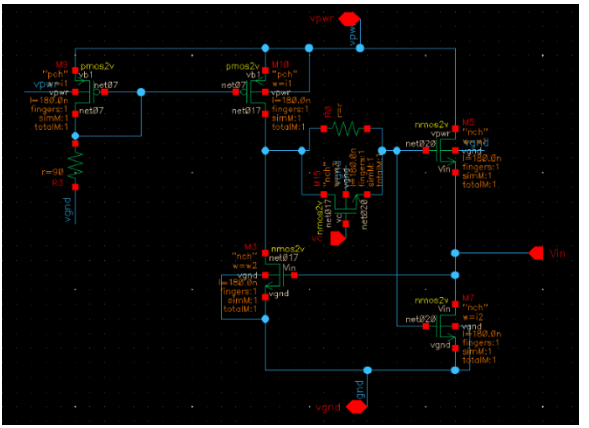

Figure 3-4: Schematic of an active inductor with transistor M7 in shunt with feedback trans-conductor M5.

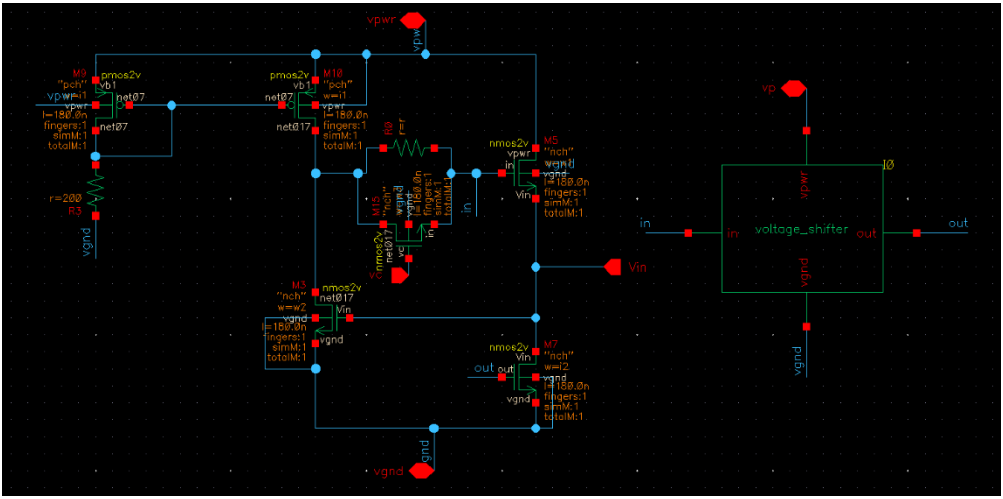

Figure 3-5: Schematic of an active inductor with transistor M7 in shunt with feedback transconductor M5 along with voltage shifter.

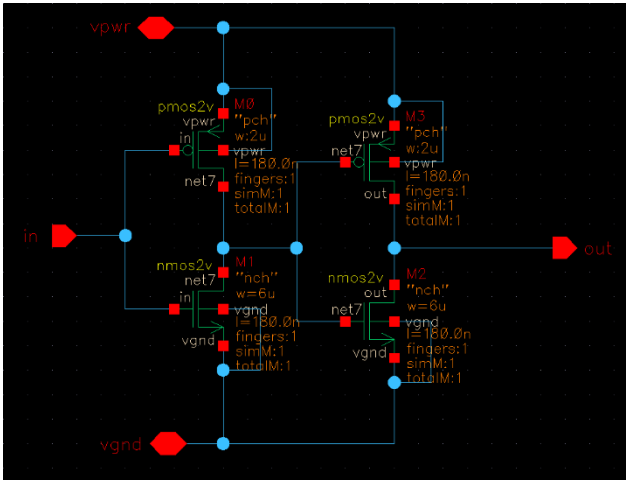

Figure 3-6: Schematic of voltage down shifter.

3.2 Hybrid Coupler Design

This section describes the method followed while designing the quadrature hybrid coupler. The contra-directional coupler topology was used to develop the hybrid coupler, as shown in Figure 2-2(a). In consideration of the large chip area by spiral inductors, lumped-element topologies have been proposed to realize the hybrid coupler circuit for applications below 10GHz. The topology used to design the coupler consists of shunt inductors and series capacitors, and the equivalent circuit model of a hybrid coupler with a centre frequency of f_0 (2GHz for this design) is shown in Figure 3-7. The equations to calculate the values of the lumped elements at the centre frequency f_0 is given by,

$$C_2 = \sqrt{2}\, C_1 = \frac{\sqrt{2}}{2\pi f_0 Z_0} \approx \frac{1}{222 f_0} \tag{3.4}$$

$$L_2 = \frac{1}{\sqrt{2}} L_1 = \frac{Z_0}{2\sqrt{2\pi} f_0} \approx \frac{5.6}{f_0} \tag{3.5}$$

Generally, the on-chip capacitors have high quality factor, and their performance is closer to ideal schematic values. The shunt inductors in the lumped circuit model are realized for this work by the single-ended/grounded Gyrator-C active inductor. The use of the active inductor eliminates the need for distributed systems and spiral inductors, thus reducing the effective chip area. In addition to this, high-quality factor can be achieved, which enhances the performance of the hybrid coupler compared to the lumped-element topology. The active inductor is highly tuneable by varying the bias current and the tuneable resistor R_f.Therefore, the effective centre frequency of the hybrid coupler can be tuned.

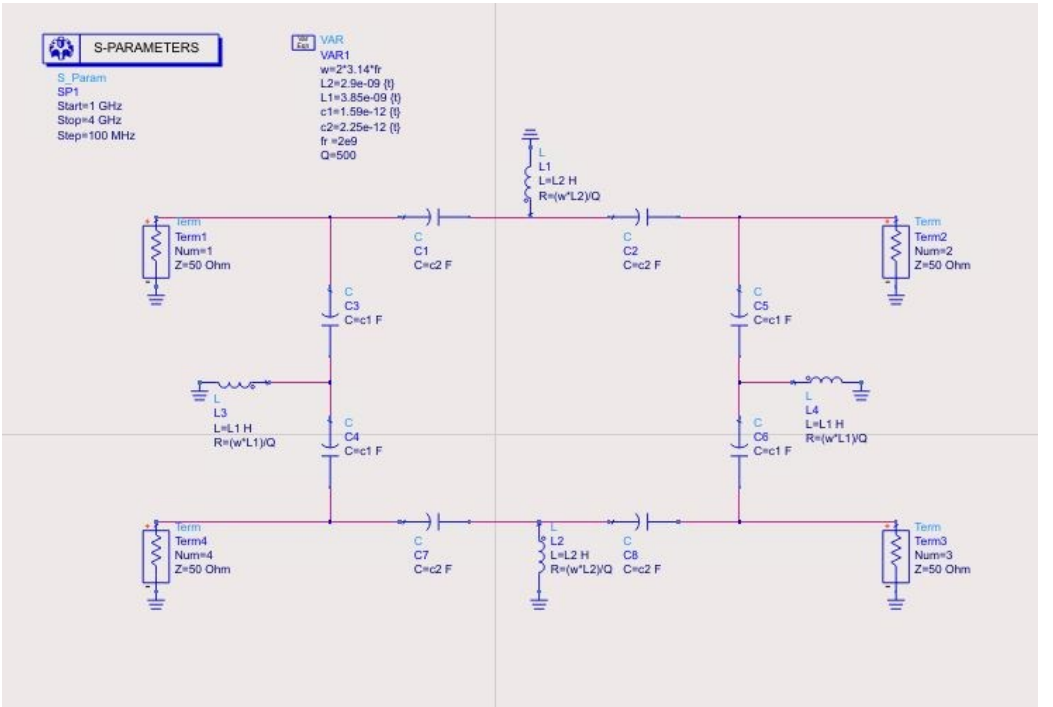

Figure 3-7: Lumped model of branch line coupler.

The S-parameter and the phase response of the lumped model of the coupler using ideal components is shown in Figure 3-8 and Figure 3-9 respectively. The coupler has a considerably good 50-ohm matching results with an input reflection coefficient of -28 dB. Since the coupler is symmetric, a 3 dB equal power split is expected at the through and coupled port. The phase difference between the output ports is a quadrature, as shown in Figure 3-9.

Figure 3-10 shows the schematic of the hybrid coupler integrated with the active inductor. The circuit parameters of the quadrature hybrid are given in the Table *1*. The schematic of an active inductor shown in Figure 3-5 is used to construct the hybrid coupler. The coupler has two different inductors, and the values of the parallel inductors are equal. The active

inductors are tuned to desired values to meet the 2GHz centre frequency requirement. The model is symmetric with similar parallel capacitors and symmetric inductors. From the equations 3.4 and 3.5, the value of L1 and L2 are 3.95nH and 2.8nH, respectively, while C1 is 1.59pF and C2 is 2.25pF.

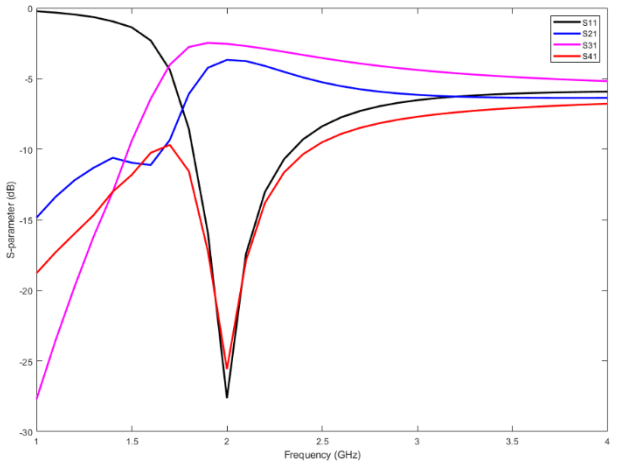

Figure 3-8: S-Parameter characteristics of coupler.

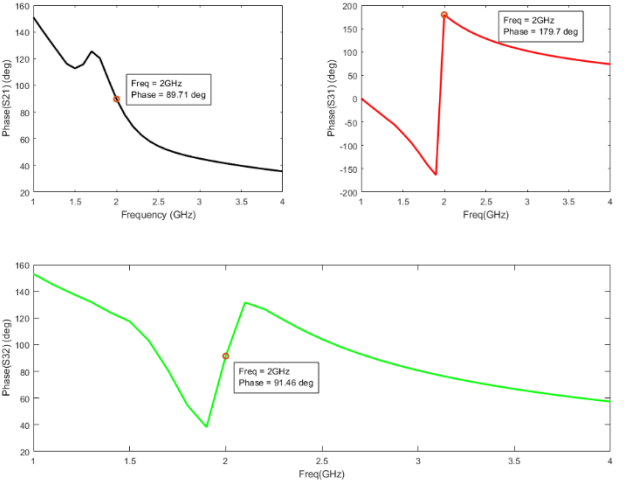

Figure 3-9: Phase response of coupler.

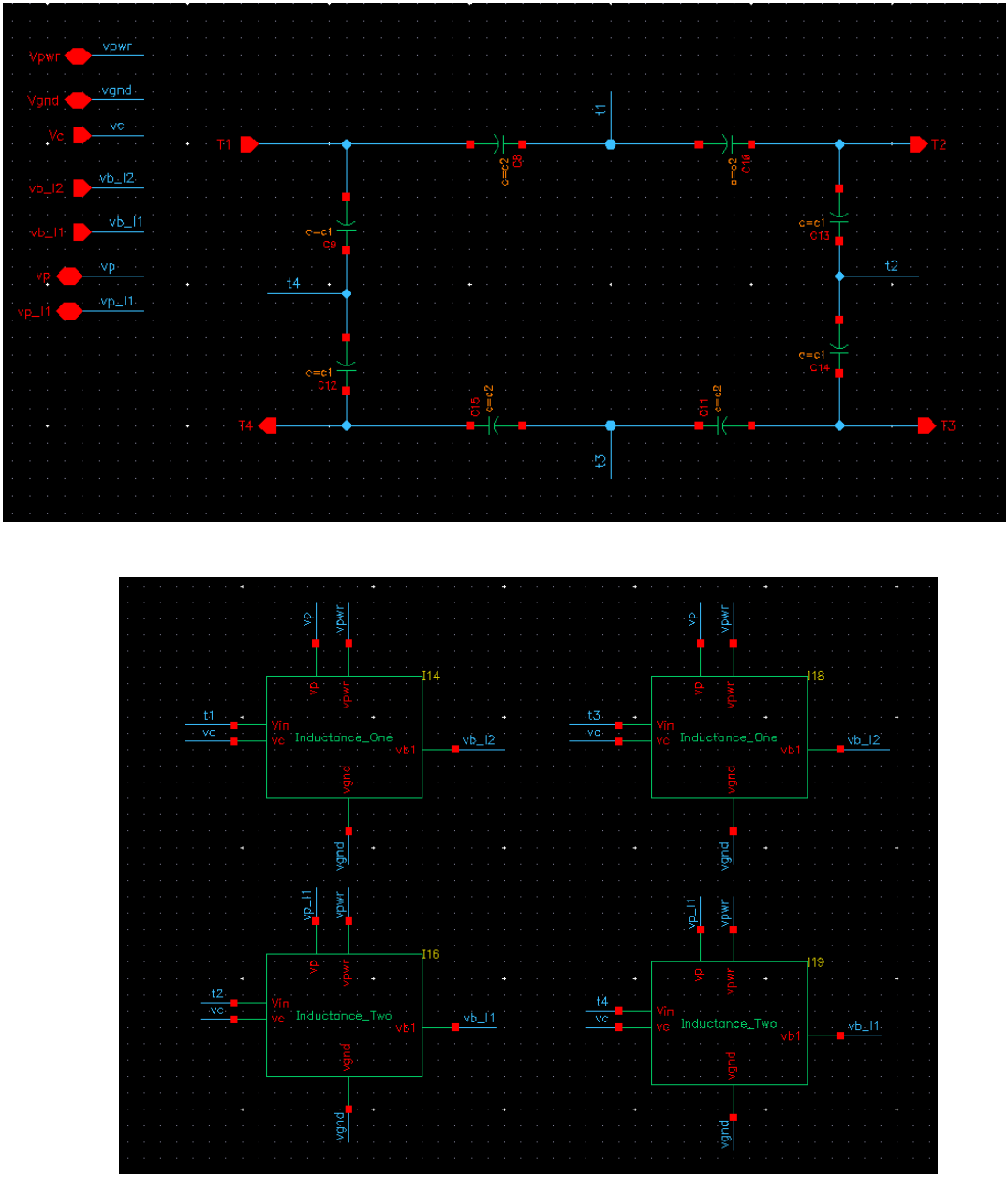

Figure 3-10: Hybrid coupler schematic using the active inductors with equal parallel inductors.

Table 1: Circuit Parameters of Hybrid coupler.

Transistor	Inductor One	Inductor Two
M3	$200\mu m/0.18\ \mu m$	$200\mu m/0.18\ \mu m$
M5	$200\mu m/0.18\ \mu m$	$200\mu m/0.18\ \mu m$
M7	$87\mu m/0.18\ \mu m$	$140\mu m/0.18\ \mu m$
M9	$150\mu m/0.18\ \mu m$	$150\mu m/0.18\ \mu m$
M10	$150\mu m/0.18\ \mu m$	$150\mu m/0.18\ \mu m$
M15	$5\mu m/0.18\ \mu m$	$5\mu m/0.18\ \mu m$
Resistor (Ohm)	1.745 kΩ	1.856 kΩ

4

Results

4.1 Active Inductor

The single-ended/grounded active inductors were designed in 180 nm TSMC CMOS technology in Cadence, and the simulation of the design was carried out on Keysight ADS. Initially, the characteristics and performance simulations of the Active inductor were carried out. Then the hybrid coupler was designed using this active inductor, and the performance characteristics of the coupler were measured. Finally, the coupler was integrated with the PA, and the performance simulation of the LMBA was performed. The schematic of the test bench used to carry out the simulations of the active inductor is shown in Figure 4-1, where the input of the inductor is connected to a 50-ohm terminator. S-parameter analysis is used to determine the quality factor and inductance value of investigated models of the active inductor. Meanwhile, harmonic balance analysis is used to assess the linearity of the active inductor for large signals.

The input impedance and the quality factor for the active inductor in Figure 3-1 are shown in Figure 4-2 and Figure 4-3. To obtain the inductive behaviour, the quality factor of the active inductor should be positive. If the imaginary part of the impedance has a negative value, it will show the capacitive behaviour. For this analysis, the active inductor is analysed over the frequency range of 1GHz to 3GHz. The equations 4.1 and 4.2 are used to plot the input impedance and the quality factor of the active inductor.

$$Q = \frac{imag(Z(1,1))}{real(Z(1,1))} \quad 4.1$$

$$L = \frac{imag(Z(1,1))}{2 * \pi * freq} \quad 4.2$$

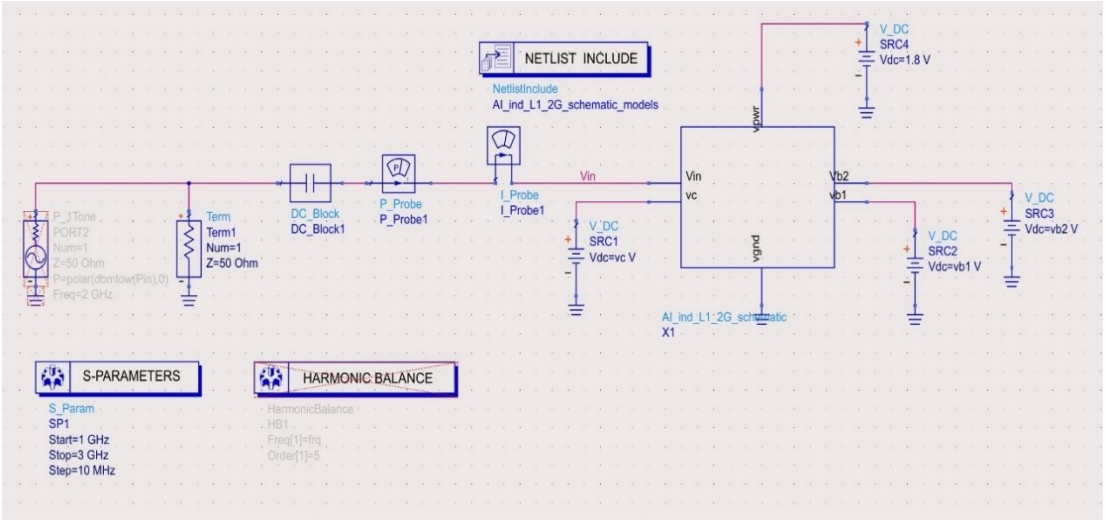

Figure 4-1: Testbench schematic for the active inductor simulation.

The quality factor and impedance plots of the circuits in Figure 3-1, Figure 3-4, Figure 3-5 are shown below. The plots show that the active inductor can achieve a high quality factor over a narrow bandwidth. However, the bandwidth over which the good quality factor is achieved can be controlled by tuning the active inductor.

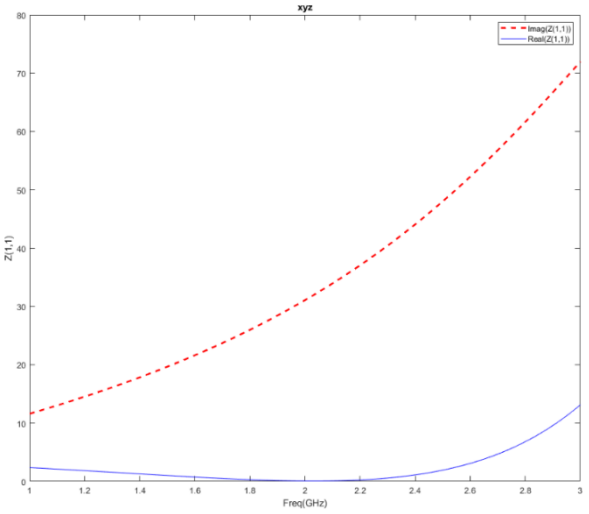

Figure 4-2: Real and imaginary part of the impedance of active inductor in Figure 3-1.

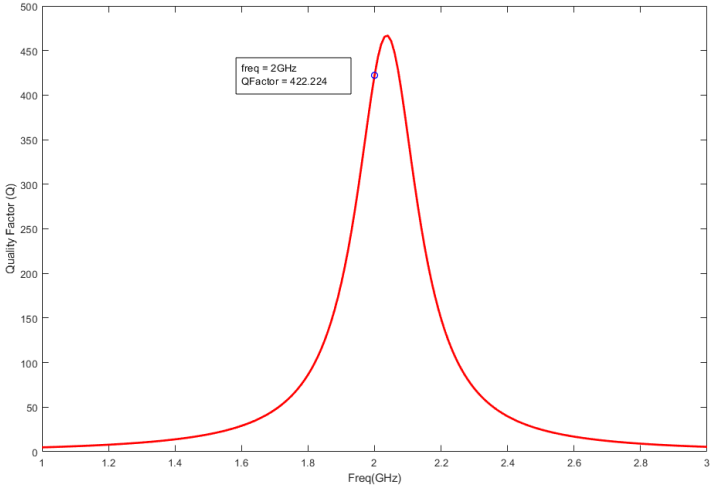

Figure 4-3: Quality factor of the active inductor in Figure 3-1. Q-factor = 422.2 at centre frequency 2GHz.

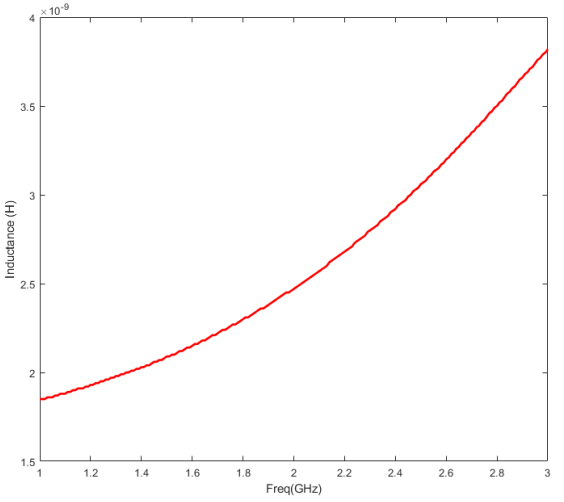

Figure 4-4: Inductance of an AI (Figure 3-1) over the frequency range.

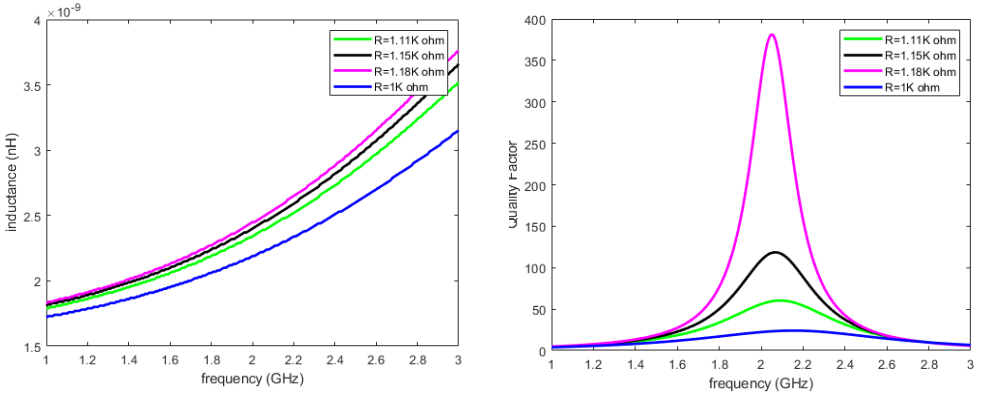

Figure 4-5: Tunability of AI's (Figure 3-1) quality factor and Inductance

By tunning the tuneable resistor R_f (resistor R0 and transistor M5 in Figure 3-1), the inductance value and the quality factor of the active inductor at the centre frequency can be set. Figure 4-5 depicts the tunability of the

active inductor. A similar analysis of the active inductor in Figure 3-4 and Figure 3-5 is performed.

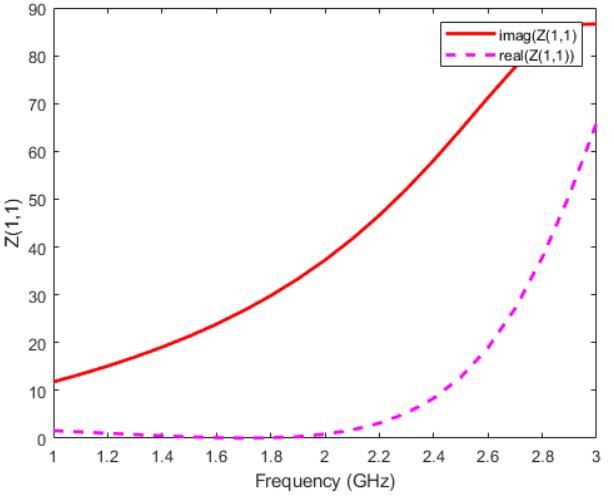

Figure 4-6 : Real and imaginary part of the impedance of active inductor in Figure 3-4.

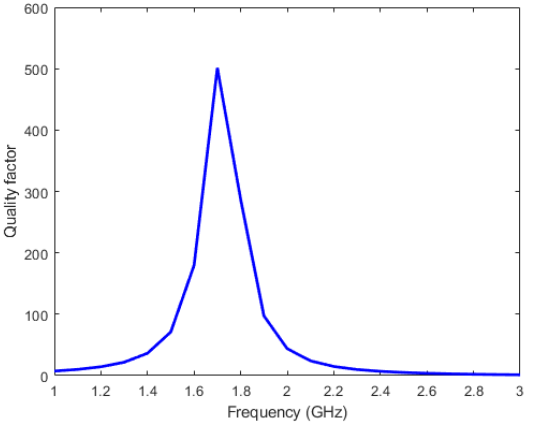

Figure 4-7:Quality factor of the active inductor in Figure 3-4.

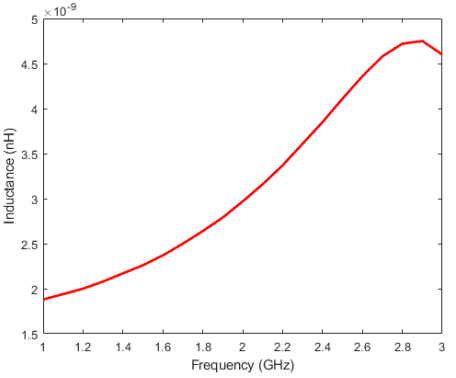

Figure 4-8:Inductance plot of an AI in Figure 3-4 over the frequency range.

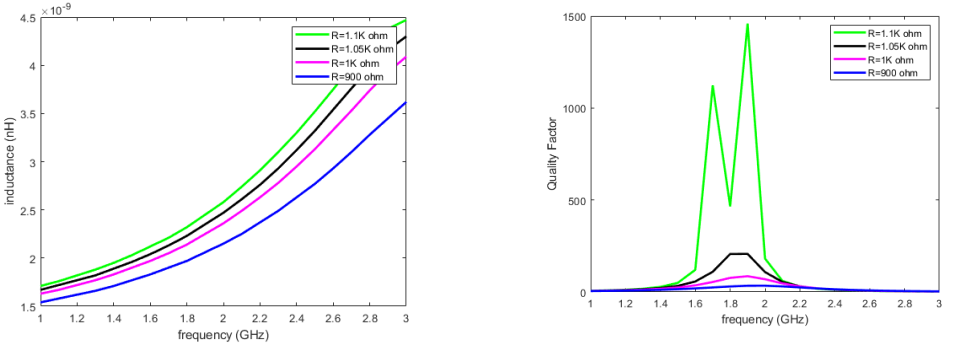

Figure 4-9: Tunability of AI's (Figure 3-4) quality factor and Inductance.

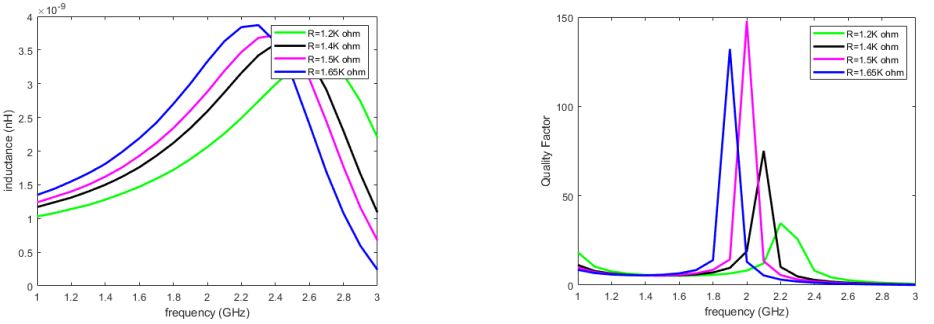

Figure 4-10: Tunability of AI's (Figure 3-5) quality factor and Inductance.

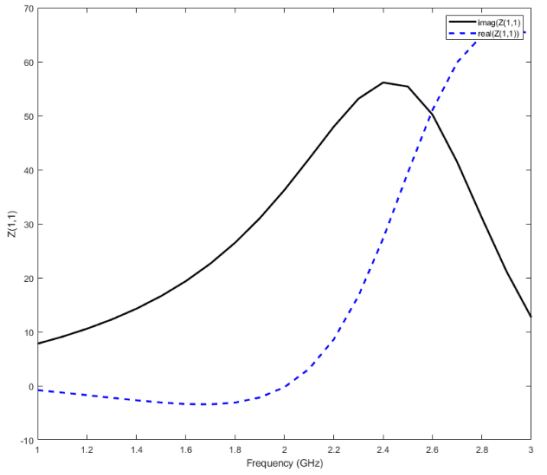

Figure 4-11: Real and imaginary part of the impedance of active inductor in Figure 3-45.

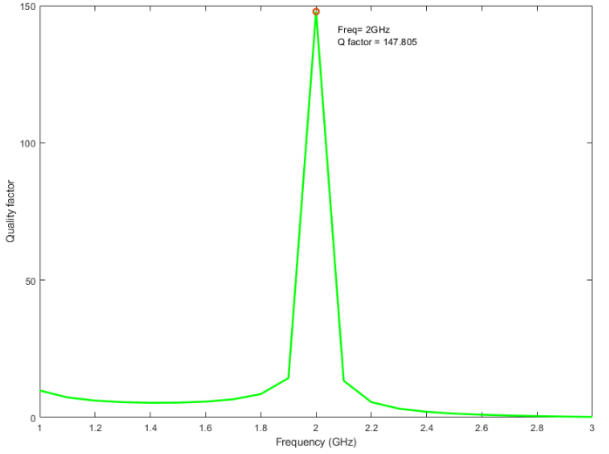

Figure 4-12:Quality factor of the active inductor in Figure 3-45.Q-factor = 147.85 at centre frequency 2GHz.

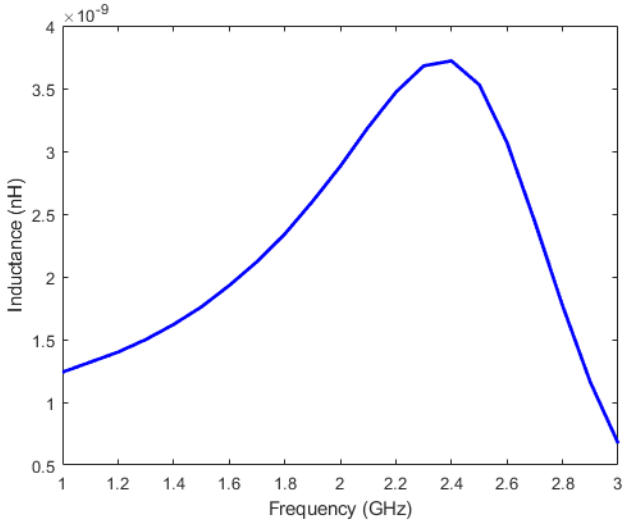

Figure 4-13: Inductance plot of an AI in Figure 3-4*5* over the frequency range.

The active inductors' quality factor and inductance analysis clearly show that they are highly tenable with a good inductance tuning range, and a good quality factor is achieved.

The large-signal analysis becomes essential when analysing the active inductor applications in hybrid couplers. With the large-signal analysis, the input power to the active inductor varied and the linearity and the power consumption of the active inductor are analysed. The power consumption of the three active inductors is shown in the Table 2. The used for generating the plots are shown below.

$$Res = {HB.Vin[1]}/{HB.I_{Probe}.i[1]} \tag{4.3}$$

$$L = {Res}/{(2 * \pi * freq)} \tag{4.4}$$

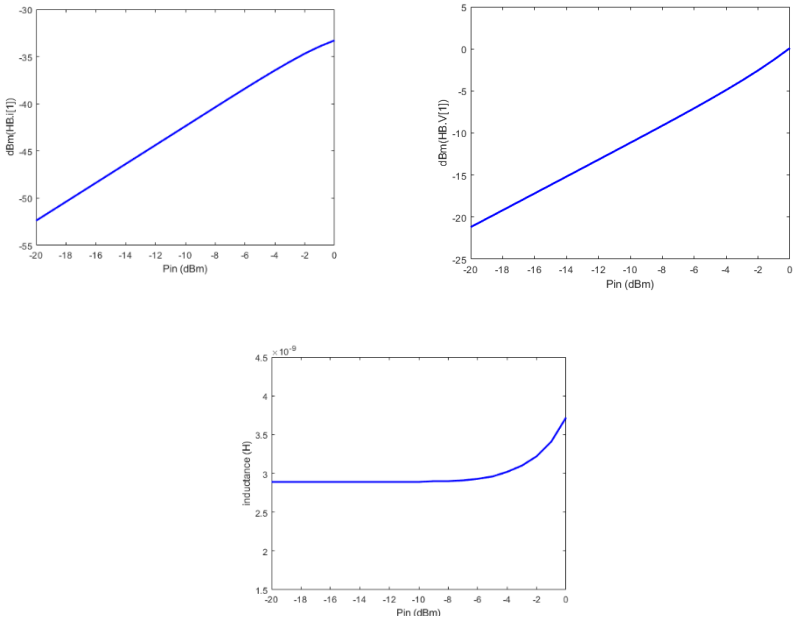

Figure 4-14: Linearity analysis of the active inductor in Figure 3-1.

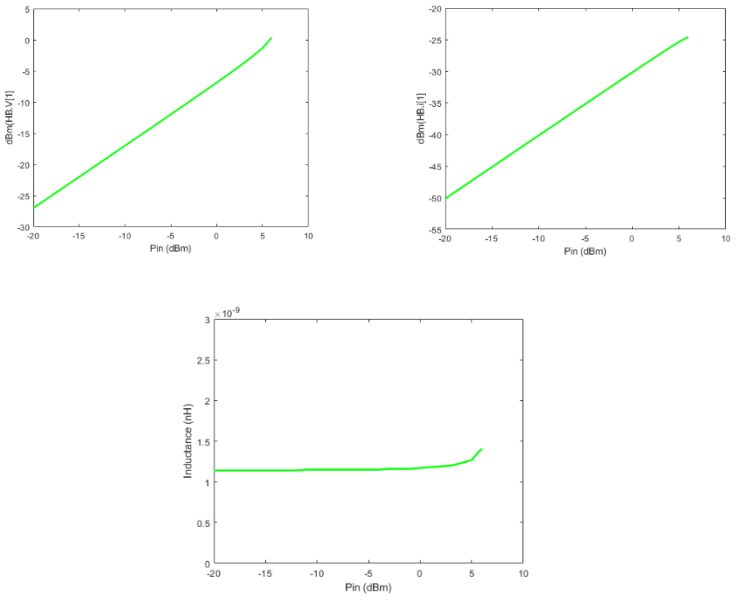

Figure 4-15:Linearity analysis of the active inductor in Figure 3-4.

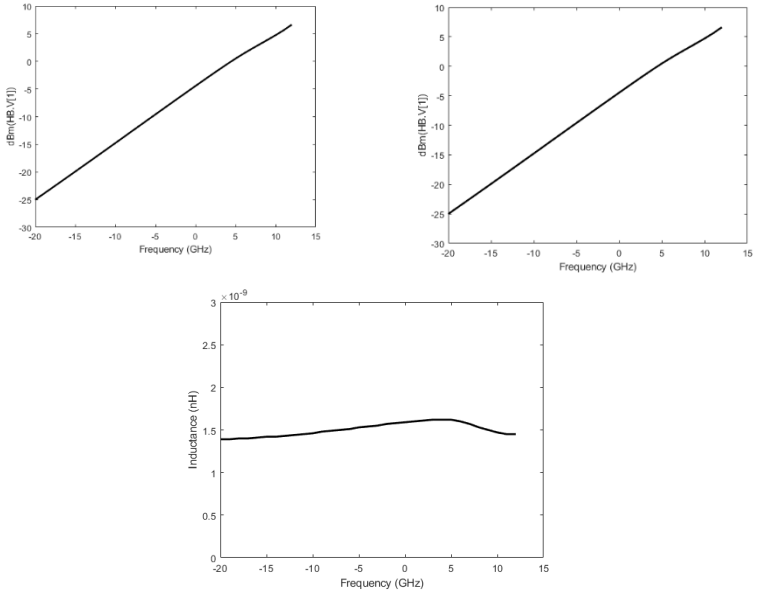

Figure 4-16:Linearity analysis of the active inductor in Figure 3-5.

Table 2: Power consumption of an AI in in Figure 3-1, 3-4 & 3-5 respectively.

Pin(dBm)	P(dBm)
-20	-51.1
-16	-47.1
-12	-42.9
-8	-38.6
-4	-34.1
-2	-32.1
0	-30.8

Pin(dBm)	P(dBm)
-20	-49.9
-16	-45.9
-8	-37.9
-2	-32.0
0	-30.1
4	-26.5
6	-25.5

Pin(dBm)	P(dBm)
-20	-17.2
-14	-16.2
-8	-14.2
0	-12.4
4	-11.6
8	-10.3
12	-9.0

4.2 Hybrid Coupler

The schematic of the hybrid coupler using the active inductor and the simulations of the coupler have been carried out in the ADS. This section discusses the simulation results of the hybrid coupler. The centre frequency of the coupler was fixed to 2GHz. First, the s-parameter and phase difference between the ports is analysed. Then the performance of the coupler at different power levels is analysed. The schematic of the hybrid coupler used for the analysis is shown in Figure 3-10, and the schematic of the testbench in ADS is given in Figure 4-18. The biasing voltages for the active inductor used in the coupler design are $V_{DD} = 1.8V$,

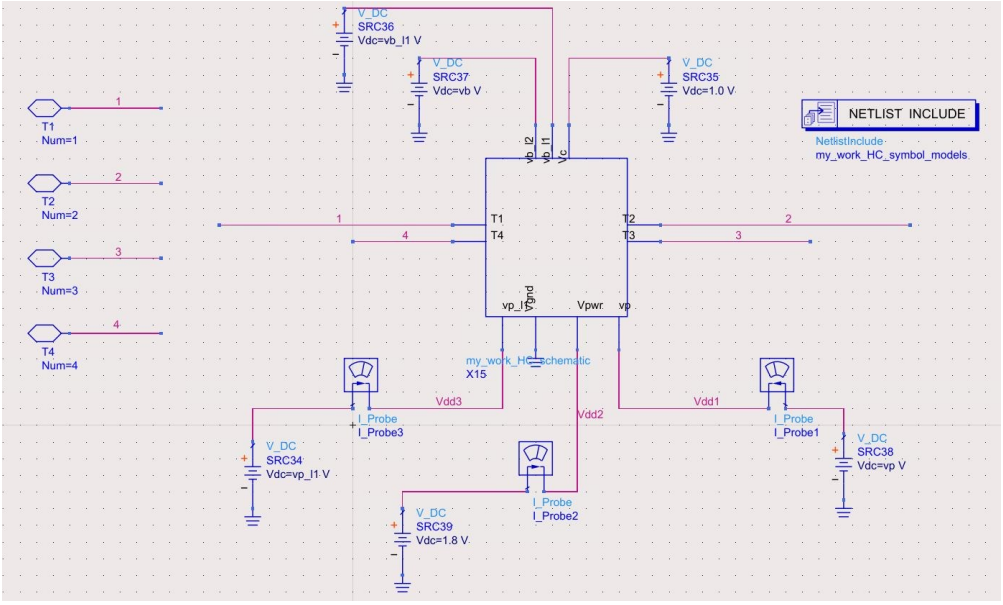

Figure 4-17: ADS schematic for hybrid coupler symbol generation.

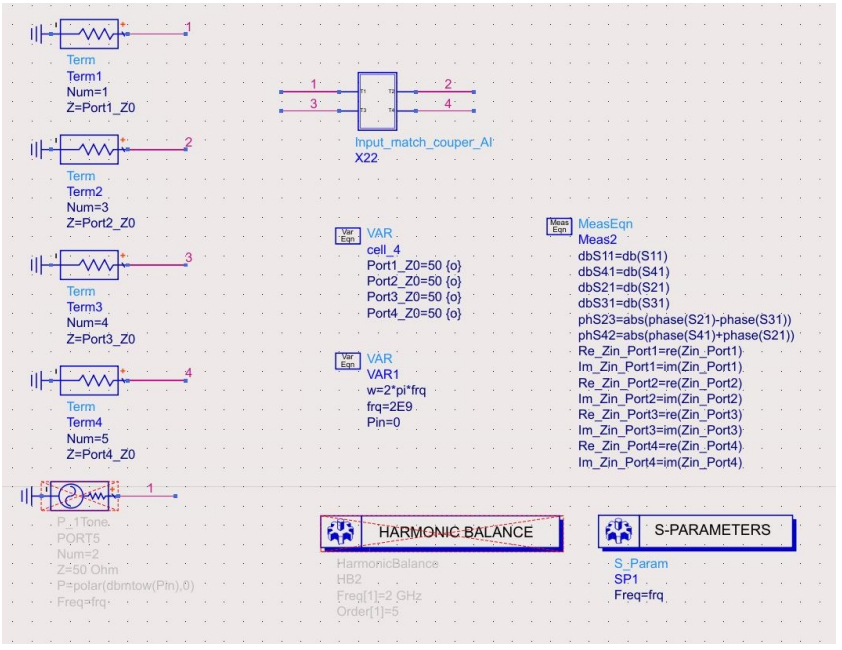

Figure 4-18: The testbench schematic of the hybrid coupler.

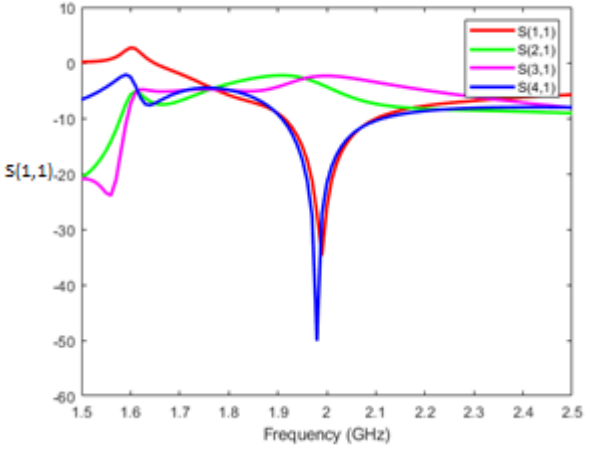

Figure 4-19: S-Parameter characteristics of Hybrid coupler using the active inductor.

Table 3: Impedance at the ports of the hybrid coupler.

Frequency	Zin_Port1	Zin_Port1	Zin_Port1	Zin_Port1
2.00 GHZ	52.7 – j4.4	52.7 – j4.4	52.7 – j4.4	52.7 – j4.4

Table 4: S-Parameter and phase response of the hybrid coupler.

Freq (GHz)	S11 (dB)	S21 (dB)	S31 (dB)	Phase(S21) (degree)	Phase(S31) (degree)	Phase(S23) (degree)
2.00	-26.00	-4.4	-2.4	84.3	176.1	91.8

Table 5: HB analysis of the hybrid coupler.

Pin (dBm)	Port1 (dBm)	Port2 (dBm)	Port3 (dBm)	Difference P2-P3	Phase (Port23)
-10	-15.9	-16.4	-16.6	0.2	28.8
-8	-13.9	-14.4	-14.6	0.2	28.7
-6	-11.9	-12.4	-12.6	0.2	28.7
-4	-9.9	-10.4	-10.6	0.2	28.7
-2	-7.9	-8.4	-8.6	0.2	28.6
0	-5.9	-6.4	-6.6	0.2	28.5
2	-3.9	-4.3	-4.6	0.2	28.4
4	-1.9	-2.3	-2.6	0.2	28.3
6	0.08	-0.3	-0.6	0.2	28.3
8	2.07	1.6	1.3	0.2	28.5
10	4.05	3.6	3.3	0.2	29.2
12	6.03	5.7	5.2	0.2	30.3
14	8.01	7.5	7.2	0.3	31.2
15	9.00	8.5	8.2	0.3	31.7

The hybrid coupler's impedance, S-parameter, phase response, and HB analysis are shown in table A, B, and C, respectively. The results were satisfactory as the phase difference between through-port and coupled-port remain close to 90°and acceptable S11 of -26 dB and the transmission coefficient (S21) of -4.36 dB, and a coupling coefficient (S31) of -2.38 dB, a slight increase in degradation compared to the ideal voltage gain of -3 dB. Table 5 and Table 6 show the coupler's HB analysis with input power varying from -10dBm to 15dBm and a centre frequency of 2GHz. As seen in the linearity analysis of the active inductor, the inductor's performance degrades with the increase in the input power, affecting the coupler. There is good matching between port two and port three. However, there is phase degradation between the through-port and the coupled-port. With the use of an addition matching network, improving the phase performance of the coupler.

Table 6: HB analysis of the hybrid coupler with addition matching at ports.

Pin (dBm)	**Port1 (dBm)**	**Port2 (dBm)**	**Port3 (dBm)**	**Difference P2-P3**	**Phase (Port23)**
-10	-10.0	-13.3	-13.3	0.004	60.3
-8	-8.0	-11.3	-11.3	0.004	60.3
-6	-6.0	-9.3	-9.3	0.003	60.3
-4	-4.0	-7.3	-7.3	0.003	60.4
-2	-2.0	-5.3	-5.3	0.003	60.4
0	-0.1	-3.2	-3.2	0.003	60.5
2	1.9	-1.2	-1.2	0.002	60.5
4	3.9	0.7	0.7	0.001	60.5
6	5.9	2.7	2.7	-0.001	60.5
8	7.9	4.7	4.7	-0.003	60.4
10	9.9	6.7	6.7	-0.005	60.3
12	11.9	8.7	8.7	-0.001	60.1
14	13.9	10.7	10.7	-0.001	59.8
15	14.9	11.7	11.7	0.001	59.7

Table 7: Power consumption by the coupler.

Pin(dBm)	P(dBm)
-10	-35.6
-6	-31.6
-2	-27.7
0	-25.7
4	-21.8
8	-17.8
12	-15
15	-13.3

4.3 LMBA simulation

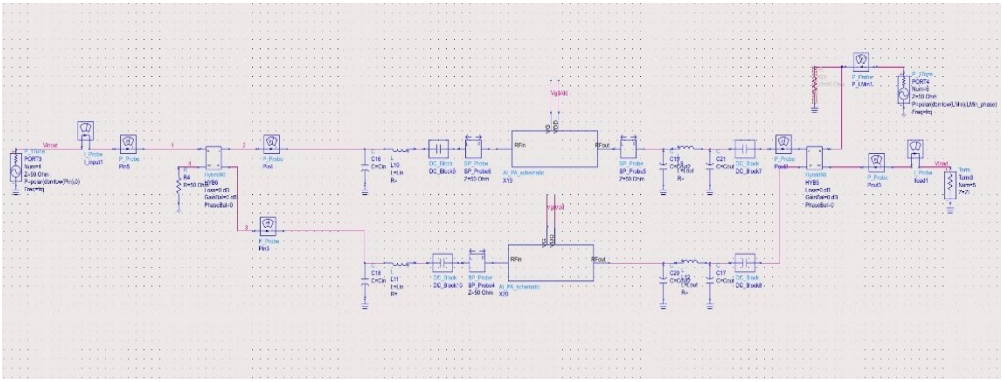

Figure 4-20:LMBA simulation setup.

The schematic of the testbench used to carry out the performance analysis of the power amplifier is shown in Figure 4-20. For the simulation, the balanced amplifier design in paper [1] has been used. The amplifier is biased in deep class AB. Initially, a single amplifier is connected to the through-port of the coupler, and the PAE and output power of the amplifier are measured, and the PAE vs. output power graph is shown in Figure 4-21. PAE of 62% for an input power of 12 dBm, and output power of 24 dBm was achieved. Then, the two amplifiers were connected to the coupler at through-port and coupled-port. This setup was analysed in two ways: the input port of the output coupler connected to a 50-ohm resistor and the input port connected to a source. The respective PAE vs. output power graphs is shown in Figure 4-22 and Figure 4-23 . PAE of 23% for an input power of 12 dBm and output power of 23.2 dBm was achieved with resistive load. PAE of 63.8% for an input power of 12 dBm and output power of 23.2 dBm was achieved with active load.

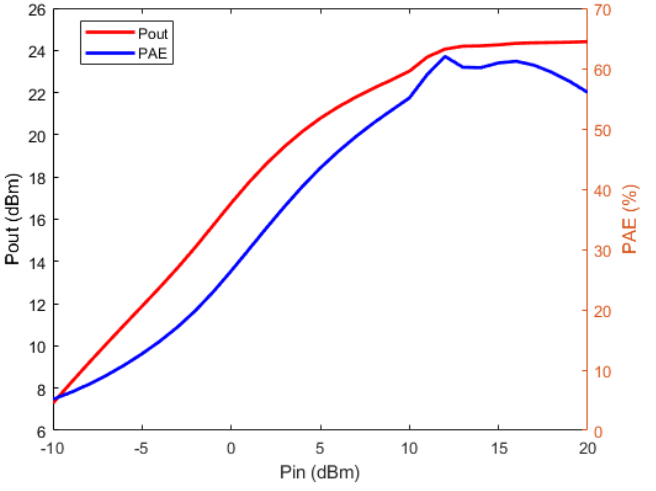

Figure 4-21: PAE vs. output power graph for a single amplifier.

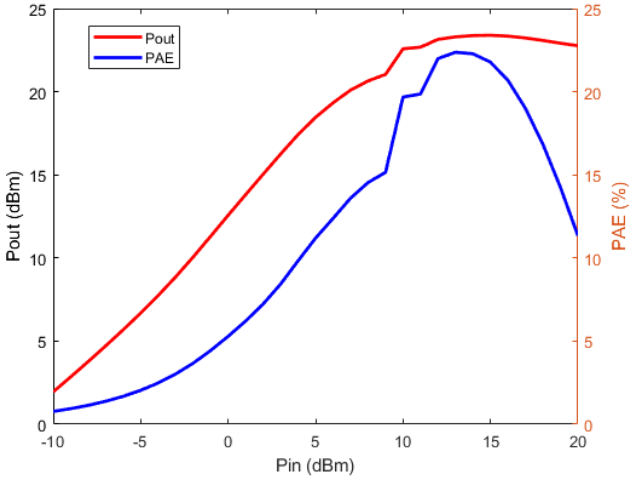

Figure 4-22: PAE vs. output power graph with resistive load.

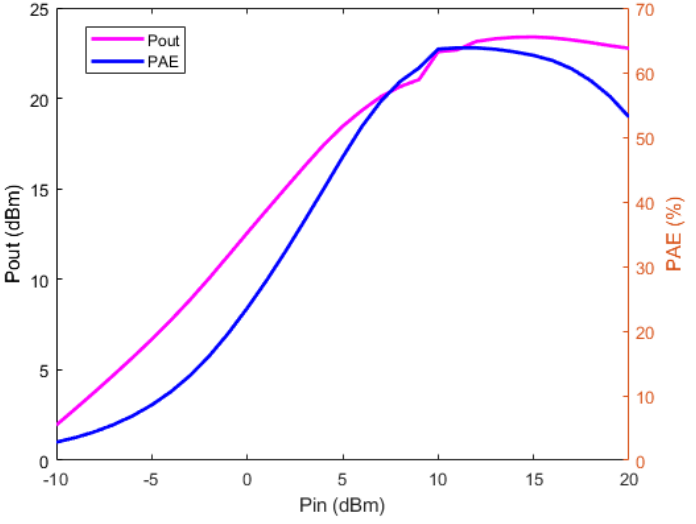

Figure 4-23: PAE vs. output power graph with active load.

5
Discussion

5.1 Results

As mentioned in the previous sections, one of the main objectives of the thesis was to show if the lumped coupler designed using a spiral inductor could be replaced by a hybrid coupler designed using active inductors for input matching in LMBA in [1]. The main observed result is that active inductor performance degraded with the increase in the input signal. When the active inductors are driven with large signals, the performance of the active inductor deviates from the small-signal performance, which in turn affects the performance of the coupler.

The simulation results of the active inductor clearly show that a good quality factor and tuneability of the inductor can be achieved. The graphs in Figure 4-14, Figure 4-15, and Figure 4-16 show the linearity performance of the active inductors. The active inductor in Figure 3-5 has high linearity, and the inductance of the active inductor is linear up to 12 dBm. However, the power consumption is increased. Observing the S-parameter simulation results of the hybrid coupler designed using the active inductor in Figure 3-5. The coupler has an input reflection coefficient (S11) of -26 dB, the transmission coefficient (S21) of -4.36 dB, and a coupling coefficient (S31) of -2.38 dB. The coupler shows good coupling and isolation characteristics. The phase difference between the through-port and the coupled-port of the coupler is 91.79°. The large signal analysis of the coupler is shown in Table 6 and Table *5*. The performance degradation of the coupler is evident from the results. There is a loss of power at through-port and coupled-port. As a result, when used as a power divider at the input of the power amplifiers, the PAE of 63% and output power of 23.2 dBm is obtained at an input power of 12dBm.

This work emphasized checking if an active inductor would be a viable solution to replace the spiral inductors in the coupler. I paper [1] where the possibility of designing an integrated load modulated balanced amplifier (LMBA) in 0.18um CMOS with an operating frequency of 2 GHz. The simulation results with on-chip inductor losses and centre frequency of 2 GHz, the peak PAE at full output power (24dBm) is 34.8%. At 6 dB OBO, the LMBA gives a PAE of 30.6% compared to 23.2% for a reference amplifier without load modulation and load optimized for peak PAE, an absolute improvement of 7.4% or a relative improvement of 31.9%.

However, from the comparison of the work from [1], there is significantly good performance achieved by the hybrid coupler using active inductors.

The overall area occupied by the coupler has significantly reduced. Though the principle of coupler designed using the active inductor worked fine, there could still be improvements in the coupler performance by tuning the active inductor and the capacitance values of the coupler. This work is a decent approach for future compact coupler design using active inductors with further optimization and modifications.

5.2 Method

Though the design approach followed here is similar to the initial work in [37] and [39], certain factors prevented achieving optimal results for the coupler. The selection of the coupler design was limited concerning the design of the active inductor. For this thesis work, grounded or single-ended active inductor topology was used. Therefore, the coupler design was chosen, which used the grounded inductors. The coupler was designed using ideal capacitors and grounded active inductors. The performance degradation of the coupler was observed as the input power increased.
For the power amplifier simulation, the testbench setup used in work [1] has been used, and the input coupler is replaced with the coupler designed in this work. The circuit designing was carried out in Cadence virtuoso, and the testbench setup and simulation of these circuits was performed on ADS. The sources that have been used are peer-reviewed articles and published books. All the figures and equations used from these articles have been referenced.

6

Conclusion and Future work

6.1 Conclusion

In this work, a design of a hybrid coupler using an active inductor is presented. The grounded active inductor based on the theory of gyrator-c was designed. The active inductor's performance characteristics, such as quality factor, tunability, linearity, and power consumption, were analysed.

The hybrid coupler based on this designed active inductor was implemented, and performance analysis was carried out. The coupler was used to feed the input to the power amplifiers designed in Figure 3-5, and the PAE was observed. The performance of the coupler depends on the performance of the active inductor as ideal capacitors have been used.
From the simulation results, the linearity of the active inductor was up to 12dBm, which is still a good performance achieved by the active inductor. The power consumed by the hybrid coupler with an active inductor is considerably low. However, there is performance degradation at higher input power. A PAE of 63% for an input power of 12 dBm and output power of 23.2 dBm was achieved in the LMBA simulation.

6.2 Future work

The current work is still in the development stage and requires further optimization and refinements. Some of the work that could be improved or included in the research work are mentioned below.

- This work does not include designing the hybrid coupler based on floating active inductors. Analysis of the performance floating active inductor for coupler application would be a good work for the future.

This design will reduce the number of inductors in the coupler design.

- Further optimization of the coupler and the active inductor and changing the operation frequency would be interesting.
- This thesis work does not include layout implementation of the designs. A detailed implementation, including parasitic extraction, DRC, LVS, and design of analog pads, would be an interesting work for the future.
- In the hybrid coupler design, ideal capacitors have been used. For future work, Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM) capacitors could be used to determine the more realistic performance of the coupler.

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