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Finite Word Length Analysis for FFT-Based Chromatic Dispersion Compensation Filters

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Abstract: Finite word length effects for frequency-domain implementation of chromatic dispersion compensation is analyzed. The results show a significant difference for the different factors when it comes to power consumption and receiver penalty.

OCIS codes: (060.0060) Fiber optics and optical communication; (060.1660) Coherent communications

1. Introduction

Coherent optical fiber communication enables employment of a variety of efficient modulation techniquws, such as quadrature-amplitude modulation (QAM). In addition, a coherent receiver can equalize linear transmission impairments such as chromatic dispersion by digital signal processing (DSP). However, with the increasing demands on data rates, the DSP power consumption has become an issue. Especially, the chromatic dispersion compensation (CDC) unit is one of the most power-hungry unit in the coherent receiver [1,2]. Therefore, optimization of the word length is crucial. The influence of ADC resolution in fiber optic communication has been studied in [3,4].

This paper presents results on finite word length effects for CDC filters implemented in the frequency-domain [5,6]. The performance is evaluated in terms of receiver power penalty at bit error rate (BER) of 10^{-3} and ASIC synthesis result to 28-nm CMOS technology.

2. System setup

The system considered here operates with 60 GBd signaling rate which, combined with 16-QAM and two polarization modes, is suitable for 400-Gbit/s systems [2]. An oversampling rate of 8/7 samples per symbol (SPS) is used. A 129-tap CDC filter, enabling up to 200 km of fiber, is implemented using overlap-save processing with 256-point FFT/IFFT and multipliers, processing 128 samples in parallel. The structure is shown in Fig. 1.

Three different word lengths are considered: the number of bits used to represent intermediate data, W_d, the number of bits for the twiddle factor multiplication coefficients,W_t, and the number of bits for the filter multiplication coefficients, W_f. These are fundamentally different in the sense that the latter two provide a static, possibly time-varying, error, as opposed to the first which results in round-off noise [7]. The data is quantized by one bit after each radix-4 butterfly to keep the data word length constant. Although theoretically the output is two bits longer compared to the input, simulations show that one bit is enough considering the statistical properties of the considered signal.

3. Results

We choose a 6-bit ADC, which is suitable for a 16-QAM coherent receiver [8]. To determine the impact of the three different word length parameters, the penalty at a BER of 10^{-3} is determined for one parameter at time, using long word lengths for the other parameters. Figure 2a shows the result. As evident, the number of bits for

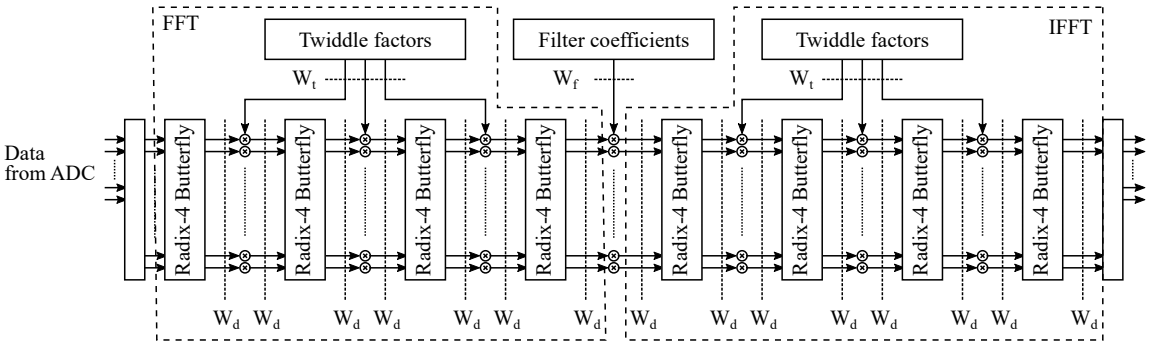
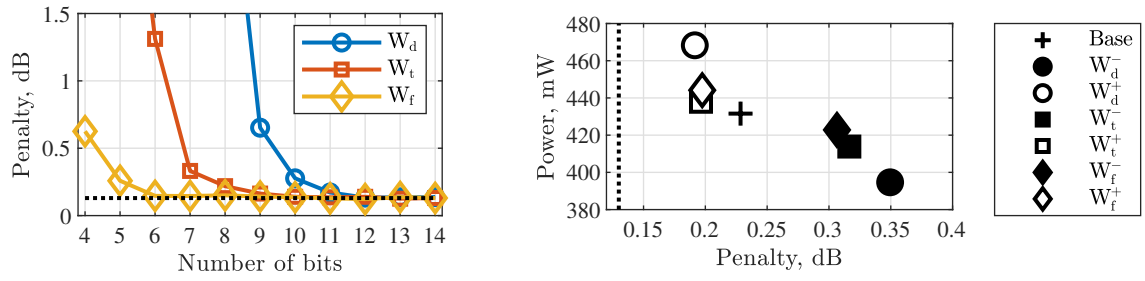
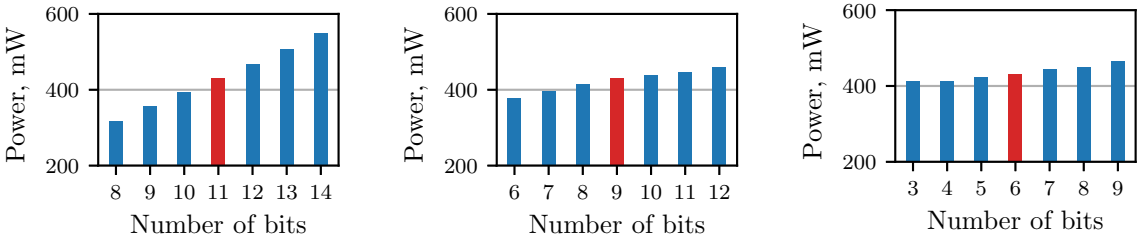


Fig. 1: FFT based CDC filter architecture with quantization. W_d: Internal data, W_t: Twiddle factors, W_f: Filter coefficients.



(a) (b)

Fig. 2: (a) Receiver penalty vs word lengths. (b) Power consumption vs receiver penalty for base case and increasing/decreasing one bit. W_i^+/W_i^- uses one more/less bit for W_i. Dotted lines: penalty from 6-bit ADC. BER$= 10^{-3}$.



(a) (b) (c)

Fig. 3: Power consumption in 28-nm CMOS. (a) data, W_d, (b) twiddle factors, W_t, and (c) filter coefficient, W_f.

internal data has the most significant influence on the penalty. The second most important word length is that of the twiddle factors, leaving the filter coefficient word length as the least influential. Clearly, one should select different values for the three different word lengths to get a similar penalty contribution. Here, we select $W_d = 11$ bits, $W_d = 9$ bits, and $W_d = 6$ bits as a base case for further work.

The design is synthesized to a 28-nm CMOS process with 0.7 V supply voltage at 536.7 MHz clock frequency. The result only includes one polarization. The base case consumes about 432 mW with penalty of about 0.23 dB.

To see the impact on power consumption, the word lengths are changed around the base case. Results are shown in Fig. 3. The data word length has the largest impact on power consumption as seen from Fig. 3a. The impact of twiddle factor word length, shown in Fig. 3b is slightly larger than that of the filter multiplications, shown in Fig. 3c.

Finally, the impact of increasing or decreasing the word lengths one bit from the base case is shown in Fig. 2b. It is interesting that a similar penalty (≈ 0.19 dB) is achieved by using one more bit, independent of which word length is changed. Hence, if a result smaller penalty is required, it is most beneficial to increase the twiddle factor word length one bit.

4. Conclusions

In this work, we have investigated the effect of word length selection in frequency-domain CDC filters for 16-QAM. The results show that selecting 11, 9, and 6 bits for data, twiddle factors and filter coefficients, respectively, is suitable for 60 GBd CDC filter having 0.23 dB penalty at BER of 10^{-3} and 432 mW power consumption.

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