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Battery Balancing on a Full-Bridge Modular Multi-Level Converter

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In memory of my father who is the first showing me the beauty of engineering.

Abstract

Batteries are becoming popular in the trend of electrification. Performance and lifespan of a battery pack are closely related to how it has been utilized. With proper balancing control to slow down aging process, variances of capacity and resistance between battery cells can be maintained at a better level. Among balancing methods, dissipative balancing is still the most common method for its simplicity in control, low cost and high speed. Non-dissipative balancing methods like converter-based and capacitor-based are of researchers' interest because of less heat generated and superior efficiency.

In this thesis, the converter-based balancing method is investigated. A modular multilevel converter (MMC) with Pulse-Width Modulation (PWM) pattern is compared with another MMC with Nearest-Level Modulation (NLM). The speed to balance six battery sub-modules, output power and battery current harmonics are examined.

Acknowledgments

I am thankful for the great help from my supervisors Tomas and Arvind. They spent their valuable time and share knowledge from the field so that this thesis can be made possible. I want to express my gratitude towards my examiner Mattias. Since the beginning of the thesis work, he has helped me with thesis planning and various administrative work. If haven't got his support, I would definitely need more time and effort to finish the work.

In addition, I am grateful that I have friends and people from Rydshemkyrka who support me through the hard time.

Linköping, February 2022
Junyu Lin

Contents

Notation

Symbols

Notation	Meaning
Ω	A unit of electrical resistance (Ohm)
ω	Angular velocity

Abbreviations

Abbreviations	meaning
AC	Alternating Current
DC	Direct Current
FFT	Fast Fourier Transform
MMC	Modular Multilevel Converter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NLM	Nearest-Level Modulation
PID	Proportional, Integral, Differential (controller)
PWM	Pulse-Width Modulation
RMS	Root Mean Square
SOC	State Of Charge
VSC	Voltage Source Converter
VSM	Virtual Sub-Module

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1

Introduction

To meet the goal of zero carbon emission by 2050, many industries are undergoing a trend of electrification. Batteries play an important role in electrification. As machines to be replaced with their electrical counterparts which are more efficient and powerful, the energy these new machines need grows quickly. To meet the fast growing demand for energy, performance of energy storage like battery packs need to be improved. Therefore, capacity and lifespan of a battery pack are of great importance. If battery cells in a pack are utilized without any balancing method, the voltages of each battery cells would vary eventually, degrading the capacity as a battery pack overall, according to [2].

1.1 Motivation

There are two types of battery balancing methods [2, 3]: active balancing (also known as non-dissipative balancing) and passive balancing (also known as dissipative balancing). The active method removes charges from battery cells with higher State of Charge (SOC) to cells with lower SOC while passive method simply drains electricity from the battery cells having higher SOC with a resistor circuit dissipating the excessive energy as heat.

One of the most fast growing application with battery packs is electromobility where energy from battery packs are converted into Alternating Current (AC) to drive motors. Therefore, converter-based cell balancing is particularly interesting not only because it is a kind of non-dissipative balancing method which results in less heat but also it is simple in circuit design perspective. This method doesn't require extra electrical components except for controllers to manage the gate switchings of the converter. The converter-based method has such an advantage in applications like passenger vehicles where size and weight of the power

train are critical.

1.2 Objective

In this thesis work, two Modular Multilevel Converters (MMC) are built in a simulation to investigate converter-based cell balancing method. One MMC is set to output AC voltage in Pulse-Width Modulation (PWM) pattern which is well investigated in researches and of which multiple variants are used in the industry. The other MMC is set to output AC voltage in Nearest-Level Modulation (NLM) pattern.

The goals of this thesis are to:

- construct of a simulation setup for a single-phase MMC in Simulink.
- design mechanisms of cell balancing using PWM and NLM patterns separately.
- investigate on performance of implementing balancing strategy with the two different patterns in terms of harmonics, output power and balancing speed.
- discuss the advantages and disadvantages of the two setups (MMC using PWM and NLM patterns).

1.3 Problem statement

The questions the thesis is investigating are as follows:

- What is converter-based cell balancing techniques?
- How to use converter-based cell balancing technique in two Modular Multilevel Converters with PWM pattern and with NLM pattern respectively?
- What is the performance of these two setups, in regard to balancing speed (given the same criteria for a sub-module being balanced), output power, modulation index, duty cycles, mean DC current and harmonics performance?
- Is the utilization of a pattern perfectly superior to the other one?

1.4 Delimitation

No hardware is implemented in the thesis, the project is a study based on a simulation model on Simulink. Due to limit on simulation time, the two MMC models haven't been tested in various cases where SOC of battery cells vary larger than

0.025 % from the average SOC, different circuit topologies or under different temperatures are presented.

As component selection is not an objective of the thesis, components used in the simulation are generic. Only those parameters relevant to cell-balancing method will be discussed. Hardware implementation would be desirable for researching on the effect of cell-balancing control because insights from simulation model and actual feedback from hardware setup are important to research on balancing methods. But that would be left for future studies.

2

Theory

This chapter is used for introducing basic theories about components of a MMC, AC output patterns to be formulated and relevant measurement. It starts from structure of a MMC, output voltage of a sub-module, state of charge (SOC) of a battery cell are presented. After sections with Pulse-Width Modulation (PWM) and Nearest-Level Modulation, descriptions of RMS value and power triangle are given. Based on the foundation of power triangle, PID controller is introduced. PID controller is key to balance control in the MMC with PWM. At the end of the chapter, Fast Fourier Transform (FFT) analysis is demonstrated with an example of a step signal and harmonics measurement is shown.

2.1 MMC

Voltage source converter (VSC) which relies on transistor technology can deliver power to both active load and passive load.[4] MMC (modular multilevel converter) is a kind of voltage source converter. MMC can be easily scaled up or down because the output voltage is determined by the number of sub-modules inserted. Figure 2.1 [1] shows a typical application: a three phase MMC consisted of $6N$ sub-modules. N sub-modules form an arm (marked as 'multivalve' in the figure). Assuming each sub-module has a battery cell of U_{batt} and the output voltage of a sub-module is $\frac{U_{\text{batt}}}{2}$ because of the use of half-bridge converter. The AC voltage output of this modular multilevel converter $U_{\text{D}} = \pm\frac{N \cdot (U_{\text{batt}})}{2} \cdot \sin(\omega t)$. An upper arm and a lower arm together form a phase leg (annotated as 'phase unit' in the figure). The number of sub-modules N can vary from dozens to hundreds depending on applications.

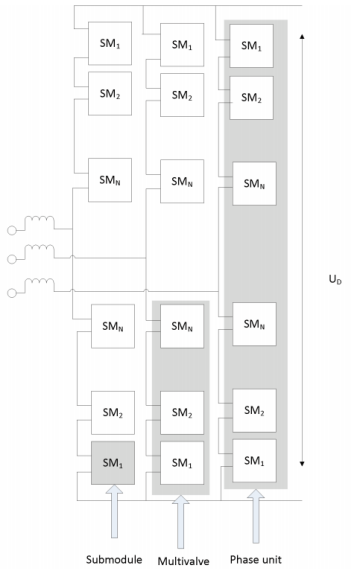


Figure 2.1: *The structure of a three-phase MMC.[1]*

2.1.1 Sub-module

For a single-phase application, a sub-module used in a Modular Multilevel Converter should contain at least a DC voltage source U_{batt} and a full-bridge converter, as shown in Figure 2.2. As demonstrated in Figure 2.3, the full-bridge converter has four switching MOSFETs instead of only two switching MOSFETs in half-bridge converter which is commonly used in a three phase applications. Since the output voltage of a full-bridge converter is referred to ground while the output voltage of a half-bridge converter is referred to the middle point of the DC voltage, a full-bridge converter can thus output $\pm U_{\text{batt}}$ rather than $\pm \frac{U_{\text{batt}}}{2}$.

By having different combination of switching state on gate `s1` to `s4`, output of the sub-module varies, as shown in table 2.1. `s1` being **on** means the switch is conductive while `s1` being **off** means the circuit is open, the switch is non-conductive.

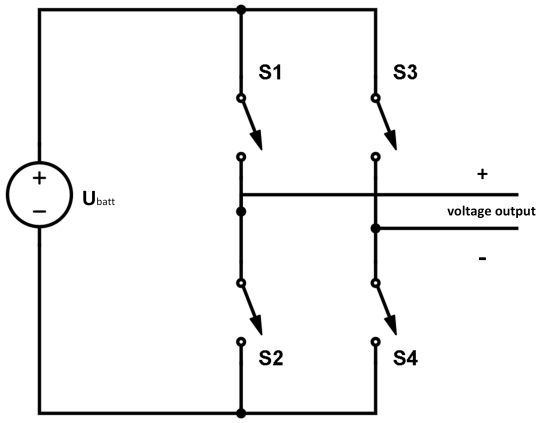
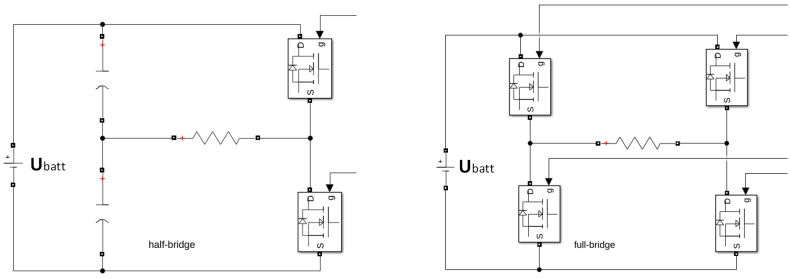


Figure 2.2: *For a single-phase application, a sub-module of MMC is consisted of a DC voltage source, a full-bridge converter of four switches.*



(a) *A half-Bridge Converter circuit.*

(b) *A full-Bridge Converter circuit.*

Figure 2.3: *A half-bridge and a full-bridge converter circuit.*

Table 2.1: *Switching state of gates and resulting output voltage.*

Voltage output of the Sub-module	S1	S2	S3	S4
$+U_{\text{batt}}$	on	off	off	on
$-U_{\text{batt}}$	off	on	on	off
0 (the sub-module is bypassed)	on	off	on	off
0 (the sub-module is bypassed)	off	on	off	on
potential difference between two terminals (the sub-module is disconnected)	off	off	off	off

2.1.2 Battery and SOC

Lithium-ion battery cells are used as DC voltage supply that can be charged and discharged. The advantages of using Lithium-ion battery are light weight, occupying less volume, higher voltage with higher energy density, and negligible memory effect. The disadvantages is higher cost than other types of batteries, lead acid battery for example. Similar to other types of batteries, variances of resistance and capacity are inevitable due to the production process of Lithium-ion battery packs where material impurity, cell grouping methods and connection with bus bars can lead to these variances.[5–7] Without proper balanced control on battery cells, these variances can grow bigger over charging/discharging cycles which are essentially chemical reactions happening on cathode and anode.[8]

Starting from fully charged , state of charge (SOC) is defined: [9, 10]

$$SOC = (1 - \frac{Q}{C}) * 100\% \tag{2.1}$$

where Q represents accumulated charge in discharge mode (integral of current drawn from the battery cell during discharging process). C represents capacity of the battery (amount of stored charge when fully charged). SOC is a state of a battery cell varying from 0% to 100%. 100% means the battery is fully charged and 0% means the battery is completely drained.

For battery cells connected in series, Q is the same; The variance of capacity C among different cells makes battery cells having lower capacity have higher SOC when charging and lower SOC when discharging, compared to cells with higher capacity. In order to maintain battery pack's performance and to improve lifespan, cell balancing techniques are needed to prevent SOC difference from growing larger.

The upper plot of Figure 2.4 illustrates a discharge process of the Lithium-ion battery model. It is consisted of three stages: exponential area, nominal area and the rest area. The exponential area refers to the rapid voltage drop since the battery cell gets discharged at nominal current 12.1739 A from being fully charged. The nominal area indicates that the energy can be drawn from the battery cell before its voltage is getting below the nominal value. The rest area shows how

the battery is drained out of all energy after its output voltage becomes lower than its nominal voltage. The lower plot of the figure where `E0`, `R`, `A` and `B` mean Constant Voltage (in V), Internal Resistance (in Ω), Exponential Voltage(in V) and Exponential Capacity (in Ah) respectively, shows the battery cell's discharge characteristic at different current. `K` means polarization constant, in V/Ah, or polarization resistance, in Ohms.

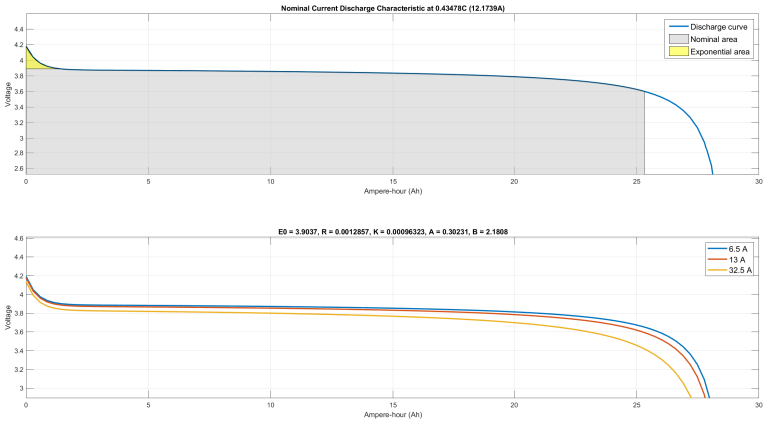


Figure 2.4: *Discharge characteristics under nominal current (*12.1739 *A) and other conditions.*

2.2 Bipolar and unipolar pattern

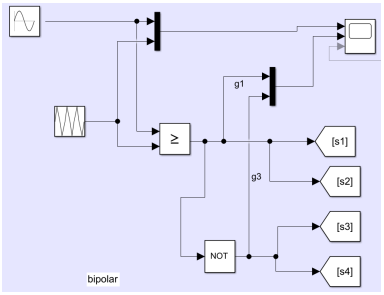
With PWM scheme, there are two types of output pattern depending on the way how to generate gate pulses to a full-bridge converter in the sub-module shown in Figure 2.2. The DC voltage connected in the full-bridge converter is 3.6 V. MOSFET used in the model (shown in Figure 2.5) has a resistance r_{on} of 0.1 ohm, current flows through two MOSFETs (`s1` & `s4` or `s2` & `s3`) in the full-bridge converter causing 0.6 V of voltage drop. Thus, the voltage output of the converter is $+U_{\text{batt}}$(+3 V) to $-U_{\text{batt}}$ (−3 V), as shown in Figure 2.6 and 2.7.

Bipolar pattern generation: in the upper plot of Figure2.6, a triangle wave of gate switching frequency (carrier wave) is compared with reference sinusoidal signal. Signal `g1` turns one when sinusoidal signal is above the triangle wave and turns to zero when sinusoidal signal is equal to or below the triangle wave. As complementary signal, signal `g3` turns one when sinusoidal signal is equal to or below the triangle wave and turns to zero when sinusoidal signal is above the triangle wave. In the lowest part of the figure, output voltage `vload` is shown, with two values: $+U_{\text{batt}}$(+3 V) or $-U_{\text{batt}}$ (−3 V).

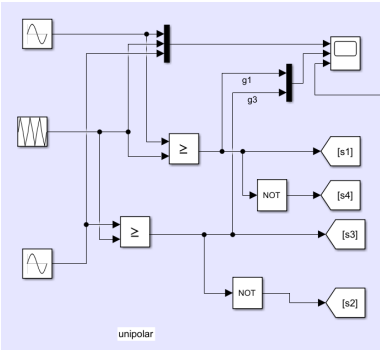
Unipolar: in the upper plot of Figure 2.7, another sinusoidal wave shifted 180 degree is added as reference.[11] Instead of being complementary to each other, signal `g1` turns to one when sinusoidal wave 1 is above the triangle wave and signal `g3` turns to one when sinusoidal wave 2 is above the triangle wave. In the lowest part of the figure, output voltage `vload` is shown, with three values: $+U_{\text{batt}}$(+3 V), 0, $-U_{\text{batt}}$ (−3 V).

As shown in both Figure 2.6 and 2.7, when signal `g1` is one and `g3` is zero, the output of converter is positive. When signal `g1` is zero and `g3` is one, the output of converter is negative. For unipolar pattern generation, when signal `g1` and `g3` are both zero/one, their complementary signal `g2` and `g4` are both one/zero; the output is zero, corresponding to 'bypassed' in Table 2.1. The generation model of both bipolar and unipolar pattern is shown in Figure 2.5.

Compared to bipolar pattern, unipolar pattern offers one additional output state (zero voltage), which is good for harmonics performance because it avoids the sudden change from $+U_{\text{batt}}$ to $-U_{\text{batt}}$.



(a) Bipolar pattern generation model.



(b) Unipolar pattern generation model.

Figure 2.5: *Bipolar and unipolar pattern generation model.*

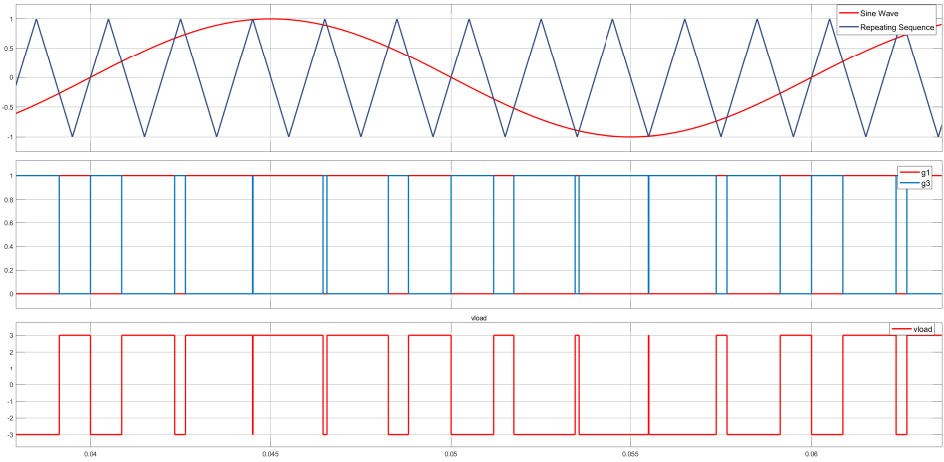


Figure 2.6: *Bipolar pattern.*

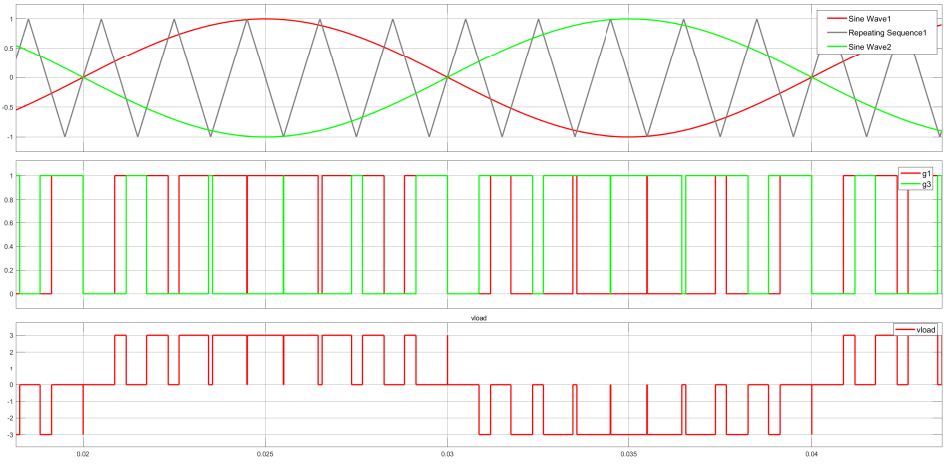


Figure 2.7: *Unipolar pattern.*

2.3 Phase-Shifted Pulse-Width Modulation

PS-PWM (Phase-Shifted Pulse-Width Modulation) is phase-shifted version of PWM. In Figure 2.8, six triangle waves with ($\frac{180}{6}$) degree shifted are compared to the sinusoidal wave in the upper figure to spread half a period phase difference evenly among six sub-modules connected in series for full-bridge converter having two complementary legs. Thus, these sub-modules are inserted or bypassed in series to output a sinusoidal-like voltage waveform as shown in the lower part of the figure. A zoom in view together with six pulse signals controlling gate 1 in the converters of six sub-modules are shown in 3rd plot of Figure 2.9.

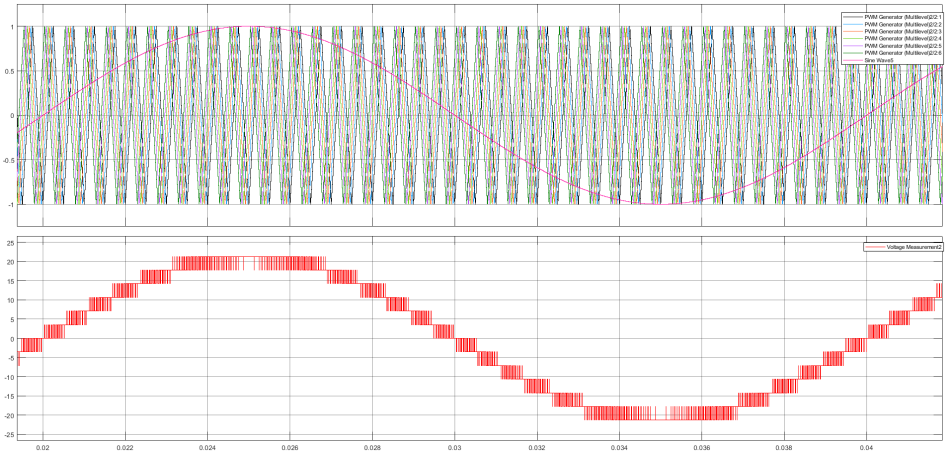


Figure 2.8: *PS-PWM pattern.*

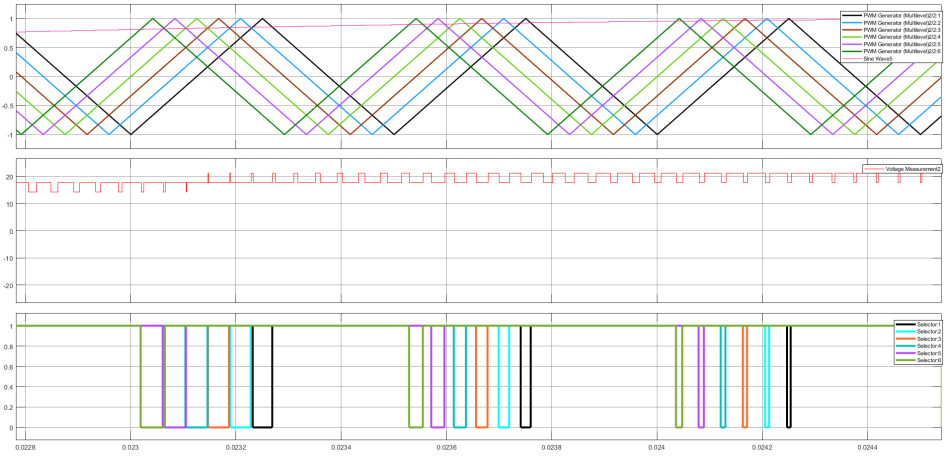


Figure 2.9: *Zoom-in view on PS-PWM pattern.*

2.4 Duty cycle and modulation index

Duty cycle is defined:

$$\text{duty cycle} = \frac{T_{\text{on}}}{T} * 100\% \tag{2.2}$$

where T_{on} is the time when the switch is conductive and T is the period of switching. As shown in both Figure 2.6 and 2.7, the duty cycle varies over time to have the output approximating the sinusoidal reference.

Modulation index m_{a} in PWM is the ratio of the amplitude of the reference sinusoidal wave to the amplitude of carrier wave (the triangle wave of 1 V here):

$$m_{\text{a}} = \frac{amplitude\ of\ reference\ sinusoidal\ wave}{amplitude\ of\ carrier\ wave} \tag{2.3}$$

If the modulation index is between 0 and 1, the gate pulses generated to the converter can output a sinusoidal voltage with the same frequency and phase as the reference sinusoidal wave has, given the frequency of the triangle wave is high enough.

The amplitude of the voltage is determined by modulation index m_{a} and the maximum DC voltage $V_{\text{dc,max}}$:

$$AC\ output\ voltage = m_{\text{a}} \cdot V_{\text{dc,max}} \tag{2.4}$$

However, if modulation index is over 1 (100%), overmodulation occurs. Voltage output from the converter cannot go beyond its maximum to meet the sinusoidal reference signal thus, degrading its harmonics performance.

2.5 NLM pattern

Unlike PWM controlling gate pulses by comparing a triangle wave of high frequency with a reference sinusoidal wave of low frequency to have an approximation of sinusoidal output voltage, NLM is straightforward. NLM directly controls when to insert or bypass sub-modules to approximate the total voltage output sinusoidal wave. Commonly, the following equation is used to determine when a sub-module should be inserted by deriving the switching angle[12]:

$$\alpha_i = \sin^{-1}(\frac{i-0.5}{n});\ \text{for}\quad \text{i=1,2,3,...,n} \tag{2.5}$$

where i is the number of the sub-module, $i = 1$ for sub-module 1. When reference sinusoidal wave exceeds $\frac{i-0.5}{n}$, corresponding sub-module i is turned on (inserted into the MMC), the switching angle calculated from the equation is used for determining the timíng of this switching event.

For harmonics performance and better control over cell balancing schemes later on the thesis, some adaptions are made. Instead of being based on switching angle, control when to insert or bypass a sub-module is based on amplitude (in positive half period, value of 1 to 6 corresponds to insert or bypass 1 to 6 sub-modules, depending on rising/falling edge). A step signal is generated by using relational operators to compare the reference sinusoidal wave with specific constants $(-5.8, -5, -4, \ldots, -1, 1, 2, \ldots, 5.8)$ to determine the operation points at which a sub-module should be inserted or bypassed so that the output voltage waveform is sinusoidal, as shown in Figure 2.10. These constants compared can also be modified to be the valued determined by equation 2.5, having more freedom on selecting duty cycles. These relational operators return Boolean value one when the conditions are fulfilled (sinusoidal wave is larger than/ equal to a positive constant or below/ equal to a negative constant). The result of Boolean values is added together to form a step signal (as shown in the middle part of Figure 2.10). This step signal determines when to insert or bypass a sub-module to keep total output voltage sinusoidal. To be specific, there are six steps to insert a sub-module positively in the rising edge and six steps to bypass a sub-module in the falling edge in the positive half period, as twelve operation points shown in the Figure 2.11. There are also another six operation points to insert sub-modules negatively and six operation points to bypass sub-modules in the negative half period, similar to the mechanism for the positive half period. Because the constants to compare in negative period have the same absolute value of the constants used in positive period, there would be 180 degree phase shift between the same operation points.

Falling edge indication (turning to one when highest step is reached and turning to zero when lowest negative step is reached, as shown in the lower figure in Figure 2.10) is added for later balancing control strategy.

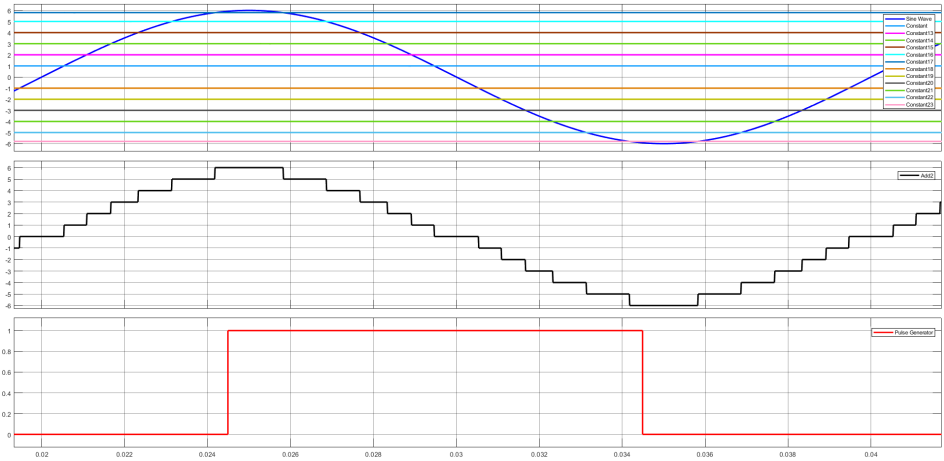


Figure 2.10: *Sinusoidal waveform compared with constants (upper), resulting step signal (middle) and falling edge indication (lower).*

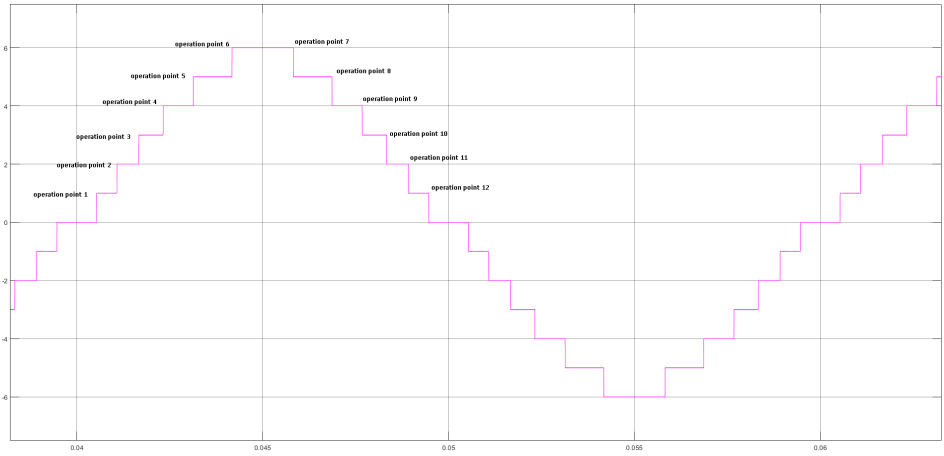


Figure 2.11: *Twelve operation points in NLM setup.*

2.6 RMS and power triangle

Known as quadratic mean, Root mean square (RMS) value of voltage or of current is the DC equivalent of alternating voltage or current flowing through the same load. RMS voltage V_{rms} over a period T is determined as:

$$V_{\text{RMS}} = \sqrt{\frac{1}{T} \cdot \int_0^T v^2(t)dt} \tag{2.6}$$

In the Figure 2.12, power triangle is illustrated. The X-axis represents active power P (also known as average power) The power does its work transforming into other kind of energy in the unit of Watt, the Y-axis represents reactive power which oscillates back and forth in the system without doing work or transforming into other kind of energy, the unit of reactive power is VAR). The longest vector is apparent power S (the unit is VA). φ is the phase difference between voltage and current. Its cosine value is known as the power factor. The relationship of these powers is shown as: [13]

$$S = \sqrt{P^2 + Q^2} \tag{2.7}$$

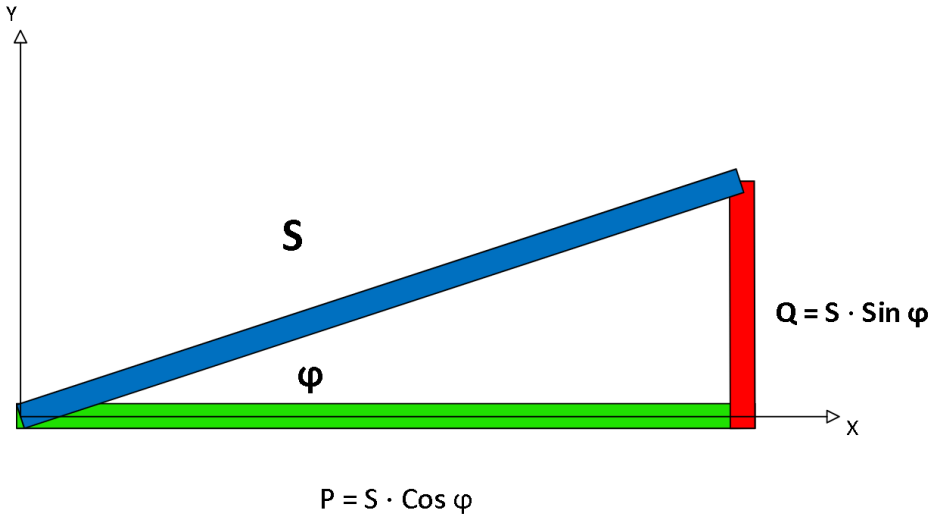


Figure 2.12: *Power triangle.*

2.7 PID control

In the modular multilevel converter with PWM scheme, a discrete PID controller is used to regulate the SOC of the battery of the sub-module closer to the average SOC so that the converter-based balancing method can be implemented in the simulation. In parallel mode, the formula to derive PID output is defined as follows:

$$PID\ output = k_p \cdot e(t) + k_i \int_0^t e(t)dt + k_d \cdot \frac{de(t)}{dt} \tag{2.8}$$

where $k_\mathrm{p}, k_\mathrm{i}, k_\mathrm{d}, e(t)$ are proportional gain, integral gain, derivative gain, current control error respectively. The proportional part is proportional gain times current control error $e(t)$. The integral part is integral gain times integral of control error $\int_0^t e(t)dt$ which is the accumulation of past error. The derivative part is derivative gain times $\frac{de(t)}{dt}$ which shows the slope of changing error. [14]

A higher proportional gain can bring faster response time but it also brings oscillations near steady state because the controller is always saturated with high gain of error either overshooting or undershooting the stable state. However, if the proportional gain is too small, the system may end up with a steady state error. Introducing an integral term can resolve steady state error but a high integral gain can also result in instability because normal fluctuation gets exaggerated. If the gain on the integral part is too small, it would take a long time to get to the stable state. A derivative term can help to correct the controller from overshooting or undershooting. But high gain on the derivative term can make output stumble.

When using PID controller to balance individual cells like the mechanism shown in Figure 2.13, the output of PID controller is in phase with reference voltage U_smref, changing active power of the battery cell changes while keeping the reactive power to zero.

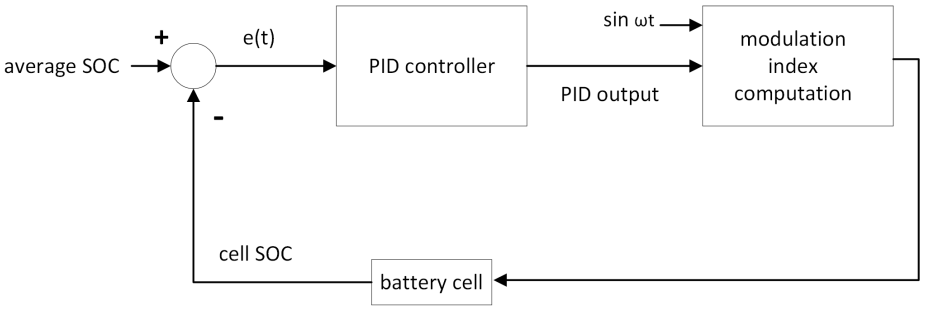


Figure 2.13: *Closed loop feedback mechanism.*

2.8 FFT analysis and harmonics performance

This section is about Fast Fourier transform (FFT) analysis and how harmonics performance is measured. FFT can decompose a signal in time domain into components with different amplitudes in frequency domain by approximating the original signal with an infinite sum of sinusoidal functions with various frequencies. The Fourier expansion looks like this:

$$f(t) = a_0 + C_1 \cdot \sin(\omega t + \phi_1) + C_2 \cdot \sin(2\omega t + \phi_2) + \dots \tag{2.9}$$

where a_0 is an offset, $C_1, \dots C_n$ is the amplitude of decomposed sinusoidal component.

Figure 2.14 shows a FFT analysis window from Simulink. Five cycles of the step signal (sum of Boolean values derived from the comparison between reference sinusoidal wave and constants) is sampled and marked with red in time domain in the upper plot. The decomposed components in frequency domain are shown in the lower plot. The dominant component in 50Hz is called the component of fundamental frequency. When this component is normalized by the peak of original sinusoidal signal (six in this case), it is 92.2978% of the original signal. The peak of six means six sub-modules are inserted at maximum.

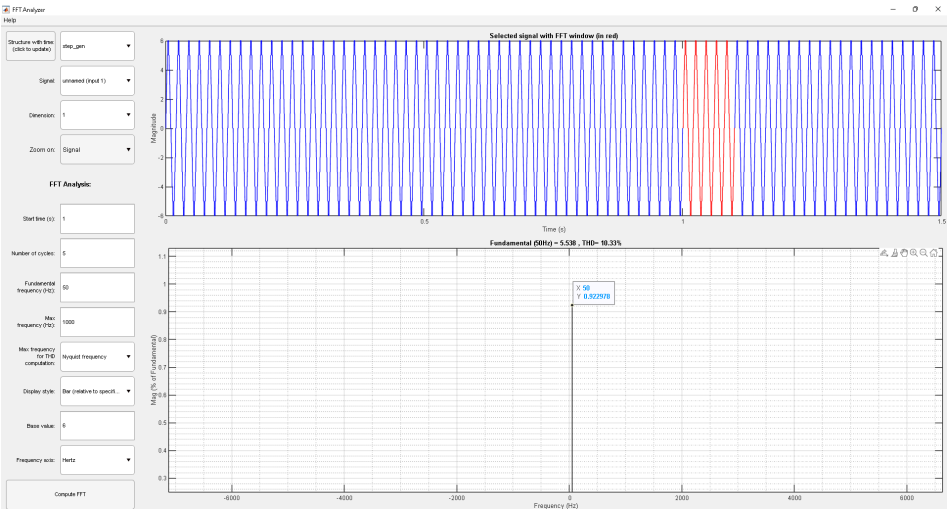


Figure 2.14: *FFT analysis on step signal in the NLM setup from Simulink window.*

When calculating battery current harmonics, the DC component and the fundamental frequency component are needed to be removed. The value also needs to be transformed into RMS value and to be summed up because the signal is sinusoidal and the sum of these decomposed components reflects the amplitude of

the harmonics. The variables needed for FFT analysis are saved into workspace and a Matlab file called $harm_proc.m$ is used for the analysis. The script is shown in appendix C.2.

3

Method

Since the scope of the thesis is about a single-phase MMC, the MMC setup shown in Figure 2.1 is adjusted to a single-phase MMC with only six sub-modules connected in a series for simplicity, as shown in Figure 3.1. Depending on usage of PWM pattern or of NLM pattern, some other components are added to achieve converter-based cell-balancing control, which is shown in details in the corresponding subsections in this chapter.

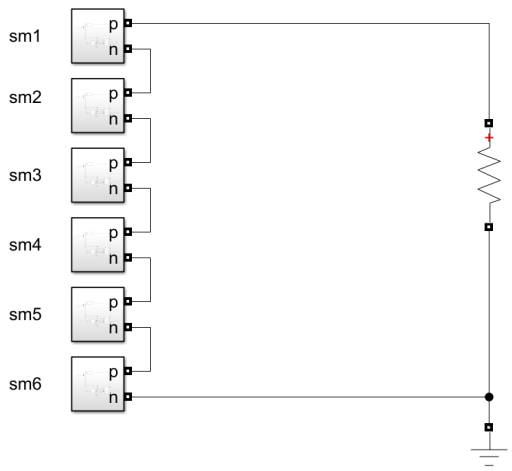


Figure 3.1: *Generic model for a single-phase MMC with six sub-modules. (SM: sub-module)*

3.1 Battery cell

The battery cell used in the sub-modules is a 28 Ah Lithium-Ion battery with 3.6 V as nominal voltage. With response time of 30 seconds, its discharging characteristics are shown in Figure 2.4. Battery cell's response time reflects its voltage dynamics. Response time is measured from the time when a discharge current step returns to zero to the time when battery voltage recovers 95 % of voltage changes.[15]

Parameters of battery cells (shown in Figure 3.2) in six sub-modules are the same except initial state of charge (SOC): the battery cell in sub-module 1 has highest SOC (90.06 %, as set in the parameter shown in section C.1) while the battery cell in sub-module 6 has lowest SOC 90.01 %. Boxes of simulating temperature and aging effects are unchecked because modeling these effects are out of the scope of this thesis work.

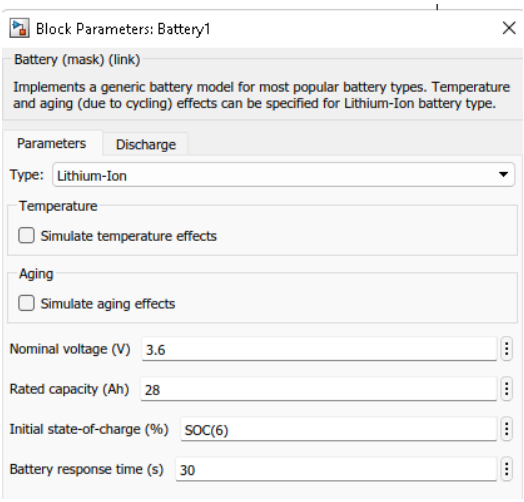


Figure 3.2: *The battery cell used in sub-modules*

3.2 PWM balancing strategy

The master system outputs sinusoidal waveform U_{smref} of $\frac{20.5}{6}$ V and phase ωt for each sub-module. 20.5 serves as the peak of reference signal. The value is determined by tests with different constants in which setting the peak of 20.5 can have similar magnitude on 50Hz component from AC output voltage of PWM setup (Modular Multilevel Converter controlled by PWM pattern) with magnitude on 50Hz component from AC output voltage of NLM setup (Modular Multilevel Converter controlled by NLM pattern) after all six sub-modules are balanced (PID offset becomes stable). Such sinusoidal reference signal of peak of 20.5 needs to be divided by six for six sub-modules.

In slave controller system, a PID controller determines an offset aiming to get the SOC values of all sub-modules equal. The offset is calculated with the equation (3.1):

$$U_{\text{ref}} = \frac{U_{\text{smref}} + \sqrt{2} \cdot PID\_output \cdot \sin(\omega t)}{U_{\text{batt}}} \tag{3.1}$$

where U_{ref} is the input to the block `PWM Generator (Multilevel)` and U_{batt} is the voltage of battery cell. The amplitude of U_{ref} serves as modulation index m_{a} of PWM pattern for the specific battery cell.

The loss at the converter is assumed to be negligible, AC power should be equal to the DC power, according to power balance:

$$U_{\text{sm}} \cdot I_{\text{sm}} \cdot \cos(\phi) = U_{\text{batt}} \cdot I_{\text{batt}} \tag{3.2}$$

where $U_{\text{sm}}, U_{\text{batt}}, I_{\text{sm}}, I_{\text{batt}}, \cos(\phi) and \phi$ are the output voltage of the sub-module, the voltage of the battery cell, the current flowing through the sub-module, the current flowing through the battery cell, power factor and the phase difference between the sub-module's current and output voltage respectively.

U_{sm} is substituted by the equation:

$$U_{\text{sm}} = \frac{U_{\text{batt}} \cdot m_{\text{a}}}{\sqrt{2}} \tag{3.3}$$

Where divisor $\sqrt{2}$ is added because U_{sm} is RMS value. Then the relationship of the current flowing through the battery cell and the current flowing through the sub-module can be obtained:

$$I_{\text{batt}} = \frac{I_{\text{sm}} \cdot m_{\text{a}} \cdot \cos(\phi)}{\sqrt{2}} \tag{3.4}$$

Based on equation (3.4), a sub-module having higher modulation index m_{a} because of positive output of PID controller would have more current drawn from the battery cell, which drives down its SOC value.

3.3 PWM implementation

Based on the generic MMC model with six sub-modules, a master controller is added into the PWM setup (Modular Multilevel Converter with PWM scheme) together with components inside sub-modules and other components for measurement that are hidden for simplicity in Figure 3.3. Master controller sends phase signal ωt and reference voltage level U_{smref} to slave controller inside each sub-modules.

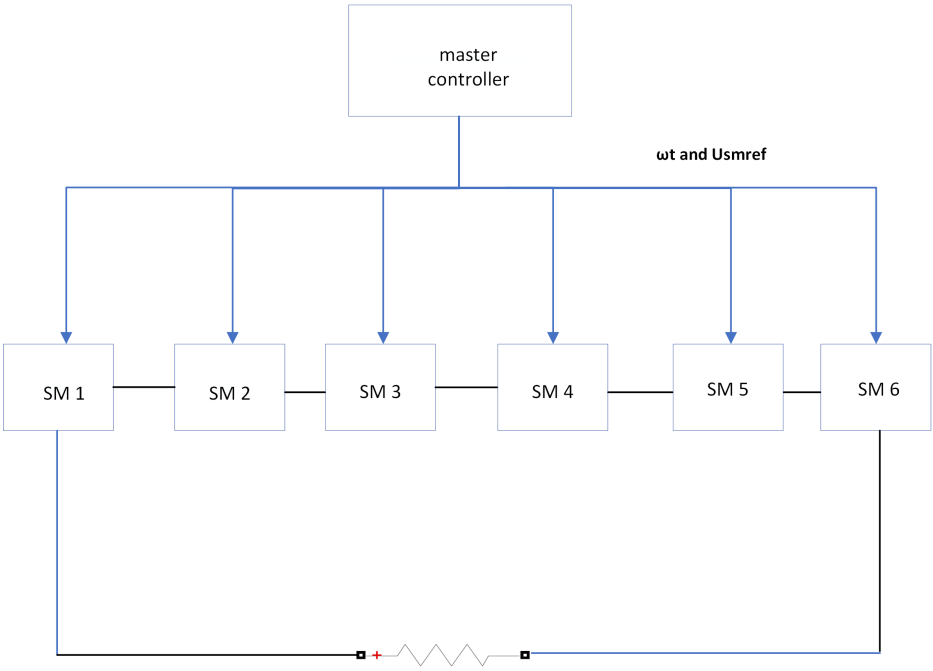


Figure 3.3: *PWM setup. (SM: sub-module)*

3.3.1 Master controller

As shown in Figure 3.4, the master controller sets the peak of reference voltage $U_{\text{smref}} = \frac{20.5}{6}$ V and sinusoidal reference signal for six sub-modules (namely, ωt to determine the frequency of the signal).

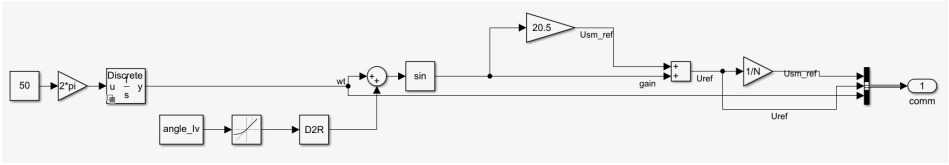


Figure 3.4: *Master controller in PWM setup.*

3.3.2 Sub-module

A sub-module is consisted of a battery cell as a DC voltage source, a full-bridge converter and a slave controller system as shown in Figure 3.5.

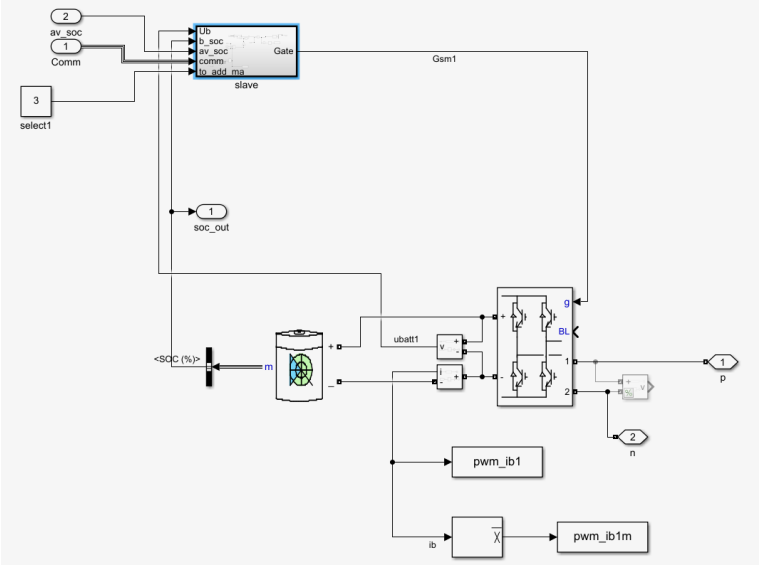


Figure 3.5: *Sub-module in PWM setup.*

3.3.3 Slave controller

In the slave controller system shown in Figure 3.6, a PID controller determines an offset based on the input of SOC difference between SOC of the battery cell and the average SOC. Proportion gain is used to make sure that the offset is large enough for the balancing process. Derivative term is used to prevent the output of the controller from either overshooting or undershooting. The saturation of PID controller's output is limited to be 0.1, corresponding to adding/subtracting 0.1 V to modulation index in equation (3.1), because modulation index of PWM cannot exceed one (100%). If the input to the block *"PWM generator (Multilevel)"* (the modulation index signal in Figure 3.6) exceeds one, which it shouldn't, then the block will saturate it to one (100%) deteriorating harmonics performance.

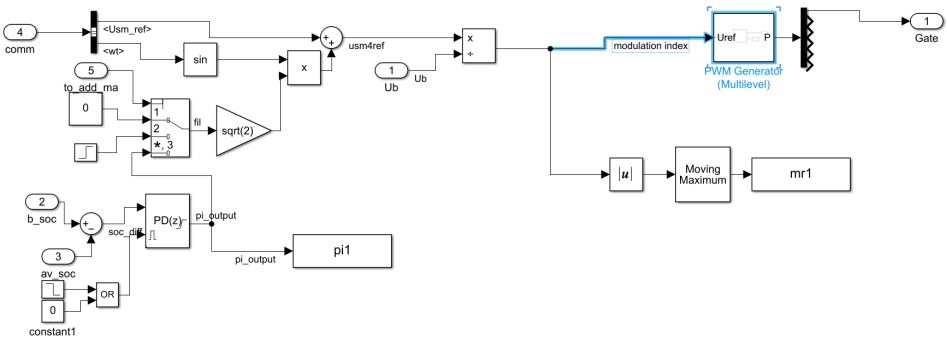


Figure 3.6: *Slave controller in PWM setup.*

3.4 NLM balancing strategy

As illustrated in section 2.5, NLM allows to control sub-modules at twelve operations points . By inserting sub-modules or bypassing them at those specific incidents (twelve operation points) given by the reference step signal, the output current and voltage of a MMC can be sinusoidal.

Initial SOC values set for six sub-modules of MMC with NLM pattern are the same as the PWM setup. SOC difference is distributed evenly over six sub-modules from 90.06 % in sub-module 1 to 90.01 % in sub-module 6, with 0.01 % difference between neighbouring sub-modules. Given extra freedom to control the output of these sub-modules, a different control strategy is proposed.

The balancing process starts with sorting SOC values from each sub-module in a descending order. SOC value in the middle of the ranking (the 3rd, 4th highest SOC value) are used to create a reference band called *'SOC balancing band'* for the master controller to change duty cycles for six sub-modules so that other sub-modules having SOC outside the reference band can eventually have their SOC inside the band. The master controller changes six sub-modules' duty cycles by offering different pre-set patterns which would be discussed in details in section 3.4.3. The relationship between control cases number in master controller (to which pre-set patterns are corresponding) and six sub-modules' duty cycles is shown in the 2nd and 3rd plots of Figure 3.7. Finally, swapping different duty cycles among sub-modules so that the gap of the reference band created by the difference of the 3rd, 4th highest SOC value can be driven narrower, as shown in Figure 3.8. Therefore, SOC of sub-modules are kept within a certain range. In section 3.6.1, a universal criterion for both the MMC with PWM and NLM on sub-modules being balanced is proposed.

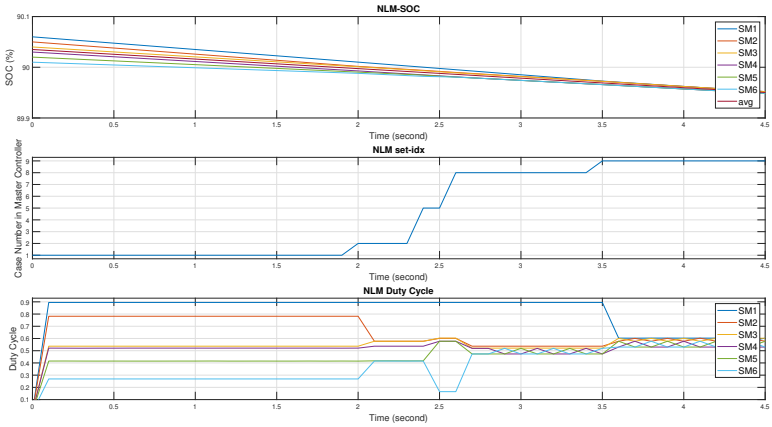


Figure 3.7: *SOC vs set_ idx vs duty cycle in NLM setup.*

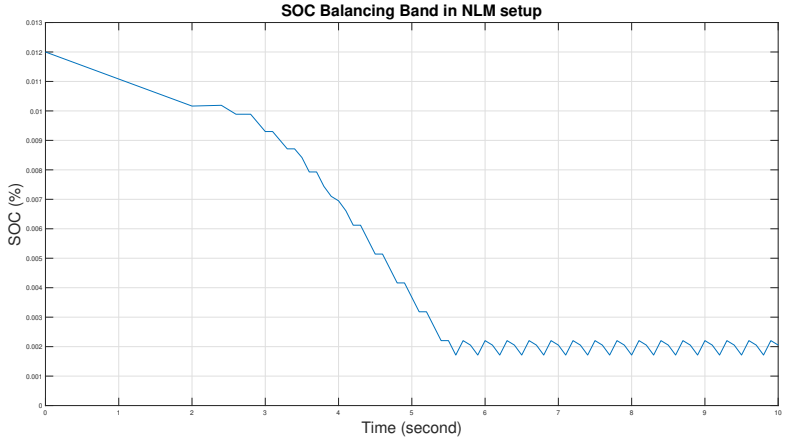


Figure 3.8: *'*SOC balancing band*' in NLM setup.*

3.4.1 Sorting subsystem, VSM and *'SOC balancing band'*

Given more freedom to control the sub-modules, more information about them is needed for balancing control, such as SOC rankings of every sub-module, sum of sub-modules of the same SOC status. SOC values of the battery cell from each sub-module would be sorted in a descending order by a sorting subsystem. Virtual sub-modules (VSM) refers to the physical sub-modules with SOC in descending order. `VSM 1` represents the physical sub-module with highest SOC value while `VSM 6` represents the physical sub-module with lowest SOC value. It's necessary to have these conceptual sub-modules because the SOC value of each physical sub-module changes over time and `VSM 1` always refers to the sub-module with highest SOC.

SOC value sorted in descending order would be used as reference for balancing control. A band called *'SOC balancing band'* is used as an reference. The bandwidth of *'SOC balancing band'* is determined by the SOC value in the middle of ranking. For example, six sub-modules are used in the simulation, the 3rd, 4th highest SOC value (from sub-module 3 and 4 at the beginning of the simulation, as set in section C.1) would be used to create the band based on the following equation:

$$SOC\ balancing\ band = (SOC_{VSM3} + 1e^{-3}) - (SOC_{VSM4} - 1e^{-3}) \tag{3.5}$$

where the value of $1e^{-3}$ serves as added tolerance for the band.

3.4.2 Summing subsystem and nine SOC cases

The summing subsystem in the MMC with NLM pattern is responsible for summing up sub-modules that are inside or above the *'SOC balancing band'* so that nine potential SOC cases are identified in the Table 3.1. As setting on sub-modules' initial SOC values, there are two sub-modules above the *'SOC balancing band'* (sub-module 1 and 2), two sub-modules inside the band (sub-module 3 and 4) and two sub-modules under the band (sub-module 5 and 6) at the beginning. So the simulation starts with case 1.

These nine cases serve as conditions to switch between nine corresponding pre-set patterns in the master controller. These pre-set patterns control when to insert or to bypass sub-modules at twelve operations. Different patterns used by the master and different parts of the pattern taken by the slave controller of a sub-module would affect the duty cycle of the sub-module's output voltage as shown from Figure A.1 to A.9.

Case	Number of sub-modules above the band	Number of sub-modules inside the band	Number of sub-modules under the band
1	2	2	2
2	1	3	2
3	2	3	1
4	0	4	2
5	1	4	1
6	2	4	0
7	0	5	1
8	1	5	0
9	0	6	0

Table 3.1: *A table of nine potential SOC cases.*

3.4.3 Nine pre-set pattern generation

In order to keep output AC voltage of the MMC (consisted of six sub-modules) sinusoidal, a sub-module must be inserted at one of six operation points and be bypassed at one of another six operation points at half positive period, as illustrated in section 2.5. Since a operation point is only available for a sub-module at a period, it would be better to numerate all the possibilities for selection as shown in Figure 3.9. Blocks of the same row indicates the same operation point to insert a sub-module. For example, blocks of the 2nd row means inserting a sub-module at operation point six. Blocks of the same color indicates the same operation point to bypass a sub-module. For example, yellow blocks mean bypassing a sub-module at operation point seven.

If a sub-module in the MMC is given a block, other sub-modules have to choose another block that is of different colors and different rows. For example, if sub-module 1 is given yellow block 1;7, then it means the sub-module is inserted at operation point 1 (positively inserted on positive half period, negatively inserted on negative half period) and get bypassed at operation point 7. Since operation point 1 and 7 are occupied by sub-module 1, other sub-modules have to choose blocks from rows other than 1 (different operation points to insert) and of different color (different operation points to get bypassed). The top row indicates resulting duty cycles of the gate pulses generated.

Because operation points at the negative half period is just the operation points from positive half period with 180 phase shifted, the table is also applicable to negative half period. For example in figure 2.11, a sub-module is inserted positively at the 1st step in the rising edge of positive half period (operation point 1). At the 1st step of falling edge of negative half period (operation point 1 with 180 degree shifted), the same sub-module would be inserted negatively. The AC output voltage of MMC with sub-modules controlled by these nine pre-set patterns

are shown in Figure A.1 to A.9

Principles to select duty cycles for each sub-modules:

- priorities are given to sub-modules which are already inside *'SOC balancing band'*, they should be given similar duty cycles.
- sub-modules having battery SOC value above SOC balancing band should be given higher duty cycle.
- sub-modules having battery SOC value under SOC balancing band should be given lower duty cycle.

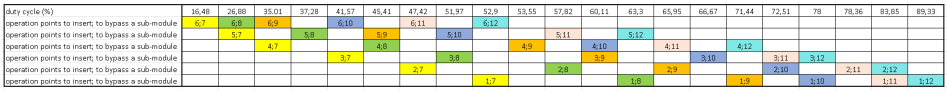


Figure 3.9: *Duty cycle selection for sub-modules.*

3.5 NLM implementation

Arrows indicate signals in the Figure 3.10. Sub-modules send SOC value of the battery cell and the SOC status (above/inside/under the *'SOC balancing band'*) to sorting and summing subsystems. These subsystem return SOC ranking and values of 3rd and 4th highest SOC for definition of *'SOC balancing band'* to sub-modules every 0.1 second.

Based on information from sorting and summing subsystem about numbers of sub-modules above or inside the *'SOC balancing band'*, the master controller is generating control signal in an order of descending SOC values (`VSM 1` to `VSM 6`, `VSM 1` refers to the sub-module with highest SOC). The slave controller of each sub-module takes this control signal according to its SOC ranking, for example if sub-module 3 has the highest SOC ranking, then it will take the control signal of `VSM 1`.

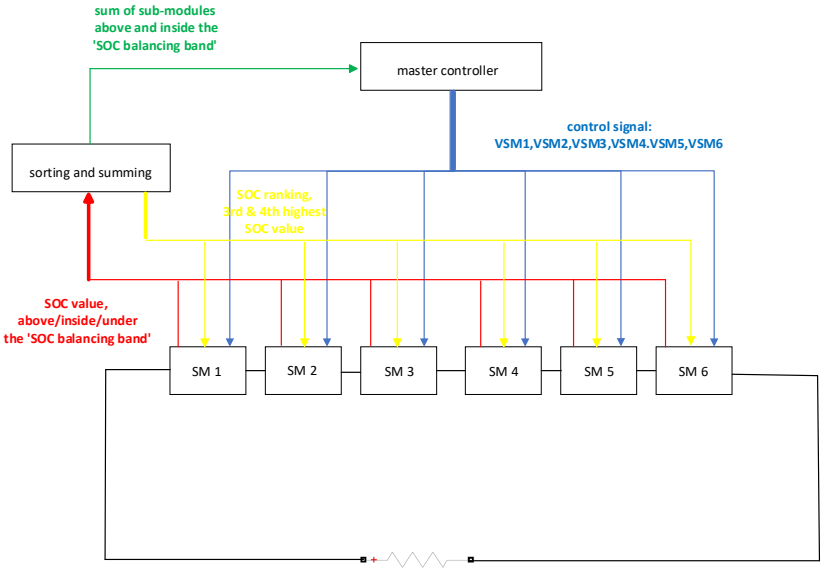


Figure 3.10: *NLM setup. (SM: sub-module)*

3.5.1 Summing and ranking system

Summing and ranking subsystem run in parallel, scanning SOC of the battery from each sub-modules every 0.1 s. These two subsystems are called by separative function call generator. The ranking system contains a sort block. It sorts SOC status in descending order. The sorted value of SOC is used to create *'SOC balancing band'* to which other sub-modules whose SOC is above or under it are controlled to approach.

The summing block sums up how many sub-modules are above or inside *'SOC balancing band'* and sends the result to master controller system.

3.5.2 Master controller system

The master controller system in MMC with NLM scheme is responsible for generation of sinusoidal reference signal, a step signal with falling edge indication and for outputting one of nine pre-set NLM gate switching patterns for all six sub-modules in the setup based on input of summing information from the summing system.

As shown in Figure 3.11, a Matlab function in the master controller system gives the index for one of nine potential schemes according to input of summing information and the multi-port does the switching between different cases. The control signal outputted from the multi-port containing gate switching pulses is called *from_master*. It is later handled in the slave controller in each sub-module.

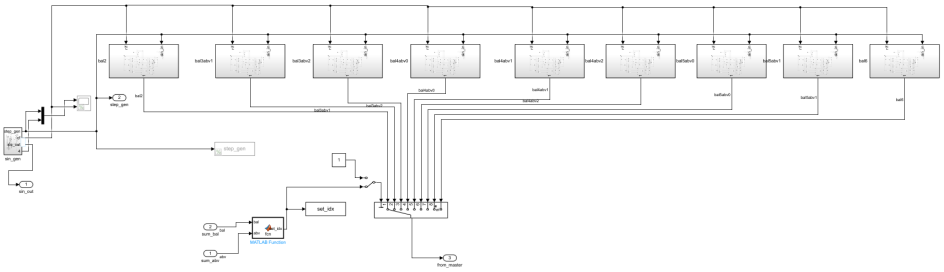


Figure 3.11: *Master controller in NLM setup.*

3.5.3 Slave controller

As shown in Figure 3.12, there are a Matlab function, a multi-port switch and some add blocks inside a slave controller. These add blocks determine that the SOC situation of the battery cell from the sub-module this slave controller is controlling is above or inside or under *'SOC balancing band'*. Such information is reported to master controller system. When the slave controller receives the control signal *from_master*. The Matlab function in a slave controller takes corresponding gate pulses for the converter connected to the slave controller based on SOC ranking of the battery cell. Since control signals from master controller is in SOC descending order(fixed, combined signals for `VSM 1`, `VSM 2` ... `VSM 6`, `VSM 1` corresponds to actual sub-module having highest SOC while VSM6 corresponds to actual sub-module with lowest SOC), the Matlab function is also used for choosing the correct control signals from master controller based on sub-module's SOC ranking besides sending situation of SOC state.

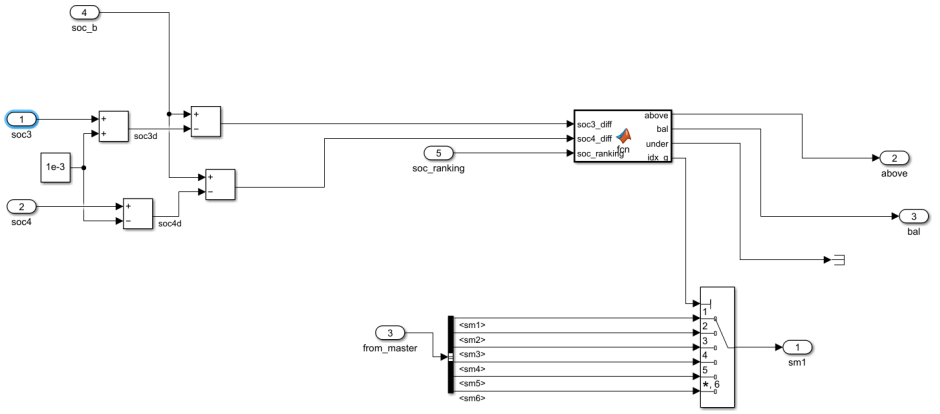


Figure 3.12: *Slave controller in NLM setup.*

3.6 Performance measurement

3.6.1 Speed to get balanced

'balanced criterion band' is used as the universal criteria for sub-modules being balanced in both PWM and NLM setup. It is created by adding ±0.002% to the average SOC value. Once SOC of a sub-module is inside the band (less than or equal to ±0.002% from the average SOC value), the sub-module is considered to be balanced. Its corresponding balancing indication will turn to one. Since the criterion is the same for both setups, the time it takes for the indication turning one demonstrates the setup's ability to balance these six sub-modules with the same SOC difference setting.

3.6.2 Battery current harmonics measurement

Battery current harmonics is important to measure because higher battery current harmonics can age the battery cell more quickly by inducing inhomogeneous current and resulting uneven heat distribution.

Last 20,000 samples (corresponding to a duration of 0.2 second when simulation is run in discrete step time of $1e^{-5}$) of DC currents flowing through the battery cells in the two setup are saved to workspace at each time step with maximum data resolution. By running *harm_proc.m file* to call function *fft_cal*, values of battery current are transformed and decomposed from time domain to components in frequency domain. The function *fft_cal* returns RMS value of harmonics of each sub-modules (DC and fundamental components are removed). The *harm_proc.m file* also plots a figure of all components (including DC, fundamental and harmonics components) from all six sub-modules under the same setup.

4

Result

This chapter presents results from balancing method implemented with PWM and NLM scheme. SOC values, battery current harmonics and electrical parameters like: AC output voltage, mean DC current and output power are shown.

4.1 SOC lines and balanced indicators

From Figure 4.1 and 4.2, all sub-modules from both PWM and NLM setup reach similar SOC values when 80-second simulation ends. Both two setups can balance six sub-modules within 80 seconds simulation and the balanced status is kept until the simulation ends. Under the same criterion of being balanced, the NLM setup can balance all six sub-modules within first 10 seconds, much faster than PWM setup, as shown by indicators in Figure 4.3 and 4.4.

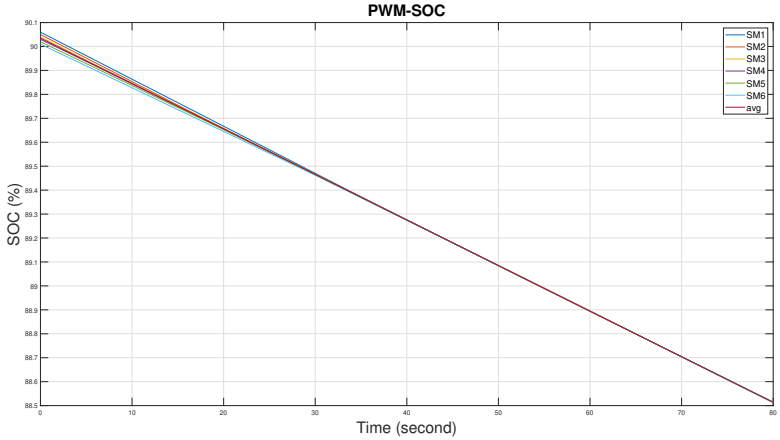


Figure 4.1: *SOC of sub-modules in PWM setup.*

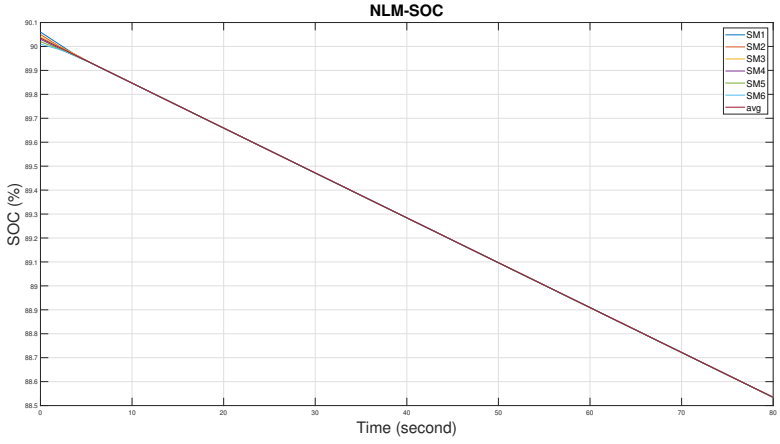


Figure 4.2: *SOC of sub-modules in NLM setup.*

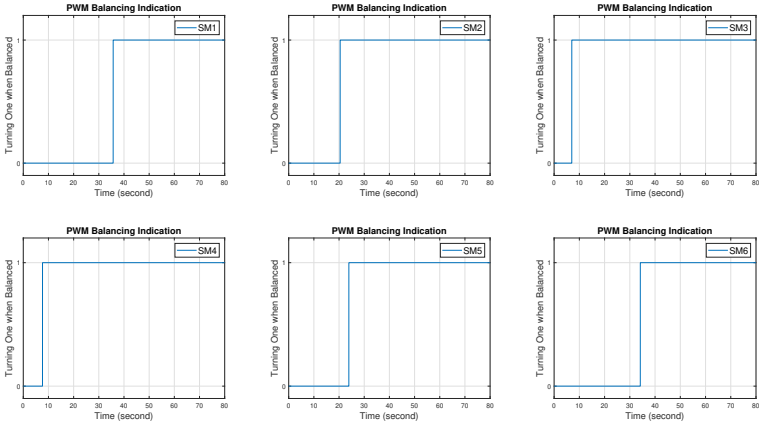


Figure 4.3: *Balancing indicators in PWM setup.*

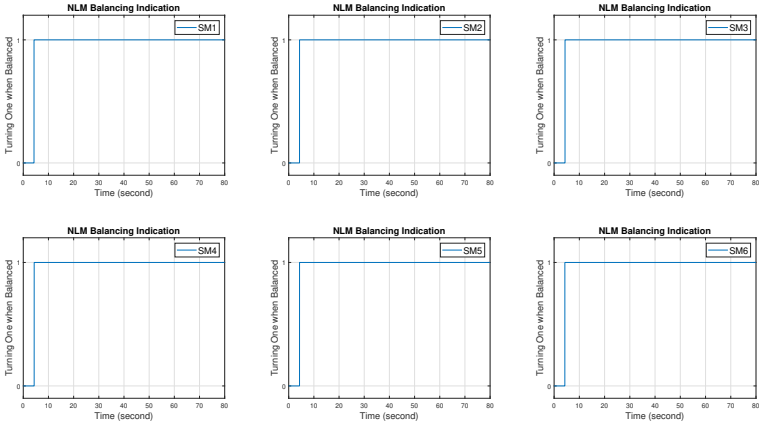


Figure 4.4: *Balancing indicators in NLM setup.*

4.2 Modulation index in PWM and duty cycle in NLM

It is reasonable to compare modulation index in PWM setup to duty cycle in NLM setup because MOSFETs of full-bridge converter in PWM setup switch 40 times per period of AC output voltage (50 Hz) and MOSFETs only switch at 50 Hz in NLM setup.

Changes of modulation index in PWM setup are shown in Figure 4.5. At the beginning, the output of the PID controller is saturated for sub-module 1, 2, 5 and 6 thus, sub-module 1 and 2 have the same highest modulation index and sub-module 5 and 6 have the same lowest modulation index. As balancing process goes on, the SOC difference is decreasing, modulation index of six sub-modules get closer to each other and eventually becomes stable.

Changes of duty cycle in NLM setup are shown in Figure 4.6. Before getting balanced, six sub-modules get different duty cycles from one of nine pre-set cases determined by the master controller which receives information about how many sub-modules are within or above the *'SOC balancing band'*. As balancing process progresses, different cases are applied to these sub-modules, resulting changes on duty cycles. After six sub-modules reach inside *'SOC balancing band'*, corresponding case (case 9, according to Table 3.1) is executed. Since SOC values are similar for six sub-modules when they are inside the band(as shown in the previous section) and SOC ranking affects the duty cycle a sub-module would take from the control signal *from_master*, these sub-modules start to swap duty cycles with each other, since around 10 second.

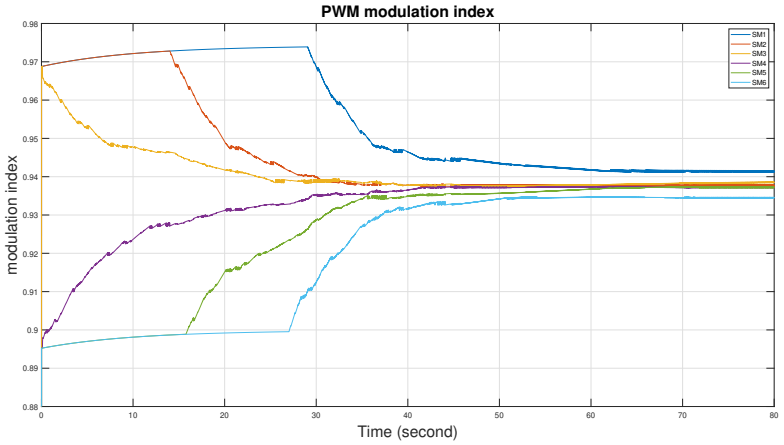


Figure 4.5: *Modulation index in PWM setup.*

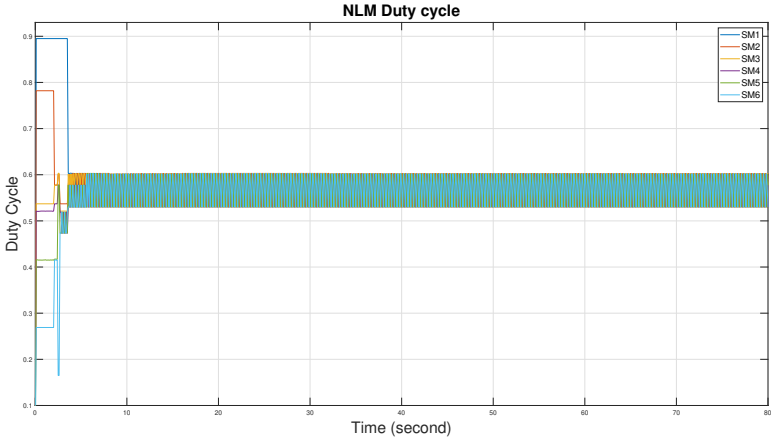


Figure 4.6: *Duty cycle in NLM setup.*

4.3 Mean DC current

For the PWM setup, mean DC current is more related to modulation index because duty cycle changes depending on the time when reference signal is compared by the triangle carrier wave but duty cycles in a whole fundamental period (0.02 s when 50 Hz) reflects modulation index. Changes of mean DC current in PWM setup is shown in Figure 4.7. As modulation index of sub-module 1, 2, 5 and 6 are constant at the beginning of the simulation, their mean DC current are thus kept on a level until SOC difference is no longer large enough to saturate the output of corresponding PID controller. Once the offset from PID controllers of six sub-modules reach zero around 60 second as shown in Figure 4.8, mean DC current of six sub-modules converge because modulation index is similar (according to equation 3.1).

For the NLM setup, patterns of DC current are similar to those in duty cycle because duty cycle directly determines the DC current. Changes of mean DC current in NLM setup is shown in Figure 4.9.

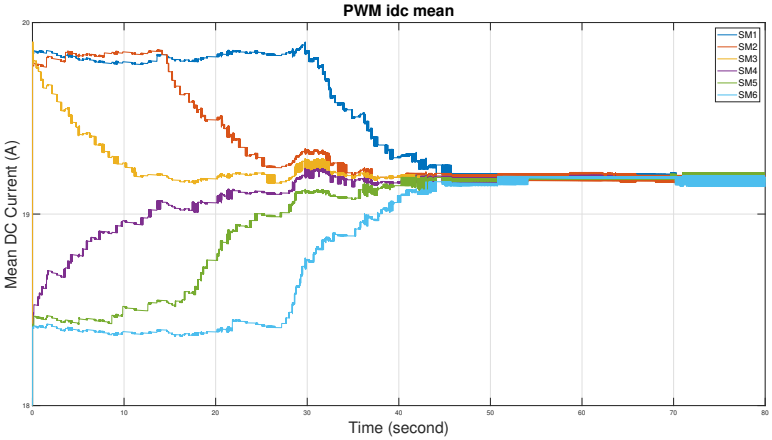


Figure 4.7: *Mean DC current in PWM setup.*

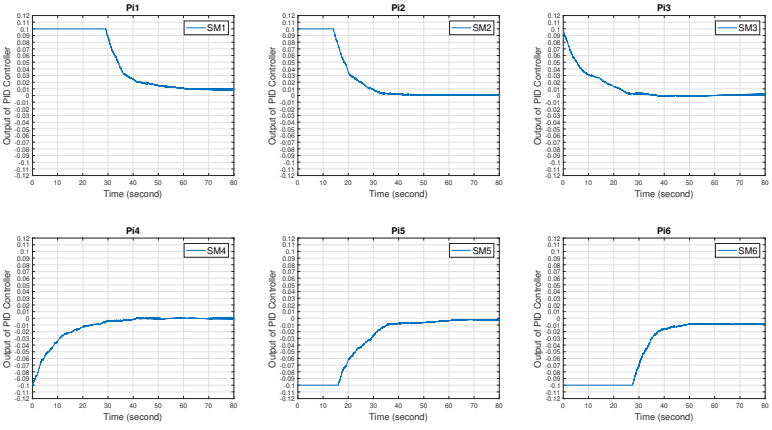


Figure 4.8: *Output of PID controllers from six sub-modules.*

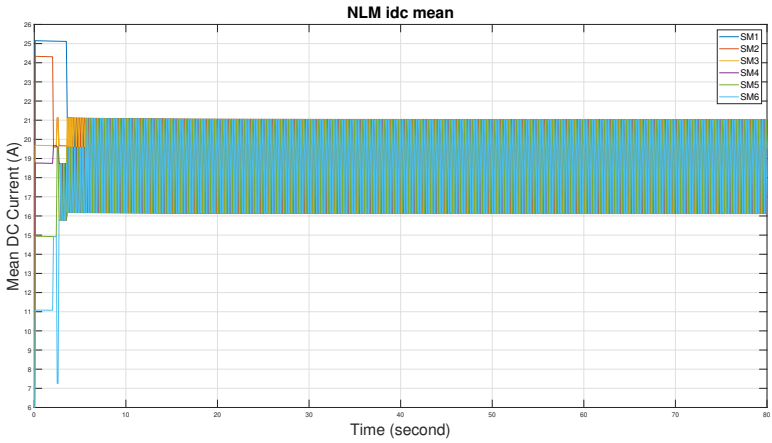


Figure 4.9: *Mean DC current in NLM setup.*

4.4 Output AC voltage in RMS value and output power

To have fair comparison for both Modular Multilevel Converters (one with PWM pattern, the other one with NLM pattern), it is important to have the same AC output voltage in RMS so that the situation of the load (a resistance of 0.5Ω connected) is similar. As seen in the final 10 s (70 to 80 s) of the simulation from Figure 4.10 and 4.12, the RMS output voltage of MMC with PWM is 14.51 V while the NLM counterpart is 14.4 V.

Since the load connected to both MMCs is only a resistance of 0.5Ω, the pattern of output power is similar to its AC output voltage. For the PWM setup, output power fluctuates between 419 and 423 Watt until the offsets added by PID controllers turn zero around 60 second as shown in Figure 4.11. Since then, the output power gets stable approximately 421 Watt. As shown in Figure 4.13, the output power of the converter with NLM pattern starts to decrease at the beginning, the slope of decrease slows down as its output voltage slow down because balancing control increases utilization of sub-modules with higher SOC and decreases utilization of sub-modules with lower SOC.

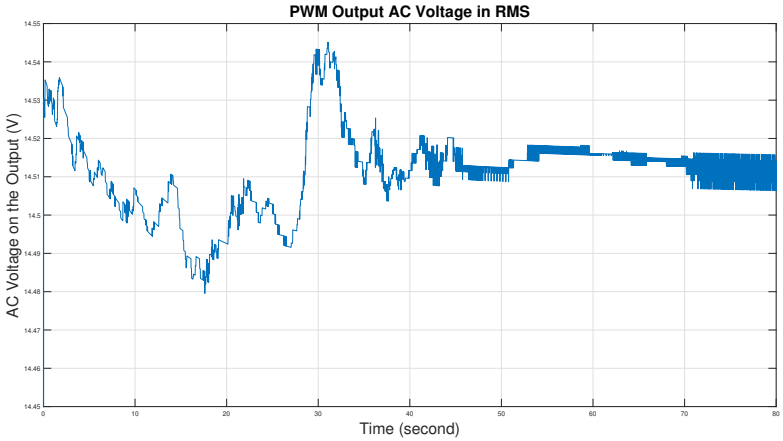


Figure 4.10: *Output AC voltage in RMS value from PWM setup*

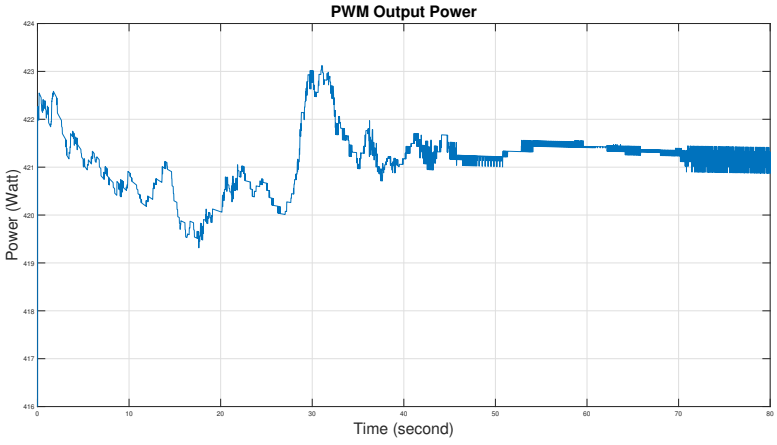


Figure 4.11: *Output power from PWM setup.*

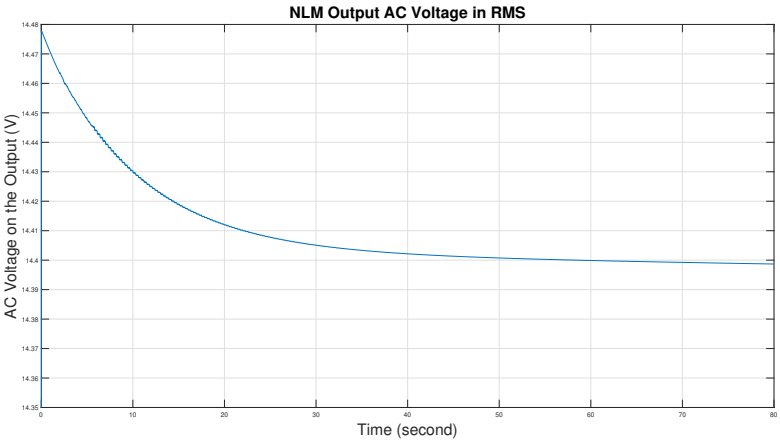


Figure 4.12: *Output AC voltage in RMS value from NLM setup.*

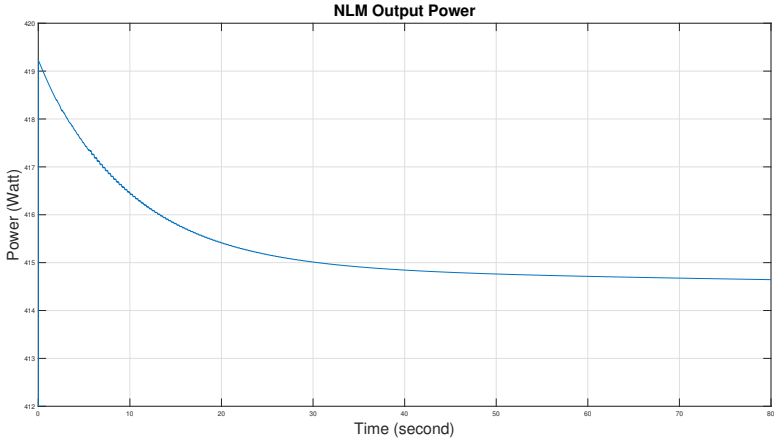


Figure 4.13: *Output power from NLM setup.*

4.5 Pre-set patterns, *'SOC balancing band'* and *'balanced criterion band'*

For NLM setup, the changes of pre-set patterns controlling all gate pulses of six sub-modules are shown in Figure 4.14. Figure 4.15 shows starting from the beginning of the simulation, the width of *'SOC balancing band'* drops overtime thanks to these changes of pre-set patterns. Once SOC values of all six sub-modules are inside the *balanced criterion band*, conditions of case 9 is fulfilled, corresponding patterns on are generated. Sub-modules start to swap duty cycles with each other based on their SOC ranking, driving *'SOC balancing band'* narrower until the width of the band only fluctuates around its initial offset of 0.002% as defined in equation 3.5.

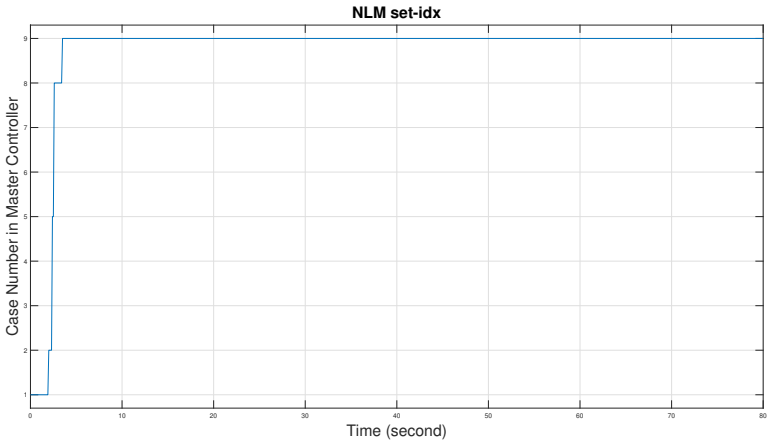


Figure 4.14: *Changes of pre-set patterns.*

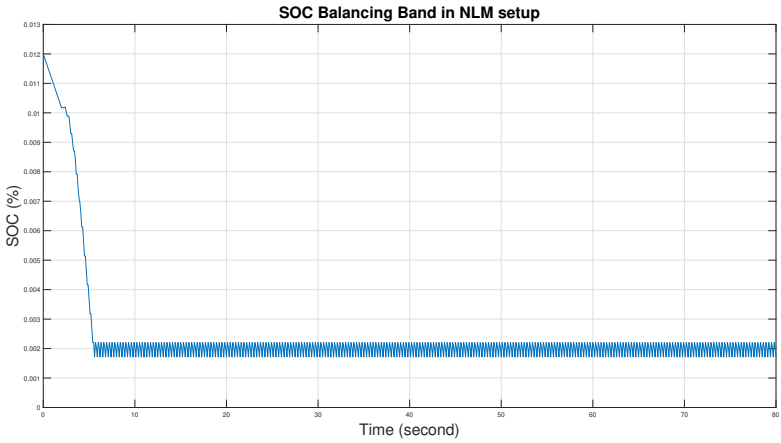


Figure 4.15: *Changes of* 'SOC balancing band'.

In addition, it is better to plot *'SOC balancing band'* and *'balanced criterion band'* for clarity. In Figure 4.16, the upper part shows *'SOC balancing band'* is outside the criterion band (none of any sub-module is balanced) at the beginning. At 78 second (at that time, the indication shows all six sub-modules are already balanced, according to the criterion), *'SOC balancing band'* is inside *balanced criterion band*.

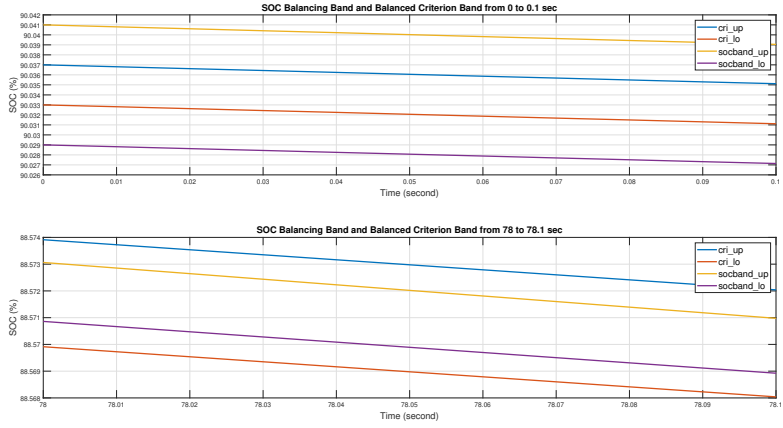


Figure 4.16: 'SOC balancing band' *and* 'balanced criterion band'.

4.6 Battery current harmonics

From Figure 4.17 to 4.19, the RMS values of battery current harmonics of each sub-module in PWM setup are shown. Besides components on DC and fundamental frequency(50Hz), there are spikes called sidebands around frequencies of even integers of switching frequency 2000 Hz.

From Figure 4.20 to 4.22, the RMS values of battery current harmonics of each sub-module in NLM setup under case 1 are shown. Harmonic components are mainly on low frequencies. The magnitude of these components soon become negligible above 2000 Hz.

In table 4.1, battery current harmonics of each sub-module and average current harmonic under different scenarios are shown. Scenario `NLM 1` corresponds to a 0.8 s simulation where MMC with NLM scheme operates with case 1. There are nine such simulations for nine different cases (from `NLM1` to `NLM9`) where control cases are set manually for the NLM setup. Scenario `PWM` corresponds to a similar 0.8 s simulation where MMC operates with PWM scheme. `NLM (80)` and `PWM (80)` correspond to a 80-second simulation where control cases selected automatically for NLM setup. All these battery current harmonics are measured by the last 20,000 samples (corresponding to a duration of 0.2 second when simulation is run in discrete step time of $1e^{-5}$).

Note that, since the NLM set up doesn't go through all nine cases in a simulation therefore, only in scenarios `NLM 1` and `NLM (80)` pre-set control cases are correctly used for the current SOC status. During the 0.8 s simulation, there are two sub-module with SOC inside *'SOC balancing band'* while others are outside the band, which only corresponds to case 1. In scenarios `NLM 2` to `NLM 9`, the same 0.8 s simulation run with cases manually set to 2 to 9 correspondingly. Control cases in these eight scenarios doesn't fit with SOC status. However, such measurement on battery current harmonics should still be sufficient. For scenario `NLM (80)`, results are measured by the last 20,000 samples of a 80 s simulation. By that time, all six sub-modules are balanced and case 9 is selected automatically, which means the control case matches SOC status.

With samples mentioned above, battery current harmonics in RMS are calculated using the method shown in section 3.6.2. For nine pre-set NLM cases, magnitudes of harmonics increase with duty cycles of the sub-module decrease. Case 1 to 9 in NLM setup basically have similar average battery current harmonics in RMS around 6.6 A. However, as balanced status is reached, sub-modules repeatedly swap duty cycles with each other causing changing current on the battery cells. As a result, average battery current harmonics in RMS is higher in scenario `NLM (80)`.

For PWM setup, average battery current harmonics in RMS is kept on the same level in both the 0.8-second simulation and of 80-second simulation.

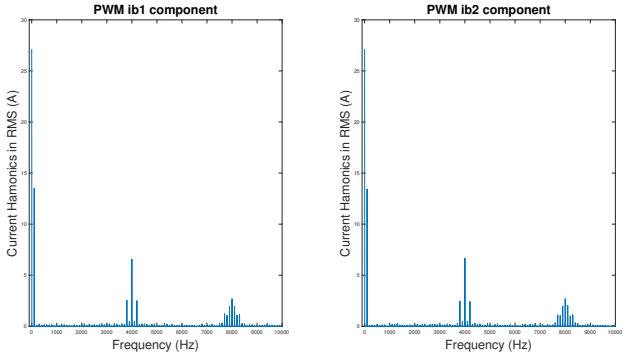


Figure 4.17: *Battery current components in sub-module 1 and 2 from the PWM setup.*

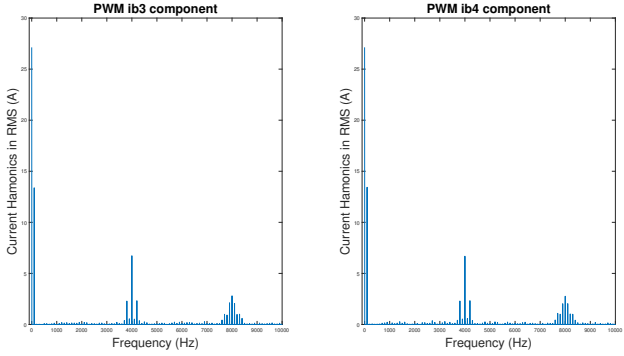


Figure 4.18: *Battery current components in sub-module 3 and 4 from the PWM setup.*

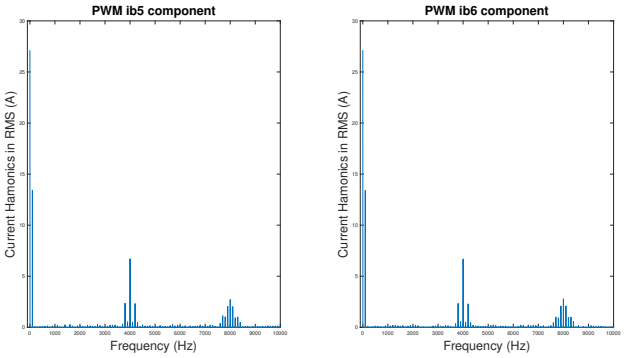


Figure 4.19: *Battery current components in sub-module 5 and 6 from the PWM setup.*

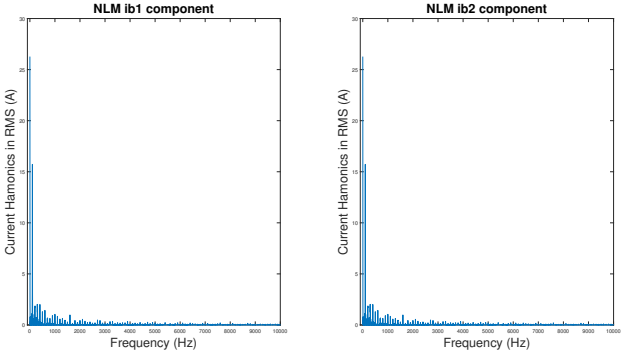


Figure 4.20: *Battery current components in sub-module 1 and 2 from the NLM setup.*

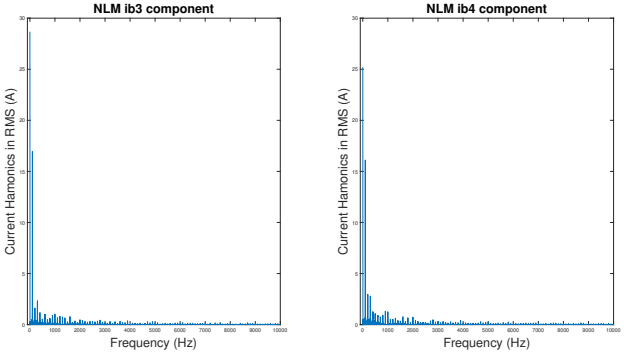


Figure 4.21: *Battery current components in sub-module 3 and 4 from the NLM setup.*

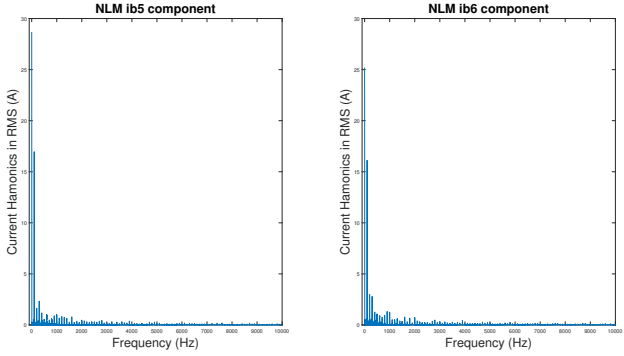


Figure 4.22: *Battery current components in sub-module 5 and 6 from the NLM setup.*

Table 4.1: *Battery current harmonics in RMS value (A).*

	SM1	SM2	SM3	SM4	SM5	SM6	Average
NLM1 (duty cycle)	3.2162 (89.33%)	3.9535 (78.36%)	6.0161 (53.55%)	6.6997 (51.98%)	8.9969 (41.57%)	11.9792 (26.88%)	6.8103
NLM2 (duty cycle)	3.2164 (89.33%)	6.3039 (57.82%)	6.3039 (57.82%)	6.0163 (53.55%)	8.9969 (41.58%)	8.9969 (41.57%)	6.6391
NLM3 (duty cycle)	3.2162 (89.33%)	3.9535 (78.36%)	6.0161 (53.55%)	6.6997 (51.98%)	6.6997 (51.97%)	13.0575 (16.48%)	6.6071
NLM4 (duty cycle)	4.3593 (72.52%)	4.3593 (72.51%)	4.9510 (71.44%)	4.9511 (71.44%)	9.6946 (37.28%)	13.0575 (16.48%)	6.8955
NLM5 (duty cycle)	3.2163 (89.33%)	5.2458 (60.11%)	5.2458 (60.11%)	6.3038 (57.82%)	6.3039 (57.82%)	13.0575 (16.48%)	6.5622
NLM6 (duty cycle)	3.2162 (89.33%)	3.9536 (78.36%)	7.7521 (45.41%)	7.7521 (45.42%)	8.9969 (41.58%)	8.9969 (41.57%)	6.7780
NLM7 (duty cycle)	4.6215 (66.67%)	5.0098 (65.95%)	5.0098 (65.96%)	6.2267 (63.31%)	6.2267 (63.30%)	13.0575 (16.48%)	6.6920
NLM8 (duty cycle)	3.2164 (89.33%)	6.0163 (53.55%)	6.6998 (51.98%)	6.6998 (51.97%)	8.3386 (47.42%)	8.3386 (47.42%)	6.5516
NLM9 (duty cycle)	5.2460 (60.11%)	5.2460 (60.11%)	6.3040 (57.82%)	6.3040 (57.82%)	8.1194 (52.91%)	8.1194 (52.91%)	6.5565
PWM	10.3515	10.4865	10.5812	11.9249	12.0552	12.0043	11.2339
NLM (80)	8.7755	8.7755	6.2192	7.9791	6.2192	7.9791	7.6579
PWM (80)	11.1377	11.2189	11.2757	11.2218	11.2147	11.2527	11.2203

5

Discussion

Based on the result from chapter 4, this chapter discuss advantages and disadvantages of implementing the converter-based cell balancing method on Modular Multilevel Converter with PWM and NLM scheme in the simulation. Dedicated subsections reviewing the active part of cell balancing mechanism: PID controller for PWM setup and switching of nine pre-set cases for NLM setup, are presented.

5.1 PWM setup

5.1.1 Result

In PWM setup, the balancing process is controlled by the modulation index equation (3.1). Outputs from the PID controllers offer different offsets to each sub-module based on their SOC value and parameter U_{smref} determines the level of AC output voltage when balancing process is finished.

The balancing speed of the PWM setup is mostly limited by the output saturation of PID controller inside the slave controller in each sub-module. Due to the limit set by the equation of modulation index calculation (3.1), the PID controller's output is saturated to 0.1 leaving a very small margin for balancing the SOC difference. The other way is to lower U_{smref}, resulting in lower AC output voltage of the setup (Modular Multilevel Converter controlled by PWM pattern) when sub-modules achieve the balanced state.

Mean DC current of sub-modules in the PWM setup is smoother than of NLM setup. At the beginning of the simulation, an offset (± 0.1, at maximum) by PID controller is added to modulation index on each sub-module thus, sub-modules 1

and 2 (positively saturated at time 10 second) have the same highest modulation index. Sub-modules 5 and 6 (negatively saturated at time 10 second) have the same lowest modulation index. Duty cycles viewed from a period (0.02 second, for 50 Hz) reflect the amplitude of modulation index. Duty cycles determines the time for which the battery cell is inserted (positively on positive half period of reference sinusoidal signal, negatively on the other half period) as part of the MMC structure. Therefore, higher modulation index results in higher mean DC current.

Once the SOC difference is balanced, the offset of PID controller becomes negligible. According to the modulation index equation (3.1), similar modulation index results in similar mean DC current and AC output voltage is determined mostly by U_{smref}. The AC output voltage in RMS stays around 14.51 V since then.

Shown in the Figure 4.17 to 4.19, having gate pulses `g1` and `g3` generated with two 180 degrees phase shifted reference sinusoidal wave (the unipolar way) via two legs of Full-bridge converter gives better current harmonics on PWM setup because output voltage being zero prevents output voltage sudden changing from $+U_{\text{batt}}$ to $-U_{\text{batt}}$ and the two complementary legs of the full-bridge converter makes current harmonics sidebands around odd integers of switching frequency (2000Hz) negligible. Nevertheless, the PWM setup still has higher harmonics on DC current and less efficient than the NLM counterpart due to much higher switching frequency on MOSFETs of the full-bridge converters (2000 Hz in PWM setup, 50 Hz in NLM setup). Note that efficiency analysis about these two setup is not included in this thesis work because it needs in-depth modelling on switching loss from specific MOSFETs rather than generic ones used here.

5.1.2 PID controller

Proportional gain of 30 and derivative gain of 80 are used. Ideally, proportional gain can be higher to achieve faster balancing result. The drawback of having higher proportional gain is the curve being too sensitive to normal minor fluctuations would be unstable causing either overshooting or undershooting. A proportional gain of 50 was investigated so that the output of the controller is kept saturated at 0.1 until the SOC difference between individual battery cells and the average SOC is less than ±0.002% (the same criterion for both PWM and NLM setup). Unlike the final result of PID output from the Figure 4.8, when proportional gain was set 50, the output of PID undershoots in the sub-module having 3rd highest SOC (one of the two sub-modules fastest to get balanced. The other is the sub-module with 4th highest SOC. They are closer to average SOC than other sub-modules). Adding high derivative gain can help ease the problem but makes the curve stumble and less stable. After fine-tuning, lowering the proportional gain to 30 and added with appropriate derivative gain help to achieve a better smoother curve shown in Figure 4.8. The integral term is not used in the PID controller because the SOC difference didn't experience steady-state error and

adding such term wouldn't help to achieve faster or smoother balancing result.

5.2 NLM setup

5.2.1 Result

In the NLM setup, the balancing control is done by utilizing different gate switching patterns on MOSFETs to have SOC value from different sub-modules fall into a band (*'SOC balancing band'*) and getting the band narrower over time.

Compared to PWM setup which suffers from small margin for balancing due to the limit of modulation index, Modular Multilevel Converter controlled by NLM pattern enjoys faster balancing process because of wide discrete duty cycles to choose (from 16.48 % to 89.33 %, see Figure 3.9).

Harmonic performance is better because the MOSFETs of full-bridge converter only switch at fundamental frequency 50 Hz.

The drawback however, is obvious. There's no control or compensation other than inserting/bypassing a sub-module at fundamental frequency. The output voltage is determined by the number of sub-modules inserted at maximum. Once sub-module's voltage drops during discharging process, the controller can only swap duty cycles to have sub-modules with high SOC have larger duty cycle, which doesn't compensate for the drop at AC output voltage.

5.2.2 *'SOC balancing band'* and nine pre-set cases

Nine pre-set cases help SOC values of sub-modules be inside *'SOC balancing band'* and shrink the band so that SOC of sub-modules can be within a certain range with each other. Such status is kept as far as the simulation goes once it's reached. Compared to PID controller used in PWM setup which can output definite precise offset by tuning some parameters, *'SOC balancing band'* acts as condition for switching different control case. The nine pre-set cases aren't the optimized solution. The drawback of using these cases is that it can increase current harmonics when switching different cases in just a few periods of reference signal or when swapping duty cycles between sub-modules under case 9.

Nevertheless, NLM pattern allows more flexibility to control a sub-module, not just these nine cases of discharging/bypassing sub-modules, possibilities like setting a sub-module on the opposite polarity of five other sub-modules can have the individual sub-module to be charged by the others.

5.3 Wider perspective

There are other cell balancing techniques in the field. Dissipative balancing which means turning extra energy into heat on resistors is still the most common method for its simplicity in control, low cost and high speed. Non-dissipative balancing techniques are of researcher's interest not only for better energy efficiency but also for increased battery pack life without compromising size or adding too much complexity of battery management system. Besides converter-based balancing method, other non-dissipative balancing methods like Double-tiered Switched Capacitors technique[16] and multi winding transformer technique[17], are popular among researchers.

The methods in the thesis are converter-based, a type of non-dissipative balancing technique. Converter-based technique is great when scaling to high power application and it can also achieve high balancing speed. However, the technique is limited by resulting bulky size on application, high cost and control complexity because every sub-module requires a DC-AC converter and synchronization with other sub-modules.[18]

6

Conclusion and future work

This chapter summarizes the thesis work and proposes future work to continue research on the field of battery cell balancing.

6.1 Conclusion

This thesis investigates converter-based cell balancing method which transfers energy from sub-modules with higher SOC value to sub-modules with lower SOC value during discharging process by using components of DC-AC converters. Two MMC setups with PWM and NLM schemes for battery cell balancing respectively are proposed. The PID controller used in MMC with PWM pattern can offer definite tune-able offset. Such offset changes modulation index, further alters active power of the specific sub-module. When the sub-module getting balanced, this offset is turning zero. This method is mostly limited by the small margin left for balancing control, according to modulation index calculation (modulation index should be between 0 and 100%). The structure of the full-bridge converter and unipolar generation help to decrease battery current harmonics. But battery current harmonics in PWM setup is still larger than NLM setup due to higher switching frequency on MOSFETs of the full-bridge converter. The advantage over the NLM alternative is more stable AC output voltage at balanced state. In addition, AC output voltage in PWM setup can also be adjusted with larger flexibility by changing modulation index while the NLM setup only has fixed discrete modulation index decided by the number of sub-modules that can be inserted at maximum.

The NLM setup uses a band (*'SOC balancing band'*) as reference for having SOC from all six sub-modules be balanced. The band doesn't directly affect

current or power of a sub-module, it serves as a reference for master controller to switch control cases. The NLM pattern has a drawback of its resulting AC output voltage. AC output voltage is discrete because modulation index is determined by the number of sub-modules inserted and may not be compensated with the same slope as voltage of battery cells drops. Nevertheless, good balancing speed and less switching activities on MOSFETs make it still attractive in certain applications.[19]

6.2 Future work

Despite the simulation shows that both PWM and NLM patterns can be used to balance battery cells in a MMC setup, the result has not been tested in the real world where PWM switching frequency can be limited by the speed of micro controller's IO port, SOC of battery cells varies in a larger extent. In addition, it is difficult to estimate/measure SOC with accuracy high enough to implement the balancing strategy used in the simulation. The accuracy of SOC in the simulation here is 0.01 % while lowest maximum error on SOC estimation currently available is 0.1 %. [20] Also, the balancing strategy should be generalized for more than six sub-modules and more than nine SOC cases can be determined in practical industry perspective. For example, three hundred cells for a three-phase application with output voltage 360V. If so many battery cells are used, more topologies of battery connections can be simulated and verified, Modular Multilevel Cascade Converter with Double-Star Chopper-Cells [21] for example. The usage of battery cells has been growing. New balancing strategies should be discovered and tested.

Appendix

A

Nine Pre-set Patterns

Every 0.1 second, information of sub-module's SOC ranking and of SOC values sorted in descending order is processed in the sorting system. Every 0.1 second, the numbers of sub-modules having SOC value above and within *'SOC balancing band'* is processed in the summing subsystem. Master controller always gives control information in an order of descending SOC values (from `VSM 1` to `VSM 6`). Slave controller inside each sub-module takes its corresponding part based on its SOC ranking.

In case 1 which is also the start of the simulation, two sub-modules are above the balancing band (`VSM 1` and `VSM 2`). Two sub-modules are within the band at the beginning (`VSM 3` and `VSM 4`). Two sub-modules are under the band (`VSM 5` and `VSM 6`). Therefore, the assignment of duty cycles aims to offer VSM1 with highest duty cycle, VSM 2 with slightly less but still high duty cycle, `VSM 3` and `VSM 4` with duty cycle around 50% because they are within the target band, `VSM 5` and `VSM 6` with less duty cycle. Choosing around 50% duty cycle for `VSM 3` and `VSM 4` is because there are more options at that part to choose while there are few options for duty cycle too low or too high in the figure 3.9. By giving sub-modules inside the target band similar duty cycles around 50%, those sub-modules whose SOC values are still outside the band can be given different duty cycles to get closer to the target band. AC output voltage of the MMC under case 1 is shown in the Figure A.1.

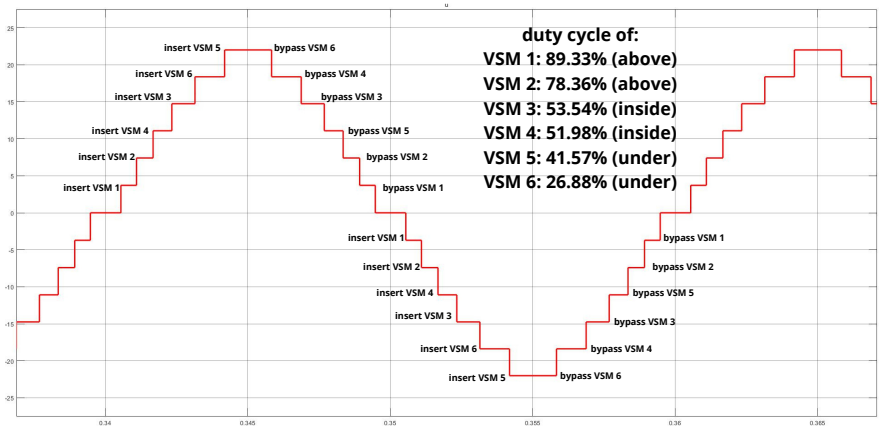


Figure A.1: *AC output voltage under case 1 in NLM setup.*

In case 2, `VSM 2`, `VSM 3` and `VSM 4` are inside the band. Thus, they get around 50% duty cycle. VSM having highest SOC is still above the band. Therefore, its duty cycle remains highest (89.33 %). Due to the limit by having 3 duty cycles around 50 % and 1 duty cycle of the highest in the duty cycle selection table (Table 3.9) , `VSM 5` and `VSM 6` have to get duty cycle of 41.57 %. AC output voltage of the MMC under case 2 is shown in the Figure A.2.

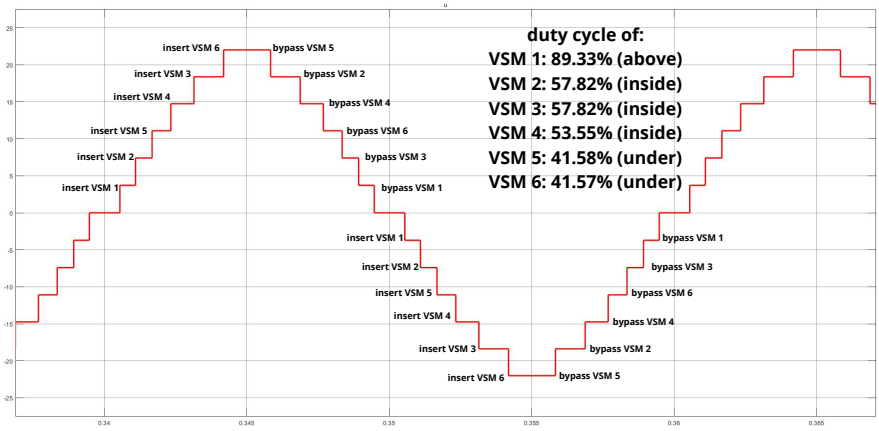


Figure A.2: *AC output voltage under case 2 in NLM setup.*

In case 3, `VSM 1` and `VSM 2` remain above SOC balancing band as the start of the process. One sub-module from under the band reaches the band making three sub-modules are within the band (`VSM 3`, `VSM 4` and `VSM 5`). `VSM 6` is still under the band. Since `VSM 1` and `VSM 2` having larger duty cycle and three balanced sub-modules require around 50% of duty cycle, `VSM 6` can have the smallest duty cycle. AC output voltage of the MMC under case 3 is shown in the Figure A.3.

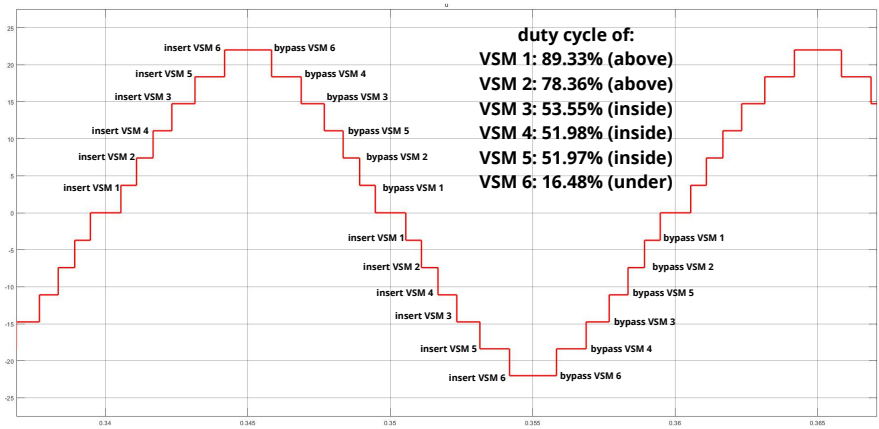


Figure A.3: *AC output voltage under case 3 in NLM setup.*

In case 4, only two sub-modules (`VSM 5` and `VSM 6`) are under while the rest of six sub-modules are within the *'SOC balancing band'*. Since `VSM 5` and `VSM 6` require less duty cycle and it is better to have similar duty cycle for four balanced sub-modules, `VSM 1` to `VSM 4` can only have around 70% of duty cycle. AC output voltage of the MMC under case 4 is shown in the Figure A.4.

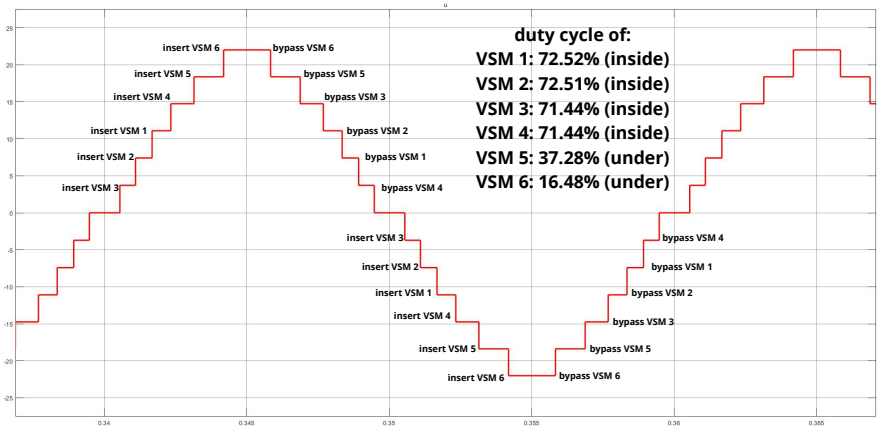


Figure A.4: *AC output voltage under case 4 in NLM setup.*

In case 5, there are one sub-module from above the band and one sub-module from under the band reach the band. `VSM 1` requires most duty cycle to get balanced while `VSM 6` needs lowest duty cycle. Thus, `VSM 2` to `VSM 5` can only have duty around 60 %, given the limit of operation point selection from Figure 3.9. AC output voltage of the MMC under case 5 is shown in the Figure A.5.

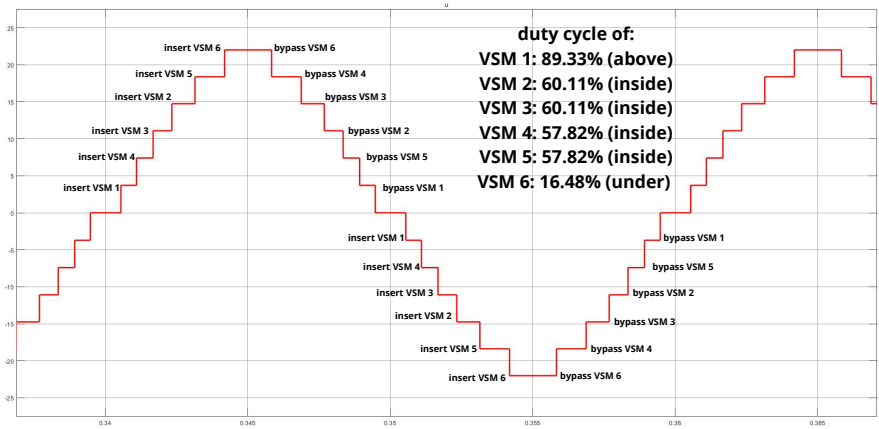


Figure A.5: *AC output voltage under case 5 in NLM setup.*

In case 6, only two sub-modules above the band remain outside the band while other sub-modules are inside the band. Thus,`VSM 1` gets the highest duty cycle and four balanced sub-modules have duty cycle of around 40%. AC output voltage of the MMC under case 6 is shown in the Figure A.6.

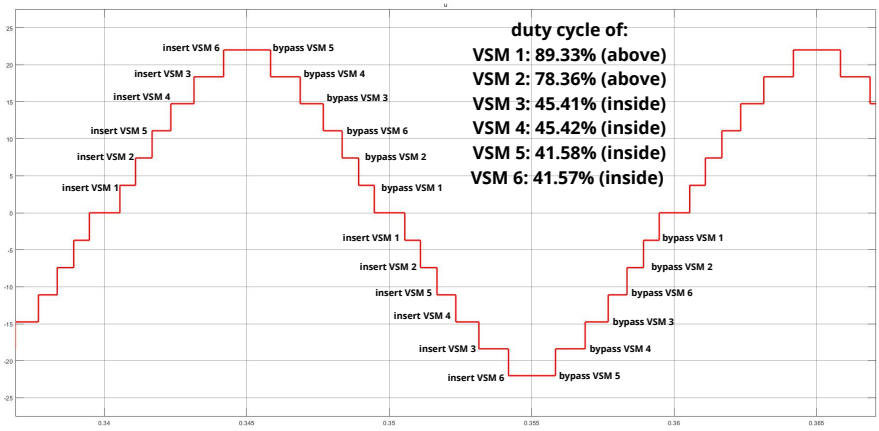


Figure A.6: *AC output voltage under case 6 in NLM setup.*

In case 7, only one sub-module remains under the band while other sub-modules are balanced into the band. Therefore, `VSM 6` gets the lowest duty cycle (16.48 %) and rest of the sub-modules have duty cycle of around 60 %. AC output voltage of the MMC under case 7 is shown in the Figure A.7.

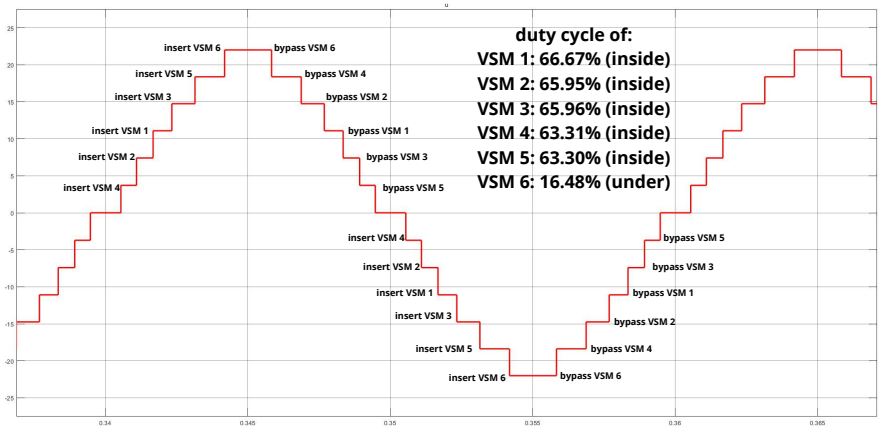


Figure A.7: *AC output voltage under case 7 in NLM setup.*

In case 8, only one sub-module (`VSM 1`) remains above the band while `VSM 2` to `VSM 6` are within the band. So `VSM 1` gets the highest duty cycle (89.33 %) and rest of the sub-modules have duty cycle of around 50%. AC output voltage of the MMC under case 8 is shown in the Figure A.8.

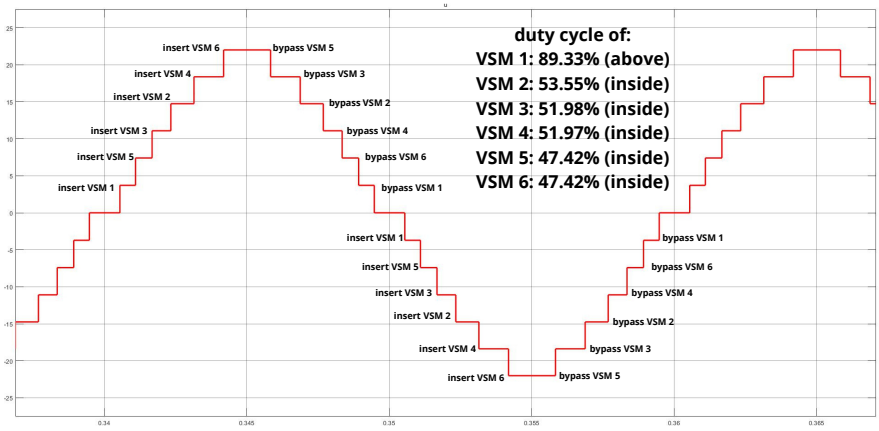


Figure A.8: *AC output voltage under case 8 in NLM setup.*

In case 9, all six sub-modules reach inside *'SOC balancing band'*. Since it is impossible to give every sub-module the same duty cycle when all sub-modules are balanced because twelve operation points determined by the reference step signal isn't divided evenly in time. Therefore, the goal is to give each sub-module similar duty cycle. In addition, these sub-modules must have their duty cycle based on their SOC ranking but their SOC ranking change easily because their SOC values are so close to others. That means these sub-modules will keep swapping their duty cycles with each other according to changes of their SOC ranking. As their swapping duty cycles would have the *'SOC balancing band'* get narrower, it helps to keep their balanced status. AC output voltage of the MMC under case 9 is shown in the Figure A.9.

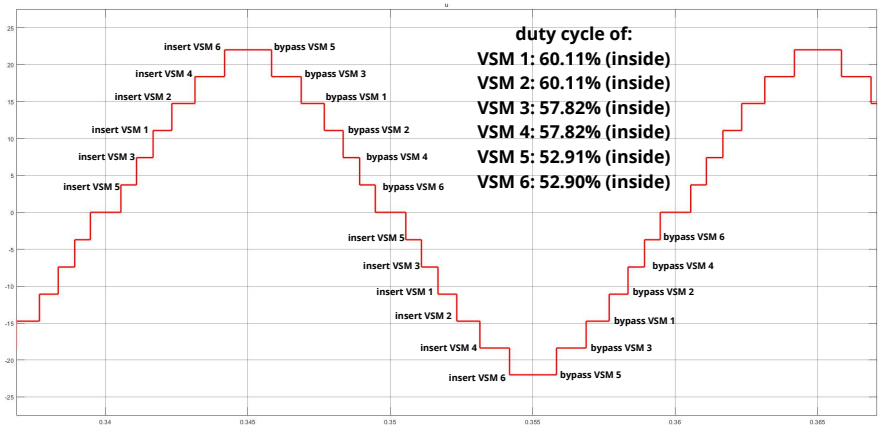


Figure A.9: *AC output voltage under case 9 in NLM setup.*

B

Variables Saved to Workspace

In table B.1, variables saved to workplace are shown together with their sample time and description.

Table B.1: *Table of variables saved to workspace.*

Variable name	Sample time (in sec)	Description
nlm_b1...nlm_b6	0.01	Balanced indicators of corresponding sub-module in the NLM setup, the value being one means the sub-module is balanced (sub-module's SOC is less than or equal to average SOC ±0.002 %).
pwm_b1...pwm_b6	0.01	Balanced indicators of corresponding sub-module in the PWM setup, the value being one means the sub-module is balanced (sub-module's SOC is less than or equal to average SOC ±0.002 %).
nlm_soc1...nlm_soc6	0.01	SOC value of corresponding sub-module in the NLM setup.
pwm_soc1...pwm_soc6	0.01	SOC value of corresponding sub-module in the PWM setup.

Continued on next page

Table B.1 – continued from previous page

Variable name	Sample time (in sec)	Description
nlm_soc_av	0.01	Average SOC value of six sub-module under NLM pattern.
pwm_soc_av	0.01	Average SOC value of six sub-module under PWN pattern.
set_idx	0.1	Case number of SOC status defined in Table 3.1 for the NLM setup.
pi1 ... pi6	0.01	Output of discrete PID controllers inside each sub-module in the PWM setup.
mr1 ... mr6	0.01	Data input to `PWM generator(multilevel)` block in slave controller system of PWM setup, reflecting the modulation index on gate pulses sent to the full-bridge converter of the sub-module.
pwm_ib1 ... pwm_ib6	$1e^{-5}$	DC current flowing through the battery cell in the PWM setup.
pwm_ib1m ... pwm_ib6m	0.01	Mean DC current flowing through the battery cell in the PWM setup over 0.01 sec.
pwm_uac	$1e^{-5}$	AC output voltage of PWM setup.
pwm_uac_rms	0.02	AC output voltage of PWM setup in RMS value.
nlm_uac	$1e^{-5}$	AC output voltage of NLM setup.
nlm_uac_rms	0.02	AC output voltage of NLM setup in RMS value.
pwm_p	0.02	Output AC power of PWM setup calculated by the multiplication of AC current and voltage in RMS form.
nlm_p	0.02	Output AC power of NLM setup calculated by the multiplication of AC current and voltage in RMS form.
nlm_ib1 ... nlm_ib6	$1e^{-5}$	DC current flowing through the battery cell in the NLM setup.

Continued on next page

Table B.1 – continued from previous page

Variable name	Sample time (in sec)	Description
nlm_ib1m . . . nlm_ib6m	0.01	Mean DC current flowing through the battery cell in the NLM setup over 0.01 sec.
nlm_dc1 . . . nlm_dc6	0.1	Duty cycle of each sub-module in NLM setup.

C

MATLAB Script and Function

In chapter C, Matlab scripts and functions used for the thesis work are shown, including parameters for the Simulink model, functions to select pre-set patterns in master controller.

C.1 Parameters for the whole simulation containing PWM and NLM setups

Parameters for Simulink model such as sample time, number of sub-modules and initial SOC of each sub-module are shown in Listing C.1.

Listing C.1: *The MATLAB script to setup parameters of the whole Simulink model.*

```
pihi=0.1;   %upper satuation limit for PID controller
pilo=-0.1;  %lower satuation limit for PID controller
SOC=[90.01 90.02 90.03 90.04 90.05 90.06];
N=6;  %number of sub-modules
Ts=1e-5; % sampling time for the simulation
f1=50;  % AC output voltage frequency
fsw=2000;  %PWM switching frequency
Rdson=2e-3; % conducting resistance on full-bridge
    converter
angle_Iv=0;  % angle offset for referrence sinusoidal
    signal in PWM setup
gp=30;  %proportional gain in PID controller
gd = 80;  %derivative gain in PID controller
```

```
samt=1e-5; % sampling time for PWM generator block
```

C.2 Matlab script for fft_cal function

In Listing C.2, the code to process frequency components after FFT and to calculate harmonics in RMS value is presented.

Listing C.2: *The MATLAB script for frequency component processing and harmonics calculation.*

```
function [f,res_abs,harm]=fft_cal(tim,da)
N=length(tim);
t_step = tim(2,1)-tim(1,1);

f_max=0.5/t_step;  %half of the sampling frequency

tem(1:N)=2/N*fft(da);
    if mod(N,2) %odd
        res(1:(N+1)/2)=tem(1:(N+1)/2);
        f=linspace(0,f_max*(N-1)/N,(N+1)/2);
    else        %even
       res(1:N/2+1)=tem(1:N/2+1);
       f=linspace(0,f_max,N/2+1);
    end

res_abs = abs(res)./sqrt(2); %divided by sqrt(2) to get RMS
    value
res_cp = abs(res)./sqrt(2);
res_cp(1,1) = 0; %remove dc component
res_cp(1,21) = 0; %remove fundamental freq component
harm = res_cp.^2;
harm = sqrt(sum(harm)); %rms value of harmonics
end
```

C.3 Matlab function of cases selection in master controller from NLM setup

In master controller of NLM setup, this function selects which one of nine pre-set cases should be applied to six sub-modules based on input info about the numbers of sub-modules reaches within SOC balancing band and of sub-modules whose SOC is above the band. The code is presented in Listing C.3.

Listing C.3: *The MATLAB function to select pre-set patterns in master controller of NLM setup.*

```
function set_idx = fcn(bal,abv)

if (bal==2)
    set_idx=1;
elseif(bal==3 && abv==1)    %% 3 balanced,1 abvove,2 below
    set_idx=2;
elseif(bal==3 && abv==2)    %% 3 balanced,2 abvove,1 below
    set_idx=3;
elseif(bal==4 && abv==0)    %% 4 balanced,0 abvove,2 below
    set_idx=4;
elseif(bal==4 && abv==1)    %% 4 balanced,1 abvove,1 below
    set_idx=5;
elseif(bal==4 && abv==2)    %% 4 balanced,2 abvove,0 below
    set_idx=6;
elseif(bal==5 && abv==0)    %% 5 balanced,0 abvove,1 below
    set_idx=7;
elseif(bal==5 && abv==1)    %% 5 balanced,1 abvove,0 below
    set_idx=8;
else
    set_idx=9;
end
```

C.4 Matlab function for case 1 to control gates on full-bridge converters of six sub-modules

The Matlab function is used to control the gate1 and gate 3 of the full-bridge converter used in six sub-modules with the input of step signal and fall indication signal in NLM setup. The code is shown in Listing C.4. Accompanied with logic blocks `NOT` which invert gate 1 and gate 3 signals for gate 2 and gate 4, four gate pulses are generated for four switches of a full-bridge converter inside a sub-module. Signal c1g1 = 1 means turning on gate 1 of sub-module 1 when condition is fulfilled. For a full-bridge converter, both gate 1 and gate3 being on means the converter is bypassed, according to the Table 2.1 . Gate pulses for switches of six sub-modules are generated in a single function. There are nine such Matlab functions corresponding to nine cases used to balance six sub-modules in different SOC conditions. The code below is for case 1.

Listing C.4: *The MATLAB function to generate gate pulses under case 1 in NLM setup.*

```
function [c1g1,c1g3,c2g1,c2g3,c3g1,c3g3,c4g1,c4g3,c5g1,c5g3
    ,c6g1,c6g3] = fcn(s,fall)
```

```
if (s==1 && fall==0)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=1;
    c3g1=1;          %% VSM 1 positively inserted, VSM 23456
        bypassed
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==2 && fall==0)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;          %% VSM 12 positively inserted , VSM
       3456 bypassed
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==3 && fall==0)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;          %% VSM 124 positively inserted, VSM 356
        bypassed
    c3g3=1;
    c4g1=1;
    c4g3=0;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==4 && fall==0)
    c1g1=1;
    c1g3=0;
    c2g1=1;
```

```
    c2g3=0;
    c3g1=1;          %% VSM 1234 positively inserted, VSM 56
        bypassed
    c3g3=0;
    c4g1=1;
    c4g3=0;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==5 && fall==0)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;          %% VSM 12346 positively inserted, VSM 5
        bypassed
    c3g3=0;
    c4g1=1;
    c4g3=0;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=0;
elseif (s==6)
    c1g1=1;
    c1g3=0;
    c2g1=1;      %% VSM 123456 positively inserted
    c2g3=0;
    c3g1=1;
    c3g3=0;
    c4g1=1;
    c4g3=0;
    c5g1=1;
    c5g3=0;
    c6g1=1;
    c6g3=0;
elseif (s==5 && fall==1)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;
    c3g3=0;          %% VSM 12345 positively inserted, VSM 6
        bypassed
    c4g1=1;
```

```
    c4g3=0;
    c5g1=1;
    c5g3=0;
    c6g1=1;
    c6g3=1;
elseif (s==4 && fall==1)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;
    c3g3=0;          %% VSM 1235 positively inserted ,VSM 46
        bypassed
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=0;
    c6g1=1;
    c6g3=1;
elseif (s==3 && fall==1)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;
    c3g3=1;          %% VSM 125 positively inserted , VSM 346
        bypassed
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=0;
    c6g1=1;
    c6g3=1;
elseif (s==2 && fall==1)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=0;
    c3g1=1;
    c3g3=1;          %% VSM 12 positively inserted , VSM 3456
        bypassed
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
```

```
    c6g3=1;
elseif (s==1 && fall==1)
    c1g1=1;
    c1g3=0;
    c2g1=1;
    c2g3=1;          %% VSM 1 positively inserted,VSM 23456
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==0)
    c1g1=1;
    c1g3=1;
    c2g1=1;
    c2g3=1;          %% VSM 123456 bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-1 && fall==1)
    c1g1=0;
    c1g3=1;
    c2g1=1;
    c2g3=1;          %% VSM 1 negatively inserted, VSM 23456
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-2 && fall==1)
    c1g1=0;
    c1g3=1;
    c2g1=0;
```

```
    c2g3=1;          %% VSM 12 negatively inserted, VSM
        3456 bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-3 && fall==1)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 124 negatively inserted, VSM 356
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=0;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-4 && fall==1)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 1234 negatively inserted, VSM 56
        bypassed
    c3g1=0;
    c3g3=1;
    c4g1=0;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-5 && fall==1)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 12346 negatively inserted, VSM 5
        bypassed
    c3g1=0;
    c3g3=1;
```

```
    c4g1=0;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=0;
    c6g3=1;
elseif (s==-6)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 123456 negatively inserted
    c3g1=0;
    c3g3=1;
    c4g1=0;
    c4g3=1;
    c5g1=0;
    c5g3=1;
    c6g1=0;
    c6g3=1;
elseif (s==-5 && fall==0)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 12345 negatively inserted, VSM 6
        bypassed
    c3g1=0;
    c3g3=1;
    c4g1=0;
    c4g3=1;
    c5g1=0;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-4 && fall==0)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 1235 negatively inserted, VSM 46
        bypassed
    c3g1=0;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=0;
    c5g3=1;
    c6g1=1;
```

```
    c6g3=1;
elseif (s==-3 && fall==0)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 125 negatively inserted, VSM 346
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=0;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-2 && fall==0)
    c1g1=0;
    c1g3=1;
    c2g1=0;
    c2g3=1;          %% VSM 12 negatively inserted, VSM 3456
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
elseif (s==-1 && fall==0)
    c1g1=0;
    c1g3=1;
    c2g1=1;
    c2g3=1;          %% VSM 1 negatively inserted, VSM 23456
        bypassed
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;

else
   c1g1=1;
```

```
    c1g3=1;
    c2g1=1;
    c2g3=1;
    c3g1=1;
    c3g3=1;
    c4g1=1;
    c4g3=1;
    c5g1=1;
    c5g3=1;
    c6g1=1;
    c6g3=1;
end
```

C.5 Slave controller

Listing C.5 shows the code used in slave controller of sub-module 1 in NLM setup. It calculates the SOC difference between the battery cell and average SOC to determine SOC OF the battery cell is inside the SOC balancing band or above it or below it. Also the function chooses which part of the signal *'from_master'* it should take for the sub-module based on the sub-module's SOC ranking.

Listing C.5: *The MATLAB function to output sub-module soc status and select control signal in slave controller of NLM setup.*

```
function [above,bal,under,idx_g] = fcn(soc3_diff,soc4_diff,
    soc_ranking)

if ((soc3_diff <= 0) && (soc4_diff >= 0))
    bal=1;
    above=0;    % SOC of the sub-module is inside the 'soc
        blancing band'
    under=0;
elseif (soc3_diff > 0)
    above=1;
    bal=0;        % SOC of the sub-module is above the 'soc
        blancing band'
    under=0;
elseif (soc4_diff < 0)
    under=1;
    bal=0;        % SOC of the sub-module is under the 'soc
        blancing band'
    above=0;
else
    bal=0;
    above=0;
```

```
    under=0;
end

if (soc_ranking(1)==1) %%max soc, select gate pulses for
    VSM1
    idx_g=1;
elseif (soc_ranking(2)==1)
    idx_g=2;
elseif (soc_ranking(3)==1)
    idx_g=3;
elseif (soc_ranking(4)==1)
    idx_g=4;
elseif (soc_ranking(5)==1)
    idx_g=5;
elseif (soc_ranking(6)==1)
    idx_g=6;    %%min soc,select gate pulses for VSM6
else
    idx_g=1;
end
end
```

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