

β -Ga₂O₃ MOSFETs electrical characteristic study of various etching depths grown on sapphire substrate by MOCVD

Chan-Hung Lu¹ · Fu-Gow Tarntair¹ · Yu-Cheng Kao² · Niall Tumilty³ · Jia-Min Shieh⁴ · Shao-Hui Hsu⁴ · Ching-Lien Hsiao⁵ · Ray-Hua Horng¹

Received: 24 April 2023 / Accepted: 18 June 2023

© The Author(s) 2023 **OPEN**

Abstract

β -Ga₂O₃ thin films with both a 45 nm Si-doped conductive epilayer and unintentionally doped epilayer were grown on c-plane sapphire substrate by metalorganic chemical vapor deposition. β -Ga₂O₃ based metal–oxide–semiconductor field-effect transistors (MOSFETs) were fabricated with gate recess depths of 20 nm and 40 nm (it indicated gate depth with 70 nm and 50 nm, respective), respectively, and without said recessing process. The conductivity of β -Ga₂O₃ epilayers was improved through low in situ doping using a tetraethoxysilane precursor to increase MOSFET forward current density. After recessing, MOSFET operation was transferred from depletion to enhanced mode. In this study, the maximum breakdown voltage of the recessed 40 nm transistor was 770 V. The etching depth of a recessed-gate device demonstrates its influence on device electrical performance.

Keywords High power MOSFETs · Enhancement mode · β -Ga₂O₃ · Recessed gate · MOCVD

Introduction

β -Ga₂O₃ is emerging as the potential high-power device candidate for next generation applications owing to its ultra-wide bandgap of 4.8 eV [1]. It is known that β -Ga₂O₃ possesses a critical electric field value of 8 MV/cm considerably higher than more established power semiconductor materials such as 4H-SiC (2.5 MV/cm) and GaN (3.3 MV/cm) [2]. From Baliga's figure of merit (BFOM) the trade-off between on-resistance and breakdown voltage demonstrates that β -Ga₂O₃ (3214) has greater potential for high power applications compared to 4H-SiC (317) and GaN (846) [3]. An on-going and critical problem for both SiC and GaN-based devices is the higher crystal growth cost. For β -Ga₂O₃, costs are an order of magnitude lower and films can be grown hetero-epitaxially by different methods [4, 5]. In this context, high quality heteroepitaxial β -Ga₂O₃ layers can be grown by metalorganic chemical vapor deposition (MOCVD) on sapphire which is clearly in reducing growth cost [5].

✉ Ray-Hua Horng, rayhua@nycu.edu.tw | ¹Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan, ROC. ²Department of Materials Science and Engineering, National Chung Hsing University, Taichung 40227, Taiwan, ROC. ³International College of Semiconductor Technology, National Yang Ming Chiao Tung University, Hsinchu 30010, Taiwan, ROC. ⁴National Applied Research Laboratories, Taiwan Semiconductor Research Institute (TSRI), Hsinchu 30091, Taiwan, ROC. ⁵Thin Film Physics Division, Department of Physics, Chemistry and Biology (IFM), Linköping University, 581 83 Linköping, Sweden.



These superlative material characteristics permit β -Ga₂O₃ to be employed for many electrical devices, such as metal–oxide–semiconductor field-effect transistors (MOSFET) [6–10], metal–semiconductor field-effect transistors (MESFET) [11], and Schottky barrier diodes [12]. In addition, to increasing conductivity, most devices are grown homoepitaxially and doped by Si-ion implantation forming a shallow donor [13]. Furthermore, there are many studies on both depletion-mode (D-mode) MOSFETs using Ga₂O₃ epilayers on bulk Ga₂O₃ substrates and Ga₂O₃ grown on sapphire substrates combined with Si-ion implantation technologies [6–8]. However, the lack of a p-type-based epitaxial substrate [14] leads to fewer enhancement-mode (E-mode) MOSFET published examples and clearly needs to be developed using other special techniques, which is the purpose of this work. Recently, a number of E-mode MOSFETs have been reported, such as Sn-doped Ga₂O₃ wrap-gate fin-array with a threshold voltage between 0 and +1 V [15], a vertical power MISFET with fin-shaped channels [16], MOSFETs with gate recess [9, 10], or using N-Si co-doping technology [17]. Regarding the above methods, Ga₂O₃ epilayers grown on native substrate generally demonstrated low breakdown voltages. Elsewhere, mechanically exfoliated Cr-doped Ga₂O₃ substrates were utilized and transferred onto SiO₂/Si substrate and then locally thinned to obtain E-mode MOSFETs [18]. Even though I_D was very low it is not feasible to mass-produce devices using exfoliation methods.

The performance of β -Ga₂O₃ based MOSFETs for D- and E Mode operation has been simulated by Kachhawa [19], but there are no comparable experimental results. In our work, different recessed gate etch depths were used to evaluate MOSFET electrical characteristics of heteroepitaxial Ga₂O₃ layers grown on sapphire substrates, for both D- to E-mode control by gate recessing. In this study, MOSFETs electrical characteristics will be discussed and compared with the previously reported simulation data [19, 20].

Experimental

An in situ doped 45 nm epilayer and a 45 nm un-intentionally doped (UID) β -Ga₂O₃ layer were grown on c-plane sapphire at 875 °C by MOCVD. The Si in situ doping layer was obtained through the TEOS precursor with a 10 sccm flow rate, resulting in a measured carrier concentration (N_D) of $7.2 \times 10^{18} \text{ cm}^{-3}$ and Hall mobility (μ_{Hall}) $7.6 \text{ cm}^2/\text{V}\cdot\text{s}$ through Hall measurement. The device active region was defined by an inductively coupled plasma reactive ion etching (ICPRIE) system using Ar and Cl₂ to isolate each device as shown in Fig. 1 (a). Following this, a Ti/Al/Ni/Au (20/100/40/50 nm) metal stack was deposited as the source (S) and drain (D) electrodes by E-beam evaporation, shown in Fig. 1 (b). To obtain an Ohmic contact for the above metals on Ga₂O₃, samples were annealed at 500 °C in an N₂ ambient for 1 min. The gate region was then etched to reduce its thickness, enhance channel control as shown in Fig. 1 (c). Thereafter, a 30 nm Al₂O₃ dielectric layer was deposited by atomic layer deposition (ALD), shown in Fig. 1 (d).

A Ni/Au (30/150 nm) metal stack of gate (G) electrode was then deposited in the gate region by E-beam evaporation, shown in Fig. 1 (e). Finally, a 200 nm thick SiO₂ passivation layer was grown on top and S, D and G contact pads and then

Fig. 1 aThe recessed MOSFET device structure and its b–f process flow

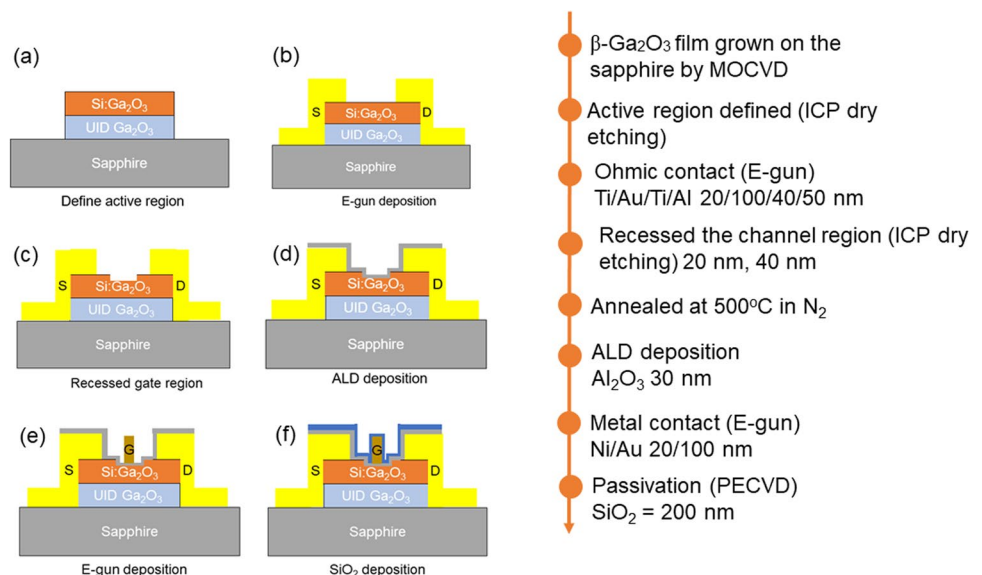
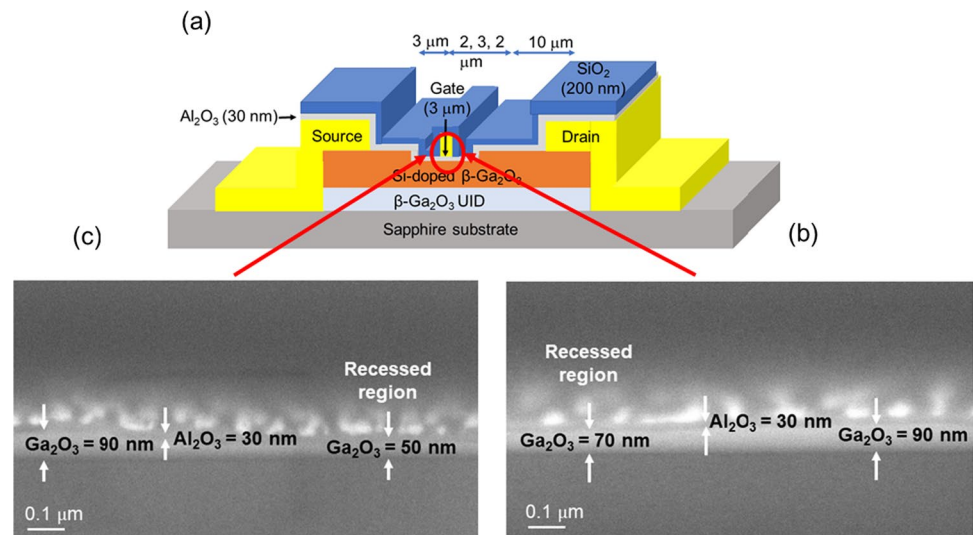


Fig. 2 **a** The cross-sectional schematic of β -Ga₂O₃ MOSFET **b** SEM cross-sectional image of Gate-recessed region etching 20 nm (remained 70 nm) and **c** 40 nm (remained 50 nm)



are opened for measurement, shown in Fig. 1 (f). Studied MOSFETs have a gate length of 3 μm (L_G), a recessed length of 7 μm , a source-gate width (L_{SG}) of 7 μm , and a gate-to-drain width (L_{GD}) of 10 μm . The final device schematic and etching depth were measured by scanning electron micrograph (SEM), shown in Fig. 2. Different etching depths were used to study this effect on MOSFET electrical properties. These are 20 nm, 40 nm, and a no-etch process, respectively. As β -Ga₂O₃ thickness before etching was 90 nm, after said etch process the remaining material thickness was 70 nm and 50 nm on sapphire substrate. The remaining material comprises a 25 nm Si-doped layer and a 5 nm Si-doped layer on 45 nm thick UID layers for 20 nm and 40 nm etched samples, respectively. After device processing, MOSFET characteristics were measured by a Keysight B1505A. Specific contact resistance (ρ_c) and sheet resistance (R_{sheet}) were measured by the transmission line measurements (TLMs).

Results and discussion

The crystallinity of the device structure (n-type β -Ga₂O₃/ UID β -Ga₂O₃/sapphire) was measured by x-ray diffraction system and shown in Fig. 3(a). There existed 38.9, 18.3 and 59.0° corresponding to $(\bar{2}01)$, $(\bar{4}02)$, and $(\bar{6}03)$ of Ga₂O₃. It was worth to mention that the epilayer presented high quality single crystal even the epilayer was doped by Si

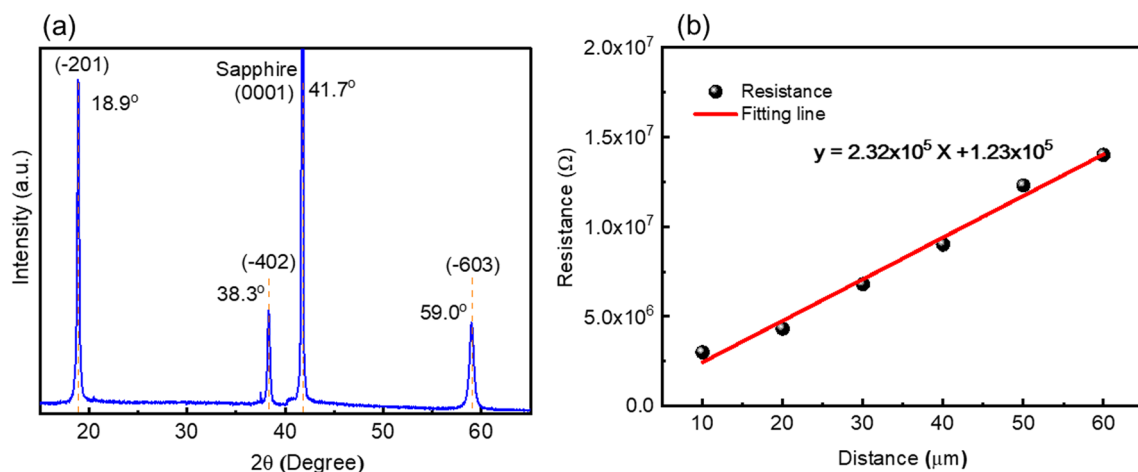


Fig. 3 **a** X-ray diffraction pattern of the device structure and **b** TLM measurement by different distance from 10 to 60 μm

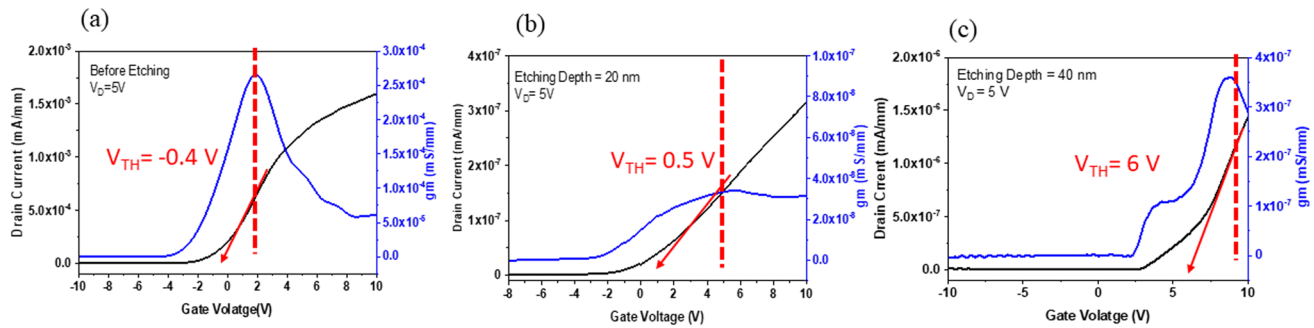


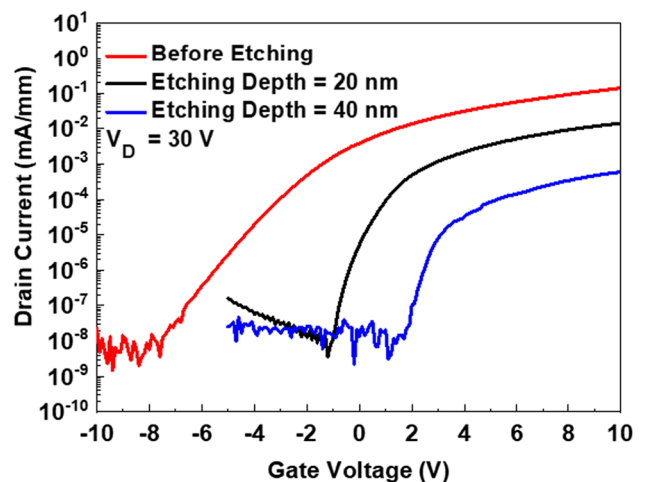
Fig. 4 Extracting the threshold voltage by $I_D - V_G$ measurements under $V_{GS} = 5$ V for **(a)** the non-recessed device at $V_{TH} = -0.4$ V, **b** the device etched a depth of 20 nm at $V_{TH} = 0.5$ V, and **c** the device etched a depth of 40 nm at $V_{TH} = 6$ V

with $7.2 \times 10^{18} \text{ cm}^{-3}$. Transmission line measurements (TLM) were used to evaluate Ohmic contact properties and semiconductor resistance between S and D electrodes for Si-doped Ga_2O_3 epilayers. The resistance as function of distance of the TLM pattern is shown in Fig. 3. The TLM was used to measure the S/D contact resistances. They are almost the same for each sample because these devices were fabricated using the same wafer. A linear relationship is clearly observed indicating that S and D metal electrodes on Si-doped Ga_2O_3 are Ohmic in nature. The sheet resistance (R_s), transfer length (L_T) and specific contact resistance (ρ_c) can be obtained using the TLM measurement. In Fig. 3, the presented TLM results were measured from 10 μm to 60 μm . The R_s and the ρ_c values can be extracted using slope $= \frac{R_s}{Z}$ and $L_T = \sqrt{\frac{\rho_c}{R_s}}$. The extracted L_T was 0.27 μm . R_s was found to be 46.4 $\text{M}\Omega/\square$ and ρ_c 3.28 Ω/mm^2 .

To understand the relationship between recessed depth and device operation mode, different recessed depths are considered including a non-recessed device; with depths of 20 nm and 40 nm, respectively. Figure 4 shows the relationship of I_D as function of V_{GS} for a Ga_2O_3 MOSFET with different etch depths. The threshold voltage (V_{TH}) is defined under drain voltage condition ($V_{DS} = 5$ V) in the MOSFET linear region. The x-intercept is determined with a tangent line from the transconductance (g_m) maximum point were $V_{TH} = -0.4$ V, 0.5 V, and 6 V for non-etched, 20 nm and 40 nm etched devices, respectively. The $I_D - V_{GS}$ electrical characteristic demonstrates that MOSFETs can be transferred from the depletion mode to enhancement mode. Prior to etching the MOSFET was in D-mode, but V_{TH} was only -0.4 V. This could be owing to a narrow 45 nm thick Si-doped layer. Clearly, reducing the thickness of doping region, increases the resistance of the channel. For an applied V_G with either zero or negative bias, the channel was totally depleted thus the normally-on channel was turned off. Further etching resulted in V_{TH} increasing, yielding E-mode device operation.

Besides V_{TH} , the etching depth also affected device saturation current, in this case deeper etching depths results in a lower saturation current, I_{SAT} . In order to confirm this point, the drain current as function of gate voltage for the Ga_2O_3 MOSFET with different etching depths was measured for $V_D = 30$ V and is shown in Fig. 5. It was found that

Fig. 5 The $I_D - V_{GS}$ transfer characteristic measurement for different etching depth **a** non etching **b** etching 20 nm and **c** etching 40 nm



the I_{SAT} is approximately 140 $\mu\text{A}/\text{mm}$, 14 $\mu\text{A}/\text{mm}$, and 0.6 $\mu\text{A}/\text{mm}$ for MOSFETs with a non-etched channel, and etch depths of 20 nm and 40 nm, respectively. Furthermore, g_m maximum saturation (not shown data) at $V_{DS} = 30\text{ V}$ is 26 $\mu\text{S}/\text{mm}$, 2.7 $\mu\text{S}/\text{mm}$, and 0.13 $\mu\text{S}/\text{mm}$ for non-etched channel, and etch depths of 20 nm and 40 nm, respectively.

Figure 6 shows $I_{DS} - V_{DS}$ measurements for different etch depths. The V_{DS} ranges from 0 to 50 V in increments of 0.5 V. The maximum current shows a consistent trend with device transfer characteristic such that deeper recessed depths give lower maximum I_{DS} current. Likewise, turn-on resistance increased in-line with etch depth, from 69 $\text{k}\Omega\cdot\text{mm}$, 128 $\text{k}\Omega\cdot\text{mm}$, and 188 $\text{k}\Omega\cdot\text{mm}$. For the singular 40 nm etched depth, under low drain bias the channel did not turn on directly. It was thought that this unusual phenomenon relates to a high channel resistance under the gate-recessed area as non-recessed devices have not experienced this problem. The contact resistances of S and D of the sample with 40 nm etching depth were the same as compared with those of sample without recess processing. The sample with 40 nm etching depth has the 50 nm channel depth (5 nm doped layer + 45 nm UID layer). Due to the channel depth being too thin, it resulted in high resistance and presented nonlinear. The device structure should be optimized for improving I_{DS} .

It is important to evaluate MOSFET breakdown voltage for different recessed channels. The breakdown voltage characteristic of the $\beta\text{-Ga}_2\text{O}_3$ MOSFETs for various etching depths was measured at room temperature. During measurement, these devices were operated in the OFF state. Gate voltages were held at -5 V , -6 , and 0 V for MOSFETs without recess and with recesses of 20 and 40 nm depth, respectively. The three-terminal off-state breakdown characteristics of Ga_2O_3 MOSFETs with different recessed depths were measured and shown in Fig. 7. The breakdown voltage was 650 V, 710 V, and 770 V for MOSFETs without recess and with recesses of 20 nm and 40 nm, respectively. Noticeably, MOSFETs with deeper etching depths demonstrated higher breakdown voltages. One possibility for this observation is that recessed regions could present a more resistor pathway under drift condition serving to divide the high voltage from the drain. These results were similar to those reported in [9], whereby MOSFETs were homoepitaxially grown on $\beta\text{-Ga}_2\text{O}_3$ by MOCVD on a Fe-doped semi-insulating (010) Ga_2O_3 substrate [9].

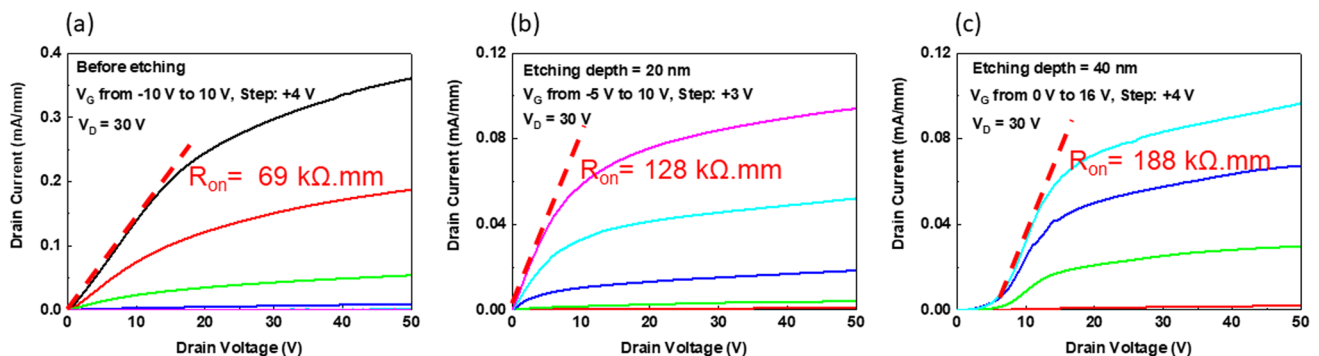


Fig. 6 $I_{DS} - V_{DS}$ measurement for different etching depths **a** before etching, **b** etching depth 20 nm and **c** etching depth 40 nm

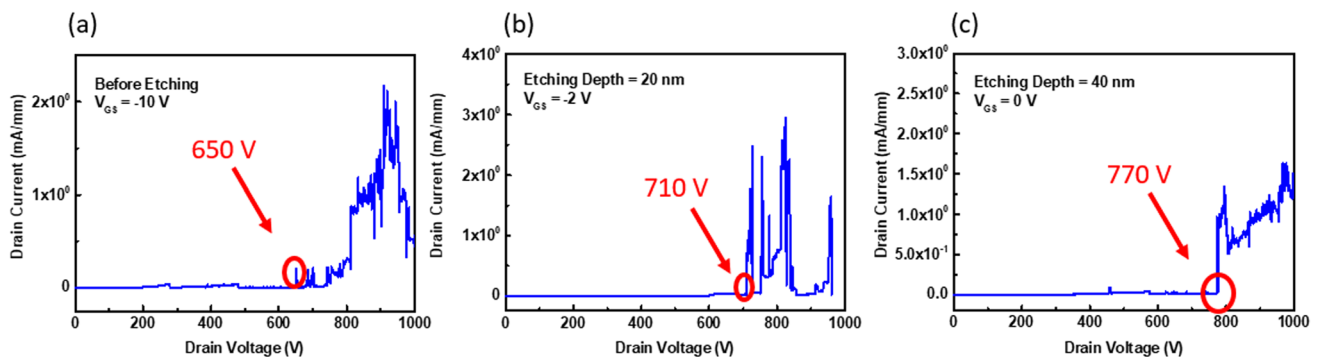


Fig. 7 Breakdown voltage for different etching depths **a** before etching, **b** etching depth 20 nm and **c** etching depth 40 nm

Table 1 Electrical characteristic for different etching depths

Sample No	V_{th} (V)	Maximum current @ $V_{GS} = 10$ V, $V_{DS} = 30$ V	Breakdown voltage (V)	gm maximum ($\mu S/mm$) @ $V_{DS} = 30$ V	R_{on} ($k\Omega mm$)
Before etching	− 0.4	0.14 (mA/mm)	650	26	69
Etching depth:15 nm	0.5	0.014 (mA/mm)	710	2.7	128
Etching depth:40 nm	6	5.9×10^{-4} (mA/mm)	770	0.13	188

Table 2 A summarizing state-of-the-art of breakdown and R_{on} performance for the E-mode Ga_2O_3 grown on different substrates

Substrate	R_{on}	Breakdown voltage (V)	References
Ga_2O_3	215 $m\Omega mm$	198	[21]
Ga_2O_3	22.5 $m\Omega cm^2$	~ 47	[22]
Ga_2O_3	–	190	[9]
Ga_2O_3 (Vertical)	13–18 $m\Omega cm^2$	> 1000 V	[16]
Ga_2O_3 (Vertical)	135 $m\Omega cm^2$	263	[17]
Sapphire	47 K $m\Omega cm^2$	~ 155	[23]
P+ – Si	35.3 M Ωcm	224	[24]
Sapphire	188 K Ωmm	770	This work

Table 1 presents all electrical characteristics of Ga_2O_3 MOSFETs grown on sapphire substrate with different recess depths compared to those without. Obviously, MOSFETs can switch from E-mode to D-mode after recess etching; unfortunately, I_{DS} and R_{on} are sacrificed. A summarizing state-of-the-art of breakdown and R_{on} performance for the E-mode Ga_2O_3 were shown in Table 2. The breakdown voltage presented the best performance in this work. In future work, the device structure will be further improved for high I_{DS} and low R_{ON} .

Conclusion

Heteroepitaxial β - Ga_2O_3 films have been successfully grown on sapphire substrate demonstrating that MOSFETs can be switched from depletion to enhancement mode by gate-recessing. It is shown the different etching depths significantly impact device electrical performance including threshold voltage, maximum current, and breakdown voltage. In this study, the maximum breakdown voltage was 770 V and maximum current attained was 140 $\mu A/mm$. Normally β - Ga_2O_3 MOSFET channel regions are doped by ion-implantation, here we instigate a novel in situ doping method using TEOS during MOCVD. Further improvements will focus on increasing device saturation current and decreasing source and drain ohmic contact resistance so that this device structure and process can employed for future high-power applications.

Acknowledgements This study was supported by the Wafer Works Corporation and National Science and Technology (NSTC), Taiwan, R.O.C., under the Grants NSTC 109-2221-E-009-143-MY3, 109-2622-E-009-033, 109-2634-F-009-028, 109-2224-E-009-002, 110-2218-E-002-037, 112-2622-8-A49-013-SB, 111-2923-E-A49-003-MY3 and 110-2218-E-A49-020-MBK. We acknowledge MAték, for funding and material measurement supporting (Grant Number: 2022-T-018). We also thank Taiwan Semiconductor Research Institute (TSRI) for the processing facility supporting.

Author contributions C.H.L designed and processing experiments. F.G.T grew the Ga_2O_3 epilayers. Y.C.K did the electrical measurements. N.T measured device characteristic. J. M. S and S.H.H analyzed the electrical data. C.L.H designed the experiments. R.H.H analyzed, verified the data and organized the paper. All authors read and approved the final version of the manuscript.

Data availability Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Declarations

Competing interests The authors declare no competing interests.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

References

1. Higashiwaki M, Jessen GH. Guest editorial: the dawn of gallium oxide microelectronics. *Appl Phys Lett*. 2018;112(6):060401. <https://doi.org/10.1063/1.5017845>.
2. Onuma T, et al. Valence band ordering in β -Ga₂O₃ studied by polarized transmittance and reflectance spectroscopy. *Jap J Appl Phys*. 2015;54(11):112601. <https://doi.org/10.7567/JJAP.54.112601>.
3. Jessen, G.H. et al., Toward realization of Ga₂O₃ for power electronics applications. In: 2017 75th Annual Device Research Conference (DRC), pp. 1–2 (2017)
4. Higashiwaki M, et al. Recent progress in Ga₂O₃ power devices. *Semicond Sci Technol*. 2016;31(3):034001. <https://doi.org/10.1088/0268-1242/31/3/034001>.
5. Alema F, Hertog B, Osinsky A, Mukhopadhyay P, Toporkov M, Schoenfeld WV. Fast growth rate of epitaxial β -Ga₂O₃ by close coupled showerhead MOCVD. *J Crystal Growth*. 2017;475:77–82. <https://doi.org/10.1016/j.jcrysgro.2017.06.001>.
6. Park J-H, McClintock R, Razeghi M. Ga₂O₃ MOSFET on sapphire substrate by MOCVD. *Semicond Sci Technol*. 2019;34(8):08LT01. <https://doi.org/10.1088/1361-6641/ab2c17>.
7. Wong MH, Sasaki K, Kuramata A, Yamakoshi S, Higashiwaki M. Electron channel mobility in silicon-doped Ga₂O₃ MOSFETs with a resistive buffer layer. *Jap J Appl Phys*. 2016;55(12):1202B9. <https://doi.org/10.7567/JJAP.55.1202B9>.
8. Shen YS, Wang WK, Horng RH. Characterizations of metal-oxide-semiconductor field-effect transistors of ZnGaO grown on sapphire substrate. *IEEE J Electron Dev Soc*. 2017;5(2):112–6. <https://doi.org/10.1109/JEDS.2017.2653419>.
9. Lv Y, et al. Influence of gate recess on the electronic characteristics of β -Ga₂O₃ MOSFETs. *Superlattices Microstruct*. 2018;117:132–6. <https://doi.org/10.1016/j.spmi.2018.03.013>.
10. Chabak KD, et al. Recessed-gate enhancement-mode β -Ga₂O₃ MOSFETs. *IEEE Electron Device Lett*. 2018;39(1):67–70. <https://doi.org/10.1109/LED.2017.2779867>.
11. Higashiwaki M, Sasaki K, Kuramata A, Masui T, Yamakoshi S. Gallium oxide (Ga₂O₃) metal-semiconductor field-effect transistors on single-crystal β -Ga₂O₃ (010) substrates. *Appl Phys Lett*. 2012;100(1):013504. <https://doi.org/10.1063/1.3674287>.
12. Sood A, et al. Electrical performance study of Schottky barrier diodes using ion implanted β -Ga₂O₃ epilayers grown on sapphire substrates. *Mater Today Adv*. 2023;17:100346. <https://doi.org/10.1016/j.mtadv.2023.100346>.
13. Horng RH, Sood A, Tarntair FG, Wu DS, Hsiao CL, Pratap SJ. Ion implantation effects on the characteristics of β -Ga₂O₃ epilayers grown on sapphire by MOCVD. *Ceram Int*. 2022. <https://doi.org/10.1016/j.ceramint.2022.08.202>.
14. Chikoidze E, et al. P-type β -gallium oxide: a new perspective for power and optoelectronic devices. *Mater Today Phys*. 2017;3:118–26. <https://doi.org/10.1016/j.mtphys.2017.10.002>.
15. Chabak KD, et al. Enhancement-mode Ga₂O₃ wrap-gate fin field-effect transistors on native (100) β -Ga₂O₃ substrate with high breakdown voltage. *Appl Phys Lett*. 2016;109(21):213501. <https://doi.org/10.1063/1.4967931>.
16. Hu Z, et al. Enhancement-mode Ga₂O₃ vertical transistors with breakdown voltage >1 kV. *IEEE Electron Dev Lett*. 2018;39(6):869–72. <https://doi.org/10.1109/LED.2018.2830184>.
17. Kamimura T, Nakata Y, Wong MH, Higashiwaki M. Normally-off Ga₂O₃ MOSFETs with unintentionally nitrogen-doped channel layer grown by plasma-assisted molecular beam epitaxy. *IEEE Electron Dev Lett*. 2019;40(7):1064–7. <https://doi.org/10.1109/LED.2019.2919251>.
18. Ge L, et al. Enhancement mode Ga₂O₃ field effect transistor with local thinning channel layer. *Crystals*. 2022;12(7):897. <https://doi.org/10.3390/cryst12070897>.
19. Kachhawa P, Chaturvedi N. Simulation of β -Ga₂O₃ based MOSFETs for depletion and enhancement mode operation. Berlin: Springer; 2021.
20. Do H-B, Phan-Gia A-V, Nguyen VQ, De Souza MM. Optimization of normally-off β -Ga₂O₃ MOSFET with high Ion and BFOM: A TCAD study. *AIP Adv*. 2022;12(6):065024. <https://doi.org/10.1063/5.0094418>.
21. Chabak KD, et al. Recessed-gate enhancement-mode-Ga₂O₃ MOSFETs. *IEEE Electron Dev Lett*. 2018;39:67–70. <https://doi.org/10.1109/LED.2017.2779867>.
22. Wong MH, Nakata Y, Kuramata A, Yamakoshi S, Higashiwaki M. Enhancement-mode Ga₂O₃ MOSFETs with Si-ion-implanted source and drain. *Appl Phys Express*. 2017;10:041101. <https://doi.org/10.7567/APEX.10.041101>.
23. Jeong YJ, Yang JY, Lee CH, Park R, Lee G, Chung RBK, Yoo G. Influence of gate recess on the electronic characteristics of β -Ga₂O₃ MOSFETs. *Appl Surf Sci*. 2021;558:149936. <https://doi.org/10.1016/j.apsusc.2021.149936>.
24. Yoon Y, Kim MJ, Cho BJ, Shin M, Hwang WS. An 8-nm-thick Sn-doped polycrystalline β -Ga₂O₃ MOSFET with a normally off operation. *Appl Phys Lett*. 2021;119:122103. <https://doi.org/10.1063/5.0065244>.

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.