Design of CMOS RF-Switches for a Multi-Band Radio Front-End

Master Thesis
Division of Electronic Devices
by

Anders Hedberg

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Supervisor: Håkan Träff, Acreo AB
Examiner: Aziz Oacha

Linköping 28 October 2003
A study has been made in CMOS RF-switches that can be used in the front-end of a multi-band radio targeting the 802.11a,b,g and W-CDMA standards and working in the frequency range 2.4-5.5GHz. Especially, one single-transistor switch and two types of transmission gates have been analyzed, simulated and compared with respect to loss, linearity, compression point and noise. From this, five different single-transistor switches have been designed for on-chip probing measurements. Special consideration has been taken to accommodate on-chip testing, thus additional structures have been designed. The simulations and design has been performed with Chartered 0.18μm RF-CMOS process.

The results from the simulations show that the single-transistor switch has better performance in loss, linearity, compression point and noise compared to the transmission gates. However, for the transmission gates the linearity can be increased beyond the linearity of the single-transistor switch if the widths of the transistors are made sufficiently large.

For the single-transistor switch, simulation results show that the transistor length shall be kept to its minimum for best performance and that the number of fingers does not influence significantly. Also, there are optimum values for the loss in on-mode, the noise and the linearity and worst-case values for the loss in off-mode when the transistor width is varied. Consequently, the single-transistor switch can be tuned by its transistor width to accommodate desired performances.

Nyckelord
Keyword
Switch, CMOS, RF, front-end, radio, SoC
Abstract

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## Terminology

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<td>Eswitch</td>
<td>Embedded switch</td>
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<tr>
<td>ETG</td>
<td>Enhanced transmission gate</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
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<tr>
<td>GSG</td>
<td>Ground-signal-ground</td>
</tr>
<tr>
<td>IIP&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Input referred third order intermodulation intercept point</td>
</tr>
<tr>
<td>IL</td>
<td>Insertion loss</td>
</tr>
<tr>
<td>IP&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Third order intermodulation intercept point</td>
</tr>
<tr>
<td>LNA</td>
<td>Low noise amplifier</td>
</tr>
<tr>
<td>LO</td>
<td>Local oscillator</td>
</tr>
<tr>
<td>NF</td>
<td>Noise figure</td>
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<tr>
<td>OIP&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Output referred third order intermodulation intercept point</td>
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<tr>
<td>P&lt;sub&gt;1dB&lt;/sub&gt;</td>
<td>1dB compression point</td>
</tr>
<tr>
<td>PA</td>
<td>Power amplifier</td>
</tr>
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<td>P&lt;sub&gt;lin&lt;/sub&gt;</td>
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<td>S&lt;sub&gt;Eswitch&lt;/sub&gt;</td>
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<td>SNR</td>
<td>Signal to noise ratio</td>
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<td>S&lt;sub&gt;open&lt;/sub&gt;</td>
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<td>S&lt;sub&gt;switch&lt;/sub&gt;</td>
<td>S-parameters of the switch</td>
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<td>S&lt;sub&gt;thru&lt;/sub&gt;</td>
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<td>STS</td>
<td>Single-transistor switch</td>
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<td>TG</td>
<td>Transmission gate</td>
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<tr>
<td>T/R</td>
<td>Transmit/Receive</td>
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1 Introduction

1.1 Background

In many RF applications it is desirable to switch an analog signal on and off without making any impact on the signal. Particularly this is relevant in the front-end of a multi-band radio transceiver where the received and transmitted signals have to be switched between different antennas, filters, amplifiers and mixers (see figure 1.1). This is also the case in the SocTRix project at Acreo AB in which this thesis is involved. SocTRix (Socware Transceiver Demonstrator Project) is a research-oriented project to develop enabling technologies for wideband, multi-mode, multi-band radio terminals for wireless communications [1]. The target of the project is a fully functional, highly integrated, and low power transceiver demonstrator.

![Figure 1.1](image-url)  
*Figure 1.1 Example on how switches can be used in a radio front-end.*
Integrated radio circuits have usually been using GaAs FET transistors due to their good performance at high frequencies. However, as the size and speed of MOSFET transistors has decreased, CMOS is becoming increasingly interesting for RF applications. This is a great advantage since thus theoretically the same CMOS process can be applied for the whole system, both analog and digital.

1.2 Purpose of the Thesis

The purpose of this thesis is to investigate different ways to design switches in CMOS technology, constructed to switch a high frequency analog signal on and off, and to decide which parameters that are critical for such a switch. Also, the aim is to make simulations and chip layouts for some interesting switch topologies, and to carefully consider layout properties to minimize errors and make accurate measurements on chip possible. Results from measurements shall be compared with simulated results and also be applied to a model of the switch that can be used in any application.

Simulations and layout work are made in Cadence CAD tools and Chartered 0.18µm RF-CMOS process with supply voltage $V_{dd} = 1.8V$. As the SocTRix project targets the 802.11a,b,g and W-CDMA standards, frequencies of 2.5GHz and 5.5GHz are of special interest in the simulations.

1.3 Outline of the Document

In chapter 2 there is a review over some switch solutions suggested in the literature and a discussion on their advantages and disadvantages. Chapter 3 considers three particularly interesting switch circuits that will be used in simulations. Chapter 4 explains the definitions of parameters that are important for a switch and used as key parameters in the simulations. All simulation results from the three switch circuits are included in Chapter 5 together with comparisons and conclusions about which switch to use in the layout.

Chapter 6 discusses strategies in the chip layout work and explains the parts of the layout. From the layout it is possible to make simulations with extracted parasitics and the results are presented in chapter 7. Chapter 8 describes how a switch can be modeled and a method called de-embedding in which parasitics in the layout and in measurement equipment can be eliminated mathematically by adding dummy circuits to the layout.

Finally chapter 9 draws conclusions from the thesis work and suggests further work in future.
2 Pre-Studied Circuits

2.1 Introduction

There are a lot of studies concerning analog switches for RF applications in the literature. Critical parameters for all of them are loss and linearity. Here, three types of switch solutions are presented with some of their advantages and disadvantages.

2.2 T/R Switch

One problem that occurs in the front-end of a radio transceiver is how to switch between the transmitted and the received signal to the antenna (see figure 1.1 in chapter 1). This is usually solved with a T/R (Transmit/Receive) switch like in figure 2.1 [2]. For transmitting, \( V_1 \) goes high and \( V_2 \) goes low, turning transistor M1 and M4 on and transistor M2 and M3 off. For receiving, \( V_1 \) goes low and \( V_2 \) goes high, turning M1 and M4 off and M2 and M3 on. M3 and M4 shunt the signal in receive- and transmit-mode respectively and thus increase isolation. Capacitance \( C_1 \) and \( C_2 \) allow DC biasing of the transmitting and receiving nodes. The purpose of resistance \( R_1 \), \( R_2 \), \( R_3 \) and \( R_4 \) is to improve DC bias isolation and has a value of about 10kΩ. This circuit has very good isolation in off-mode but suffer from high loss in on-mode because of the shunt transistors. It also has non-linear properties when the power of the signal increases.

![T/R Switch Diagram](image_url)
2.3 LC-Resonance Switch

An interesting alternative to a T/R switch is suggested in [3]. It consists of switchable LC-resonance circuits as in figure 2.2. In off-mode, transistor M1 and M2 are on which will cause inductance L and capacitance C\textsubscript{1} to form a band-stop filter with \(\omega\text{stop} = 1/\sqrt{LC_1}\) that will cut the signal. In on-mode M1 and M2 are off which will cause L and capacitance C\textsubscript{2} to form a band-pass filter with \(\omega\text{pass} = 1/\sqrt{LC_2}\) that will let the signal through. In this way the signal does not have to pass the transistors. This is interesting because transistors are non-linear and distort signals, especially at high signal powers. One problem though is to design an inductor with an acceptable tolerance. Another disadvantage is that only signals at a specific frequency can be switched.

![LC-Resonance Switch Diagram](image)

**Figure 2.2** LC-resonance switch.

2.4 Bootstrapped Switch

Distortion caused by the non-linearity in the transistor is a main problem for all switches. The non-linearity is mainly due to the fact that the voltage difference between gate and channel is not constant. This problem can be handled by a bootstrapped switch [4]. Its fundamental function in off- and on-mode is explained in figure 2.3 and 2.4 respectively where transistor M1 is switching the signal. In off-mode switch S3, S4 and S5 are on and switch S1 and S2 are off. This charges capacitance C to V\textsubscript{dd} and turns M1 off.

In on-mode S3, S4 and S5 are off and S1 and S2 are on. Now the gate of M1 will have a voltage of V\textsubscript{dd} plus the channel voltage and M1 turns on. This will make the gate-to channel voltage constant and thus M1 more linear. However, to maintain the high linearity it is important to not have too much charge leakage in C if the switch has to stay in on-mode for a long period. Another disadvantage is that a realization of the bootstrapped switch requires at least nine transistors except from M1 and that these transistors increase the loss of the signal in on-mode.
Figure 2.3  Bootstrapped switch in off-mode.

Figure 2.4  Bootstrapped switch in on-mode.
3 Analyzed Circuits

3.1 Introduction

The switch solutions presented in chapter 6 all suffer from high loss in on-mode, low linearity or high complexity. Instead, three other types of switches are here discussed that are easier to realize, analyze and design. These switches are used in the simulations of chapter 9.

3.2 Single-Transistor Switch

The simplest form of switch is the single-transistor switch (STS) where a single NMOS transistor performs the switching function [5]. NMOS is used instead of PMOS since the NMOS has larger transconductance, which provides lower loss per unit area than for the PMOS. A STS can be realized as in figure 3.1 where $R = 10k\Omega$ and $C = 1\text{pF}$. Drain and source are biased equally by $V_{\text{bias}}$ and the switch is turned on and off by $V_C$. The switch is protected from high frequency noise on the bias and control signal by low-pass filters consisting of resistance $R$ and capacitance $C$ with $\omega_{3\text{dB}} = 1/(RC) = 100\text{MHz}$. $R$ is made large to avoid any loss of the signal at drain and source and to decrease the fluctuations of $V_{\text{gd}}$ and $V_{\text{gs}}$. These fluctuations affect the linearity of the transistor and may also result in excessive voltage across the gate dielectric and cause breakdown [2]. As can be seen from the schematic, the switch is symmetric, i.e. there is no difference between input and output.

![Figure 3.1 Single-transistor switch.](image)

The NMOS transistor shall work in the linear region. Assuming $v_{\text{in}} = v_{\text{out}}$, the conditions for this are

\[
\begin{align*}
\text{off mode: } & \quad V_{\text{gs}} < V_T \Rightarrow V_{C,\text{off}} - V_{\text{bias,off}} - v_{\text{in}} \leq V_T \\
& \quad v_{\text{in}} > V_{C,\text{off}} - V_{\text{bias,off}} - V_T
\end{align*}
\]  
(3.1)
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on mode: \[
\begin{align*}
V_{gs} > V_T & \Rightarrow V_{C,on} - V_{bias,on} - V_{in} > V_T \Rightarrow V_{in} < V_{C,on} - V_{bias,on} - V_T \\
V_{ds} << V_{gs} - V_T & \Rightarrow V_{ds} << V_{C,on} - V_{bias,on} - V_{in} - V_T
\end{align*}
\]
\[
I_d = k_n \left[2(V_{gs} - V_T)V_{ds} - V_{ds}^2\right], \quad k_n = \frac{\mu_n C_{ox} W_n}{2L}
\]

where \(V_{gs}\) is gate-source voltage, \(V_{ds}\) is drain-source voltage, \(V_T = 0.5V\) is threshold voltage, \(V_{C,off}\) is control voltage in off mode, \(V_{C,on}\) is control voltage in on mode, \(V_{bias,on}\) is bias voltage in on mode, \(V_{bias,off}\) is bias voltage in off mode, \(I_d\) is drain current, \(\mu_n \) and \(C_{ox}\) are process parameters, \(W_n\) is transistor width and \(L\) is transistor length [5]. From (3.1) and (3.2) the swing of \(v_{in}\) will be

\[
V_{C,off} - V_{bias,off} - V_T < v_{in} < V_{C,on} - V_{bias,on} - V_T
\]

Setting \(V_{C,off}\) and \(V_{bias,on}\) to zero and \(V_{C,on}\) and \(V_{bias,off}\) to \(V_{dd} = 1.8V\) in (3.5) will maximize the swing of \(v_{in}\) to \(-2.3V < v_{in} < 1.3V\) or, for a sinusoidal signal without DC component, \(|v_{in}| < 1.3V\). This choice of control and bias voltage will also put the transistor in its most linear region according to (3.3) and (3.4).

If the signal power is high there will be a significant voltage drop \(V_{ds}\) over the transistor and it will become non-linear according to (3.4). However, at low signal powers the ‘on resistance’, an indication of the loss in on-mode of the switch, of the single transistor switch is approximately

\[
R_{STS} = \frac{V_{in} - V_{out}}{i_d} = \frac{V_{ds}}{I_d} = \frac{1}{2k_n(V_{gs} - V_T)} = \frac{L}{\mu_n C_{ox} W_n (V_{c} - V_{bias} - V_T)} = \frac{L}{1.3\mu_n C_{ox} W_n}
\]

With \(L = 0.18\mu m\) and \(W_n = 100\mu m\), a typical value for \(R_{STS}\) is about 4.8\(\Omega\).

### 3.3 Transmission Gate

As previously mentioned the STS will be non-linear when signal power increase. A well-known way [5] to solve this problem is to connect an NMOS and a PMOS transistor in parallel to form a transmission gate (TG) as in figure 3.2. This will make the ‘on resistance’ of the switch signal independent. As with the STS the bias and control signals are filtered with low-pass filters with \(\omega_{3dB} = 1/(RC) = 100MHz\). The circuit is symmetrically designed and with large \(R\) as in the STS.
The formulas for a PMOS transistor in the linear region are the same as for a NMOS but with opposite signs on the voltages:

**off mode:**
\[
V_{sg} < V_T \Rightarrow V_{bias,off} + v_{in} - V'_{C,off} < V_T \Rightarrow v_{in} < V'_{C,off} - V_{bias,off} + V_T
\]

**on mode:**
\[
V_{sg} > V_T \Rightarrow V_{bias,off} + v_{in} - V'_{C,off} > V_T \Rightarrow v_{in} > V'_{C,off} - V_{bias,off} + V_T
\]

\[I_d = k_p \left[ 2(V_{sg} - V_T) V_{sd} - V_{sd}^2 \right], \quad k_p = \frac{\mu_p C_{ox} W_p}{2L}\]

where \(V'_{C,off}\) is the control voltage of the PMOS in off mode, \(V'_{C,off}\) is the control voltage of the PMOS in on mode, \(\mu_p\) is a process parameter and \(W_p\) is the width of the PMOS [5]. \(L\) is the same for both NMOS and PMOS. From (3.7) and (3.8) the swing of \(v_{in}\) over the PMOS will be

\[V'_{C,off} - V_{bias,off} + V_T < v_{in} < V'_{C,off} - V_{bias,off} + V_T\]

To maximize the swing, \(V'_{C,off}\) shall be zero and \(V'_{C,off}\) shall be \(V_{dd}=1.8V\). The bias voltage has to be decided another way since it influence the swing over the NMOS as well. Using (3.1) and (3.7) gives

\[V_{bias,off} - V_T < V_{bias,off} + v_{in} < V'_{C,off} - V_T \Rightarrow -0.5V < V_{bias,off} + v_{in} < 2.3V\]

which indicates a value of 0.9V for \(V_{bias,off}\). In the same way (3.2) and (3.7) gives

\[V'_{C,off} + V_T < V_{bias,off} + v_{in} < V'_{C,off} - V_T \Rightarrow 0.5V < V_{bias,off} + v_{in} < 1.3V\]
which indicates a value of 0.9V for $V_{\text{bias, on}}$ too. Consequently, the bias signal in the TG shall constantly be 0.9V. This turns the voltage swings over the NMOS and PMOS in (3.5) and (3.11) to be

\[
\begin{align*}
-1.4V < v_{in} < 0.4V \\
-0.4V < v_{in} < 1.4V
\end{align*}
\Rightarrow -0.4V < v_{in} < 0.4V \Rightarrow |v_{in}| < 0.4V
\]

(3.14)

Thus the TG seems to have very poor capacity to handle signals with high power.

To show that the “on resistance” of the TG is signal independent, (3.4) and (3.10) can be used to calculate the current through the switch. Assuming that $k_n = k_p = k$ gives

\[
i_d = k_n \left[ 2(v_{gs} - V_T) v_{ds} - V_n^2 \right] + k_p \left[ 2(v_{sg} - V_T) v_{sd} - V_p^2 \right] = \\
k \left[ 2(V_C - v_{out} - V_{\text{bias}} - V_T)(v_{in} - v_{out}) - (v_{in} - v_{out})^2 \right] + \\
k \left[ 2(v_{in} + V_{\text{bias}} - V_C - V_T)(v_{in} - v_{out}) - (v_{in} - v_{out})^2 \right] = \\
= 2k(V_C - V_T)(v_{in} - v_{out}) - 2k v_{out}(v_{in} - v_{out}) - 2k V_{\text{bias}}(v_{in} - v_{out}) - k(v_{in} - v_{out})^2 - \\
- 2k(V_C + V_T)(v_{in} - v_{out}) + 2k v_{out}(v_{in} - v_{out}) + 2k V_{\text{bias}}(v_{in} - v_{out}) - k(v_{in} - v_{out})^2 = \\
= 2k(V_C - V_C' - 2V_T)(v_{in} - v_{out}) + 2k(v_{in} - v_{out})(v_{in} - v_{out}) - 2k(v_{in} - v_{out})^2 = \\
= 2k(V_C - V_C' - 2V_T)(v_{in} - v_{out}) \Rightarrow \\
\Rightarrow R_{\text{TG}} = \frac{(v_{in} - v_{out})}{i_d} \frac{1}{2k(V_C - V_C' - 2V_T)} = \frac{L}{\mu_n C_{ox} W_n (V_C - V_C' - 2V_T)} = \frac{L}{0.8 \mu_n C_{ox} W_n}
\]

which is signal independent. With $L = 0.18\mu\text{m}$ and $W_n = 100\mu\text{m}$, a typical value for $R_{\text{TG}}$ is about 7.7Ω. Comparing (3.15) with (3.6), assuming equal $L$ and $W_n$, shows that the TG has higher “on resistance” than the single transistor switch and may thus have a higher loss in on-mode. The relationship between the NMOS and the PMOS in the TG is

\[
k_n = k_p \Rightarrow \frac{\mu_n C_{ox} W_n}{2L} = \frac{\mu_p C_{ox} W_p}{2L} \Rightarrow W_p = \frac{\mu_n}{\mu_p} W_n = 4.62 W_n
\]

(3.16)

where $\mu_n$ and $\mu_p$ are process parameters. Hence, the PMOS must be 4.62 times larger than the NMOS and thus the TG consumes much more chip area than the STS.

### 3.4 Enhanced Transmission Gate

As mentioned earlier the TG suffers from poor capacity to handle high power signals. It also has higher “on resistance” than the STS. To address this, an enhanced transmission gate (ETG) like in figure 3.3 can be used. It is equal to the TG but the NMOS and PMOS transistor are biased separately with $V_{\text{bias}}$ and $V'_{\text{bias}}$ respectively. $C_C$ act as coupling capacitors to separate the different bias voltages and have values high enough to not influence the signal, thus making comparison with the STS and TG possible. For frequencies in the GHz range this means $C_C = 1\mu\text{F}$. However, such a high value is too large for on-chip layout and can only be used in simulations.
Figure 3.3 Enhanced transmission gate.

The signal swing is now expressed from (3.2) and (3.8) as

$$\begin{align*}
V_{C,\text{off}} - V_{\text{bias,off}} - V_T < v_{\text{in}} < V_{C,\text{on}} - V_{\text{bias,on}} - V_T \\
V'_{\text{C,off}} - V'_{\text{bias,off}} + V_T < v_{\text{in}} < V'_{\text{C,off}} - V'_{\text{bias,off}} + V_T
\end{align*} \tag{3.17} \tag{3.18}$$

Setting $V_{C,\text{off}} = V'_{\text{bias,off}} = V_{\text{bias,off}} = V_{C,\text{on}} = 0$ and $V_{C,\text{on}} = V_{\text{bias,off}} = V'_{\text{C,off}} = V'_{\text{bias,off}} = V_{\text{dd}} = 1.8V$ optimizes the signal swing to

$$\begin{align*}
-2.3V < v_{\text{in}} < 1.3V \\
-1.3V < v_{\text{in}} < 2.3V \Rightarrow -1.3V < v_{\text{in}} < 1.3V \Rightarrow |v_{\text{in}}| < 1.3V
\end{align*} \tag{3.19}$$

which is much better than (3.14) for the TG and equal to the STS.

Using the same method as in (3.15) it can be shown that the “on resistance” of the ETG is

$$R_{\text{ETG}} = \frac{L}{\mu_n C_{\text{ox}} W_n \left( V_C + V'_{\text{bias}} - V_{\text{bias}} - V'_C - 2V_T \right)} = \frac{L}{2.6\mu_n C_{\text{ox}} W_n} \tag{3.20}$$

With $L = 0.18\mu m$ and $W_n = 100\mu m$, a typical value for $R_{\text{ETG}}$ is about $2.4\Omega$. Comparing (3.20) with (3.15) and (3.6), assuming equal $L$ and $W_n$, shows that the ETG has lower “on resistance” than both the single transistor switch and the TG or

$$R_{\text{ETG}} < R_{\text{STS}} < R_{\text{TG}} \tag{3.21}$$

indicating a lower loss for the ETG in on-mode. (3.21) can be rewritten to a relative comparison as

$$R_{\text{ETG}} : R_{\text{STS}} : R_{\text{TG}} \Rightarrow 0.38 : 0.77 : 1.3 \tag{3.22}$$
3.5 Summary

The properties of the three switches presented in this chapter are summarized in table 3.1. The STS has a wide swing and thus good capacity to handle high power signals. For low signal powers, the “on resistance” is low which indicates low loss in on-mode. Linearity is good for low signal powers but will get bad as the power increase.

The TG has a narrow swing and thus poor capacity to handle high power signals. For low signal powers, the “on resistance” is high which indicates high loss in on-mode. Linearity is very good at low signal power but will get bad as the power increase.

The ETG has a wide swing and thus good capacity to handle high power signals. For low signal powers, the “on resistance” is very low which indicates very low loss in on-mode. Linearity is very good at both low and high signal powers.

<table>
<thead>
<tr>
<th>Switch</th>
<th>Signal Swing</th>
<th>Loss in On-Mode at Low Signal Power</th>
<th>Linearity</th>
</tr>
</thead>
<tbody>
<tr>
<td>STS</td>
<td>Good</td>
<td>Low</td>
<td>Low Signal Power: Good, High Signal Power: Bad</td>
</tr>
<tr>
<td>TG</td>
<td>Bad</td>
<td>High</td>
<td>Low Signal Power: Very good, High Signal Power: Bad</td>
</tr>
<tr>
<td>ETG</td>
<td>Good</td>
<td>Very low</td>
<td>Low Signal Power: Very good, High Signal Power: Very good</td>
</tr>
</tbody>
</table>

It shall be mentioned that the predictions are only valid for low signal frequencies. As frequency increase, parasitics in the transistors may influence significantly, especially in the TG and ETG, which have two transistors and thus more parasitics than the STS. This will be further examined through the simulations in chapter 5.
4 Measured Parameters

4.1 Introduction

Four parameters turn out to be interesting for simulation of a switch. This chapter explains why and describes their definitions.

4.2 Insertion Loss

Loss is naturally an important parameter for a switch. Too high loss in on-mode will make the signal weak and too low loss in off-mode (isolation) will result in signal leakage. High loss in off-mode is especially important for switches separating the transmitter and the receiver while low loss in on-mode is important for switches before the LNA in the receiver (see figure 1.1 in chapter 1). However, loss can be defined in many different ways. At high frequency measurements, it is common to use S-parameters to describe the properties of a two-port as in figure 4.1. They are based on powers rather than voltages and currents since voltages and currents are difficult to measure at high frequencies. The S-parameters are defined by [6]:

\[
\begin{align*}
    b_1 &= s_{11}a_1 + s_{12}a_2 \\
    b_2 &= s_{21}a_1 + s_{22}a_2
\end{align*} \tag{4.1} \tag{4.2}
\]

Where

- \(a_1 = (\text{incoming power at port 1})^{1/2}\)
- \(b_1 = (\text{outgoing power at port 1})^{1/2}\)
- \(a_2 = (\text{incoming power at port 2})^{1/2}\)
- \(b_2 = (\text{outgoing power at port 2})^{1/2}\)

From (4.1) \(s_{21}\) can be written as

\[
s_{21} = \frac{b_2}{a_1}, \quad a_2 = 0 \tag{4.3}
\]

![Figure 4.1 A two-port.](image-url)
At high frequency measurements, the loss of a device is usually defined as the power loss resulting from the insertion of the device in a transmission line and is simply called insertion loss (IL). It is expressed as the reciprocal of the ratio of the signal power delivered to the part of the line following the device to the signal power delivered to that same part before insertion assuming 50Ω load at port 1 and 2. From this definition and (4.3), insertion loss can be expressed as $1/|s_{21}|^2$ or in decibels

$$\text{IL} = -20\log_{10}|s_{21}|$$

which is the parameter that will be used in the loss measurements. Insertion loss is measured in both on-mode and off-mode.

### 4.3 Linearity

A system that is non-linear and fed with an input signal $x(t)$ will produce harmonics in the output signal $y(t)$ [7]:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots$$  \hspace{1cm} (4.5)

where $\alpha_i$ are constants. The output signal becomes distorted and signal information corrupted. If $x(t) = A\cos(\omega t)$ and (4.5) is restricted to three terms then

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2} \cos(2\omega t) + \frac{\alpha_3 A^3}{4} \cos(3\omega t)$$  \hspace{1cm} (4.6)

Looking at (4.6), the output signal is distorted by a DC component, an amplification of the fundamental tone and harmonics at the second and third tone. The harmonics contribute to signal information corruption. In this case however, they are at a much higher frequency than the fundamental and can be filtered out easily.

A more troublesome problem called intermodulation occurs if the input signal consists of two interfering signals close in frequency. If $x(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t)$ the output signal, using (4.5) restricted to three terms, becomes after discarding DC terms

$$y(t) = \left(\alpha_1 A + \frac{9\alpha_3 A^3}{4}\right)\cos(\omega_1 t) + \left(\alpha_1 A + \frac{9\alpha_3 A^3}{4}\right)\cos(\omega_2 t) + \alpha_2 A^2 \cos((\omega_1 + \omega_2) t) + \alpha_2 A^2 \cos((\omega_1 - \omega_2) t) + \frac{3\alpha_3 A^3}{4} \cos((2\omega_1 + \omega_2) t) + \frac{3\alpha_3 A^3}{4} \cos((2\omega_1 - \omega_2) t) + \frac{3\alpha_3 A^3}{4} \cos((2\omega_2 + \omega_1) t) + \frac{3\alpha_3 A^3}{4} \cos((2\omega_2 - \omega_1) t)$$  \hspace{1cm} (4.7)

With a small difference between $\omega_1$ and $\omega_2$, the third-order intermodulation tones at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will be very close to the fundamental tones at $\omega_1$ and $\omega_2$. This is a problem because if two interferers that are close in frequency to a desired channel pass a non-linear system, their intermodulation tones will fall into the desired channel as shown in figure 4.2.
This problem is so common and so critical that there is a special parameter for it called third-order intercept point (IP$_3$). It is defined as the point where the function of the dominant term for the fundamental tone $\alpha_1A$ crosses the function of the term for the intermodulation tones $3\alpha_3A^3/4$ when $A$ is variable. See figure 4.3 where the functions are plotted on a logarithmic scale and can be treated as the powers of the fundamental tone and the third-order intermodulation tone. $P_{\text{in}}$ is the input power. Usually, power is measured in dBm = $10\log_{10}(P_{\text{10}}}^3)$ where $P$ is the power. Ideally, the angle of the power functions shall be one for the fundamental tone and three for the intermodulation tone. The third-order intercept point is measured as the input IP$_3$ (IIP$_3$) or the output IP$_3$ (OIP$_3$). As linearity is depending on power, it especially important for switches after the PA in the receiver to have good linearity (see figure 1.1 in chapter 1).
\[ P_{\text{lin}} = P_{1, \text{dBm}} - P_{3, \text{dBm}} = 10 \log_{10} (10^3 P_1) - 10 \log_{10} (10^3 P_3) = 10 \log_{10} \left( \frac{P_1}{P_3} \right) \Rightarrow \]
\[ \Rightarrow 10 \frac{P_{1, \text{dBm}} - P_{3, \text{dBm}}}{10} = P_1 - P_3 \]

where \( P_1 \) and \( P_2 \) are the real powers of the fundamental tone and the third order intermodulation tone respectively. (4.8) indicates that the difference between the powers in dBm corresponds to the ratio of the real powers. The linearity is measured in on-mode and with \( \omega_2 - \omega_1 = 20 \text{MHz} \).

### 4.4 1dB Compression Point

For low power signals the switches in chapter 3 will work properly but as the power increase, the switching function will fail. As for the linearity this is critical for switches after the PA in the receiver (see figure 1.1 in chapter 1). To measure how much power that can be delivered the 1dB compression point can be used (\( P_{1\text{dB}} \)). It is defined as the input signal power that causes the small signal gain to drop by 1dB, see figure 4.4. The compression point is measured in on-mode.

![Figure 4.4](image.png)

**Figure 4.4** Definition of the 1dB compression point.

### 4.5 Noise Figure

Finally, it is interesting to measure how much noise that is generated by a switch. Too much noise will corrupt the signal and make it hard to detect for systems after the switch. Hence, low noise is especially important for switches before the LNA in the receiver (see figure 1.1 in chapter 1). In RF design, noise is usually measured by the noise figure (NF) defined as

\[ NF = 10 \log_{10} \frac{SNR_{\text{in}}}{SNR_{\text{out}}} \]  

(4.9)
where $\text{SNR}_{\text{in}}$ is the ratio of the input signal power to the input noise power and $\text{SNR}_{\text{out}}$ is the ratio of the output signal power to the output noise power. Therefore, for a noiseless system $\text{SNR}_{\text{in}} = \text{SNR}_{\text{out}}$ and $\text{NF} = 0$, independently of the gain of the system since the input signal and input noise are amplified equally. The noise figure is measured in on-mode.
5 Simulation

5.1 Introduction

The three switches from chapter 3 are simulated one by one and the results are compared. The bias and control signals change according to table 5.1 and the input and output of the switches are terminated with 50Ω impedance. Frequencies of interest are 2.5GHz and 5.5GHz. For the TG and the ETG, widths are measured as the total width of the NMOS and PMOS transistor, which with (3.16) gives

\[
\begin{align*}
W &= W_n + W_p \\
W_p &= 4.62W_n \\
&\Rightarrow W_n = 0.178W \\
&\Rightarrow W_p = 0.822W
\end{align*}
\]

Table 5.1 Bias and control signals

<table>
<thead>
<tr>
<th>Switch</th>
<th>Signal</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>STS</td>
<td>(V_{\text{bias}})</td>
<td>1.8V</td>
</tr>
<tr>
<td></td>
<td>(V_C)</td>
<td>0</td>
</tr>
<tr>
<td>TG</td>
<td>(V_{\text{bias}})</td>
<td>0.9V</td>
</tr>
<tr>
<td></td>
<td>(V_C)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(V'_{\text{bias}})</td>
<td>1.8V</td>
</tr>
<tr>
<td>ETG</td>
<td>(V_{\text{bias}})</td>
<td>1.8V</td>
</tr>
<tr>
<td></td>
<td>(V_C)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(V'_{\text{bias}})</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(V'_{C})</td>
<td>1.8V</td>
</tr>
</tbody>
</table>

5.2 Models

Simulations are made in Cadence CAD tools and Chartered 0.18μm RF-CMOS process. The simulations are performed with pure circuit models without any extracted parasitics from layout (see chapter 7). However, the circuit models do take parasitics in the transistor into account, such as capacitance, inductance and resistance between gate, source, drain and substrate.

5.3 Single-Transistor Switch

Three variables can be changed in a transistor; the length, the width and number of fingers. The fingers are the gate of the transistor and divide the width, resulting in constant width per finger (see figure 6.1 in chapter 6). Thus, the STS is simulated with varying fingers \((F)\), length \((L)\), and width \((W)\).
5.3.1 Fingers Variable

In these simulations, the number of fingers varies from 1 to 40 with the length and width constant to 0.18µm and 100µm respectively. Figure 5.1 to 5.6 show that insertion loss in on- and off-mode, noise figure, 1dB compression point and linearity are weakly influenced by the number of fingers at both 2.5GHz and 5.5GHz. It is only in the extreme case of one or very few fingers that the insertion loss in on-mode becomes high.

![Figure 5.1](image1.png)  ![Figure 5.2](image2.png)

Figure 5.1 IL in on-mode with varying fingers F for the STS.

Figure 5.2 IL in off-mode with varying fingers F for the STS.

![Figure 5.3](image3.png)  ![Figure 5.4](image4.png)

Figure 5.3 NF with varying fingers F for the STS.

Figure 5.4 P_{1dB} with varying fingers F for the STS.

![Figure 5.5](image5.png)  ![Figure 5.6](image6.png)

Figure 5.5 P_{lin} with varying fingers F at 2.5GHz for the STS.

Figure 5.6 P_{lin} with varying fingers F at 5.5GHz for the STS.
5.3.2 Length Variable

Having the width and number of fingers constant to 100μm and 11 respectively, simulations with the length varied from 0.18μm to 2.88μm are presented in figure 5.7 to 5.12. For all parameters except the insertion loss in off-mode, the length shall be as short as possible. For the insertion loss in on-mode, this corresponds well to the expression for $R_{STS}$ in (3.6). Choosing $L = 0.18μm$ generate an insertion loss in off-mode of 40.3dB at 2.5GHz and 33.5dB at 5.5GHz which is probably sufficient for most applications.

![Figure 5.7](image1)  
**Figure 5.7** IL in on-mode with varying length $L$ for the STS.

![Figure 5.8](image2)  
**Figure 5.8** IL in off-mode with varying length $L$ for the STS.

![Figure 5.9](image3)  
**Figure 5.9** NF with varying length $L$ for the STS.

![Figure 5.10](image4)  
**Figure 5.10** $P_{1dB}$ with varying length $L$ for the STS.

![Figure 5.11](image5)  
**Figure 5.11** $P_{lin}$ with varying length $L$ at 2.5GHz for the STS.

![Figure 5.12](image6)  
**Figure 5.12** $P_{lin}$ with varying length $L$ at 5.5GHz for the STS.
5.3.3 Width Variable

From the simulations with varying length it is obvious that \( L \) shall be kept to its minimum 0.18\( \mu \)m. The simulations with varying fingers indicate that \( F \) can be chosen freely. If the number of fingers is chosen so that the transistor has a square appearance in the layout, it results in minimized chip area. This is approximately achieved if \( F = 1.1W^{0.51} \) when \( L = 0.18\mu m \). Additionally, setting the number of fingers to an odd value will generate a symmetric transistor. With these values of \( F \) and \( L \) the width is varied from 100\( \mu \)m to 1600\( \mu \)m and the simulation results are shown in figure 5.13 to 5.18. Obviously, there are optimums for the insertion loss in on-mode and for the noise figure at both 2.5GHz and 5.5GHz. For the insertion loss in off-mode there is a worst-case at both frequencies. Table 5.2 summarizes the optimum values. The values for insertion loss in on-mode and noise figure are better at 2.5GHz than 5.5GHz because of frequency sensitive parasitics in the transistor.

Table 5.2 Optimums for the STS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>2.5GHz</th>
<th></th>
<th>5.5GHz</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Optimum [dB]</td>
<td>Width [( \mu )m]</td>
<td>Optimum [dB]</td>
<td>Width [( \mu )m]</td>
</tr>
<tr>
<td>IL on-mode</td>
<td>0.462</td>
<td>210</td>
<td>0.73</td>
<td>125</td>
</tr>
<tr>
<td>IL off-mode (worst-case)</td>
<td>22.5</td>
<td>1560</td>
<td>22.5</td>
<td>700</td>
</tr>
<tr>
<td>NF</td>
<td>0.19</td>
<td>800</td>
<td>0.334</td>
<td>400</td>
</tr>
</tbody>
</table>

Figure 5.16 shows that the 1dB compression point increases with increasing width. According to figure 5.17 and 5.18, the linearity change considerably with input power and width. At low input powers, widths around 100\( \mu \)m give best linearity at both 2.5GHz and 5.5GHz. As input power increase, switches with larger widths have an abrupt increase in linearity and become even better than switches with small widths. This can be useful if the input power is constant but usually power fluctuates and thus a more constant decreasing linearity as for switches with small widths is preferable.
5.4 Transmission Gate

For the TG and the ETG, length and number of fingers are chosen from the simulation results of the STS, i.e. \( L = 0.18 \mu m \) and \( F = 1.1W^{0.51} \) odd. The simulation results with varied width for the TG can be seen in figure 5.19 to 5.24. As for the STS, there are optimums for the insertion loss in on-mode and for the noise figure at both 2.5GHz and 5.5GHz. Also, there is a worst case for the insertion loss in off-mode at both frequencies. Both 1dB compression point and linearity increase with increasing width. Furthermore, linearity is approximately constantly decreasing for all widths when input power is increasing.
Design of CMOS RF-Switches for a Multi-Band Radio Front-End

5.5 Enhanced Transmission Gate

As mentioned earlier, simulations for the ETG are carried out with $L = 0.18 \mu m$ and $F = 1.1W^{0.51}$ odd. Simulation results with varied width are shown in figure 5.25 to 5.30. Here too there are optimums as for the two other switches and the 1dB compression point increase with increasing width. Figure 5.29 and 5.30 show that linearity is decreasing constantly for all widths at low input powers but as the power increase, there are abrupt fluctuations as for the STS. In addition, it seems like 200\(\mu m\) gives best linearity at 2.5GHz. However, simulations
with larger widths show that the linearity increase infinitely and has a more constant decrease for increasing input power as for the TG.

**Figure 5.25** IL in on-mode with varying width W for the ETG.

**Figure 5.26** IL in off-mode with varying width W for the ETG.

**Figure 5.27** NF with varying width W for the ETG.

**Figure 5.28** $P_{1dB}$ with varying width W for the ETG.

**Figure 5.29** $P_{lin}$ with varying width W at 2.5GHz for the ETG.

**Figure 5.30** $P_{lin}$ with varying width W at 5.5GHz for the ETG.

### 5.6 Comparisons and Conclusions

In figure 5.31, the three switches are compared with respect to their optimum values for insertion loss in on-mode. The STS has lowest loss followed by the ETG and the TG. This
corresponds to table 3.1 in chapter 3 except for the ETG, probably because of parasitics in the transistors. In figure 5.32, the switches are compared with respect to their worst-case values of insertion loss in off-mode. Here the STS has much better result than the TG and ETG. In addition, for the noise figure compared in figure 5.33, the STS has better performance than the TG and ETG. Comparing the 1dB compression point in figure 5.34 and 5.35 shows a great advantage for the STS and the TG at 2.5GHz and no particular difference at 5.5GHz. This does not agree with the predictions in table 3.1 for the signal swing, probably because of parasitics in the transistors.

For the TG and the ETG, the simulations show that linearity can be increased infinitely with larger widths. Thus, to make a fair linearity comparison between the switches, the width of the STS is set equal to the total NMOS and PMOS widths of the TG and the ETG, i.e. \( W_{\text{STS}} = W_n + W_p \). \( W \) is set to 100\( \mu \text{m} \) since this gives best linearity result for the STS. In figure 5.36 and 5.37 the linearity is plotted for the three switches at 2.5GHz and 5.5GHz. Obviously, the STS has best linearity followed by the ETG and the TG for all input powers. This does not correspond to table 3.1, probably because of parasitics in the transistors.

---

**Figure 5.31** Optimal IL in on-mode for the STS (1), TG (2) and ETG (3).

**Figure 5.32** Worst-case IL in off-mode for the STS (1), TG (2) and ETG (3).

**Figure 5.33** Optimal NF for the STS (1), TG (2) and ETG (3).

**Figure 5.34** \( P_{\text{1dB}} \) at 2.5GHz for the STS (1), TG (2) and ETG (3).
From the comparisons above, the switch chosen for layout is the STS. It has the best performance for insertion loss in on- and off-mode, noise figure and 1dB compression point. Additionally, it has the best linearity performance assuming $W_{STS} = W_n + W_p$. From table 5.2 and the results from the linearity simulations, interesting widths to use in the layout are 100$\mu$m, 200$\mu$m, 400$\mu$m, 800$\mu$m and 1600$\mu$m. Consequently, the five switches in the layout will be called switch 100, 200, 400, 800 and 1600. All these switches shall have 0.18$\mu$m transistor length and number of fingers resulting in a square transistor layout.
6 Layout

6.1 Introduction
The five single-transistor switches with width 100\textmu m, 200\textmu m, 400\textmu m, 800\textmu m and 1600\textmu m are designed for on–chip measurements. The layout work is carefully performed to minimize measurement errors and chip area.

6.2 Transistor Layout
The switching NMOS transistor for the five switches has a layout as in figure 6.1. The fingers, i.e. the gate, are connected on both sides of the transistor. Drain and source are connected at the left and right side respectively. There is also a guard ring around the transistor connected to the substrate to protect from noise from surrounding circuits. The guard ring has a gap at the top to avoid induced currents in the ring.

![NMOS transistor layout](image)

**Figure 6.1** NMOS transistor layout.

6.3 Switch Layout
Figure 6.2 to 6.6 shows the layout of each switch. The size of each switch is 300\textmu m x 400\textmu m. At left and right there are GSG (Ground-Signal-Ground) pads with common ground for probing input and output signals. The switching transistor is located in the middle with the guard ring connected to signal ground. Just above the transistor and at the top between the pads, there are five resistors and two capacitors building up the low-pass filter.
Because of different transistor widths, there is an additional signal path length (i.e. drain and source connections) for switch 100, 200, 400 and 800. This makes it possible to use the same de-embedding circuits (see chapter 8) for all switches and to minimize chip area but will introduce an error in the measurements. In table 6.1, these errors are listed as relative errors found from simulations. \( R_{\text{path}} \) is the resistance in the additional path on one side and \( R_{\text{on}} \) is the resistance in the transistor in on-mode (\( R_{\text{on}} < R_{\text{off}} \)). \( C_{\text{path}} \) is the capacitance from the additional path on one side to the substrate and \( C_{\text{off}} \) is the capacitance from drain or source to the substrate in off-mode (\( C_{\text{off}} < C_{\text{on}} \)). None of these relative errors reaches 5% but may be taken into account when making measurements. Switch 1600 has no additional signal paths and thus none of these errors.

Table 6.1 Signal path errors

<table>
<thead>
<tr>
<th>Switch</th>
<th>( 2*R_{\text{path}}/R_{\text{on}} )</th>
<th>( C_{\text{path}}/C_{\text{off}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>4.1%</td>
<td>2.9%</td>
</tr>
<tr>
<td>200</td>
<td>4.6%</td>
<td>1.9%</td>
</tr>
<tr>
<td>400</td>
<td>4.9%</td>
<td>1.0%</td>
</tr>
<tr>
<td>800</td>
<td>3.7%</td>
<td>0.5%</td>
</tr>
<tr>
<td>1600</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Figure 6.2  Layout of switch 100.  
Figure 6.3  Layout of switch 200.  
Figure 6.4  Layout of switch 400.
6.4 Complete Instance Layout

The complete instance on chip where all switches and de-embedding circuits (see chapter 8) are located is market SWITCH ARRAY and shown in figure 6.7. The de-embedding circuits have the same size as the switches. The total size of the complete instance is 600µm x 1760µm. At the bottom of the instance, there are pads to connect $V_C$, $V_{\text{bias}}$ and DC ground marked with V_CONTROL, V_BIAS and GND respectively. This can be done by bonding wires or by probing. The last pad is a dummy to make probing with a four finger DC probe possible. These DC signals are common for all switches. DC ground is the same as signal ground for the GSG probes. The structures have common signal ground that is overlapping each other, thus saving chip area.
Figure 6.7 Layout of the complete instance on chip.
From the layout of the switches, it is possible to extract parasitics that can be used in simulations of the switches that are more accurate. These parasitics arise mainly as capacitances from pads and traces to substrate and as resistances in traces. Figure 7.1 to 7.5 shows the results from these simulations together with simulations without extracted parasitics. No de-embedding has been made in the simulations (see chapter 8). Insertion loss in on- and off-mode has a significant degeneration at both 2.5GHz and 5.5GHz because of the parasitics. On the other hand, the noise figure shows an improvement for both frequencies. For the 1dB compression point, it is hard to see any trend in change because of large fluctuations. The linearity is plotted for $W = 100\mu m$ and is remarkably degenerated by the parasitics.

**Figure 7.1** IL in on-mode with varying width $W$ for the STS with extracted parasitics.

**Figure 7.2** IL in off-mode with varying width $W$ for the STS with extracted parasitics.

**Figure 7.3** NF with varying width $W$ for the STS with extracted parasitics.

**Figure 7.4** $P_{1\text{dB}}$ with varying width $W$ for the STS with extracted parasitics.
Figur 7.5 $P_{in}$ with $W = 100\mu m$ for the STS with extracted parasitics.
8 Modeling and De-Embedding

8.1 Introduction

In the measurements on chip, S-parameters will be measured, not only to get the insertion loss but also to create a model of the switch that can be used in any application. When making the S-parameter measurements, parasitics have to be taken into account. These arise mainly as capacitive parasitics from pads and traces to substrate and as resistive parasitics in traces and probes. One way to do this is to make measurements on dummy circuits with the switch excluded and use the results to eliminate the parasitics mathematically. This is called de-embedding and the dummy circuits are here called de-embedding circuits. Here two different de-embedding methods are presented, one using an ‘open’ and a ‘short’ de-embedding circuit and a second using an ‘open’ and a ‘thru’ de-embedding circuit. Both methods require three measurements, one on the ‘open’ circuit, one on the ‘short’ or ‘thru’ circuit and one on the embedded switch (Eswitch), i.e. switch with parasitics.

8.2 Switch Model

A switch can be modeled as a two-port named ‘Switch’ in figure 8.1. Except from the signal ports there is a control signal $V_C$ to put the switch in on- or off-mode and bias voltage $V_{bias}$ to bias the switch. The switch has Y-parameters $Y_{switch}$. Assuming the switch is reciprocal, i.e. $y_{12} = y_{21}$, it is possible to make a pi-model of the switch as in figure 8.2. The admittances may be converted to lumped resistors and capacitors. If the switch is not reciprocal, a model like the one in figure 8.3 has to be used. However, simulations predict a more reciprocal appearance.

![Figur 8.1 Switch model.](image1)

![Figur 8.2 Pi-model of the switch with $y_{12} = y_{21}$.](image2)
8.3 Embedded Switch

An accurate model of the embedded switch is shown in figure 8.4. \( V_c \) and \( V_{bias} \) are not included for simplicity. Admittances \( y_1 \) and \( y_2 \) represent parallel parasitics between the pads and the substrate and impedances \( z_1 \) and \( z_2 \) represent the series parasitics in the probes and in traces on chip. The embedded switch has Y-parameters \( Y_{Es w i t c h} \).

8.4 De-Embedding Circuits

8.4.1 “Open” Circuit

In the “open” circuit, modeled in figure 8.5, only parallel parasitics \( y_1 \) and \( y_2 \) are present. It has Y-parameters \( Y_{open} \). The “open” circuit layout in figure 8.6 shows that it has the same structure as the switch layouts but with the transistor excluded.
8.4.2 “Short” Circuit

The ‘short’ circuit is modeled in figure 8.7. Here both parallel parasitics $y_1$ and $y_2$ and series parasitics $z_1$ and $z_2$ are present. The ‘short’ circuit has Y-parameters $Y_{\text{short}}$. The ‘short’ circuit layout in figure 8.8 shows that the input and output connections for the transistor are well grounded. The resistance in this return path to ground is neglected as well as the difference in the layout compared to the switch layout.

![Figur 8.7 Model of the ‘short’ circuit.](image)

![Figur 8.8 ‘Short’ circuit layout.](image)

8.4.3 “Thru” Circuit

In the ‘thru’ circuit, modeled in figure 8.9, parasitics $y_1$, $y_2$, $z_1$ and $z_2$ are present as well but there is no return path to ground as in the ‘short’ circuit. This eliminates the error caused by neglecting the resistance of the return path. However, the ‘thru’ circuit layout in figure 8.10 shows that there is another error since the signal path now has become longer. The GSG pads have to be kept at the same distance as in the other layouts due to geometrical issues when putting all layouts together on chip. Anyhow the structure of the ‘thru’ circuit layout is more similar to the switch layouts that the ‘short’ circuit layout is. The ‘thru’ circuit has Y-parameters $Y_{\text{thru}}$. 
8.5 Correction Procedure

From the S-parameter measurements on the embedded switch and the de-embedding circuits, $Y_{E\text{switch}}$, $Y_{\text{open}}$, $Y_{\text{short}}$ and $Y_{\text{thru}}$ are extracted after parameter transformation. See Appendix A for transformation formulas. Choosing the ‘short’ method for de-embedding it can be shown that the Y-parameters of the switch are calculated from

$$Y_{\text{switch}} = \left( (Y_{E\text{switch}} - Y_{\text{open}})^{-1} - (Y_{\text{short}} - Y_{\text{open}})^{-1} \right)^{-1}$$

(8.1)

If the ‘through’ method is used it can be shown that the Y-parameters of the switch are calculated from [8] [9]

$$Y_{\text{switch}} = \left( (Y_{E\text{switch}} - Y_{\text{open}})^{-1} + Y_x^{-1} \right)^{-1}, \text{ where } Y_x = \begin{bmatrix} y_{12\text{thru}} + y_{21\text{thru}} & 0 \\ 0 & y_{12\text{thru}} + y_{21\text{thru}} \end{bmatrix}$$

(8.2)

assuming the circuits are symmetrical. $y_{12\text{thru}}$ and $y_{21\text{thru}}$ are elements of $Y_{\text{thru}}$. Both of these methods may be used to estimate proper values for de-embedding.
9 Conclusion and Future Work

9.1 Conclusion

The simulation results from chapter 5 showed advantages for the STS in insertion loss in on- and off-mode, noise figure, 1dB compression point and linearity compared to the TG and ETG. However, the TG and ETG can have a higher linearity if the width is increased, even if this will consume a lot of chip area. The ETG was supposed to improve signal swing and thus the 1dB compression point but did not show any such improvement. For the STS, the results were degenerated when simulations were performed with extracted parasitics, except for the noise figure. Still, the STS is preferable to use as a switch for analog high frequency signals. It is also less complex than the ET and ETG and is thus easier to design and requires less chip area.

According to chapter 5, the length of the transistor in the STS shall be set to its minimum and the number of fingers does not influence the performance significantly, thus enabling a square layout of the transistor to minimize ship area. The simulations also indicate that the STS can be tuned for different performances at different frequencies by changing the width of the transistor. Insertion loss in on-mode and noise figure can be optimized and there is a worst case for the insertion loss in off-mode (see table 5.2). Also for the linearity there is an optimum at a width of about 100μm. The 1dB compression point is increasing for increasing width, though. Consequently, the choice of width depends on the requirements of the switch.

9.2 Future Work

As mentioned in chapter 5, the simulations are carried out with a source and load impedance of 50Ω, which is the standard characteristic impedance in laboratory measurement equipment. Also it enables the definition of insertion loss in chapter 4. However, in the front-end of a radio transceiver the impedance may be higher to limit the currents and thus the losses in the circuits. Thus, further work should be to investigate the performances of the STS for source and load impedances different from 50Ω that may be used e.g. in the SoCTRix demonstrator. Using different impedances will move the optimum and worst-case values for the STS but trends in the analysis will remain.

Another issue for future work is laboratory on-chip measurements of the five designed switches. Procedures for these measurements are described in [11].
References


# Appendix A  Transformation Formulas

<table>
<thead>
<tr>
<th>S-parameters in terms of Y-parameters</th>
<th>Y-parameters in terms of S-parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s_{11} = \frac{(1 - y_{11})(1 + y_{22}) + y_{12} y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} y_{21}}$</td>
<td>$y_{11} = \frac{(1 + s_{22})(1 - s_{11}) + s_{12} s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12} s_{21}}$</td>
</tr>
<tr>
<td>$s_{12} = -\frac{2y_{12}}{(1 + y_{11})(1 + y_{22}) - y_{12} y_{21}}$</td>
<td>$y_{12} = -\frac{2s_{12}}{(1 + s_{11})(1 + s_{22}) - s_{12} s_{21}}$</td>
</tr>
<tr>
<td>$s_{21} = -\frac{2y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} y_{21}}$</td>
<td>$y_{21} = -\frac{2s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12} s_{21}}$</td>
</tr>
<tr>
<td>$s_{22} = \frac{(1 + y_{11})(1 - y_{22}) + y_{12} y_{21}}{(1 + y_{11})(1 + y_{22}) - y_{12} y_{21}}$</td>
<td>$s_{22} = \frac{(1 + s_{11})(1 - s_{22}) + s_{12} s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12} s_{21}}$</td>
</tr>
</tbody>
</table>
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