RF front-end CMOS design for build-in-self-test

Master thesis performed in *Electronic devices*

By

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Master thesis

Electronic Devices

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Abstract
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Keyword
RF front-end, Attenuator, Low Noise Amplifier
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In this master degree work, a digital attenuator and a low noise amplifier (LNA) have been designed and integrated with the RF front-end receiver for IEEE 802.11b Wireless LAN standard. Firstly, the 4-bit digitally controlled attenuator has been designed with the attenuation range of 50 to 80 dB and reflection coefficient less than -25 dB. Next, the single stage wide band low noise amplifier with voltage gain larger than 14 dB and noise figure below 4 dB has been designed to operate at frequency 2.4 GHz. Finally, the integration with a down-conversion mixer has been done and evaluated its performance.

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Chapter 1  Introduction

1.1 Motivation

Recently, the demand for the wireless communication devices is growing rapidly. The consumer products such as mobile phone, wireless LAN, etc. also require high integration in order to reduce the cost per unit. The electronics of wireless devices consist of two parts, radio frequency (RF) and intermediate-frequency (IF) analog front-end responsible for reception and transmission and the digital base band back-end. Today’s high-end RF front-end are still implemented in BiCMOS, SiGe HBT, bipolar or GaAs technologies which are suitable for the RF circuit design with a good performance. However, these processes are still more complex and more cost than CMOS process technology. Therefore, CMOS technology becomes a preferable alternative low-cost technology for building an application in RF front-end application and integrating it with a base band digital part, which has mostly been implemented in standard CMOS.

A highly-integrated CMOS transceiver is feasible to implement but the correctness verification of the circuit is a difficult and costly task. In order to reduce the cost of verification, the idea of design for testability (DFT) can be introduced. In this case a special solution uses the Built-in Self Test (BIST) technique. BIST requires an additional circuitry to be used for testing the functionality or correctness of a chip without external equipment. The Loop-back BiST for digital transceivers proposed in [8] is a reasonable choice in the design for testability of RF front-end. With this topology, the required additional circuit is a test attenuator used to close the loop of the signal from the transmitter back to the receiver input as well as a test pattern generator and response analyzer for generating the test signal and validating the incoming loop back response.

The work in this project focuses on the BiST design for RF transceivers including the topology to implement RF front end and additional hardware used in the loop back test.

1.2 Specification

The BiST for RF front end design addressed in this work is based on the loop back technique model as shown in Figure 1.1.
This model is composed of the base band DSP processor, transmitter (TX), receiver RX, and additional Test Attenuator (TA) that are all integrated in one chip. The first module, DSP processor, serves as base band signal processing such as modulation, demodulation and pulse shaping. In the test mode, it plays a role of the test pattern generator and response analyzer. The test pattern signal generated in DSP is applied to the transmitter and passed further through the on chip test attenuator to the receiver input. In the end, the DSP is also responsible in analyzing received signal.

Test Attenuator is the crucial part of the loop back test setup. This circuit must provide enough attenuation value, low nonlinearity, and must occupy a small area on silicon.

This thesis work includes the research part and design part. The first task is to examine previous work in the Test Attenuator (TA) and Low Noise Amplifier (LNA) topologies which has been proposed. The second task is to design the TA and LNA with the schematic simulation and layout implementation. Finally, the integration with a mixer must be performed and followed by evaluation of the front-end receiver which aims at standard IEEE802.11b.
1.2.1 Target Specification

**Attenuator**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>DC to 2.4GHz</td>
</tr>
<tr>
<td>Attenuation Range</td>
<td>50 to 80 dB</td>
</tr>
<tr>
<td>Return loss</td>
<td>&lt; -10 dB</td>
</tr>
</tbody>
</table>

**Low Noise Amplifier**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain Av</td>
<td>&gt; 15 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>DC to 2.4 GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3 to 4 dB or lower</td>
</tr>
<tr>
<td>Input Reflection Loss S11</td>
<td>&lt; -10 dB</td>
</tr>
<tr>
<td>1 dB compression Point</td>
<td>&gt; -15 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>&gt; -10 dBm</td>
</tr>
</tbody>
</table>

1.3 Outline of this thesis

- **Chapter 2 - RF Background**: provides the theoretical background on RF fundamental such as nonlinearity, noise, S-parameters.
- **Chapter 3 - Test Attenuator**: design of the attenuator and its simulation result.
- **Chapter 4 - Low Noise Amplifier**: LNA design strategies and result of the simulation.
- **Chapter 5 - RF front-end integration**: LNA is integrated in RF front-end and evaluated its performance.
- **Chapter 6 - Conclusions**
Chapter 2  RF Background

2.1 Nonlinearity

A nonlinear system is a system which outputs signal $y(t)$ is a nonlinear function of the input $x(t)$. A simple model of the nonlinear system can be defined with a polynomial function, usually of the third order:

$$y(t) = a_1x(t) + a_2x(t)^2 + a_3x(t)^3 \quad (2.1)$$

The nonlinearity leads to many effects in the system. In RF design, the nonlinearity is the criterion that defines the upper limit of the RF input signal power and can be characterized by the performance parameters such as 1dB Compression Point and Third-Order Interception Point (IIP3) value.

2.1.1 Harmonic Distortion

In a nonlinear system, supposing that the input signal is $x(t) = A\cos\omega_0 t$, then the output can be written as:

$$y(t) = a_1A\cos\omega_0 t + a_2A^2 \cos^2 \omega_0 t + a_3A^3 \cos^3 \omega_0 t$$

$$= \frac{a_2A^2}{2} + (a_1A + \frac{3a_3A^3}{4})\cos\omega_0 t + \frac{a_2A^2}{2}\cos 2\omega_0 t + \frac{a_3A^3}{4}\cos 3\omega_0 t \quad (2.2)$$

The output consists of the fundamental frequency, which is the term with the same frequency as input, and the Harmonics, that are terms with higher frequencies. The harmonic distortion is defined as the ratio of the amplitude of particular harmonic frequency to the amplitude of the fundamental frequency, for example, the third order distortion $HD_3$ is equal to:

$$HD_3 = \frac{1}{a_1A} \frac{a_3A^3}{4} \quad \text{if} \quad a_1A \gg \frac{3a_3A^3}{4}. \quad (2.3)$$

2.1.2 Gain Compression

In the fundamental frequency, the amplitude equals to $a_1A + \frac{3a_3A^3}{4}$. Clearly as the amplitude of the input signal increases, the gain of the system can be affected by the 3rd harmonic. If the term $\frac{3a_3A^3}{4}$ is negative then the gain will decrease.
considerably. This effect can be expressed by the “1dB Compression Point”, defined as the input signal level that causes the gain to drop by 1 dB compared to the linear system. The plot of input-output relation in log scale shows this point for the output of 1dB drop from the ideal level as shown in Figure 2.1.

![1 dB Compression Point](image)

**Figure 2.1 1- dB Compression Point.**

### 2.2 Intermodulation

In the nonlinear system, Intermodulation (IM) occurs when two strong input signals having frequency near the desired band are mixed due to the nonlinearity of the system, this process can generate a product of the undesired component with the frequency falling in the desired channel. This nonlinear behavior can be used to characterize the nonlinearity of the system by using the two tone test as shown in the figure 2.2.

![Two Tones Test](image)

**Figure 2.2 Two Tones Test.**

The component of interest is the third-order IM which fall in the desired band. The corruption of this component can be measured by the Third Order Interception point (IP3) which is determined by using the two-tone power sweep and plotting the output power of the first order and the third order with the input signal power. The
The intersection of the first order term, \( a_1 A \), and the third order term, \( \frac{3a_3 A^3}{4} \), is the output IP3 (OIP3) and the input IP3 (IIP3) as shown in Figure 2.3.

![Figure 2.3 Input third order interception point (IIP3)](image)

In fact, if all the input signal levels are expressed in dBm, the input IP3 equals to half the difference between the magnitudes of the fundamentals and the IM3 products at the output plus the corresponding input level [6], as shown in Figure 2.4.

![Figure 2.4 Calculation of IIP3](image)

\[
IIP_3 \bigg|_{dBm} = \frac{\Delta P}{2} \bigg|_{dB} + P_{in} \bigg|_{dBm}
\]
2.2.1 Cascaded Nonlinear Stages

In the RF system having cascaded stages, the nonlinearity of each stage is referred to the input of the cascade. The IIP3 can be determined by

\[
\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{G_1^2}{A_{IP3,2}^2} + \frac{G_1^2 G_2^2}{A_{IP3,3}^2} + \ldots \tag{2.4}
\]

where \( A_{IP3} \) is the input IP3 of each stages.

2.3 Noise

Noise is a random signal that presents in the system and the noise performance of the system defines the sensitivity of the system. There are many noise sources that contribute to the system but the major noise source are from electronic devices such as Resistor Thermal Noise and Flicker Noise which are considered in this section and can be calculated as:

\[
\bar{e}_n^2 = 4kTR \ [V^2/\text{Hz}] \tag{2.5}
\]

where
- \( k \) = the Boltzman’s constant = \( 1.38 \times 10^{-23} \)
- \( T \) = the temperature in Kelvin
- \( R \) = the resistance value
In MOSFET, noise can be modeled as the current source noise connected between the drain and the source as shown in Figure 2.6.

\[ \bar{T}_n^2 = 4kT\gamma g_m \]

**Figure 2.6 noise model in MOSFET.**

The current source noise is defined \( \bar{T}_n^2 = 4kT\gamma g_m \) [A²/Hz] where \( \gamma = \frac{2}{3} \) for long channel transistor.

Flicker noise arises from the charge trapping phenomena and the model of this kind of noise is the voltage source connected to the gate of the transistor

\[ \bar{V}_n^2 = \frac{K}{C_{ox}WL} \cdot \frac{1}{f} \]  \[\text{[V}^2/\text{Hz}] \] (2.6)

In the circuit with one input and one output port, noise in the circuit is usually measured at the output port when the input signal is set to zero. The level of noise depends on the gain of the circuit that is not correct if being use to compare the performance of the system. To get the correct calculation of the system’s noise, the input referred noise is used to represent the noise in the system by connecting the noise voltage source and noise current source to the input of the system as depicted in the figure below.

**Figure 2.7 Noise representation with voltage and current source.**

To measure the noise performance of the system, i.e., how much the input signal is corrupted by noise, the noise figure (NF) is used.
\[ NF = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} \]  \hspace{1cm} (2.7)

where SNR\textsubscript{in} is usually defined for noise of 50 Ω source resistor.

### 2.3.1 Noise figure in cascade stages

![Cascade of noisy stages](image)

The over all noise figure of the cascaded stages can be obtained from the equation known as Friis formula:

\[ NF = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1G_2} + \ldots + \frac{(NF_k - 1)}{G_1G_2\ldots G_{k-1}} \]  \hspace{1cm} (2.8)

The important assumption here is that the stages must be impedance matched.

### 2.4 Scattering Parameter (S-Parameter)

The system usually can be characterized in many ways. In order to simplify the analysis of an RF system, the system can be defined as the two port system as shown in Figure 2.9

![S-parameter port variable definitions](image)

Both the source and load terminations are \( Z_0 \) and the two-port relations maybe described as

\[ b_1 = s_{11}a_1 + s_{12}a_2 \]  \hspace{1cm} (2.9)

\[ b_2 = s_{21}a_1 + s_{22}a_2 \]  \hspace{1cm} (2.10)
where
\[ a_1 = \frac{Ei1}{\sqrt{Z_0}}, \]
\[ a_2 = \frac{Ei2}{\sqrt{Z_0}}, \]
\[ b_1 = \frac{Er1}{\sqrt{Z_0}}, \]
\[ b_2 = \frac{Er2}{\sqrt{Z_0}}. \]

When the input port is droved with output port terminated with \( Z_0 \), the term \( a_2 \) in the previous equation becomes zero. This implies that the parameters, \( s_{11} \) and \( s_{21} \), can be determined as follows:
\[ s_{11} = \frac{b_1}{a_1} = \frac{Er1}{Ei1} = \Gamma_1 \] (2.11)
\[ s_{21} = \frac{b_2}{a_1} = \frac{Er2}{Ei1} \] (2.12)

Therefore, \( s_{11} \) is the input reflection coefficient and \( s_{21} \) is the forward power gain.

In the similar way, if the input port is terminated with \( Z_0 \) and driving the output port gives:
\[ s_{22} = \frac{b_3}{a_2} = \frac{Er2}{Ei2} = \Gamma_2 \] (2.13)
\[ s_{12} = \frac{b_1}{a_2} = \frac{Er1}{Ei2} \] (2.14)

where \( s_{22} \) is the output reflection coefficient and \( s_{12} \) is the reverse power gain.

Since the system is characterized by S-parameter, the design of the RF system can easily proceed without any knowledge on how the internal system works.

### 2.5 Receiver Architecture

In the wireless system, the receiver is used to process the desired transmitted RF signal while rejecting the interfering signals. For a preview of the two architectures, the heterodyne and homodyne receivers will be demonstrated in this section.
2.5.1 Heterodyne Receiver

The heterodyne receiver is a well known architecture which has been used for a long time since the early days of radio communication and it is still widely used in the current wireless communication. Since the RF signal transmitted from the transmitter is in the high frequency, the signal in the desired band will be processed and the interferer signal in the nearby band will be filtered out. With this approach, it is very difficult to build the band-pass filter that requires a very high Q. In the heterodyne topology, the signal band is down-converted into a much lower frequency by a mixer as depicted in Figure 2.10. The desired band has the center frequency at $\omega_c$ and it is down-converted to $\omega_{IF}$ by a mixer with the sinusoidal signal having frequency $\omega_{LO}$ where $\omega_{LO} = \omega_c + \omega_{IF}$. This yields the signal with a frequency around $\omega_{IF}$ and $2\omega_c - \omega_{IF}$ where the later band is removed by the low pass filter.

![Figure 2.10 Heterodyne downconversion](image)

The major problem in this approach is that the signal at the image frequency $\omega_{im} = \omega_{LO} + \omega_{IF}$, as shown in Figure 2.11, will be down-converted to the frequency $\omega_{IF}$ and in turn can corrupt the desired signal band.

![Figure 2.11 Image Problem in Heterodyne down-conversion](image)
The signal at the image frequency can be suppressed by using the image-reject filter which is placed in front of the mixer before mixing the signal as shown in Figure 2.12.

![Image Reject Filter](image)

**Figure 2.12 Image Reject Filter**

### 2.5.2 Image Reject Receiver

The drawback of the heterodyne receiver is the formation of the image frequency interference as shown in the previous section. The image frequency is cancelled by using the image reject filter. This approach still requires a filter with a high Q so the implementation of the filter needs an external component to realize the filter. To cope with this problem, other topologies such as Hartley and Weaver architectures are used.

#### Hartley Architecture

![Hartley image rejection architecture](image)

**Figure 2.13 Hartley image rejection architecture**

This image-reject architecture is introduced by Hartley in 1928 as shown in Figure 2.13. The RF signal is mixed with the quadrature phase local oscillator, $\cos \omega_{\text{LO}} t$ and $\sin \omega_{\text{LO}} t$. The resulting signal is passed through the low pass filter and shifts one signal path by 90 degrees to produce the same polarities for the desired signal and opposite polarities for the image. When the signals from two paths are
added together, the image component cancels out and the IF signal is not corrupted by the image.

The problem with this architecture is the sensitivity of phase and amplitude imbalance between the quadrature mixers caused by a mismatch between the two mixers.

**Weaver Architecture**

![Weaver image rejection architecture](image)

The Weaver architecture replaces the 90 degrees stage by a second quadrature mixing operation. Here, the RF signal is mixed with the quadrature phase shift oscillator with the frequency $\omega_{LO1}$ and the result from both paths is passed through the low pass filter and mixed again with another quadrature phase shift oscillator with the frequency $\omega_{LO2}$. The results of the two paths are subtracted to get the IF signal where the image is cancelled out. This architecture gives a better image rejection than Harley architecture because it does not suffered from the amplitude mismatch.

### 2.5.3 Homodyne Receivers

In homodyne architecture, the desired RF signal is down-converted directly to base-band using a local oscillator with a frequency equals to the frequency of the input carrier. This kind of architecture can be called the Homodyne, Direct conversion
or Zero-IF. This topology has the advantage since the image frequency problem is eliminated because IF is zero. Therefore no requirement for the image reject filter exists. Another advantage of this architecture is that only low-pass filter and baseband amplifier follows the down-conversion part. This makes the homodyne suitable for monolithic integration. The homodyne receiver with quadrature down conversion is shown in Figure 2.15.

![Figure 2.15 Homodyne Receiver with quadrature downconversion.](image-url)
Chapter 3 Test Attenuator

Digital MMIC (Microwave Monolithic Integrated Circuit) RF attenuators are widely used in modern communication devices. In designing this kind of attenuator, the input and output impedance matching with the characteristic impedance is given importance aside from the accurate attenuation value that must be met. Many topologies have been proposed and most of them are based on the simple implementation of the attenuator using the resistive-network. There are three different forms of resistive networks that are used as basic configuration for the attenuator. The analysis of these three resistive-network forms is performed where their input impedance are matched with characteristic impedance \( Z_0 \) (in this case \( Z_0=50 \, \Omega \)).

3.1 Resistive Configuration

3.1.1 Pi-configuration

\[
Z_{in} = \frac{Z_0 R_p^2 + Z_0 R_S R_p + R_S R_p^2}{Z_0 R_p + R_p^2 + Z_0 R_S + R_S R_p + Z_0 R_p} \quad (3.1)
\]

Attenuation Value = \( \frac{Z_0 R_p}{R_S R_p + Z_0 R_S + Z_0 R_p} \) \quad (3.2)
3.1.2 T-configuration

\[
Z_{in} = \frac{(R_S + Z_0)R_P}{R_S + R_P + Z_0} + R_S
\]  
(3.3)

\[
\text{Attenuation value} = \frac{R_PZ_0}{R_S^2 + 2R_SR_P + R_SZ_0 + R_PZ_0}
\]  
(3.4)

3.1.3 Bridge-T configuration

\[
Z_{in} = Z_0 \cdot \frac{Z_0^2 + 2Z_0R_1 + 2Z_0R_2 + 3R_1R_2}{3Z_0^2 + 2Z_0R_1 + 2Z_0R_2 + R_1R_2}
\]  
(3.5)

\[
\text{Attenuation value} = \frac{R_2}{R_2 + Z_0} = \frac{Z_0}{R_1 + Z_0}
\]  
(3.6)

where \( R_1R_2 = Z_0^2 \) and \( R_s = 50\Omega \)

From the equation used to calculate input impedance and attenuation value, we can draw a conclusion that a Pi-configuration has a large attenuation range and a good impedance matching to 50 Ω with realizable resistance sizes. For T-configuration, it is suitable for high source and load impedance level but the impedance matching to 50 Ω is poor with feasible impedance levels. The impedance matching for Bridge-T configuration is not difficult, but large attenuation values are impossible to achieve in a 50 Ω environment.
3.2 Case Study

Since the resistive network gives fixed attenuation values by the resistor value set in the network, application that requires the variable attenuation value is not possible in this case. In order to make the resistive network adjustable, previous topologies for the variable attenuators are implemented in GaAs [1]. Some examples are Segmented dual-gate FET, Switched attenuators, Switched scaled FET, Switched bridged-T attenuator and others.

![Switched Attenuator Schematic](image)

**Figure 3.4 Schematic diagram of a switched attenuator.**

Figure 3.4 shows the schematic diagram of a switched attenuator. The input signal power is attenuated when both SPDT switch selects the attenuation path. The attenuation path can be implemented by resistive network such as T network or Pi network.

![Switched Bridged-T Attenuator](image)

**Figure 3.5 Switched bridged-T attenuator configurations.**

Shown in Figure 3.5 is the schematic of a *Switched bridged-T attenuator*. The transistors are used as switches and attenuation value is provided by the bridged-T network.

The proposed implementation of the attenuator in CMOS process is the Linear-controlled CMOS Attenuator [7]. This attenuator uses the pi network form in
the attenuator core where all passive components (resistors) are replaced by active devices (transistors working in triode region). The attenuation value can be varied by controlling the gate voltage of the transistor to change the on-resistance value of each transistor as shown in Figure 3.6.

As shown in Figure 3.6, the attenuator is composed of three separated circuit blocks namely: Control Linearization, Attenuator Core and Matching Control. All transistors in the attenuator core that works in the triode region have on-resistances as nonlinear functions of the gate voltage. The gate voltage is equivalent to the v-linear in the Control Linearization block. The attenuation value is varied linearly by v-control and it is fed to the input of the operational amplifier of the Control Linearization Circuit. The v-linear is generated to adjust the gate voltage of the transistor and this voltage has to keep all transistors stay in the triode region. At the same time, the Matching Control block generates v-matching to the control input impedance of the attenuator to be matched with 50Ω resistance. One difficulty of this approach is that the matching control requires a feedback control loop which makes the design too sophisticated to implement. It also requires a replica of the attenuator core and that the test current feed has to be done into the replica block all the time implying more power consumption. Another difficulty to be considered is how to provide an accurate control voltage to a particular desired attenuation value.
3.3 Digital Attenuator

The previous work of attenuator implemented in CMOS process uses a voltage to adjust a value of the attenuator. Since this approach is too difficult to make all transistors stay in triode-region, therefore the new approach must be used to avoid the problem from the control signal. The switched attenuator is a suitable choice and should be considered. All basic forms of the resistive network are analyzed for the proper resistance values that can achieve the desired attenuation value and input impedance matched a 50 Ω.

<table>
<thead>
<tr>
<th>Network Form</th>
<th>Resistor</th>
<th>Attenuation Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>3dB</td>
</tr>
<tr>
<td>T</td>
<td>R_s</td>
<td>8.58Ω</td>
</tr>
<tr>
<td>T</td>
<td>R_p</td>
<td>141.42Ω</td>
</tr>
<tr>
<td>Pi</td>
<td>R_s</td>
<td>17.7Ω</td>
</tr>
<tr>
<td>Pi</td>
<td>R_p</td>
<td>291.42Ω</td>
</tr>
<tr>
<td>Bridge-T</td>
<td>R1</td>
<td>21Ω</td>
</tr>
<tr>
<td>Bridge-T</td>
<td>R2</td>
<td>120.71Ω</td>
</tr>
</tbody>
</table>

Table 3.1 Resistance value of each network.

From Table 3.1, T-network and Bridge-T have possibility to implement small attenuation values. If high attenuation values are required, > 24 dB, Rp in T-Network or R2 in Bridge-T are not possible to realize a very small resistance value by using either sheet resistor or transistor. However, if one consider the resistance value of the Pi-network, high attenuation values are feasible to implement. A resistance level is large enough to be realized by sheet resistor, therefore Pi-network is chosen to implement the attenuator. The basic configuration of this approach is shown in Figure 3.7.
This configuration consists of resistors, where some of them are in series with transistor for switches. All transistors work in the triode region when the digital control signal is applied to the gate-source voltages. The on-resistance of the transistor can be approximated by:

$$R_{on} \approx \frac{1}{k \frac{W}{L}(V_{GS} - V_{TH})}$$

This attenuator provides two different attenuation values by setting the value of the resistance and the on-resistance of the transistors. The attenuation value can be changed by applying the control signal $D$ and $\overline{D}$ to turn on and off the transistor. When $D$ is logic 0, the transistor $M1$ is turned on and transistors $M2$ and $M3$ are turned off. The attenuation path is formed by $R1$, $R2$, $R4$, $R6$ and $M1$ which can be determined by:

$$A_{D=0} \text{ dB} = 20 \log_{10} \frac{R_pZ_0}{R_sR_p + R_sZ_0 + R_pZ_0}$$

where $R_p = R4 = R6$ and $R_s = (R1 + R_{on,M1}) \parallel R2$

When $D$ is logic 1, the transistor $M1$ is turned off and transistor $M2$ and $M3$ are turned on. The attenuation path is formed by $R2$, $R3$, $R4$, $R5$, $R6$, $M2$ and $M3$. The attenuation value can be calculated by the equation as mentioned above but $R_s$ and $R_p$ are changed to $R2$ and $(R3 + R_{on,M2}) \parallel R4 = (R5 + R_{on,M3}) \parallel R6$, respectively.
3.4 4-bits digital attenuators

From the basic configuration of Switched II Attenuator shown in the previous section, the 4 bits digital attenuator can be implemented by cascading the basic block. The arrangement of the attenuator block is shown in Figure 3.8.

![4-Stages Cascade Attenuator](image)

The total attenuation value can be determined by summing of the attenuation values in dB of all blocks together.

\[ A_{dB} = A_{dB,stage0} + A_{dB,stage1} + A_{dB,stage2} + A_{dB,stage3} \]  

where \( A_{dB} \) is attenuation value expressed in dB.

The arrangement shown in Figure 3.9 is implemented by choosing the attenuation value of each stage as shown in the Table 3.3.

<table>
<thead>
<tr>
<th>Digital Value</th>
<th>Attenuation Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Stage 0</td>
</tr>
<tr>
<td>0</td>
<td>3 dB</td>
</tr>
<tr>
<td>1</td>
<td>6 dB</td>
</tr>
</tbody>
</table>

Table 3.2 Attenuation Value Configuration

- The smallest attenuation value is 21 dB.
- The highest attenuation value is 90 dB.

The resistors were implemented by using the poly-silicon resistor, \( r_{poly2} \), which has sheet resistance equals to 50 \( \Omega \) per square sheet. The transistor was sized so that the on-resistance is smaller than its series resistance to reduce the effect of nonlinearity of the transistor. The simulation results of the circuit implementation are shown in Figure 3.9 for the S21 parameter and Figure 3.10 for the S11 parameter.
The obtained result shows that the attenuation values drop significantly at the high attenuation value as the frequency increases. At the frequency 2.4 GHz, the attenuation value differs from the desired value and the reflection coefficient S11 is below -10 dB.
The realization with the resistors does not seem to be a good approach. First, the high parasitic capacitance of the sheet resistance gives a poor frequency response. Second, the difficulty of the implementation of a small sheet resistance is sensitive to the tolerance of the process variation. For these two reasons, another approach using a larger resistance values has been proposed. A configuration of this new approach is shown in Figure 3.11.

![Figure 3.11 4-Stages Cascade Attenuator with high value resistance](image)

In this topology, each resistor in the attenuator block has 10 times increased and the input impedance matching is achieved by using the additional matching network. The attenuation value can be determined as:

\[ A_{\text{dB}} = A_{\text{dB,stage0}} + A_{\text{dB,stage1}} + A_{\text{dB,stage2}} + A_{\text{dB,stage3}} + A_{\text{dB,matching}} \]  \hspace{1cm} (3.10)

where \( A_{\text{dB}} \) is attenuation value expressed in dB.

<table>
<thead>
<tr>
<th>Digital Value</th>
<th>Attenuation Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>3 dB</td>
</tr>
<tr>
<td>1</td>
<td>6 dB</td>
</tr>
</tbody>
</table>

**Table 3.3 Attenuation Value Configuration**

- Matching Network Attenuation value = 20 dB
- Minimum attenuation value = 35 dB,
- Maximum attenuation value =110 dB

The simulation result for the attenuation value (S21) for this approach is degraded too much with the frequency. The difference between the expected attenuation value and the attenuation value at 2.4 GHz is 15dB which has a very large variation. The reflection coefficient (S11) is below -10dB which is still acceptable. All the simulation results are shown in Figure 3.12 and Figure 3.13 respectively.
The simulation obtained with increased resistance from the previous approach is also not acceptable because of a very large variation in the attenuation values. Therefore, another alternative has to be considered to avoid this problem. The resistors can be replaced by the active devices such as transistors operating in triode region. However, this solution may not be better because the nonlinearity of the on-resistance which can contribute significantly to the effectiveness of the attenuator. Hence, special attention must be paid to the linearity performance of the circuit.
The attenuator consists of series and shunt transistors, the series and shunt transistor controlled by En (enable) signal which has a fixed width size. The series transistors controlled by D0, D1, D2 are sized in the ratio 2:4:8 times of the fixed sized series transistor in order to get the different width size when the input data is changed. When input data is set from 000 to 111, the attenuation value will decrease because the total width of series transistor is increased. The simulation result is shown in Figure 3.15 and Figure 3.16.
From the simulation result above, the plot of S21 shows that the attenuation is not much degraded while the frequency increases. If the S21 is considered for each input data, S21 decreases when the total width size of the transistor increases but is not in the linear manner. The reflection coefficient is degraded when the total width of the series transistor increases, therefore the input matching has to be improved in this approach by putting the input matching in front of the attenuator as shown in Figure 3.17.
After preceded by the matching network, the reflection coefficient value is now in the acceptable range when sizing the shunt transistor with the proper transistor width. The matching problem is solved but the attenuation value is still not changed linearly when changing the input data. If one consider the width size with its corresponding attenuation value, the result shows that the attenuation value vary in a nonlinear order, hence the transistor has to be changed in the nonlinear value. In order to increase the total width of the transistor in a nonlinear order, the new configuration of the switched Π attenuator is proposed. The digital input is first encoded by a thermometer code circuit to get the control signal as shown in Figure 3.19 and Table 3.4.

If the inputs D0 to D2 of the Switched Π attenuator are applied by T0 to T2 respectively, the total width of the series transistor is appended by the transistor width of each bit when it is turned on by input signal.
The implementation of the control signal in this way can linearly change the attenuation value of the attenuators. Figure 3.20 shows the circuit of Switched Π attenuator using the thermometer code.

![Figure 3.20 Switched Π Attenuator with Thermometer code](image)

From Figure 3.20, the configuration and the width size of each transistor is shown. The functionality of the circuit can be explained such that input signals D0 and D1 are applied to the thermometer code circuit. Suppose the input is 00 then the output of the thermometer code is 111, so that all series transistor are turned on. The total width of series transistor is 105µm and gives an attenuation value roughly equal to 25dB. If the input changes to 01, the total width of the attenuator decreases to 50µm and the attenuation value increases to 27dB, which is 2 dB larger. If the input is changed to 10 and 11, the output will be 29dB and 31dB, respectively. Therefore, the attenuation value can be changed to 2 dB for each step. Figure 3.21 shows the simulation result of the attenuation value (S21).
The result from the previous configuration shows that the realization of Switched II attenuator can achieve the variable attenuation value but can only provide 4 steps. Therefore the new configuration for 4 bits, with 16 steps is proposed as shown in Figure 3.22 and Figure 3.23.
The attenuator core shown in Figure 3.23 consists of two cascaded attenuator networks and the input-output matching network. The first network provides 4 levels with 8 dB separations, and the second attenuation network provides 4 levels with 2 dB separations. The digital signal to control both networks is encoded by the thermometer code circuit, as shown in Figure 3.23. D3 and D2 are the input signal of the first attenuator network and D1 and D0 are the input signal for the second attenuator network. Therefore, $4 \times 4 = 16$ different outputs with 2 dB steps can be achieved by this configuration. The simulation result for attenuation value $S_{21}$ and reflection coefficient are shown in Figure 3.24 and Figure 3.25, respectively.
Figure 3.24 Attenuation value $S_{21}$

Figure 3.25 Attenuation value $S_{21}$
Figure 3.26 Input third interception point (IIP3)
3.5 The Complete layout of the attenuator

Figure 3.27 Attenuator Layout
3.6 The post layout simulation result

Figure 3.28 $S_{21}$ for each input data

Figure 3.29 $S_{11}$ for each input data.
Chapter 4  Low Noise Amplifier

Low-Noise Amplifier (LNA) is an essential part in the RF front end receiver. Since the weak signal coming from the antenna is first amplified by LNA, noise introduced from LNA is directly added to the system. It is shown in the Friis’ formula that noise contributed from LNA must be as low as possible. In order to bring the smallest wanted signal sufficiently above the noise floor and compress the noise in the subsequence stages, the gain of LNA must be high enough. In addition to noise and gain, input impedance matching is also important. The main purpose of matching is to reduce the reflection from the cable or to avoid the alteration of the characteristic of the preceding RF filter.

The linearity of the LNA has to be considered too. It is supposed that the desired signal is very weak while the nearby signal is very strong. The nonlinearity of the LNA can introduced the undesired component into the desired band, called Intermodulation. Another phenomenon which is a direct consequence of the nonlinearity of LNA is the gain compression. If the input signal amplitude is increased and the gain of the LNA can not keep constant, the output signal is clipped or gain is compressed. This characteristic can be defined as the 1-dB compression point and Input IP3.

4.1 Amplifier Function Requirements

- **Forward Gain**, The voltage gain is required to boost the weak input signal and overcome the noise in the following stage.

- **Input impedance matching**, To avoid the reflection of the signal if connected with the input from outside or give a good termination for band-pass filter.

- **Stability**, The amplifier has to be unconditionally stable.

- **Noise Figure**, NF must be low, because noise from this stage is directly added into the system.
4.2 LNA Design Strategy

4.2.1 Impedance Matching

In the design of LNA, the 50Ω resistive input impedance is required to limit the reflections of the signal on the cable or to avoid the degradation of the performance of the preceding RF filter. The simple approach is to put the 50Ω resistor across the input terminal as shown in Figure 4.1. This approach provides a good broadband matching but the considerable thermal noise coming from this resistor can degrade the noise figure of the system. Therefore the resistive termination topology is not widely used for input matching.
Shunt Series Feed Back as shown in Figure 4.2 is another topology used in many LNA design. The input impedance can be achieved by the feed back resistor $R_F$. The input impedance is given by:

$$R_{in} = \frac{R_F}{1 - A_v}$$  \hspace{1cm} (4.1)

This topology can give a better noise figure than the previous one but it still has a thermal noise from the feedback resistor.

![Common Gate Amplifier](image)

**Figure 4.3 Common Gate Amplifier**

Common Gate topology (CG) shown in Figure 4.3 is another choice for impedance matching. For the CG, the input resistance looking into the source terminal equals to $\frac{1}{g_m}$ of the MOSFET. Therefore, the desired 50Ω input resistance can be achieved by selecting the proper transistor size and bias current.

The calculation of the noise factor of the common gate can deduce the lower bound on the noise factor which is approximated to be:

$$F \geq 1 + \frac{\gamma}{\alpha g_m R_s}$$  \hspace{1cm} (4.2)

From the lower bound noise factor, it is found that the noise can be minimized by increasing $g_m$. If the impedance matching is achieved, $g_m$ has to be equal to $\frac{1}{R_s}$, resulting to $F \geq 1 + \frac{\gamma}{\alpha}$. Therefore, the result of the noise figure of this lower bound for
long channel device is about 2.2 dB and can be as high as 4.8 dB for short channel device. This topology still suffers from the noise figure and is not a good choice if a small noise figure is required.

![Figure 4.4 Common Drain feedback](image)

The Common Drain feedback as shown in Figure 4.4 is another approach which can be used. The input impedance can be determined as:

$$R_{in} = \frac{1}{g_{m2}(1 + g_{m1}R_D)}$$  \hspace{1cm} (4.3)

Therefore, with the proper selection of $g_{m1}$, $g_{m2}$ and $R_D$, the 50 Ω input resistance can be achieved. The noise factor of this topology can be calculated as [5]:

$$NF = 1 + \frac{\gamma}{\alpha(1 + g_{m1}R_D)} + \left(1 + \frac{\gamma}{\alpha g_{m1}}\right)\left(1 + \frac{1}{g_{m1}R_D}\right)^2$$  \hspace{1cm} (4.4)

Where $g_{m2}R_S = \frac{1}{(1 + g_{m1}R_D)}$

From the noise factor calculation, the noise factor can be minimized by maximizing $g_{m1}$. This topology might be a good alternative for the implementation of the LNA with low noise factor requirement.
4.2.2 Bandwidth Extension with Shunt Peaking [2]

In the design of wide band amplifier, more details are considered at high frequency than at the lower frequency. The performance of the amplifier will be degraded due to the limitation of the device itself and also the parasitic capacitance and inductance. These can cause serious problem to the design of wide band amplifier. The general problem is the gain bandwidth product of the amplifier. In order to enhance the bandwidth of the amplifiers, the topology called Shunt Peaking, found during the 1940’s to extend the bandwidth of the television tubes, can be used. Although this topology has been used for a long time ago, it’s still a useful technique in the modern RF circuit design technology.

The example for common source amplifier with shunt peaking is shown in Figure 4.5. The gain of the common source with a purely resistive load is $g_mR_L$ while the load of the amplifier includes the capacitive load. The effect is that the gain of the amplifier will reduce as the frequency increases because the impedance of the capacitive load decreases. An inductor is added in series with the load resistor to improve the performance. As the frequency increase, the impedance of the inductance increases. The net load impedance of the amplifier can be kept roughly constant resulting for the bandwidth to be further extended which is wider than the original amplifier.

![Figure 4.5 Shunt-Peaked amplifier](image)
For the small signal model on the right of Figure 4.5, the load impedance is equal to 

\[ Z(s) = (sL + R) \parallel \left( \frac{1}{sC} \right) = \frac{R[s \left( \frac{L}{R} \right) + 1]}{s^2 LC + sRC + 1} \]

since the gain of the amplifier is equal to \( g_m |Z(s)| \) so that the gain of the amplifier is varied by the frequency. The magnitude of \( Z(s) \) can be calculated as

\[
|Z(j\omega)| = R \sqrt{\frac{(\omega \frac{L}{R})^2 + 1}{(1 - \omega^2 LC)^2 + (\omega RC)^2}} \quad (4.5)
\]

In order to find the value of \( R, L, C \) for the circuit, the new term, \( m \), is defined as the ratio of the RC and \( \frac{L}{R} \) time constants:

\[
m = \frac{RC}{L} \quad (4.6)
\]

In the design of shunt peaked amplifier, the maximum bandwidth can be achieved by selecting \( m=1.41 \) resulting in the 85% improvement of the bandwidth. If \( m = 2.41 \) is selected, 72% bandwidth improvement can be obtained. The summary of the factor \( m \) with the response is shown in Table 4.1

<table>
<thead>
<tr>
<th>Factor (m)</th>
<th>Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \infty )</td>
<td>no shunt peaking</td>
</tr>
<tr>
<td>1.41</td>
<td>85% improvement, Maximum bandwidth</td>
</tr>
<tr>
<td>2.41</td>
<td>Maximally flat frequency response</td>
</tr>
<tr>
<td>3.1</td>
<td>60% improvement, Best group delay</td>
</tr>
</tbody>
</table>

Table 4.1 Summary of the factor(m) and Response
4.3 Design and Circuit Simulation

In the previous section, the demonstration about the essential topology in the design of a wide band low noise amplifier was presented. In this section, the topology of the design of low noise amplifier used in this thesis is presented. Table 4.2 shows the target requirement of the LNA which is used in RF front end at frequency 2.4 GHz for the WLAN standard IEEE802.11b.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Gain $A_v$</td>
<td>$&gt; 15$ dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>DC to 2.4 GHz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>3 to 4 dB or lower</td>
</tr>
<tr>
<td>Input Reflection Loss $S_{11}$</td>
<td>$&lt;-10$ dB</td>
</tr>
</tbody>
</table>

Table 4.2 Design Specification

4.3.1 Design Topology

This section describes the selected topology for LNA. From the specification, this LNA is aimed at 2.4GHz and will be interfaced with a Mixer in RF front-end. The circuit must have $50\,\Omega$ input impedance. Care must be taken, since the input impedance is $50\,\Omega$ while the output impedance is not $50\,\Omega$. The design should then be optimized and simulated in the voltage domain (not in the power domain).

The topology used for this LNA is a *single stage cascode common source with common drain feedback* as shown in Figure 4.6.
This approach is selected for the LNA because of several reasons. Firstly, the input impedance matching is achieved by using the common drain feedback. This approach does not require the resistor as in the resistor termination or shunt-series feedback. Secondly, the noise performance of this topology can be minimized by maximizing the $g_m$ of transistor M1 so that the noise figure can be lower than 4 dB. However, this topology is selected rather than the common gate because it was found from the previous section that the minimum noise figure of common gate topology for the short channel device is 4.8 dB. This value is greater than the noise figure of the requirement. Finally, the cascode transistor can reduce the Miller effect of the transistor M1 and improve the reverse isolation.

A wide band input matching is performed by M2 as a common drain feedback. The 50 $\Omega$ input resistance obtained from selecting the width size of the transistor M2 results to $g_{m2} = \frac{1}{R_s(1 + g_{ml} R_D)}$. Transistor M3 serves as the current source. In order to reduce the noise contribution from this transistor, the small transistor size is used with low bias current. M1 is the input amplifier transistor and is made so that the value of $g_{m1}$ is large enough to compress the noise and provide enough gain.
4.3.2 Design Consideration
Noise Figure and Input Matching

Figure 4.7 Reflection Coefficient, $S_{11}$.

Figure 4.8 Noise Figure

Figure 4.7 shows the reflection coefficient obtained from the simulation of two different values of the width of transistor M2. Although a good impedance matching at 2.4GHz can be achieved by selecting the larger transistor size, noise figure is poorer as shown in Figure 4.8. For this reason, in order to get a better noise figure, the good input impedance matching can’t be met but it is still acceptable as long as the reflection coefficient value is under -10 dB.
For this design, if the larger bandwidth is required, the bandwidth of the amplifier can be further enhanced by using the inductive shunt-peaking. The inductor is connected in series with the resistive load \( R_D \). The value of the inductor used in the design can be chosen by selecting the factor \( m \), for example if \( m=2.41 \), the required shunt peaking inductor can be calculated as:

\[
L = \frac{R^2 C}{2.41} \approx 4nH
\]

where \( R = 200 \) \( \Omega \) and \( C \) is a total capacitance at the output node including the capacitance of the transistor and the load capacitance \( \approx 250fF \). The planar spiral inductor used in this design is readily implemented in AMS 0.35\( \mu \) standard CMOS technology.

The simulation for the voltage gain is shown in Figure 4.9 for shunt peaking with the selected value \( m \) and no shunt peaking. The bandwidth is much improved as seen below but a larger area required for the on-chip inductor.

![Figure 4.9 Bandwidth Extension](image)

The DC Blocking capacitor (\( C_b \)) is selected so that the impedance of this capacitor at 2.4 GHz can not effect to the input impedance matching of the amplifier.

Since \( Z_b = \frac{1}{2\pi fC_b} \), so that the chosen value \( C_b \) (10pF) in this design has the absolute value of 6.6 \( \Omega \) at 2.4 GHz.
4.3.3 Simulation Result

Figure 4.10 Voltage Gain

Figure 4.11 Reflection Coefficient S11
Figure 4.12 Noise Figure

Figure 4.13 1-dB Compression Point
4.3.4 Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>14.5 dB</td>
</tr>
<tr>
<td>S11</td>
<td>&lt; -10 dB</td>
</tr>
<tr>
<td>NF</td>
<td>3.6 dB</td>
</tr>
<tr>
<td>1-dB Compression Point</td>
<td>-27.1 dBV</td>
</tr>
<tr>
<td>IIP3</td>
<td>-15 dBV</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>30 mW</td>
</tr>
</tbody>
</table>

Table 4.3 LNA Performance
4.4 Layout Implementation

Figure 4.15 LNA Layout

Note:

The pre layout and post layout simulation do not match closely for this design because a high parasitic capacitance between metal plate and substrate. In this design, the capacitor is implemented by using two metal plates, Metal-3 and Metal-4, in order to reduce the substrate capacitance. However, the capacitance level is still high, 17% of the required capacitance value so that the Metal-insulator-metal (MIM) must be used instead.
Chapter 5  RF Front-End Integration

The CMOS receiver for Standard IEEE 802.11b Wireless Local Area Network (WLAN) is selected to be use in the loop back BiST design. The receiver employs the direct-conversion or Zero IF architecture which is suitable for the Direct Sequence Spread Spectrum (DSSS) technique. The block diagram of the receiver is shown in Figure 5.1

The LNA is integrated with a quadrature down-conversion by differential double balance mixer. From the IEEE 802.11 spread-spectrum standard, the bandwidth of each channel is 22 MHz and the required sensitivity across this bandwidth is -80 dBm. The required NF for the front end can be determined as:

\[ \text{NF} = -174 \text{ dBm} + 10 \log B + \text{SNR} - P_{\text{in,min}} \]  

If \( P_{\text{in,min}} = -80 \text{dBm} \) \( , \) \( B = \) Bandwidth = 22 MHz and \( \text{SNR} = 10 \text{ dB} \) for frame error rate (FER) of \( 8 \times 10^{-2} \) \( , \) NF can be calculated as:

\[ \text{NF} = -174 \text{ dBm} + 10 \log (22 \text{MHz}) + 10 \text{ dB} - 80 \text{ dBm} \]

so that NF must be lower than 10.6 dB.

The completed direct down conversion front end has been simulated and the simulation result obtained is shown in Figure 5.2 to 5.4.
Figure 5.2 Conversion Gain

Figure 5.3 Noise Figure
From the simulation result, the conversion gain for the front end is about 23 to 25 dB and the Noise Figure is lower than 10 dB which is an acceptable value while the average noise figure in the band of interest 1 MHz to 23 MHz is about 9 dB.
Chapter 6  Conclusions

6.1 Conclusions

The 4-bits digital attenuator and LNA has been designed and simulated using a 0.35 µm standard CMOS process from AMS. Aside from that, they have been integrated with RF front-end for WLAN standard IEEE802.11b and the performance is evaluated. The simulation result obtained shows that the attenuator can provide attenuation value range of -54 dB to -92 dB, the reflection coefficient (S11) below -25 dB and IIP3 -21.4 dB.

A design topology used for LNA in this thesis is a single stage cascode common source with common drain feedback. The simulation result for LNA achieved the voltage gain 14.5 dB, NF lower than 4 dB, reflection coefficient (S11) less than -10 dB, 1-dB Compression Point -27.1 dBV, and IIP3 -12 dBV. The result obtained satisfied the target requirement.

After two differential double balance mixers are integrated, the result shows that LNA gave a good performance. The result obtained from the simulation of the whole front-end achieved the conversion gain of 23 dB, average NF 9 dB, and IIP3 -12 dBm.
References


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