Institutionen för systemteknik
Department of Electrical Engineering

Examensarbete

A Comparative Study of Efficient Power Amplifiers in CMOS

Examensarbete utfört i Elektronik
vid Tekniska högskolan i Linköping
av

Gustav Östberg

LiTH-ISY-EX--08/4165--SE

Linköping 2008

Linköpings universitet
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Linköping, 22 December, 2008

Avdelning, Institution
Division, Department

Division of Electronic Devices
Department of Electrical Engineering
Linköpings universitet
SE-581 83 Linköping, Sweden

Datum
Date

2008-12-22

Språk
Language

☐ Svenska/Swedish
☒ Engelska/English
☐ _____

Rapporttyp
Report category

☐ Licentiatavhandling
☒ Examensarbete
☐ C-uppsats
☐ D-uppsats
☐ Övrig rapport
☐ _____

ISBN
__

ISRN
LiTH-ISY-EX--08/4165--SE

Serietitel och serienummer **ISSN**
Title of series, numbering __

URL för elektronisk version
http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-4165

Titel
Title
Jämförelse Mellan två Effektförstärkararkitekturer i CMOS
A Comparative Study of Efficient Power Amplifiers in CMOS

Författare
Author
Gustav Östberg

Sammanfattning
Abstract

During later years communication schemes for handheld devices have increased in complexity due to the desire to increase the throughput, i.e. the amount of information sent over a medium simultaneously. Increasing throughput can be accomplished, not only by modulating the phase or frequency, but also the amplitude. This leads to tougher requirements on the power amplifier. The conventional power amplifiers, which have the ability to follow the envelope of the carrier, are inefficient. This thesis aims to compare two old but revived architectures which exploit high-efficiency amplifiers and still have a linear relationship between the input and output. The architectures; the Polar Linearization Technique and Outphasing share the same foundation. Based on literature, the polar technique have been more successful of employing examples fufilling communication standards. The polar technique is also more versatile regarding power combiners, distortion correction and alternative implementations. The simulations performed in this thesis results show that the polar amplifier is less sensitive to process variations and has higher maximum efficiency. On the other hand, the outphasing topology have the highest linearity figures.

Nyckelord
Keywords
Power Amplifier, Integrated Circuit

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During later years communication schemes for handheld devices have increased in complexity due to the desire to increase the throughput, i.e. the amount of information sent over a medium simultaneously. Increasing throughput can be accomplished, not only by modulating the phase or frequency, but also the amplitude. This leads to tougher requirements on the power amplifier. The conventional power amplifiers, which have the ability to follow the envelope of the carrier, are inefficient. This thesis aims to compare two old but revived architectures which exploit high-efficiency amplifiers and still have a linear relationship between the input and output. The architectures; the Polar Linearization Technique and Outphasing share the same foundation. Based on literature, the polar technique have been more successful of employing examples fufilling communication standards. The polar technique is also more versatile regarding power combiners, distortion correction and alternative implementations. The simulations performed in this thesis results show that the polar amplifier is less sensitive to process variations and has higher maximum efficiency. On the other hand, the outphasing topology have the highest linearity figures.

Acknowledgments

First I would like to thank my supervisor professor Atila Alvandpour for giving me the opportunity to do my master thesis in his group, and also for the guidance and support I received during the time of the project. I would also like to thank my co-supervisor, M.Sc. Jonas Fritzin, which have been supportive and a big source of knowledge. Even though the questions have been many, he has shown large portions of patience. At last I would like thank all of the PhD students and staff at Electronic Devices, which have from the very beginning made me feel welcome, and have been most helpful in all problems I have encountered.

Gustav Östberg, December 2008

Contents

Chapter 1

Introduction

The focus of this thesis is do a comparison on two power amplifier architectures for communication systems, namely the Polar and Outphasing amplifiers. Architectures in this context means a compound object of circuit blocks that together forms a amplifier. Both these share some important aspects, such that a modulated input signal which contains information in amplitude and phase are paraphrased and divided into two signals. Then the signals are amplified separately and recombined. The motivation behind these two architectures is that higher levels of efficiency can be achieved than conventional power amplifiers. The architectures discussed in this survey share some similarities and the goal of this thesis is to find advantages and disadvantages in a highly integrated environment.

This chapter aims to show the fundamentals of the behavior of different kinds of amplifiers together with performance metrics used in this thesis. Chapter 2 gives a mathematical description and discusses the architectures on a system level. Factors of distortion are described, together with proposed system level corrections. Power combiners are very important for both architectures, common implementations and variations are described in chapter 3. Chapter 3 also builds a foundation for chapter 4 were recent research regarding the two architectures are discussed. Some simulations of the polar and outphasing architectures are presented and analyzed in chapter 5. Both architectures are simulated using two switching amplifier configurations. Many circuit parameters are held constant to be able to analyze the the behavior of the two architectures. Chapter 6, serves as summary and the advantages and disadvantages are emphasized. The conclusions of this thesis are also presented, with proposals of a future research projects.

1.1 Performance Metrics for Radio Frequency Amplifiers

A power amplifier that operates on radio frequency signals have several requirements from various parts of the aimed application. From the communication

standard come requirements for linearity and output power. A certain amount of output power give the physical range of the transmitter. More output power will make the electromagnetic waves travel longer. The signal should also not be altered or distorted so that the receiver cannot decode the information. From the system context requirements can contain efficiency and cost. Efficiency is important especially for handheld devices, operated on battery power.

In Figure 1.1 a general power amplifier is shown, the input signal P_{in} or the power within it, together with the power consumed in the power amplifier itself P_{dc} is needed to produce the output signal P_{out}. The matching network is an arbitrary network which alters the behavior of the amplifier or modifies the signal, or both.

The *power gain* of the amplifier is defined as

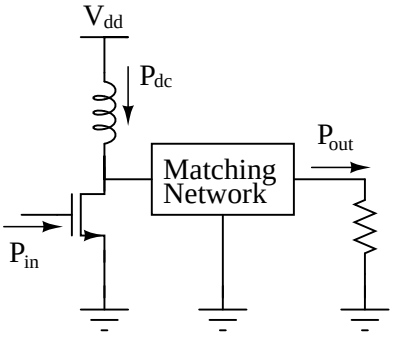

Figure 1.1. A general power amplifier

$$G_P = \frac{P_{out}}{P_{in}} \tag{1.1}$$

One common metric of efficiency is *drain efficiency* [2]:

$$\eta_{drain} = \frac{P_{out}}{P_{dc}} \tag{1.2}$$

It relates to how much power is wasted in the process of amplify the signal. To take the input power in respect, the *Power Added Efficiency* is defined as [2]

$$PAE = \eta_{power-added} = \frac{P_{out} - Pin}{P_{dc}} \tag{1.3}$$

1.1.1 Linearity Metrics

The linearity of an power amplifier shows how much the signal has been altered in the process of increase the power in the signal. There exist many metrics on linearity, one often used metric is the *Two Tone Test* [68]. The amplifier is fed

with the sum of two sinusoids, and at the output any non-linearities in the system will show up as spectral components in addition to the two fundamental tones. A linear system in mathematical sense means that a system with the outputs $y_1(t)$ and $y_2(t)$ for the inputs $x_1(t)$ and $x_2(t)$ respectively gives [62]

$$\alpha y_1(t) + \beta y_2(t) \quad = \quad \alpha x_1(t) + \beta x_2(t) \tag{1.4}$$

whera α and β is constants. The non-linearities of a system can be modeled with a polynomial model[27]

$$y(t) \quad = \quad \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x(t)^3 + ... \tag{1.5}$$

For example, a system with only cubic non-linearities, will produce when applied with a two tone test

$$y(t) \quad = \quad \alpha_1(cos(2\pi\omega_1 t) + cos(2\pi\omega_2 t)) + \alpha_3(cos(2\pi\omega_1 t) + cos(2\pi\omega_2 t))^3 \tag{1.6}$$

where the fundamental tone is left out. Using

$$cos^2(x) \quad = \quad \frac{1}{2}(1 + cos(2x)) \tag{1.7}$$

and

$$cos(x)cos(y) \quad = \quad cos(x+y) + cos(x-y) \tag{1.8}$$

gives that the spectral components except the fundamental tones will show up at the frequencies:

$$\begin{cases} 3\omega_1 \\ 3\omega_2 \\ 2\omega_1 + \omega_2 \\ 2\omega_1 - \omega_2 \\ 2\omega_2 + \omega_1 \\ 2\omega_2 - \omega_1 \end{cases} \tag{1.9}$$

The first two components are referred as *Harmonic Distortion*, these often do not need to be considered because they are often outside the designated frequency band, and thereby not disturb the transmission. There is a large chance these will be filtered out. The same can be said about the third and fifth terms. The fourth and sixth term usually end up very close to the fundamental tones, so they lie within the designated bandwidth and cannot be filtered out. The components that are dependent on both of the fundamental terms are called *Intermodulation Distortion* and these are the tones that are measured in a two tone test. The ratio between the fundamental and largest intermodulation product are called the *Carrier to Intermodulation Ratio* (C/I). A two tone test with the 3^{rd} intermodulation products and fundamentals are visualized in Figure 1.2. In general the fundamental tones will *blend* with each other producing tones at $\pm n \cdot f_1 \pm m \cdot f_2$, where m and n are integers. Some of these tones will show up in band were the system is transmitting which makes them impossible to filter out. [27]

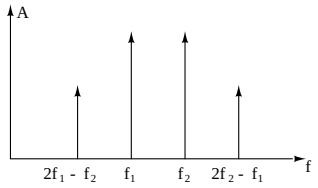

Figure 1.2. Two fundamental tones with their 3^{rd}-order intermodulation products

Other Common Linearity Metrics

The simulations regarding linearity in Chapter 5 are measured in carrier to interferer ratio. But many publications described in this thesis use other linearity metrics, depending on the aimed application. This sections purpose is to describe some of the commonly used metrics.

Multitone Intermodulation Ratio, M-IMR is a linearity metric for modulation formats which employs several carriers. It is defined as the ratio between the magnitude of the carrier to the magnitude of the largest intermodulation product. [27]

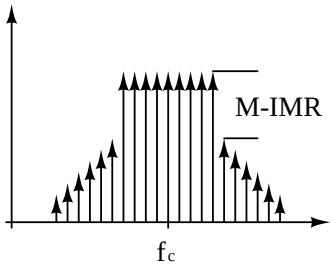

Figure 1.3. Multitone intermodulation ratio [27]

The *Adjacent Channel Power Ratio*, ACPR is defined as the power contained within the designated bandwidth divided by the power within the adjacent channels bandwidth. This metric describes how much power is spread into ambient channels and might corrupt other receivers ability to decode their signals properly. [27]

A common linearity measurement for modulation formats where the transmitted and received symbols can be visualized in a *Constellation Diagram* are *Error Vector Magnitude*, EVM. Every symbol that is transmitted can be visualized as dots in the imaginary plane. EVM is the magnitude of the error vector, defined as the difference of the ideal vector and the actual transmitted vector.

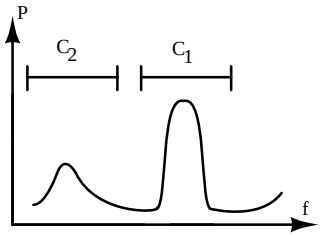

Figure 1.4. Adjacent Channel Power Ratio

1.2 Power Amplifier Classes

Even though the architectures discussed in this thesis most often use non-linear power amplifiers, it can have some value to briefly consider classes that are not relevant to the investigated topologies.

1.2.1 Linear Amplifiers

Linear amplifiers use the active device as a voltage controlled current source [36], the drain current follows voltage that are applied to the gate of the input transistor. The part that differs between these three amplifiers is how large part of the period the active device is conducting current, the biasing. For operation in class A the current source follows the input voltage for the whole period, 360°. An amplifier the operates in class B is conducting current exactly the half period 180°. Any amplifier that conducts current between one full to one half period is denoted as class AB.

The advantage with these amplifiers are the the drain-source voltage in the Figure of the general power amplifier 1.1 have a relatively linear relationship with the gate-source voltage.

Their disadvantage is that the efficiency is poor. Since the transistors conduct current large parts of the period, in addition to, at the same time have a non-zero voltage over it makes the transistor dissipates power. Under ideal circumstances these have an efficiency between 50%-78.5%. In an integrated environment these figures are hard to get even with switching amplifiers, which are described in the next section.

Overdriven Linear Amplifiers

The efficiency can be improved on linear amplifiers by *overdriving* them, by appying input signal levels that is larger than the linear range of the amplifier. The result is clipping of both the drain current and drain-source voltage. This will in turn lead to less current-voltage overlap. As larger the input signal amplitude is, as more the current through, and voltage over it look like anti-phase square waves.

This will increase the effectiveness of the amplifier, although the linearity will decrease. More harmonic components are added, as a result of the square-wave like behavior. The power gain will decrease by this method, but the output power is increased. The explanation for the rise in power is that the fundamental tone is higher than for its not over-driven counterpart.[15]

To conclude, as the harmonic content of the transistor will increase, the waveforms will *square-up*. The derivative will be sharper and decrease the voltage-current overlap, therefore increase the efficiency.

1.2.2 Switching Power Amplifiers

Another way to increase efficiency is to use the transistor as a switch. Instead of using the active device as a voltage controlled current source which decides when and how much current that flows to the load. The switch only decides when current should flow to, or from the load. How much current is decided by the surrounding components to the transistor.[36]

Class D

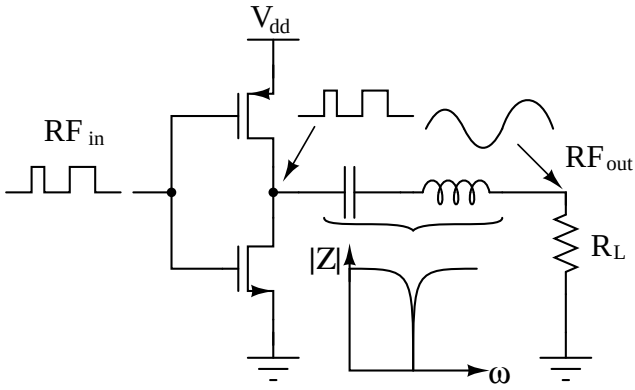

Figure 1.5. CMOS class D amplifier

In Figure 1.5 a Class D amplifier is shown. It works as a CMOS inverter, except for an added matching network. The operation is basically as the overdriven linear amplifiers described in previous section. The NMOS transistor is conducting for the positive half of the period and the current is drawn from the load, and for the negative half of the period the PMOS transistor is conducting and current flows into the load. The transistor completely switch on and off forcing the voltage waveform at the drains to change. The drain voltage are going to be a square-wave in anti-phase to the input. At the output a inductor-capacitor series tuned

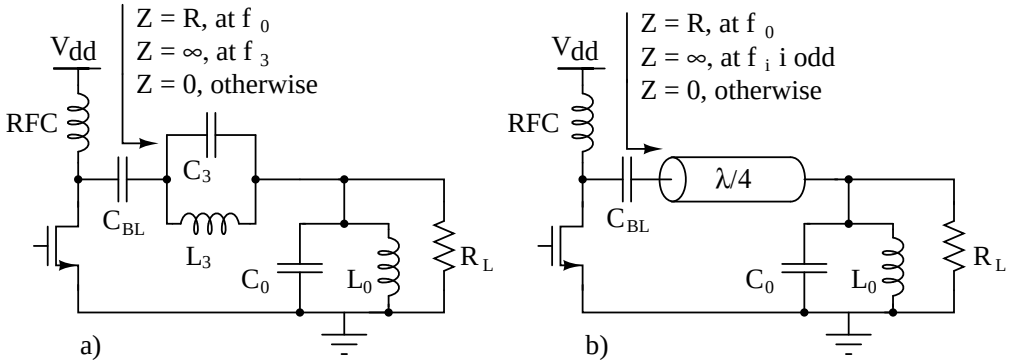

Figure 1.6. Two class F amplifiers, **a)** with parallel resonance at f_3 and **b)** with quarter-length transmission line

network which ideally has zero impedance at the frequency of interest and infinite impedance at any other frequency, so the current through the load is sinusoidal. This implies that the voltage over the load is sinusoidal. If the current through the load is sinusoidal at any period of time it means that current taken from the supply is a half sinusoid. The PMOS are conducting for the negative period in a half sine-wave fashion. If the active devices are operating together as a perfect switch no power can be dissipated in them, all power have to be dissipated in the load, and the efficiency is 100%. Of course this is an idealized situation which cannot be achieved, one of the disadvantages with class D is the short circuit current, the small periods of time of when both transistors are conducting. Currents will flow through the transistors at the same time as a non-zero voltage lies over it. [27]

A big drawback of this topology is the use of PMOS transistors. They are not as good as NMOS devices in their driving capability, which requires the PMOS to be several times larger than the NMOS. This leads to larger parasitic capacitance, which contributes to more loss. This action can be described as these capacitances are charged when during the negative part of the period, and during the positive part of the period they are discharged to ground. But also the input capacitance gets larger with increasing width of the transistors, which leads to higher input power needs to be supplied for correct switching action. [51] [2]

Class F

To achieve a small voltage current overlap the class F amplifier use a passive network to shape the waveforms at the drain. In Figure 1.6.a), two resonance networks consisting of $L_0 - C_0$ and $L_3 - C_3$ are added to the basic amplifier in Figure 1.1. The resonance network which are in parallel over the load R_L is tuned at the fundamental frequency which work as a harmonic trap, shorting every other frequency than the fundamental to ground. $L_3 - C_3$ are tuned at the third multiple of the fundamental and since $L_0 - C_0$ is presented as a short this resonance

network $L_3 - C_3$ are in parallel over drain of the transistor helping the voltage waveforms at the transistor drain to approximate a square wave. A square wave only contain odd harmonics, and the voltage over the resonator will add with the fundamental sine-wave which approximates a square-wave.

More resonators can be added in series with $L_3 - C_3$. Next that would be added is a resonator for the fifth multiple of the fundamental, and then seventh and so on. Addition of extra resonators will square up the drain voltage even more to reduce the voltage-current overlap.[46]

To have a perfect square wave at the drain of the transistor one an infinite number of resonators have to be added in series. This is of course not very practical, instead a transmission line can be used, see Figure 1.6.b). The transistor sees the impedance:

$$Z = Z_0 \frac{R_L + jZ_0 tan(\beta l)}{Z_0 + jR_L tan(\beta l)} \tag{1.10}$$

where Z_0 is the characteristic impedance of the transmission line, l=$\lambda/4$ the physical length of the transmission line and $\beta = 2\pi/\lambda$ the propagation constant which defines how the phase of the wave is affected by the transmission line. λ is the wavelength of the wave traveling in the transmission line [44].

For the fundamental frequency the impedance seen by transistor equals:

$$Z = \frac{Z_0^2}{R_L} \tag{1.11}$$

This can be used for up or down -convertion of the load, see chapter 3. For every other frequency than the fundamental the parallel network $(C_0 - L_0)$ is shorted to ground meaning that for equation (1.10) $R_L = 0$. [44]:

Then equation (1.10) gives for even harmonics of of the fundamental ($\beta l = \frac{\pi n}{2}$, n even) [44]:

$$Z = Z_0 \frac{jZ_0 tan(\beta l)}{Z_0} = 0 \tag{1.12}$$

And for odd harmonics ($\beta l = \frac{\pi(n+1)}{2}$, n even) of the fundamental

$$Z = Z_0 \frac{jZ_0 tan(\beta l)}{Z_0} = \infty \tag{1.13}$$

The use of quarter-wavelength transmission lines in integrated circuits should be avoided due to the huge area they would consume [51],[32], but as the applications using higher frequencies than 1-2 GHz will be more common, the size of the transmission lines will decrease. Thus, when designing integrated class F amplifiers in CMOS maybe the best choice at the moment is not to use a quarter-wavelength even if the space were unlimited because higher harmonics will be shorted to

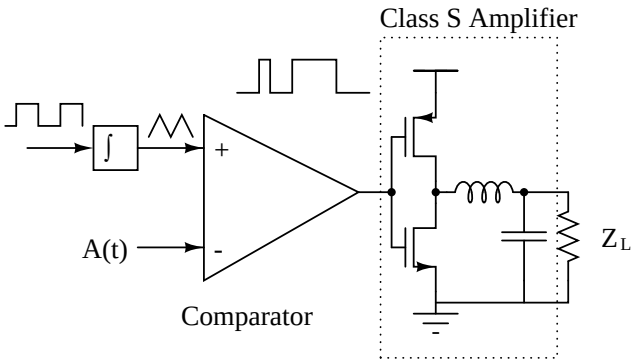

Figure 1.7. A class S amplifier in a common application; driven by a Pulse Width Modulator

ground through the parasitic drain-source capacitance of the transistor [69].

One advantage the class F power amplifier has for some applications that if the transmission line can be realized, it can serve several purposes at the same time. The transmission line both realize the class F amplifier but also as the power combiner, adding the output power from several amplifiers.[20]

Class S

As will be evident later a descendant of the class D amplifier, namely the class S amplifier is important to one of the discussed architectures. It is used not as the main power amplifier but to provide a variable power supply. As seen in Figure 1.7 the class S amplifier is the same topology as the class D amplifier except that a lowpass filter structure is in place of the series tuned LC network. By starting from left in the picture, a square wave with a 50% duty cycle is integrated resulting in a triangular wave. An analog signal (for example the amplitude, A(t) of equation 2.3)) is compared against a triangular waveform creating pulses, with the width proportional to the amplitude of the analog signal. This is called *Pulse Width Modulation* or PWM. These pulses are then amplified of the CMOS inverter structure and low pass filtered, diminishing the switching noise.[2]

Other possibilities of modulation is often used in conjunction with a Class S amplifiers with the use of polar transmitters but only PWM is described here to illustrate the concept.

Class E

The class E amplifier has some advantages over other classes. One is the ability to use parasitic capacitances of the transistor in the amplifier operation. But also the relative low number of extra components needed makes it a godd class for high efficiency solutions for radio frequency CMOS applications. [51] Therefore it can

be of value to describe somewhat more in detail. A schematic of a general class E amplifier can be seen in Figure 1.8.

As already seen there exist several ways to increase the efficiency of a power amplifier. The class E amplifier focus to maximize the efficiency by trying to have as little energy as possible to be dissipated in the transistor, which at times cannot be considered an ideal switch. As the class D amplifier forces the waveforms at drains to change, and if the transistors then are not ideal, there will be moments when large currents will go through the transistor at the same time as there are a non-zero voltage over it due to the on-resistance of the transistor, hence dissipating power.

If a passive network can be designed such as the voltage over the transistor goes to zero, just before the switch turn on. But also if the current through the transistor would drop to zero just as the transistor turns off, the efficiency will be very high. These waveforms are shown in Figure 1.9. What these highly speculative waveforms also is trying to show, is that it is not possible to have the current and voltage in total anti-phase, there will always be some current-voltage overlap for either the moments of switching.[2] [15]

The definition of a amplifier works in class E mode is that voltage over the transistor, should be zero just before switch opens, and this can be formulated as

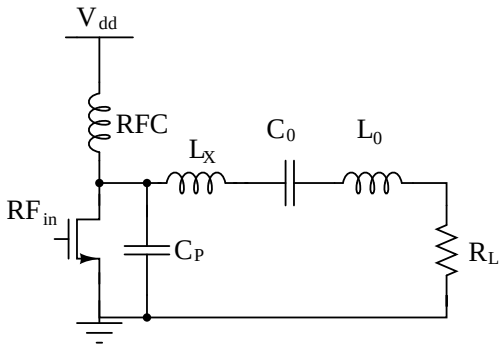

Figure 1.8. General topology of the Class E amplifier

$$\text{Class E} = \begin{cases} v_{DS}(t) = 0 \\ \\ \dfrac{dv_{DS}(t)}{dt} = 0 \end{cases} \tag{1.14}$$

where t is the time when the switch closes. The fact that the derivative should be zero means that the current through the switch is also zero when the switch

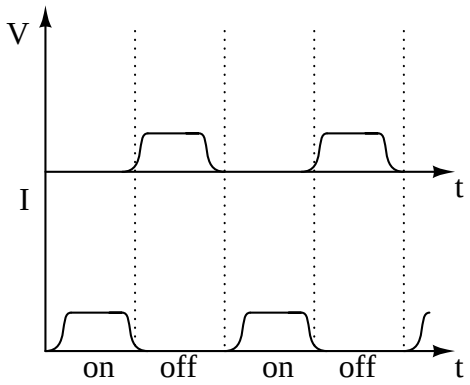

Figure 1.9. Conceptual waveforms of class E

starts to open. This is not necessary but gives headroom for eventual component mismatches. [27]

To have some relation to the class E operation more in detail one can describe the voltage over the switch capacitor network; The current through the load is sinusoidal because of the series tuned matching network, $L_0 - C_0$, which equals $I_{rf}\cos(\theta)$. This current has to alternate between the switch and capacitor C_P. When the switch closes the capacitor starts to charge, but before the switch opens again it discharges the capacitor through the load network. Therefore the voltage over the switch is [15]:

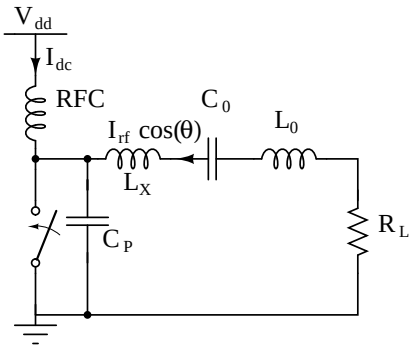

Figure 1.10. Class E with transistor as a switch

$$
\begin{aligned}
v(\theta) &= \frac{1}{\omega C_P} \int_{\alpha_2}^{\theta} I_{dc} + I_{rf} cos(\theta) \\
&= \begin{cases} 0, & -\alpha_1 < \theta < \alpha_2 \\ \dfrac{I_{dc}}{\omega C_P}(\theta + m \cdot sin(\theta) - \alpha_2 - m \cdot sin(\alpha_2)), & \alpha_2 < \theta < 2\pi - \alpha_1 \end{cases}
\end{aligned} \tag{1.15}
$$

where α_1, α_2 are the instants when switch closes and opens respectively, m equals the ratio between I_{rf} and I_{dc}, and $\theta = \omega t$. When the switch opens the voltage starts to rise but due to the sinusoidal current the capacitor discharges after a while and both the voltage and the slope of the voltage reaches zero just before the switch turns on again. Which means losses can be reduced. A more realistic voltage waveform over the capacitor and switch can be seen in 1.11.

To reflect back at the claim of that transistor parasitics can be used as a part of the amplifier operation, means that the drain source capacitance can be included in the shunt capacitor C_P. So a very large transistor can be used to decrease the on-resistance of the switch but will also have the positive side effect of a smaller C_P. The limit of the transistor width is when C_P depends solely on transistor parasitics. [51]

Moreover this parasitic capacitance is non-linear should be accounted for. If not, unexpected voltage peaks can be seen over the device which can potentially destroy the transistor.[37]

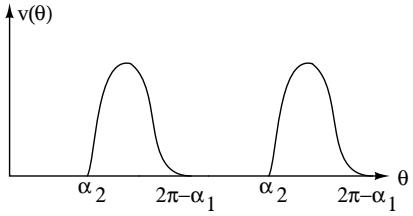

Figure 1.11. Conceptual waveform of the voltage over the switch capacitor network in class E amplifier [15]

Chapter 2

Linearization Techniques

This chapter aims to describe the two discussed architectures on a block level together with their major sources of distortion. Some publications will be described that focus on how to minimize these sources of distortion on a system level. Also in the beginning of this chapter, linearization techniques that are often used in conjunction with these two are briefly described.

2.1 Auxiliary Linearization Techniques

2.1.1 Feedback

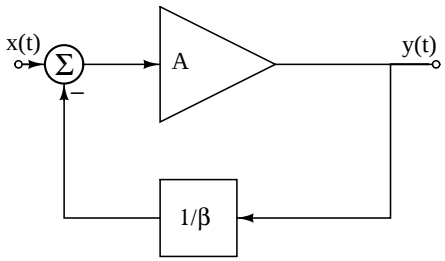

Figure 2.1. Basic block diagram of negative feedback

Examining Figure 2.1 there is an amplifier with gain A and a feedback network with feedback factor $\frac{1}{\beta}$. A part of the output signal is led back and is subtracted from the input. The difference between these two signals is called the error term, which amplified is equal to y(t). To investigate how distortion acts on feedback system a distortion source d(t) is added after the amplifier adding directly to the

output y(t). Solving for y(t) with the assumption that A » β will result in [27]:

$$y(t) \quad = \quad \beta x(t) + \frac{\beta d(t)}{A} \tag{2.1}$$

Evident from the equation is that β defines the gain of the system rather than the amplifier gain A. Also a higher β will also result in higher distortion. The amplifier gain will minimize the distortion proportionally.[27]

Other important properties of feedback is that it can lead to stability problems if the phase of the input is altered to much in the feedback loop the negative feedback can turn out to add in-phase with the input. A positive side effect is that the bandwidth is increased. If the bandwidth of the amplifier without feedback is B_0 the bandwidth with feedback equals $B_0(1 + A \cdot \beta)$. [49]

2.1.2 Predistortion

Another way to trying to correct the nonlinearities of a system is to find the inverse of the system transfer curve, and to complementary distort the input signal in a opposing way. Hopefully this will lead to that the output characteristic will have the desired linear shape. Looking at Figure 2.2 the dashed curve is the power amplifier characteristic. The complementary distorted function is the dotted line and the combined function is the solid line. [27]

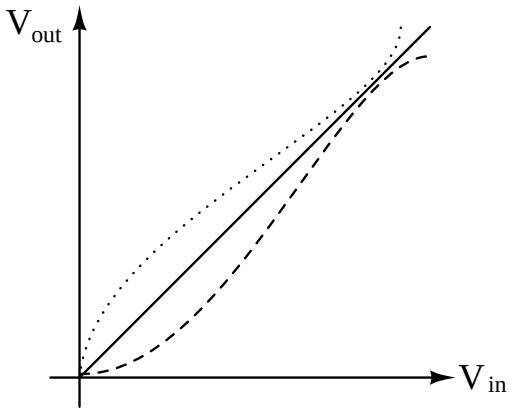

Figure 2.2. Predistortion

2.2 The Polar Linearization Technique

2.2.1 Mathematical Representation

Digital modulation systems systems can be represented as

$$m(t) \quad = \quad x(t)cos(\omega_c t) - j \cdot y(t)sin(\omega_c t) \tag{2.2}$$

Where ω_c is the carrier of the signal. The baseband data or the information to be transmitted are represented as the *In-phase* component, x(t) and the *Quadrature* component y(t). [51]

A visualization of the equation can be seen in Figure 2.3. Each point in the

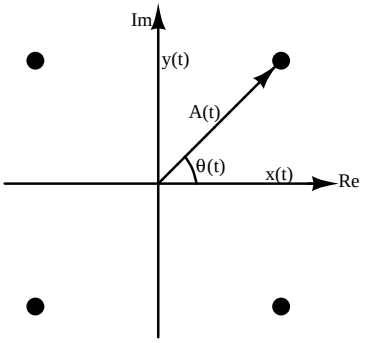

Figure 2.3. Polar representation

figure can be represented by its polar coordinates instead [12],

$$m(t) \quad = \quad A(t) \cdot cos(\omega t + \phi(t)) \tag{2.3}$$

where

$$A(t) \quad = \quad \sqrt{x(t)^2 \quad + \quad y(t)^2} \tag{2.4}$$

$$\theta(\mathrm{t}) \quad = \quad arctan\left(\frac{y(t)}{x(t)}\right) \tag{2.5}$$

Equation (2.4) and (2.5) forms the basis of the *Polar Linearization Technique*. The phase and amplitude can be separated, and precessed individually before recombination.

2.2.2 Block Level Description

The Polar Linearization Technique was first proposed in the fifties under the name of *Envelope Restoration and Elimination*, EER [24]. The idea was to eliminate the use of linear amplifiers that operates on high frequency signals, such as AM broadcasts. In Figure 2.4 the original proposed architecture with associated waveforms

is shown. The AM signal, which has a varying envelope, is fed to an envelope detector and a limiter. The limiter preserves the carrier and eliminates the envelope of the signal. In the lower path the opposite is performed and the envelope is preserved and the carrier is eliminated from the signal. The envelope is then fed to an *Audio Frequency amplifier*, and works as the power supply for the main amplifier which can of be any high-efficiency amplifier class such as D,E or F. When the envelope is used as a power supply the voltage waveform at the transistor drain, the carrier, is amplitude modulated. Thereby the original signal is restored. [24] Modern variants of the polar architecture do not have the need for the limiter

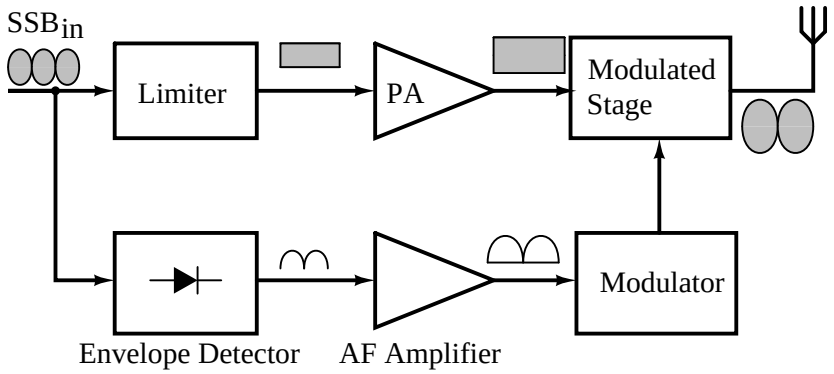

Figure 2.4. Block diagram of Envelope Restoration & Elimination

or the envelope detector. A digital signal processor could provide these signals instead. In Figure 2.5 a block diagram is shown. The baseband processor provides the in-phase and quadrature symbols that should be transmitted to a converter for Cartesian to Polar representation. The phase data is up-converted in frequency by a carrier generated by a *Phase Locked Loop*, PLL. The efficiency of a polar system is dependent of course not only on the main amplifier but all the components used in the architecture. If the signal generation is considered lossless in comparison to the amplifier part the efficiency can be formulated as [51]

$$\eta_{polar} \quad = \quad \eta_{MainAmp} \cdot \eta_{AFamp} \tag{2.6}$$

As the efficiency is closely dependent on the audio frequency amplifier there exist an incitement that this also should be a switching amplifier, however the factors of distortion associated with these make some recommend linear amplifiers [51]. The switching amplifiers used in polar transmitters are often class S amplifiers described in Section 1.2.2.

2.2.3 Factors of Distortion

The polar amplifier architecture have three major sources of distortion. The first two, time delay and the bandwidth of the envelope can be considered architectural

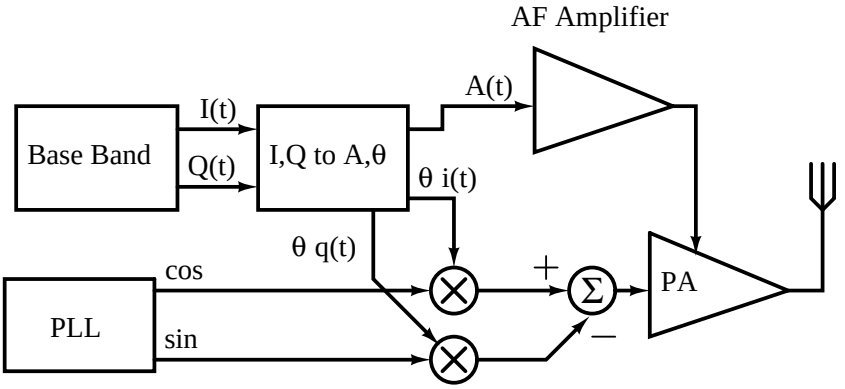

Figure 2.5. Modern polar transmitter [51]

problems, whereas feedthrough in the main power amplifier is dependent of the class of operation, circuit topology or maybe the process which the amplifiers are manufactured in. The first two can also be considered to stem from the same component, namely the choice of the audio frequency amplifier.

Delay between Envelope and Phase Path

The envelope path is relatively slow compared to the phase path in the polar architecture. This depends mostly if a low pass filter is incorporated in the audio frequency amplifier. Then the delay can become several large which have to be compensated by adding delays in the phase path [45]. This kind of distortion is inherent in the polar transmitter and cannot be avoided. At least in the topology investigated in this thesis.

A mathematical investigation performed predicts that power in the intermodulation sidebands are proportional to the square of the delay τ times the square of bandwidth of the radio frequency signal, or [45]:

$$S_{IMD} \quad = \quad \pi(\tau \cdot B_{RF})^2 \tag{2.7}$$

And the theoretical carrier to interferer ratio are plotted for several values of $\tau \cdot B_{RF}$ in 2.6. A RF bandwidth of 20 MHz and a wanted carrier to interferer ratio of 35 dB the delay cannot be more than 5 ns.

Finite Bandwidth of the Envelope Amplifier

The other source of distortion that is highly dependent on the low pass filter are the bandwidth. Fast fluctuations in the envelope will be obstructed by the filter and this will lead to distortion. Since the bandwidth of the envelope is related to the bandwidth of the original signal the filters is measured in the ratio of the two. In a polar transmitter the separated signals have very large bandwidths compared to

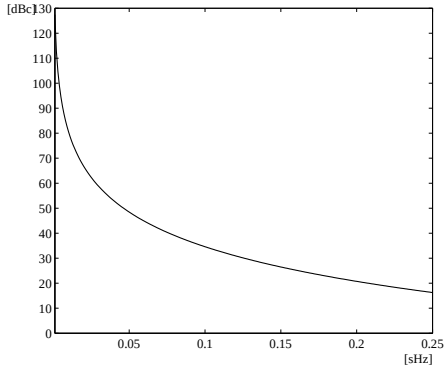

Figure 2.6. Carrier to interferer ratio as a function of τB_{RF} [45]

the compound signal. In a two tone test the largest unwanted spectral components should be the next to N^{th} odd order intermodulation product, where N equals:

$$N = INT(\frac{B_e}{B_{rf}}) \tag{2.8}$$

where INT means a truncated integer, and B_e is the bandwidth of the envelope and B_{rf} is the bandwidth of the original signal. So if N is calculated to be equal to 7, the dominating intermodulation product is predicted to be the 9^{th}. So, theory predicts that one could choose a bandwidth for the class S modulator where the 3^{rd} order not dominates the spectrum, unfortunately measurements have shown that theory do not pitch well with practice in this case. [45]

So there exists a tradeoff between how large bandwidth of the envelope and the switching frequency of the class S modulator. For the distortion from the switching to be under 40 dB under the fundamental tone the frequency should be between five times larger than the envelope bandwidth [2] to more than ten times [51]. What kind of filters used have an impact on the magnitude of the intermodulation products. It is generally better in terms of distortion not to use filters with the focus on a linear groupdelay characteristic, such as Bessel-filters. Butterworth and Chebyshev has shows comparable distortion, but has focus of maximum flat passband and large attenuation in the stopband respectively, but larger variations in groupdelay.[35]

Feedthrough

The *dynamic range* of a transmitter is the difference between the highest and lowest output power. Ideally for a polar transmitter one should be able to use the whole power supply as dynamic range. [29] A phenomena called feedthrough limits the lower bound of the usable envelope, and it worsens at low supply voltages. This

is called AM-AM distortion since because it is an input amplitude component producing an error in the amplitude of the output signal. [50]. The input signal

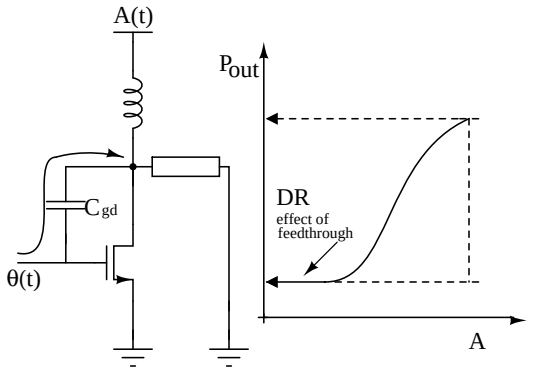

Figure 2.7. Feedthrough in polar transmitters, AM-AM curve is in log-log scale

couples via the gate-drain parasitic capacitance of the transistor, see Figure 2.7. Not only does the drain voltage not go to zero but distortion mechanisms are corrupting the phase of the output signal at low supply voltages. The output voltage is 180° out of phase with the input voltage, and the voltage that appears at the output due to feedthrough is only 90° out of phase with respect to the gate voltage. In addition since it is not the gate voltage controlling the output voltage but the envelope. The feedthrough voltage will be the same, independent of the envelope. Therefore the phase of the output voltage will vary when the envelope varies. The distortion mechanism is called AM-PM distortion due to it is an amplitude component creating a phase error. [51]

2.2.4 System Level Distortion Correction

This section explores recent research system level distortion correction applicable to polar transmitters.

Envelope Feedback

One of the first integrated polar transmitters employed envelope feedback around the power supply modulator, see Figure 2.8.a. And in 2.8.b the schematic of the envelope detector used, where transistor M_1 works as a diode. The right half of the circuit is an attempt to decrease the distortion by keeping the gate of M_2 equal to the envelope of s(t). This circuit could extract the envelope with a bandwidth of around 100 kHz. The EVM requirement were not fulfilled without the envelope feedback [60]. To the author's knowledge there have not been any recent publications exploring envelope feedback for larger bandwidths.

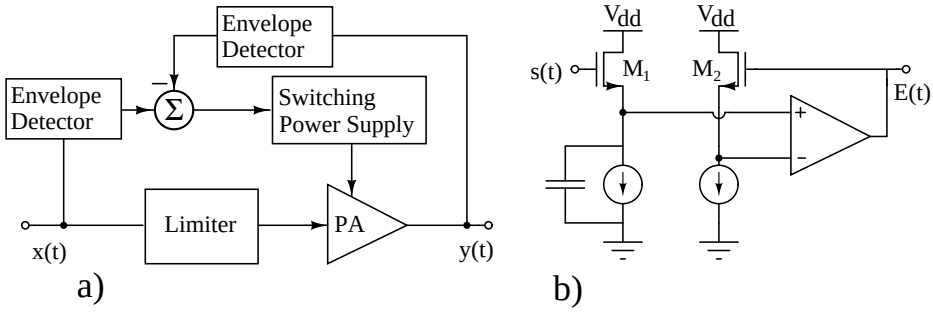

Figure 2.8. Envelope Feedback in a polar transmitter

Phase Feedback

Feedback is not limited for for envelope signals as described above but can also be used to mitigate some of the AM-PM distortion in switching amplifiers. A basic block diagram can be seen in Figure 2.9. As seen in the block diagram the phase of the input signal is shifted to counteract the distorted output signal. The input is phase shifted since the class E amplifier is an inverting amplifier. This is used by the phase detector to compare the input and output phase. The phase detector outputs a pulse train corresponding to phase differences, which is filtered so that a DC-like voltage controls a phase shifter. Reported measurements shows that the phase error can be reduced to around 4°, over the whole range of the power supply. The amplifier solely had a phase error for some values of the power supply near 30°. [59]

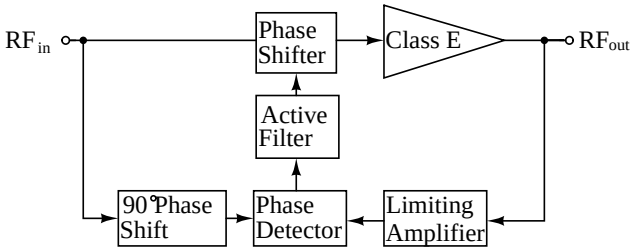

Figure 2.9. Phase feedback [59]

Feedthrough Reduction

Feedthrough can be omitted by several approaches, in this section two approaches are briefly described. The gate-drain capacitance can be resonated out at the frequency of interest with an inductor as in Figure 2.10.a). The impedance seen at the gate are then infinite. Simulations show a 5 dB improvement in feedthrough,

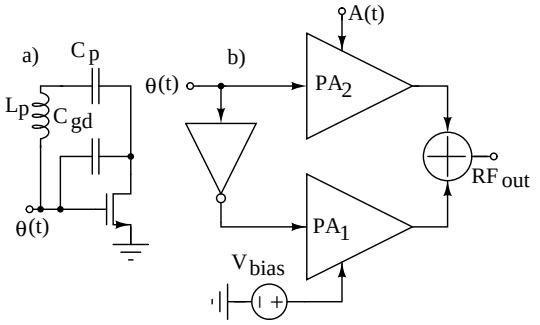

Figure 2.10. Reducing feedthrough in polar transmitters with **a)** resonance [21] and **b)** Feedforward [39]

but this come with rather high price. The gain is reduced and for high envelope levels the circuit experience some amplitude compression. The amplitude of the output have a square-wave like behavior.[21]

The feedthrough can also be corrected on a system level as seen in 2.10.b). Two identical power amplifiers PA_1 and PA_2 are fed with the a differential signal which the anti-phase signal is created by the means of an inverter. PA_2 does not have a power supply attached, thereby only creating feedthrough. The outputs is then added, or rather subtracted since the changing the phase of signal is equivalent of changing sign. So the idea is to subtract the feedthrough from the main amplifier. The bias voltage to PA_2 is equal to zero if both amplifiers are matched, so that the output of PA_2 only contains the feedthrough level. It is not easy to match to amplifiers, so V_{bias} can be changed to make up for mismatch. Results of a multi-carrier signal, although only simulations shows a improvement of ACPR with 19 dB and a improvement of M-IMR of 21 dB. [39]

Predistortion

A polar transmitter with digital predistortion has shown that an improvement of ACPR of 6 dB. The focus on the predistorter was to correct for the transistor knee voltage, and that output voltage from a polar transmitter have not a linear relationship to with the supply voltage.[33]

2.3 The Outphasing Linearization Technique

2.3.1 Mathematical Representation

Equation (2.3) also forms the foundation for the Outphasing Linearization Technique. If one rewrites that equation as

$$m(t) \quad = \frac{\hat{A}}{\hat{A}} \quad A(t) \cdot cos(\omega t + \phi(t)) \tag{2.9}$$

$$m(t) \quad = \quad \hat{A}cos(cos^{-1}(\frac{A(t)}{\hat{A}})) \cdot cos(\omega t + \phi(t)) \tag{2.10}$$

and using that

$$cos(x)cos(y) \quad = \quad cos(x+y) + cos(x-y) \tag{2.11}$$

$$m(t) \quad = \quad \hat{A}(cos(\omega_c t + \phi(t) + \alpha(t)) + cos(\omega_c t + \phi(t) - \alpha(t))) \tag{2.12}$$

where

$$\alpha(t) \quad = \quad cos^{-1}((\frac{A(t)}{\hat{A}}) \tag{2.13}$$

α is called the *Outphasing Angle*. So one can also accomplish the same purpose as the polar method by only using two phase modulated signals, if the signals are then added after amplification.

2.3.2 Block Level Description

The Outphasing Technique, or *Linear Amplification with Nonlinear Components* (LINC) [13], are based on the derivations in the previous section. Two signals that only varies in phase would after combining produce a signal that both varies in phase and amplitude. m(t) and the two constant envelope signals, $m_1(t)$ and $m_2(t)$ in a vector diagrams can be seen in Figure 2.11. So the maximum amplitude m(t) will occur when $m_1(t) = -m_2(t)$. However if the summing component has an additive or subtractive property depends on the component used. Which implies that the power combiner used will have an impact on the function of the signal separator. Signal separation by analog means for the outphasing technique is com-

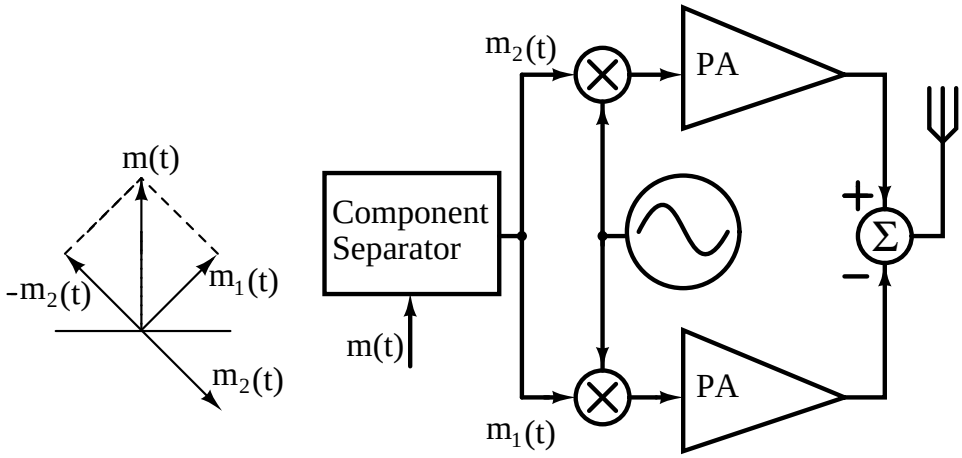

Figure 2.11. Block diagram of the LINC transmitter with upconversion, after [13]

plex [27], and often includes more components than for the polar counterpart [13]. But recent studies have shown that, single carrier constant envelope applications

it is possible to get a suppression of the intermodulation products of around 50 dB [56]. But also for multi carrier applications an ACPR of 33.9 dB [40] is possible.

When using digital signal processors the signal generation for baseband data are not all different from polar transmitter. The quadrature and in-phase component are used to generate two constant envelope functions by [27]:

$$\begin{cases} m_1(t) &= m(t) + e(t) \\ m_2(t) &= m(t) - e(t) \end{cases} \tag{2.14}$$

where

$$e(t) = -y(t)\sqrt{\frac{1}{x(t)^2 + y(t)^2} - 1} + j \cdot x(t)\sqrt{\frac{1}{x(t)^2 + y(t)^2} - 1} \tag{2.15}$$

and x(t) and y(t) are as before the in-phase and quadrature components respectively.

2.3.3 Factors of Distortion, Mismatch

The large source of distortion in the outphasing technique are if the two paths are in any way asymmetric. If the signal is phase-shifted or amplified differently, the result will be incorrect cancellation at the output.

If one of the paths were introduced with an imbalance,

$$\begin{cases} S_1(f) &= S(f) - E(f) \\ S_2(f) &= (S(f) + E(f))(1 + G_{error})e^{j\theta_{error}} \end{cases} \tag{2.16}$$

then the sum at the output will be

$$O(f) = S(f)(1 + (1 + G_{error})e^{j\theta_{error}}) + E(f)((1 - (1 + G_{error})e^{j\theta_{error}})) \tag{2.17}$$

The difference for the first part is negligible if the error are small enough. The second part will never become zero, if not both the phase error and gain are zero, so there will always be some error at the output. So the distortion could be traced back to the component which makes the signals in the two paths constant envelope, e(t). [27]

Both gain and phase mismatches will show up at the output as fluctuations in the envelope and phase. However the LINC architecture does not amplify asymmetrically added distortion in one of the paths. But for small values of the envelope the distortion can be comparable or larger than the wanted signal.[13]

Different modulation formats have different sensitivity to mismatch. For example, n-QAM formats will respond differently to imbalances in the paths. 4-QAM, with four constellation points have been shown to be much more forgiving than 16 or

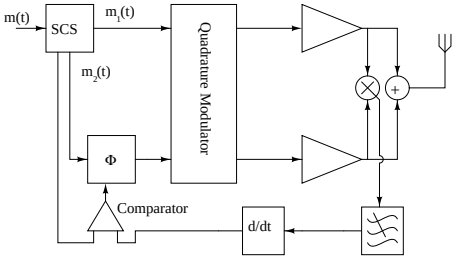

Figure 2.12. Outphasing distortion correction [66]

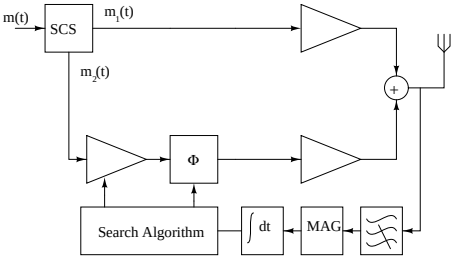

Figure 2.13. Outphasing distortion correction [61]

64-QAM. This may seem obvious when the later two have 16 or 64 constellation points distributed over the same area in the imaginary plane. [8]

One common multicarrier system with 52 carriers, where each carrier are modulated with 64-QAM have requirements of a -27 dB, ACPR and a 5.6 % EVM. The requirement of ACPR can be fulfilled with hefty 10 degrees and around 1 dB of phase and gain mismatch respectively. But the error vector magnitude sets tougher requirements of symmetry, only a 0.3-0.4 dB gain error, but still several degrees of mismatch are tolerated.[53]

2.3.4 System Level Distortion Correction

Several system level designs have been proposed to reduce effects of mismatch, where a couple is described here. In Figure 2.12 a mixer is used to find the phase error of a outphasing transmitter. The result is compared with a reference to shift the phase of one of the branches. If y(t) is the output of the mixer, and α_e is the phase error introduced in one of the paths:

$$\begin{aligned} y(t) &= sin(\omega_c t + \theta(t) + \alpha + \alpha_e) sin(\omega_c t + \theta(t) - \alpha) \\ &= -\frac{1}{2}(cos(2\omega_c t + 2\theta(t)) + cos(2\phi + \alpha_e)) \end{aligned} \tag{2.18}$$

which is low pass filtrated leaving only

$$y_{LPF}(t) = \frac{1}{2} cos(2\alpha + \alpha_e) \tag{2.19}$$

and differentiated

$$y'_{LPF}(t) = \frac{-1}{2} sin(2\alpha + \alpha_e) \tag{2.20}$$

So the phase error can be quantified with relatively easy.

$y'_{LPF}(t)$ can be measured and compared against a reference signal. The difference are thereafter used in a variable phase shifter which changes the phase in one of the branches accordingly. Reported results have shown that with a single

carrier system at 900 MHz and with a phase distortion of 20°, gave a reduction in phase error around 2°.[66]

In Figure 2.13 both phase and gain error can be corrected for. The output is highpass filtrated for finding the magnitude of the out of band distortion. These are integrated for to find a mean value which controls a search algorithm to find the optimum phase and gain compensation. Measurements with a narrowband signal show that the simulations get more effective as more symbols are integrated over, with convergation to around 70 dB ACPR with 70 or more symbol integrations. [61]

These tactics for diminishing errors needs a fairly large amount of components to work. Even though neither have to be converted back to baseband symbols before correction many of these would require digital computations. But an advantage of these approaches are that they are indifferent on the modulation formats used [3].

Chapter 3

Power Combiners & Matching

This chapter has the intention to first describe the matching problems associated with radio frequency power amplifiers, then transformers in integrated circuits and at last transcend into power combiners and their applications. The purpose of this chapter is to describe combiner topologies used in next chapter but also make to build a foundation for an evaluation what types of combiners are suitable be used for both discussed architectures.

For the outphasing topology the power combiner is a vital part of the architecture, there is no way without using it. One cannot simply short-circuit the drains of the output transistors. It will lead to a variable envelope at the transistor drain, which may disturb the operation of the amplifier and to a droop in efficiency [38]. Recent publications regarding the polar topology also often make use of power combiners. The purpose is though, totally different from the motivations for the outphasing technique. The intention for the polar architecture is to enhance various properties of the amplifier, where to most obvious are to use multiple amplifiers to increase output power.

3.1 Matching

For the general amplifier in Figure 1.1 in the introductory chapter it was stated that the output network was to filter out or modify the signal in some way. One important factor is to filter out unwanted tones to preserve spectral purity. By contaminating the spectrum one can can potentially destroy other receivers ability to receive their designated signal pleasantly. A maybe more important factor is that the transmitted signal power can be increased by *down-converting* the load R_L in Figure 1.1.

Antennas often have an impedance of 50 Ω, and in recent CMOS processes have

a supply voltage close to 1 V. It is not possible to output enough power for many communications systems, not even under ideal circumstances [5]. For example consider the above, with a 50 Ω load and 1 V power supply. The power dissipated in the load for some amplifiers are equal to $V_{dd}^2/(2R_L)$ [2] gives

$$\mathrm{P_{out}} = \frac{\mathrm{V_{dd}^2}}{2\mathrm{R_L}} = \frac{1}{100}\mathrm{W} \tag{3.1}$$

The power supply cannot be increased very much, but the load can made smaller with various circuit topologies. A simple circuit for impedance matching is shown in Figure 3.1. The reactances X_S and X_P indices means that the reactances are in *series* and in *parallel* in relation to the source and load respectively. The idea is that the drain of the transistor should see a smaller load than it really is. How the circuit in 3.1 fools the power source into believing that the load is small, it is dependent of that the inductor-capacitor have a resonance frequency. So with appropriate values of $\mathrm{X_S}$ and $\mathrm{X_P}$, energy is transferred back and forth between the two reactive elements. A voltage source driving the L-match which together with the load, would look like a RLC tank, due to the zero impedance of the voltage source. The current through the inductor due to the resonance will be much larger than the current provided by the voltage source so it will look like the resistance have dropped in magnitude. [32]

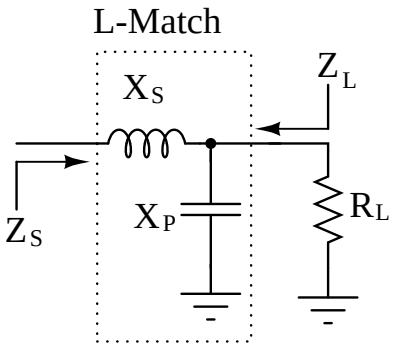

Figure 3.1. A L-match with down-conversion

3.1.1 Resistive Parasitics Due to Finite Q

The *Quality factor*, or the Q-factor of an arbitrary reactance is a measure of how lossy a component is. Since energy cannot be dissipated in an ideal reactance the lossy part can be modeled by a resistor either in series or in parallel with the

component. The Q-factor relates to the resistance as [32]:

$$\begin{cases} R_S = \dfrac{X_S}{Q} \\ R_P = \dfrac{Q}{X_P} \end{cases} \tag{3.2}$$

When values of the quality factors are declared in publications, at least for inductors it is often in the order of 6-13. There exists at least one publication with higher values. A reported inductor with a Q around 15 over a bandwidth of several hundred megahertz, with a center frequency of 5 GHz [58].

3.2 LC-Combiners

Combining power from several differential amplifiers can be performed with only inductors and capacitors. The LC-combiner is derived from the L-match previously discussed. In Figure 3.2 two amplifiers combine their powers through the combining network which is made up through C_m and L_m. Where the series components are made up from the basic L-match and the shunt reactances provides so that each amplifier branch sees a resistive load at the frequency of operation.[52], [51]

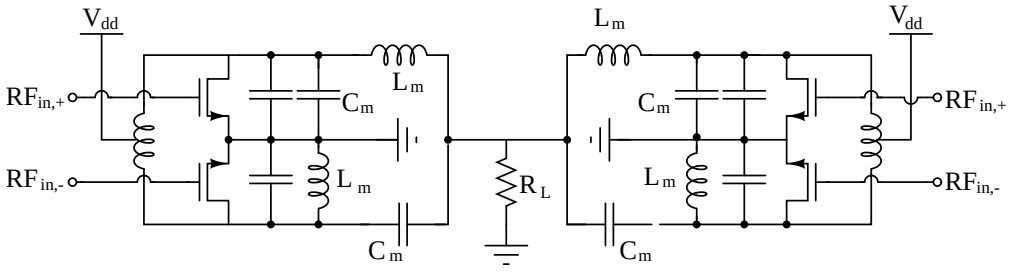

Figure 3.2. A LC-Combiner combining power from two differential power amplifiers

3.3 Transformers

An ideal transformer as seen in Figure 3.4 have two sides, the primary and secondary. Two inductances with number of turns N_i and its inductance L_i. A test source (not shown) applied over the primary side (V_P) which produces a current I_P. This current through the primary will produce a magnetic field which induces a voltage over at the secondary side proportional to the derivative of I_P. [63]

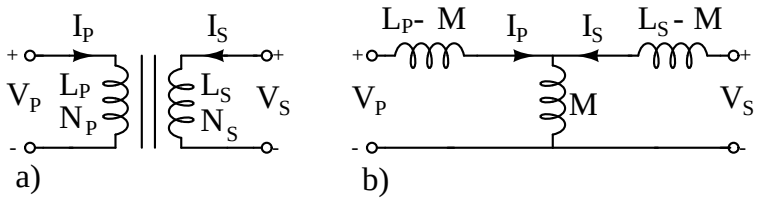

Figure 3.3. A Transformer, indexes denote the primary and secondary side, **a)** Symbol **b)** Equivalent Circuit

If the transformer is ideal, it is lossless and linear, one can derive that a transformer can be used as transforming impedances via:

$$Z' \quad = \quad (\frac{N_S}{N_P})^2 \cdot Z \tag{3.3}$$

The impedance looking into the transformer can be converted up or down from Z to Z' by appropriately changing the turns ratio of the transformer. [63]

Transformers in integrated circuits can be formed in a number of ways, in Figure 3.4 shows a *Interleaved Transformer*. The name relates to that the primary and secondary turns are together forming a spiral. The interleaved transformer main advantages is symmetry and the relatively separated ports makes connections to related circuitry an ease. Another advantage is that they only use one metal layer, preserving space for other circuitry. [34]

The *Stacked* transformer is constructed in at least two metal layers to maximize the flux between the two sides. However processes where the metal layers have different thickness will introduce asymmetry. Another drawback is that the parasitic capacitance to the substrate differ from the two layer since the lower shields the upper and so that the power loss differs. Maybe the biggest drawback is that the metal in the two layers couple through parasitics, forming a parallel plate capacitor. This parasitic capacitance limit the bandwidth of the transformer because high frequency signals will shunt to the secondary. This can be partially removed by offsetting the two inductors. If more than two metal layers are available one can leave out one metal layers, which will not seriously reduce the effectiveness of the transformer.[32], [34]

So there exist some tradeoffs when constructing integrated transformers, an investigation that tested transformers in balun configurations showed that less loss can be expected over larger frequency ranges for interleaved types. [16]

3.3.1 Distributed Active Transformer

One of the most frequently used techniques for power combining is the *Distributed Active Transformer*, DAT. Originally proposed to solve several issues with combining and transformation networks. The motivations of using transformers are

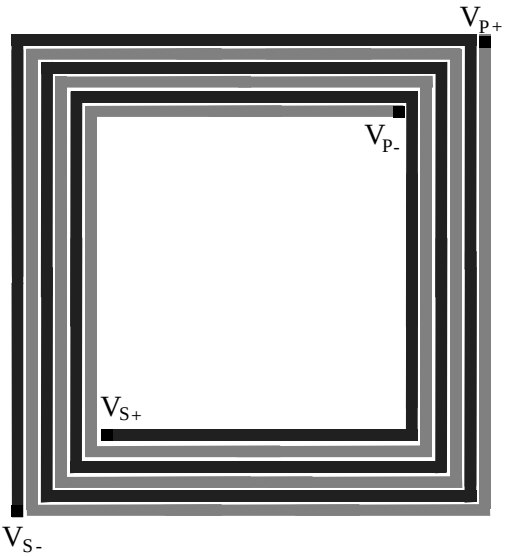

Figure 3.4. An integrated transformer implemented in one metal layer, and shadings clarify primary and secondary

largely based on that impedance transformation compared to than resonant downconversion is less lossy. The loss for both types are relative to how much the load is downconverted, however transformers are also less lossy for higher downconverions. [5], [6]

The idea is that instead of downconverting the load by changing the turns ratio of the transformer, several differential amplifiers connected to several transformers, connected in series can accomplish the same thing, see Figure 3.5. N differential amplifiers will downconvert the load N times. The inductors used are only a very wide metal layer, or *slab* inductors. Which has the advantage of high quality factor due to low series resistance, because of the large conductor width. The amplifiers in Figure 3.5 are also put in such a configuration that virtual grounds can be shared not only within the differential pair but also with neighboring amplifiers, as long as the closest amplifier branch are in anti-phase. This can seen in Figure 3.5 that the input bias inductors and drain capacitors are for layout reasons not shared in the differential pair but with the closest amplifier branch. [6]

The amplifiers in Figure 3.5, which are extracted from the original publication, are not operating in class E [26], but the exact topology can be used [30], which is essentially copied by many for the polar amplifier topology. Even though the the DAT is supposed to downconvert the load by N, an investigation have shown that it is not always the case: An implementation from that publications shows that a conversion of 50 Ω by four, should make each amplifier see 12.5 Ω, however variations due to parasitics aree rather large. The lowest measured in the investigation

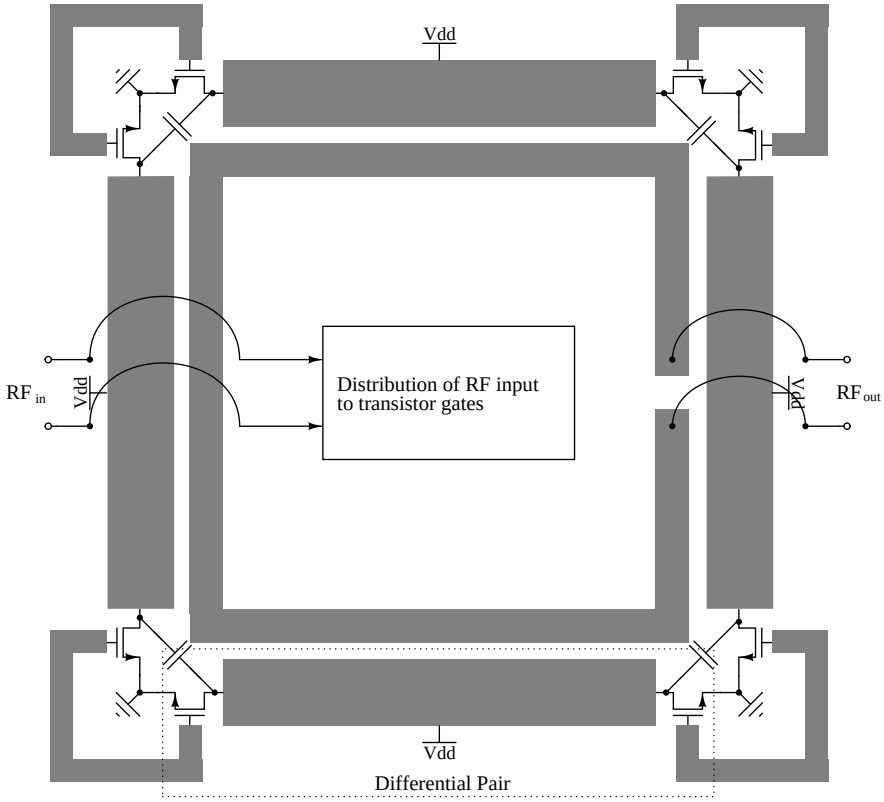

Figure 3.5. A complete DAT with four power amplifier cells [6]

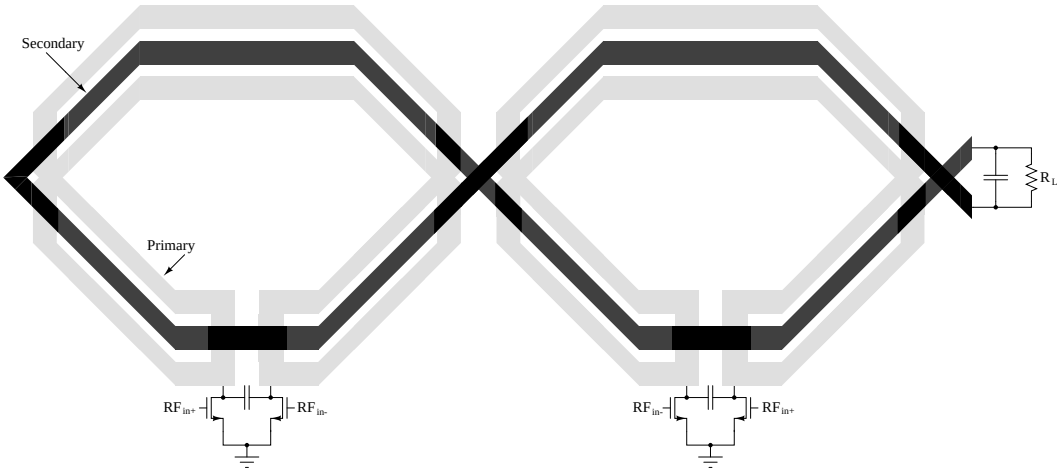

Figure 3.6. Parallel Combining Transformer [19], [18]

were around 43 Ω and highest impedance over 7 times to the ideal, 92 Ω. [9]

Series/Parallel Combining Transformers

A distinction can be made between different distributed active transformers. If the amplifiers are connected in series or in parallel they are called *Series Combining Transformers* (SCT) and *Parallel Combining Transformers* (PCT) respectively. The power combiner described in previous section are an example of a SCT, and an example of a PCT can be seen in 3.6. Much of the differences between the PCT and SCT can be seen by their respective input impedance [4]:

$$\text{input impedance} = \begin{cases} \mathrm{R_{in,SCT}} = \mathrm{R_1} + \dfrac{1}{\mathrm{N}}\dfrac{\mathrm{N_1^2}}{\mathrm{N_2^2}}(\mathrm{R_2} + \mathrm{R_{load}}) \\ \mathrm{R_{in,PCT}} = \mathrm{R_1} + \mathrm{N}\dfrac{\mathrm{N_1^2}}{\mathrm{N_2^2}}(\mathrm{R_2} + \mathrm{R_{load}}) \end{cases} \tag{3.4}$$

Where $\frac{N_1}{N_2}$ is the turns ratio, R_1, R_2 are parasitic resistances in series with the primary and secondary side on both sides and N is the number of power amplifiers connected to the power combiner. The impedance is linearly increasing with the number of amplifiers for the PCT but decreasing for the SCT with a factor of $\frac{1}{N}$. Thereby enabling higher output powers for the SCT compared against the PCT. Both these traits can be compensated for by altering the turns ratio, but the fundamental impedance sets the design approach for what is of importance, efficiency or gain. The efficiency is the other way around [4], in favor of the PCT due to up conversion of the load will draw less current from the power supply.

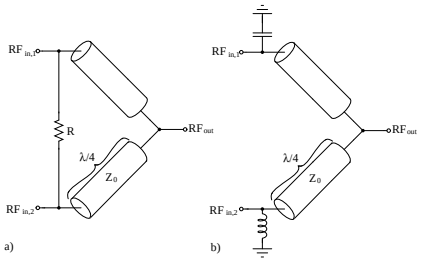

Figure 3.7. The Wilkinson Power Combiner **a)** and the Chireix power combiner **b)**

At least for the PCT topology an even number of amplifiers are recommended, common mode disturbances will hopefully affect all windings the same [19], but also that symmetry can be harder to achieve which can cause significant phase and gain error [4].

3.4 Transmission Line Power Combiners

In Section 1.2.2 it was stated that for a transmission line with the length equals the signals wavelength divided by four, the impedance the transistor sees equals Z_0^2/R_L. Where Z_0 is the characteristic impedance of the transmission line. This can be used for impedance matching. Transmission lines can also be used for power combining. However, some argue that the physical lengths these transmission lines make them not suited for integrated circuits [32]. However they are often used in conjunction with the outphasing technique, with at least one integrated example [43], which makes the discussion relevant.

3.4.1 Wilkinson

In Figure 3.7.a) the *Wilkinson Power Combiner* combiner is shown. The resistor between the transmission lines makes the power amplifier see a resistive load at all times [44]. When the inputs are in phase with each other no current goes through the dummy resistor. On the other hand when the inputs are in anti-phase all power gets dumped in the dummy resistor. [14], [68]

3.4.2 Chireix

The Wilkinson combiner without the dummy load are referred to as the *Tee* combiner. This combiner is under ideal circumstances lossless. When used in a outphasing amplifier, and the two amplifiers provide current in phase to the load, they sum up to the load. If the are in anti-phase one amplifier pushes current to the load, while the other drags current from the load, so that the net current in the antenna will be zero. Amplifiers in this kind of configuration should not load

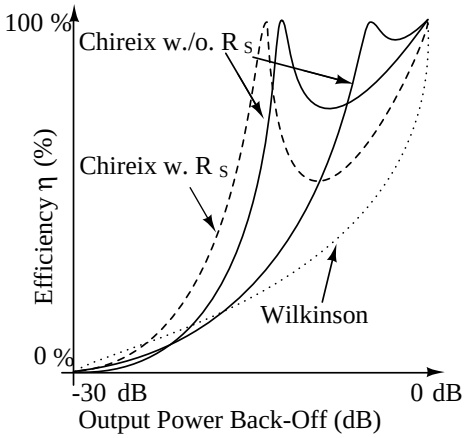

Figure 3.8. Conceptual figure of efficiency versus power output back-off for a Wilkinson and Chireix power combiners, with and without source resistance [17]

each other, when each amplifier ideally behaves like a voltage source. Thus, zero impedance of the voltage source would make the other amplifier see an infinite impedance [57]. However, the trade for better efficiency, compared to the Wilkinson combiner is a degradation in linearity due to reflections between the input ports [11].

For outphasing systems where the currents interact with each other, each amplifier sees a variable reactive part in the total load impedance. During ideal circumstances this would not constitute any problems as only the voltage peak will be decreased. For a realistic amplifier this may not be the case. Instead of only having a changing peak amplitude the phase will also change. This will degrade the efficiency as more the current and voltage overlap [14]. But may lead to distortion since the phase of the carrier is modulated by the outphasing angle [38].

In the Chireix combiner this variable load is compensated for one value of the outphasing angle. Shunt elements with are added before the transmission lines, as in Figure 3.7.b). So the impedance by the amplifiers at that angle can be chosen by the designer. This will have an effect a peak in efficiency in addition to the in-phase case. [10] A probable disadvantage with the Chireix combiner is that the reactive elements make the combiner asymmetrical, disturbing cancellation for low envelopes, which deteriorates the dynamic range. A conceptual figure of the efficiency of an outphasing angle for the Wilkinson and Chireix combiners can be seen in Figure 3.8. Also the effect of the source resistance R_S, which imitates how well the amplifier works as a ideal voltage source.

3.4.3 Lumped Approximation of Transmission Lines

There is a possibility to approximate a transmission line with lumped components by cascading LC-sections as in Figure 3.9. Each lumped element consists of a series inductor with 2 capacitors shunted to ground, forming a π-like structure. Thus Figure 3.9 consists of three element approximation. However to get a good approximation many sections have to be used. For the error in magnitude to become under 1% in comparison to a real transmission line eight section have to be put in series [20]. As the number of sections is increased, the loss can be expected to increase due to the longer distance to the antenna and more lossy components are added in series with the power amplifier [20]. Lumped approximations of

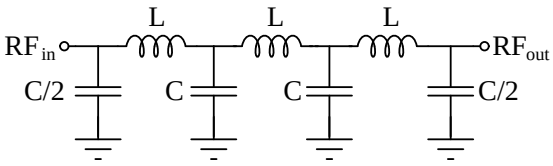

Figure 3.9. Approximating transmission lines with lumped elements

transmission lines are associated with large losses with increasing frequency. Not only due to the lossy passives but also due skin effect and ground planes often are used to protect the passives gets less effective at higher frequencies. A ten section approximation gives in one study 2 dB loss at 2 GHz, and gets worse as frequency increases. [57]

Chapter 4

Publications of Integrated Outphasing and Polar Power Amplifiers

This chapter briefly describe recent research performed regarding the two discussed architectures. The polar topology can be considered mature, in the sense that reports for amplifiers in an integrated environment have been published where one or more communications systems specifications are completely fulfilled. Later publications often focus to improve different properties in the architecture. Such as dynamic range, power control or efficiency for low envelope levels. The outphasing technique has until recently only had publications regarding that it is possible to implement integrated versions of the architecture. Only one publication have been found which claim they fulfill at least some communication system standards.

4.1 Power Amplifiers in Outphasing Configurations

The class D topology can be considered more easier to use in an outphasing system. It is less sensitive to loading than for example class E amplifiers. As described in previous chapter that lossless combining means that the amplifiers are not isolated from each other which leads the load seen by each amplifier varies over for different outphasing angles. The class E amplifier are sensitive for phase variations in the load and the voltage current overlap can grow large, thus degrading efficiency [68]. Ideally for outphasing, the amplifiers currents should affect each other for good efficiency. When the amplifier outputs are canceling each other, fully or partly, the sum of the currents should also cancel to some extent to preserve high efficiency. [14]

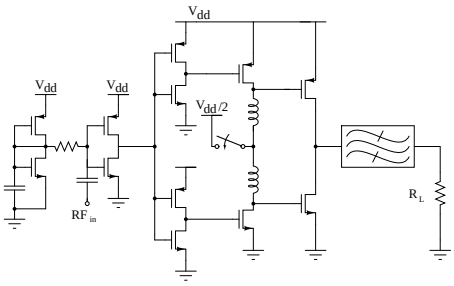

Figure 4.1. A class D power stage, with inverter and class E driver stages [64]

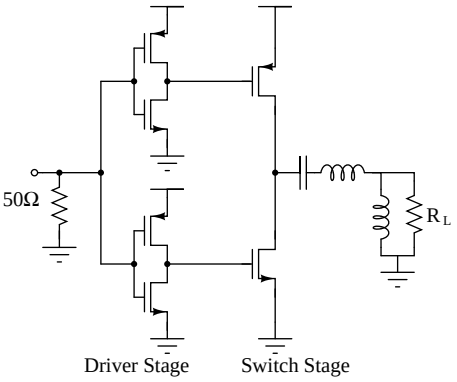

Figure 4.2. A class D power stage with inverter driver stages [22]

4.1.1 Class D Based

Some of the drawbacks with the power consuming traits of the class D topology can be somewhat corrected for. The large parasitics associated with large PMOS devices are hard to mitigate, but they can be compensated for by driving the PMOS and NMOS differently. If the output transistors are driven with non-overlapping signals the large output capacitance can be charged or discharged through the load network instead of between the power supply and ground. The non-overlapping signals provide so neither of the PMOS and NMOS are conducting, which also would minimize short-circuit current. This can be accomplished by sizing the drivers asymmetrically. [64] [22]

In Figure 4.1 and 4.2 two recent publications where the class D topology is used. A difference is that one incorporates a class E driver to have less parasitics but also a switchable power supply. The switchable power supply is used for time slot based communication systems, to have less power consumption when not transmitting.

The big difference between these two are the output combiners. Both use off-chip combiners but the one in Figure 4.2 has a Chireix combiner implemented one the PCB microstrips. When the other, (Figure 4.1) use a simpler approach with an in-phase LC-combiner. Extracted data from the publications can be seen in Figure 4.3. The Chireix combiner has high losses for small power back off levels. While the simpler LC-match have high efficiency for the whole range of output power. It is hard to speculate exactly why these two show fundamentally different figures. For the LC-combiner this can depend on that the load seen by the amplifiers increases which then increases the efficiency. However, Chireix combiner should in theory at least, show another peak in efficiency.

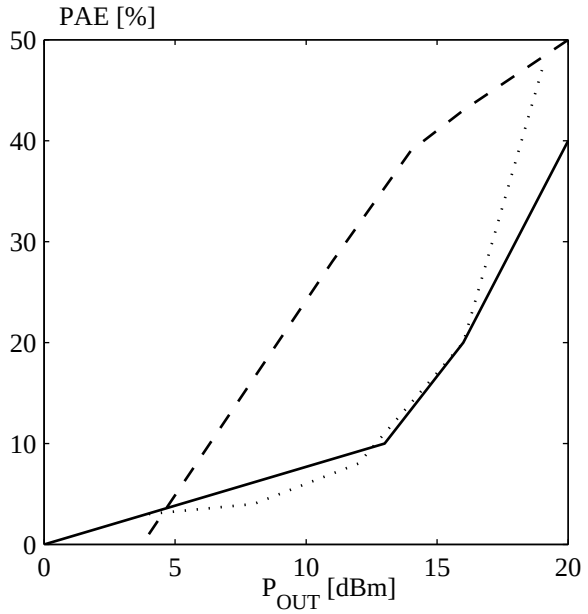

Figure 4.3. PAE vs. P_{out}, dashed line [64] with LC combining and solid line [43] with a Wilkinson combiner and dotted line [22] with a Chireix combiner

4.1.2 A Class E with Wilkinson Combiner

That transmission lines are expensive area wise to be integrated have been stated earlier. For future communication systems with larger carrier frequencies, they however might be a possibility. An outphasing amplifier in the 5.8 GHz range with an integrated transmission line of 2.8 mm Wilkinson combiner with differential class E have shown that it is feasible with integrated versions. [43]

The efficiency for power back off levels more than a few decibels the disadvantages with the Wilkinson combiner can be seen, see Figure 4.3. However maximum efficiency of the combiner around 82% which have to be regarded as pretty good. For example an implementation of the distributed active transformer had a maximum efficiency of 75% [5]. The size of the transmission line is still very large, an estimation of the size is that it takes up at least one half of the 1.8mm X 2.5mm chip.

4.2 Power Amplifiers in Polar Configurations

In publications the main amplifier for polar configurations is almost always operating in class E. Differential structures to make use of virtual grounds and higher output power. A disadvantage is the high voltage peaks over the transistor class E operation cause. Modern CMOS devices have low tolerance for drain source

voltages, precautions have to be taken for avoid transistor breakdown. A common measure is to stack the main power transistor, an extra, biased cascode transistor is added to have the drain source voltage shared over more than one active device [51].

The low supply voltages available also sets a fundamental limit to what is realizable output powers. Therefore of the the recent polar architectures discussed here are using multiple power amplifiers in a distributed active transformer type combiners for increased output power. There are examples of polar amplifiers with a rated power of over 2 Watts [31], [29].

4.2.1 Dynamic Range & Efficiency Improvements

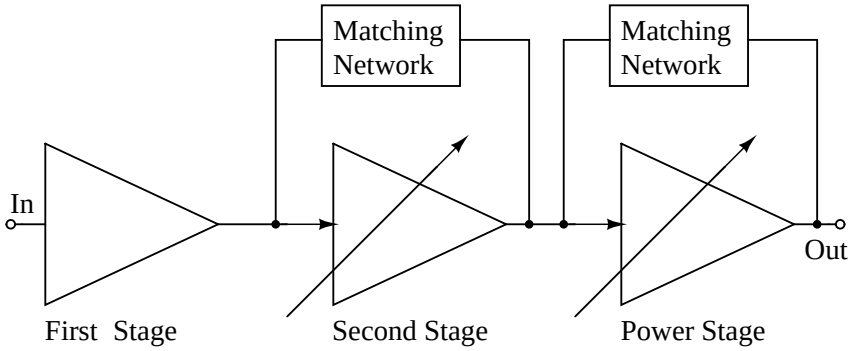

Figure 4.4. Three stage polar power amplifier architecture with adaptive load technique [42]

Two problems with the polar transmitter have gotten much focus in recent research. Feedthrough which limits the dynamic range, and the efficiency for low levels of the envelope. The dynamic range of an amplifier is the difference between the highest and lowest output power:

$$\mathrm{DR} = 10log\frac{(\frac{V_{dd,max}}{R_L})}{(\frac{V_{dd,min}}{R_H})} = 20log\frac{V_{dd,max}}{V_{dd,min}} + 10log\frac{R_H}{R_L} \quad (4.1)$$

For example, for some CMOS processes, with 3.3 V power supply and a hypothetical feedthrough level of 0.5 V, if the load remains constant the dynamic range would be a moderate 16.4 dB. However if the load would be larger while the power supply is decreasing, the output power will be decreased even further. Hence larger dynamic range. This can be accomplished by letting the drivers not only drive the next stage but also can bypass some of the power to the load through an upconverting matching network, as seen in Figure 4.4. In addition, the envelope can bias the cascode transistor of each amplifier branch so that the on-resistance

of the cascode device is increasing, when the envelope is decreasing. This action decreases the output power at low envelope values and thereby increasing the dynamic range. [42]

The upconversion can be accomplished by LC-matching [42], but the DAT offer

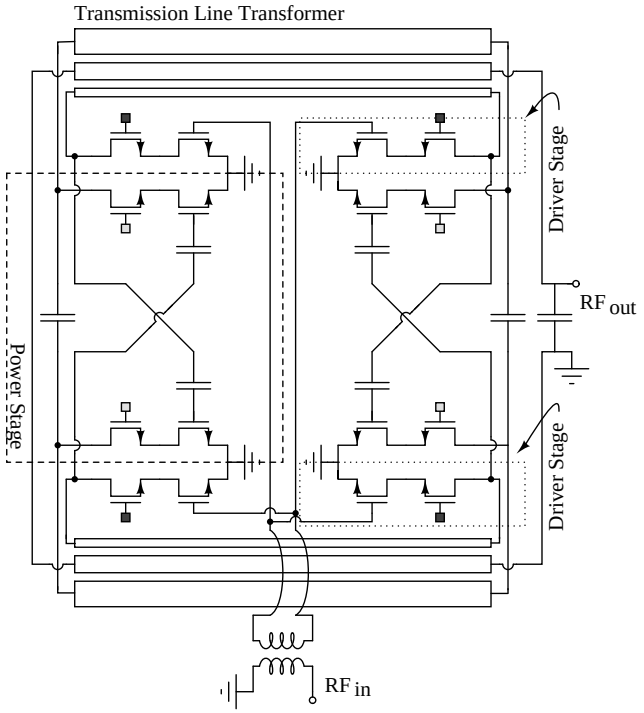

Figure 4.5. Schematic of a power amplifier using the asymmetric transmission line transformer, biasing not shown [41]

another possibility. If the drivers sees a high impedance primary, a corresponding upconversion would be the case. As in Figure 4.5, with two primaries. The drivers are still driving the power stage but also providing power to the load through the thinner slab primary which have been sized to have a high input impedance. The gain in dynamic range have by these methods been extended by over 17 dB [42]. It could probably be extended even further if more drivers and up conversion solutions are implemented. Also for efficiency enhancements or power control purposes, the distributed configuration can be a possibility. The power amplifiers can be switched on or off which would have a similar effect [29].

Efficiency are also dependent on the load. So improvement in efficiency can be performed by the same technique:

$$\text{PAE} \quad \propto \quad \frac{R_{load}}{R_{load} + R_{on}} \left(1 - \frac{P_{in}}{P_{out}}\right) \tag{4.2}$$

As the output power decreases, an increase in load impedance would compensate. This efficiency improvement can become very large if the power stage completely turn off. The largest drivers and power stage gradually turn on so for small envelope levels only the first driver are consuming power. The dashed line in Figure 4.6 represent the efficiency improvement that have been shown possible for these kind of adaptive load techniques [41].

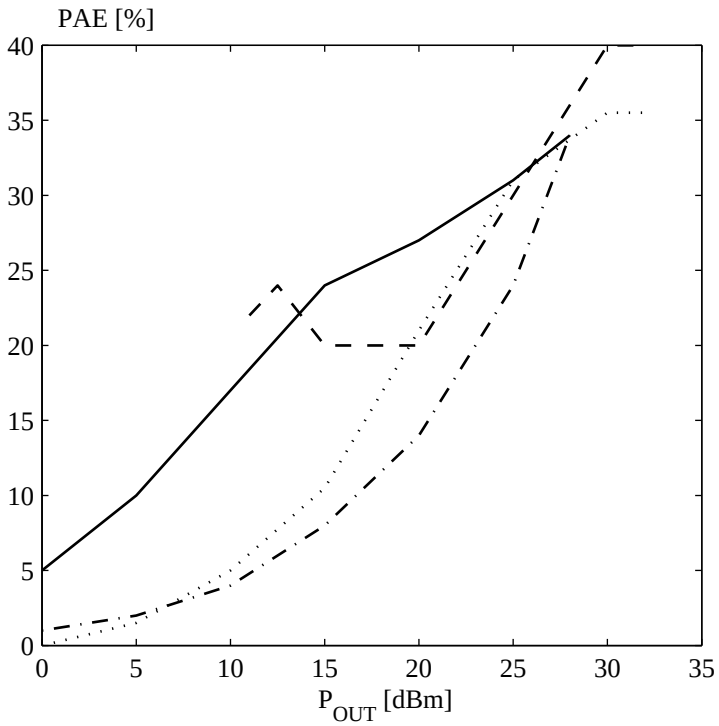

Figure 4.6. PAE vs. P_{out}, dashed line [41], solid and dashed-dotted line [54] and dotted line [30]

Instead of up converting the load, efficiency enhancements can also be performed in other ways. By scaling the power supply after the envelope not only for the power stage but also for the drivers, the total current drawn from the power supply will decrease with the envelope, thus higher efficiency figures can be accomplished for low envelope levels. The most straightforward way to implement this is to let the the AF amplifier modulate the drivers too. The tradeoff is that the output signal will be modulated as multiple times, inducing extra distortion. [23]

Another drawback is that transistors gain gets smaller as with decreasing power supply, or smaller envelopes, so that the driving possibility may suffer. One can then modulate the drivers with an offset, seen in Figure 4.7. where the offset

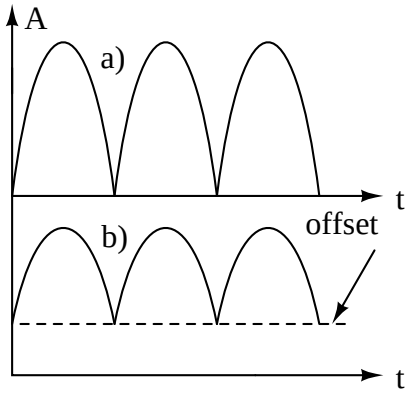

Figure 4.7. a) Fully modulated b) Partly modulated

should be chosen so low that it not interferes with the driving of the next stage. [47]

4.2.2 Current Source Configurations

To totally overcome the problem with dynamic range other structures than the common class E other configurations have emerged. These are inspired by digital to analog converters and have an advantage that there exist no need for the audio frequency amplifier. The envelope is applied through digital bits, $B_0 \ldots B_N$, in Figure 4.8. Each bit control whether a current source should conduct current or not. The carrier is applied through the local oscillator (LO) in the mixer like structure. The spectral components associated with the switching are filtered out in a bandstop filter. So the current that flows through the balun are proportional to the envelope, A(t). Three sections are used with different widths of the input transistors for the local oscillator, for dynamic range and power control purposes. The dynamic range of these kinds polar amplifiers have shown to be more than all other polar topologies, 62 dB. This kind of current source configurations have also shown the possibility of very large bandwidths for the envelope, 20 MHz [25]. The power supply can also be modulated to increase efficiency and extracted data can be seen in Figure 4.6, both with (solid line) and without double modulation (dashed-dotted line). Possible drawbacks are that double modulation are more or less necessary for efficiency reasons and the filters inability to diminish the switching components. Implementations of this kind have been unsuccessful of fulfilling some communications systems requirements, even with predistortion in the envelope path.[54], [55]

The linearity have shown to improve if interpolation techniques are used. If the amplifiers are cloned multiple times and driven by quadrature clocks the transition of the envelope becomes smoother, which should decrease the number of

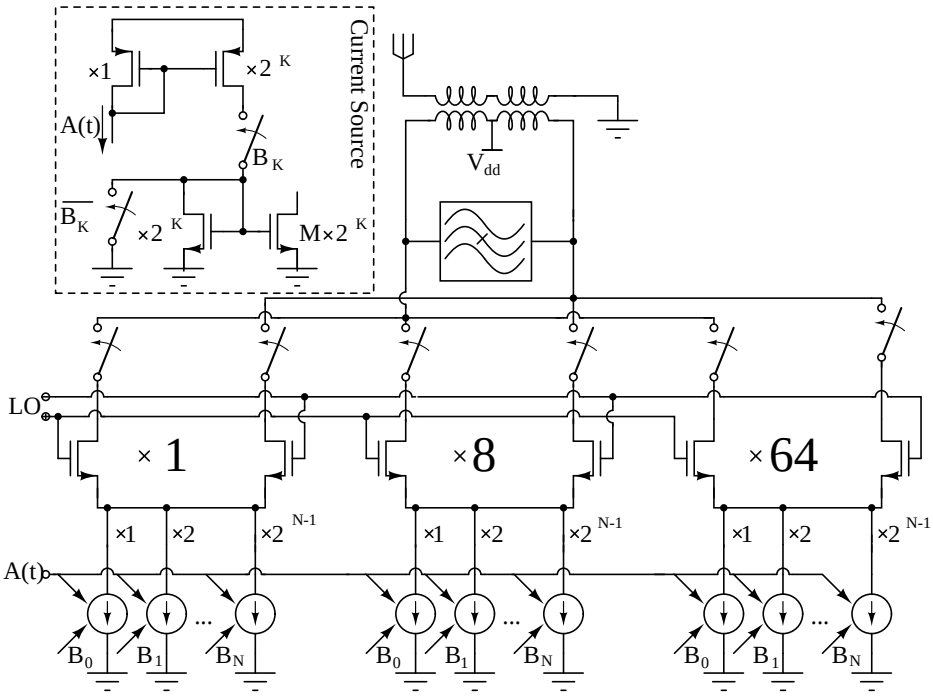

Figure 4.8. Circuit configurations of the driver stage and the power stage [54]

unwanted spectrum components at the output.[25], [70]

4.3 Listing of State of the Art Publications

Below is a short list of recent publications regarding both types of architectures. Some important properties such as maximum drain efficiency and power added efficiency are displayed. The last column shows some *Figures of Merits*, FoM described in each publication. The values shown in that column depend on what application and the focus of the publication. The *Combiner* column defines what type of combiner or matching network have been used, *OC* means off-chip combiner the rest of the abbreviations are self explanatory. The *Application* defines for what kind of communication format is used, the *M* or *S* means that if it is Multi or single carrier system, which describes the bandwidth of the amplifier.

Table 4.1. Comparison of recent Polar/LINC Power Amplifiers

Comparison of Recent Polar/LINC Power Amplifiers

	Application	Process	Type	Class	Combiner	V_{dd} [V]	P_{out} [dBm]	DE/PAE [%]	FoM
[30]	S	0.18-µm[1]	Polar	E	PCT[4]	3.3	32.2	43.7/35.6	44dB DR
[29]	S	0.18-µm[1]	Polar	-	PCT[4]	3.3	33.5	-/41	EDGE DR fulfilled
[42]	S	0.25-µm[1]	Polar	E	TL-Balun	3.3	28.5	33/	34dB DR
[41]	S	0.18-µm[1]	Polar	E	SCT[2]	3.3	32	-/40	15-20% Min. PAE
[25]	M	0.18-µm[1]	Polar	-	OC Balun	1.7	13.6	-/7.2	20MHz BW,3.71% EVM
[50]	S	0.18-µm[1]	Polar	E	-	2.9	23.8	34/	1.67% EVM
[54]	S/M	0.18-µm[1]	Polar	DAC	Transformer	3.3	27.8	34/26.5	62dB DR
[33]	M	SiGe	Polar	E	LC	3.3	19	-/36	PAE 19-36% at 4-19 dBm
[67]	S	65-nm[1]	Polar	E	-	2.5	28.6	-/28.5	4.6% EVM
[38]	S/M	90-nm[1]	LINC	E	OC	1.2	20	56/-	1.2% EVM, GSM
[64]	S	0.25-µm[1]	LINC	D	OC LC	2.5	20	-/50	-35dB IMD
[20]	M	0.18-µm[1]	LINC	F	LC-TL	1	22	-/38	-42dBc ACPR
[22]	M	0.18-µm[1]	LINC	D	OC Chireix	1	15.4	42%/-	-45dBc ACPR
[43]	M	SiGe[2]	LINC	E	Wilkinson	1.3	18.5	-/47	-32dBc ACPR

Chapter 5

Simulations

This chapter presents some simulations based on a CMOS 90 nm radio frequency applications kit. The purpose of the simulations are based on that publications seldom publish enough material, so it is hard to do a comparison purely based on literature. The intention is to have as many parameters to try to emphasize similarities and differences as well as advantages and disadvantages of the two architectures.

5.1 Method

Two classes of amplifiers are discussed, the class E and class D. The decision is based on that both can be considered most popular for the two architectures, class E for the polar architecture and class D have some successful implementations for the outphasing technique.

The simulated models will only take in respect the main amplifiers. Both need some signal decomposition and generation to function properly. This is assumed to be done in a digital signal processor ideally and the upconversion of the baseband symbols are also assumed to be performed ideal.

Considering only the main amplifiers will have the effect that the audio frequency amplifier for the polar architecture are ideal in sense of efficiency, timing and bandwidth. Measured efficiencies of switching class S amplifiers are very high, so this effect is maybe not negligible, however only considered in the discussion. The timing and bandwidth are certainly not negligible, as described in Chapter 2 they are large contributors of distortion in polar amplifiers so models of these non-idealities are simulated and discussed.

5.1.1 Amplifier Design

The amplifiers are designed from an assumed criteria to at maximum *towards* 150 mW of output power. Since the amplifiers are not made for any communication

standard it does not matter if they are not fulfilling that specification, more than for the sake of comparison.

The amplifiers are designed in three steps. First how large the load should be is dependable of the class used. Since the load have to be downconverted for the output power to be anywhere close the 150 mW. The amplifier is first designed as a stand alone amplifier. No output filters or matching are introduced. This depends on that the architectures will be using different matching networks or combiners so most fair design will be to design with a purely real load. So the second step is to optimize the devices sizes for maximum output power and power added efficiency. The output power is measured at the fundamental tone alone. The optimization process relies fully on the built in optimizer in Advanced Design System. The maximum width for the transistors for the NMOS and PMOS is set to 5000 and 8000 micrometers respectively. The channel width is set to the minimum 0.28 µm in the RF kit. This is based on the assumption that performance will only be degraded by longer channels for transistors working as switches. The on-resistance will increase with a longer channel.

The last step is to optimize the matching network for both amplifier architectures. The load is then set to 50 Ω. The optimization process is terminated when no improvement can be found, or is too small to do any impact on the comparison. So both architectures are using the same device sizes for all transistors. This makes the comparison easier, both architectures share the same main amplifier. The behavior of both topologies can then be more easily discussed, with in a more realistic environment, than for example if the comparison would only depend on publications or ideal devices.

5.1.2 Simulation

All simulations except the ones involving linearity are made in *Harmonic Balance*. It is a frequency based simulation method for quickly evaluating circuit spectral behavior. It can also quickly from the frequency domain find steady-state time domain characteristics [1].

Gain, Efficiency and Output Power Calculations

The harmonic balance simulations are performed with a constant sinusoid as input. For the polar architecture the envelope is treated as a DC-voltage source where the magnitude is swept as parameter.

$$\begin{cases} \theta(t) &= \hat{A}sin(2\pi ft) \\ A(t) &= V_{DD} \end{cases} \tag{5.1}$$

The amplifiers in the outphasing architecture have each a sinusoidal voltage source as input, where a phase addition or subtraction to each source is treated as the

outphasing angle, such that:

$$\begin{cases} S_1 &= \hat{V} sin(2\pi ft + \alpha) \\ S_2 &= \hat{V} sin(2\pi ft - \alpha) \end{cases} \tag{5.2}$$

where α serves as the outphasing angle.

The power that is dissipated in the load for complex currents and voltages are equal to the real part for complex power [63]

$$P_{out} = \Re(V_{out} I^*_{out}) \tag{5.3}$$

where the I^*_{out} is the conjugate of the current. The power are only measured for the fundamental tone and not of the sum of all tones. The power gain of the polar architecture is calculated as:

$$G_{p,polar} = \frac{P_{out}}{P_{in}} \tag{5.4}$$

and for the outphasing technique as

$$G_{p,outphasing} = \frac{P_{out}}{2P_{in}} \tag{5.5}$$

Where the factor of two depends on that the outphasing has two power sources and thereby consume twice the amount of power. The efficiency are measured as

$$\eta_{drain} = \frac{P_{out}}{V_{DD,0} I_{DD,0}} \tag{5.6}$$

The fundamental tone divided by the supply voltage times the current drawn from the power supply. The index, 0 means that only the DC current are measured.

Linearity Simulations Modeling

The linearity measures of this comparison are made with a two tone test, which is a commonly used for this purpose [68]. The advantages are that it is easy to model and easy to compare. A disadvantage is that it may not be as truthful against real modulation specifications where the amplitude modulation is not as deep as a two tone test [68]. To clarify, in Figure 5.1 the two tone test signal in time domain and in 5.2 in frequency domain, which are going to be used to compare polar and outphasing amplifiers is shown. The envelope varies between maximum amplitude and zero which is not the case in all real modulation formats. This will make the results more pessimistic, but since this comparison is against two architectures and not against any real world examples the ease of measuring is favored. The test is modeled as voltage sources and the response is simulated in a transient simulations for the amplifier architectures. A two tone test consists of two sinusoids where one has high frequency represent the carrier and a low frequency sinusoid represent the data, such as:

$$T(t) = sin((\omega_c - \omega_d)t) + sin((\omega_c + \omega_d)t) = sin(\omega_d t) \cdot cos(\omega_c t) \tag{5.7}$$

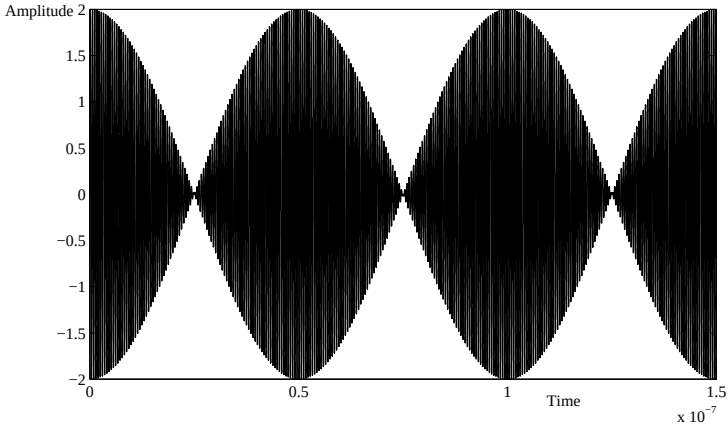

Figure 5.1. Two tone test in time domain

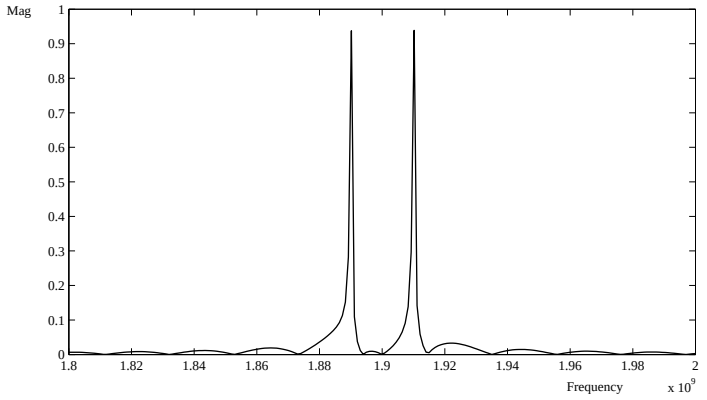

Figure 5.2. Two tone test in frequency domain

To extract the different signals for polar modulation T(t) can be rewritten as [51]:

$$T(t) = |sin(\omega_d t)| \cdot sign(sin(\omega_d t)) \cdot cos(\omega_c t) = |sin(\omega_d t)| \cdot cos(\omega_c t + \pi/2 - \frac{\pi}{2} \cdot sign(sin(\omega_d t))) \tag{5.8}$$

$|sin(\omega_d t)|$ can then be modeled as the envelope and the *cosinusoidal* term as the phase modulated carrier. So the time domain voltage sources for the polar architecture are modeled as.

$$\begin{cases} A(t) & = & |sin(\omega_d t)| \\ \theta(t) & = & cos(\omega_c t + \pi/2 - \frac{\pi}{2} \cdot sign(sin(\omega_d t))) \end{cases} \tag{5.9}$$

For the outphasing signals the signals can be written as:

$$\begin{cases} S_1 &= S(t) + i \cdot S(t)\sqrt{\frac{\hat{A}^2}{A(t)^2} - 1} \\ S_2 &= S(t) - i \cdot S(t)\sqrt{\frac{\hat{A}^2}{A(t)^2} - 1} \end{cases} \tag{5.10}$$

since A(t) is found in equation 5.9, the equation above can be rewritten as:

$$S_i(t) = S(t) \pm i \cdot S(t)\sqrt{\frac{\hat{A}}{A(t)} - 1} = S(t) \pm i \cdot S(t)\sqrt{\frac{sin^2(\omega_d t) + cos^2(\omega_d t)}{sin^2(\omega_d t)} - 1} \tag{5.11}$$

$$S_i(t) = S(t) \pm i \cdot S(t)\sqrt{1 + \frac{1}{tan^2(\omega_d t)} - 1} = S(t) \pm i \cdot S(t)|\frac{1}{tan(\omega_d t)}| \tag{5.12}$$

Where the ±i means that S(t) needs to be shifted in phase ±90° and can serve as the outphasing angle for the two tone test:

$$i \cdot S(t) = i \cdot cos(\omega_c t) sin(\omega_d t) \tag{5.13}$$

$$= 1 \cdot i \cdot cos(\omega_c t) sin(\omega_d t) \tag{5.14}$$

$$= e^{i\frac{\pi}{2}} \cdot cos(\omega_c t) sin(\omega_d t) \tag{5.15}$$

$$= e^{i\frac{\pi}{2}} \cdot \frac{e^{i\omega_C t} + e^{-i\omega_C t}}{2} sin(\omega_d t) \tag{5.16}$$

$$= \frac{e^{i(\omega_C t + \frac{\pi}{2})} + e^{-i(\omega_C t + \frac{\pi}{2})}}{2} sin(\omega_d t) \tag{5.17}$$

$$= cos(\omega_C t + \frac{\pi}{2}) sin(\omega_d t) \tag{5.18}$$

The derivation above would be analogous for - i S(t). The voltage sources for the outphasing technique are then modeled as:

$$\begin{cases} S_1(t) = cos(\omega_c t) sin(\omega_d t) + cos(\omega_c t + \pi/2) sin(\omega_d t) \frac{1}{|tan(\omega_d t)|} \\ S_2(t) = cos(\omega_c t) sin(\omega_d t) + cos(\omega_c t - \pi/2) sin(\omega_d t) \frac{1}{|tan(\omega_d t)|} \end{cases} \tag{5.19}$$

The choice of doing the linearity simulations in time domain are based on the difficulties involved by modeling the sources for both amplifier architectures. The harmonic balance simulation were not satisfactory with several sources which had the complex spectral behavior as the two tone test modeled for the two architectures.

5.2 Class D

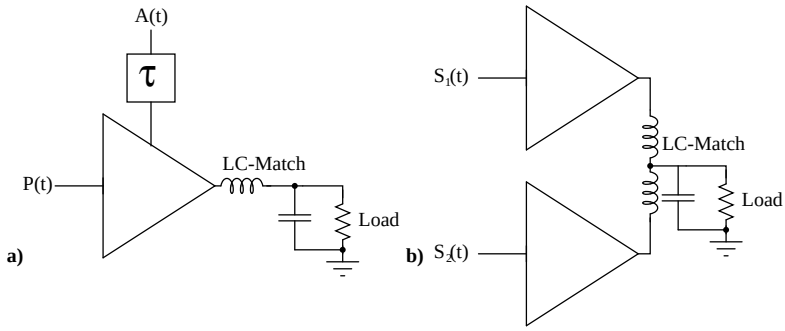

Figure 5.3. Testbench setup for comparison

The first examined topology is a triple-stage class D amplifier configured as a chain of inverters. For the amplifier to have 150 mW in the fundamental tone when the supply voltage is 2.5 V and with a 50 Ω load, it have to be downconverted to 8.44 Ω approximately [51]:

$$P_O = \frac{2}{\pi^2}\frac{V_{DD}^2}{R_L} \Rightarrow R_L = 8.4\Omega \tag{5.20}$$

This value are entered in the testbench as a pure resistive load and and then the circuit transistors width and numbers of fingers are optimized. The results after circuit sizing are shown in table 5.2. Except for the components shown in the table both architectures have a DC-block capacitor of 100 pF on the transistors drains. The choice of 100 pF for the DC-block depends on it is assumed to be highest reasonable value concerning chip area. The circuit configurations can be seen in Figure 5.3. Both use a simple LC-match topology for matching and combining. The quality factor of the inductors are assumed to be 10. Reasonable values are as described in Chapter 3 between 6-13. The outphasing variant have an in-phase combiner, when both outputs of the amplifiers are in-phase the output power is at its highest. The impedance seen from each amplifier with the values specified from table 5.2 can be seen in Figure 5.4. For larger outphasing angles the load increases so that the efficiency should increase. From the beginning when the audio frequency amplifier is assumed to be ideal, a time delay is introduced in the envelope path of the polar architecture to compensate for the delay due to the

Table 5.1. Specification of class D CMOS 90nm Amplifier

	Name	Width [μm]	Inductance [nH]	Capacitance [pF]
Main Amplifier	NMOS	1648		
	PMOS	3000.5		
First driver	NMOS	620		
	PMOS	1028		
Second driver	NMOS	195		
	PMOS	396		
Polar Matching	L		1	
	C			7
Outphasing Matching	L		1.39	
	C			10

drivers in the phase path. The delay is simulated to be 0.11 ns with a square wave input and measured at $V_{DD}/2$ at the output of the second driver.

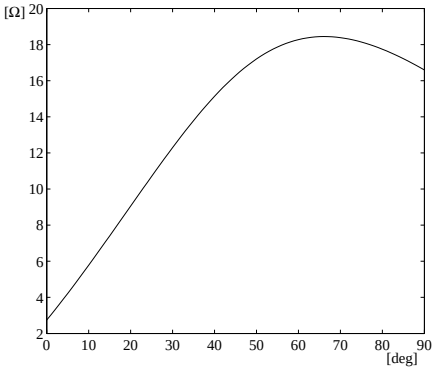

Figure 5.4. Impedance seen by the amplifiers in the class D outphasing topology

5.2.1 Performance Results

In Figure 5.5 and 5.6 the spectra's for both amplifiers with a two tone test with 20 MHz of bandwidth is shown. The arrows shows the magnitude of the fundamental tone and the largest intermodulation product. The carrier to intermodulation ratio is roughly 8 dB in favor of the outphasing amplifier. Even though the audio frequency amplifier is ideal in this simulation, and the time delay have been compensated for. A probable cause of these high order intermodulation products are a result of feedthrough due to the large PMOS transistors. The outphasing amplifier is more forgiving in these kind of distortion, dependent on path symmetry, the non-idealities is canceling each other out.

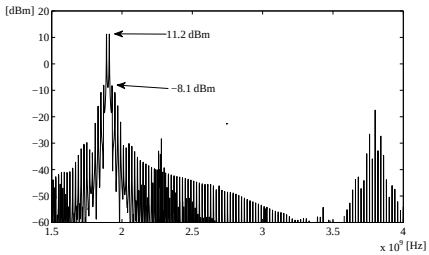

Figure 5.5. Spectrum at output for class D polar amplifier

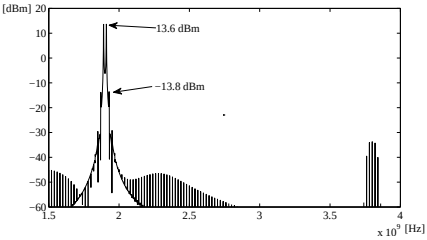

Figure 5.6. Spectrum at output for class D outphasing amplifier

Output Power

Not surprisingly the outphasing amplifier is able of higher output power since there are two amplifiers contributing directly. In Figure 5.7 the horizontal axis are normalized for both amplifiers. The polar amplifier are normalized for supply voltage, maximum 2.5 Volts and the outphasing amplifier is normalized against outphasing angle 90°. Both curves show similar shape to around 0.25 at the horizontal axis. The *foot*, at around 0.3 on the polar amplifier is a result of feedforward which places a fundamental limit on the dynamic range of the polar amplifier. The outphasing amplifier goes way under -100 dB for small outphasing angles. So high dynamic range is in this model clearly favors the outphasing amplifier. However mismatch will degrade the dynamic range, as will be seen later.

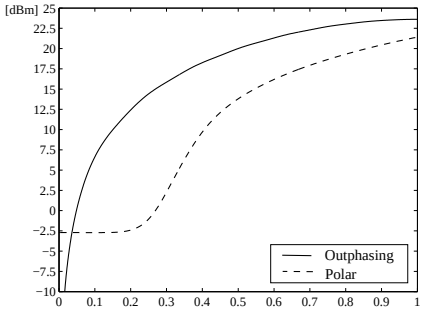

Figure 5.7. Output power versus normalized outphasing angle and V_{dd}

Gain

As the input power is the same for both architectures in this comparison the gain is not a surprise. The gain is constantly larger for the outphasing amplifier except at the very end of the horizontal axis. The amplifiers are optimized at highest output levels and the outphasing amplifier cannot manage to put out the double amount of power (3 dB) which can be seen in the Figure 5.8. So the gain plots looks like a shifted version of the output power figure. The behavior difference between the two in both the output power and gain figures, is that the outphasing angle have to be large before the output power decreases more than a few decibels.

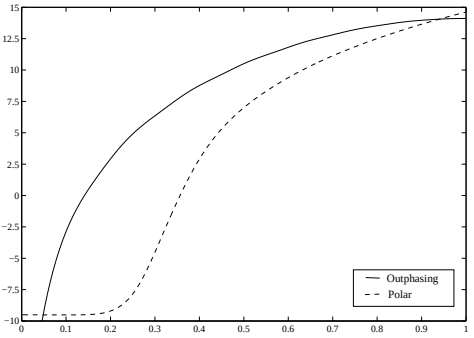

Figure 5.8. Gain versus normalized outphasing angle and V_{dd}

Efficiency

Simulated efficiencies show the variation of the load in the outphasing architecture have better results than the polar topology. Especially for small and medium output power levels. At high power levels the efficiency is significantly better for the polar architecture. The reason why the efficiency of the outphasing topology is saturates depends probably on that the impedance seen by each amplifier is getting smaller, close to 2 Ω, when the outphasing angle equals zero, see Figure 5.4. And in general for LC-matching the efficiency drops with larger downconversion [51]. However, there are examples where this kind of drop is not as significant [64], see Section 4.1.1. So the efficiency drop does not depend on the combiner used, but probably on the high level of downconversion. To enhance to low and medium power efficiency for the polar architecture, the approach described in Section 4.2.2 where the drivers are modulated are simulated for the class D polar architecture. No time is spent on finding the optimum offset, only two simulations have been performed to examine the concept and how it applies to the polar amplifier. Firstly when the drivers are modulated fully, they use the same power supply as the power stage. The other case is with an offset, which is set to $\frac{V_{DD}}{2} = 1.25$ V. So that the

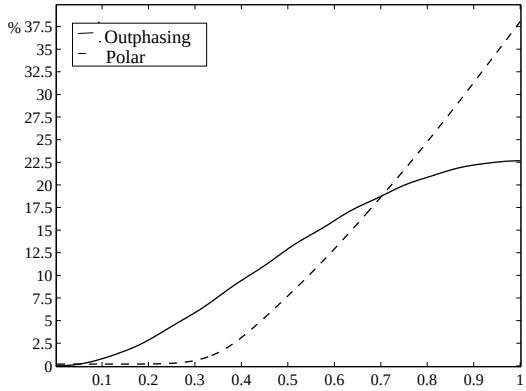

Figure 5.9. Drain efficiency in percent versus normalized outphasing angle and V_{dd}

power supply varies between 1.25 and 2.5 Volts. In Figure 5.10 these are denoted as *fully modulated* and *half modulated*.

Some of the traits described in Section 4.2.2 can be seen in 5.10. The effi-

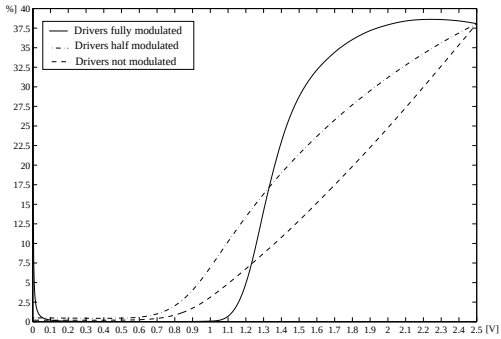

Figure 5.10. Drain efficiency for polar amplifiers with modulated drivers

ciency is significantly higher for the fully modulated case for large parts of the envelope. Under 1.2 Volts the drain efficiency is actually lower than for the half modulated case and the reference. This is probably the result of, that for too low values of the envelope the drivers cannot drive the power stage so the output power becomes very low. The half-modulated case have not this problem and has larger efficiency for the whole range than the reference. The biggest drawback of modulating the drivers is that the already poor linearity degrades even more. This

is illustrated in Figure 5.11 which should be compared against Figure 5.5. The ratio between the fundamental and the third intermodulation product closest to the fundamental are now approximately 15 and 9 dB for the half and the fully modulated drivers respectively. When comparing both images the spectrum for the modulated cases are more concentrated to fewer frequencies, but with higher peaks than for the non-modulated case which looks more *smeared* out.

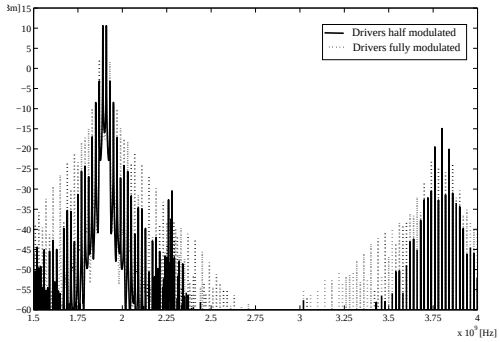

Figure 5.11. Output spectrum for polar modulated when drivers are modulated

5.2.2 Results on Polar Linearity

As described already the basic setup simulated of the polar architecture have only one of the large sources of distortion, namely feedthrough from the gates to the drains in the class D amplifier. This section show how the other two distortion mechanisms behave for the discussed amplifier.

Envelope Bandwidth

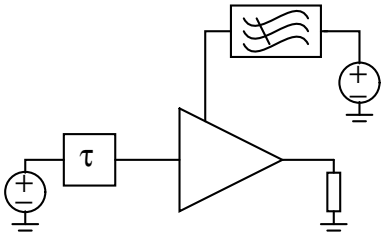

Figure 5.12. Testbench setup for simulating envelope bandwidth and timing errors

In this chapter it is assumed that the envelope amplifier is a class S amplifier with very high efficiency and infinite bandwidth. In a real class S amplifier

the bandwidth cannot be infinite, a low pass filter have to implemented to filter out the switching noise effectively. As described in Section 2.2.3 the third order products will dominate if practical models are used. The model used here is the same voltage source as envelope amplifier but with a Butterworth low pass filter in series, which models the class S amplifier filter. The testbench is shown in Figure 5.12. A Butterworth filter is chosen due to its better performance than for example Bessel filters [35]. A reasonable filter order is assumed to two if the filter is going to be integrated and not to have to large loss in the inductors. And also take cost, or take chip area into account. There is a tradeoff when choosing the bandwidth. To compensate for the time it takes for the signal to propagate through the filter a time delay is introduced in the phase path for compensation. The delay of the filter is measured in the time domain for the filter and then updated for different bandwidths. These values are then updated in the time delay in the phase path. In Figure 5.13 the envelope for the two tone test with 20 MHz bandwidth is displayed. Almost all visible components lies beneath 200 MHz, which then serves as a crude approximation of the envelope bandwidth. Simulations show that for

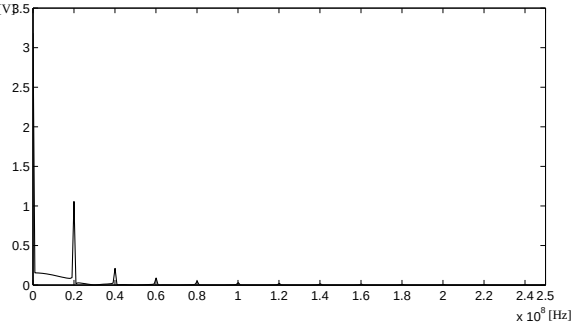

Figure 5.13. The spectrum of the envelope for a two tone test

the two tone test signal used, the bandwidth of the filter can be set relatively low without too much distortion, see Figure 5.14. The vertical axis show the ratio between the largest intermodulation product and the fundamental. Not until N is below 2 significant linearity degradations can be expected. The two tone test has its dominating spectral components within that range, so there is maybe no surprise that there are at this range the carrier to interferer really starts to degrade. This means that the switching frequency should be between 200-400 MHz (when N=2) to be ensured that the switching noise to be more than 40 dB under the fundamental tone, see section 2.2.3. And of course if larger suppression is needed, the switching frequency need to be even higher.

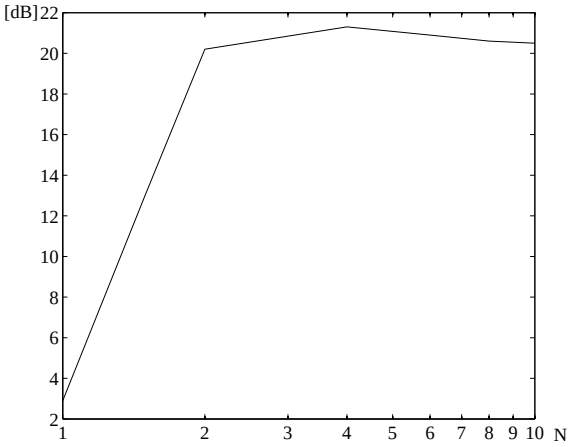

Figure 5.14. Carrier to interferer ratio for different audio amplifier filter bandwidths

Time Mismatch

The third large source of distortion in polar transmitter are the time delay between the envelope and phase path. The simulations done in previous section the delay was always compensated for, to see only how linearity degrades due to envelope bandwidth. The largest delay were simulated to be over 17 ns which roughly equals 32 periods for the phase modulated carrier. Which according the the simulations described in this section would be very large. In the testbench used in this section the filter in the envelope is removed and a time delay is introduced. The filter is removed to have infinite bandwidth, the purpose is to see only how timing errors disturb the operation. Figures 5.15-5.22 shows the simulations with various time delays in the envelope path in respect to the period of the carrier of 1.9 GHz. It is obvious by looking at these figures and comparing with previous section that some kind of delay compensation is always needed. The actual difference in carrier to interferer ratio not very large, merely 8 dB. But the spectral components is increasing very much. Up to a three period delay or around 1.5 ns the 3^{rd} intermodulation products dominate but with higher order delays it is harder to estimate the order. Especially in Figure 5.22 the unwanted spikes near the fundamental tones often contain several different order tones. The intermodulation products stays fairly constant up the the delay of three periods. The simulations with 4 or more periods of delay the higher order distortion dominates and seem to get closer to the fundamental tones. In Figure 5.20 the dominating distortion lies at 2.1 and 1.79 GHz, 91 MHz from the closest fundamental tone. But in Figure 5.22 the dominating intermodulation product are 60 MHz from the closest fundamental tone. The figures also show that the amount of unwanted spectral components are increasing with increasing delay. To conclude a timing mismatch

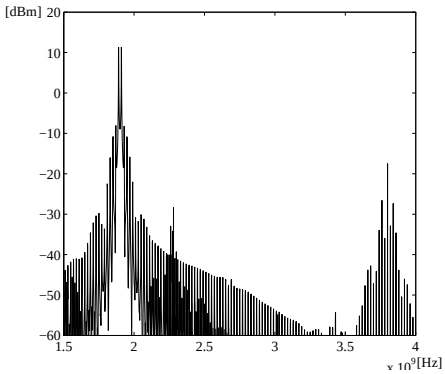

Figure 5.15. Spectrum at output for class D polar amplifier, without time mismatch

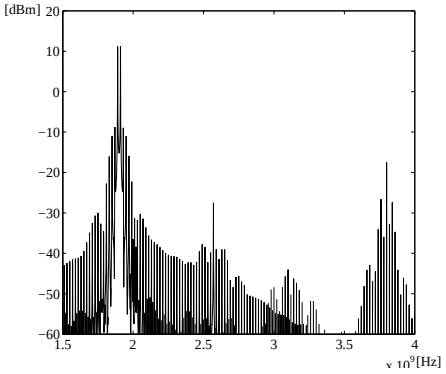

Figure 5.16. Class D polar amplifier spectrum, time delay of one half RF period or 0.26 ns

of a couple of periods do not severely degrade overall linearity of this circuit setup. The largest source of distortion is still feedthrough.

5.2.3 Results on Outphasing Linearity

The major sources of distortion for the outphasing amplifier are phase and gain mismatch between the two paths, see Section 2.3.3. This effects could in terms depend on any asymmetry between the paths. The first simulation performed on the class D outphasing architecture is showing how asymmetry of the inductance between give rise to distortion. The purpose of the simulation is to show the high sensitivity to mismatch. Varying an inductance like this are equivalent of both varying the phase and gain. The inductor are simulated with a quality factor so increased inductance gives higher loss.

The results can be seen in 5.23. The degradation of intermodulation performance really starts when to inductors have a 20% mismatch. With careful layout this should not be impossible.

Asymmetries like the one described here seriously limits the dynamic range, for large outphasing angles full cancellation cannot be performed. Already for a 5% asymmetry in the inductance value the dynamic range has dropped with 15 dB, see Figure 5.24. Some asymmetry in the paths have to be accounted for, which would led one to believe that the figures of dynamic range are hard to predict.

Phase variations between paths

To see how only variations in phase between the paths is degrading performance an error term are multiplied to one of the input signals:

$$S_{1,new} \quad = \quad S_{1,old} \cdot e^{j\theta_{error}} \tag{5.21}$$

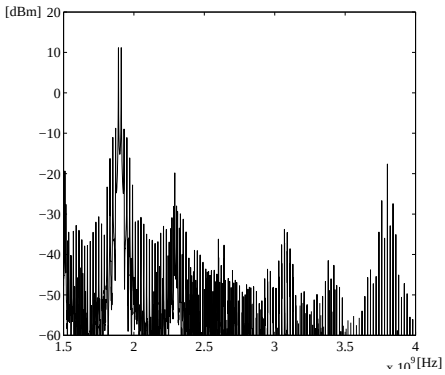

Figure 5.17. Class D polar amplifier spectrum, time delay equal to one RF period 0.56 ns

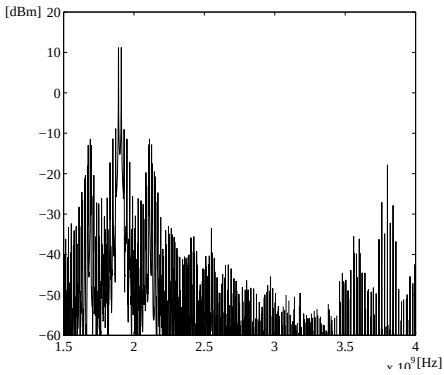

Figure 5.18. Class D polar amplifier spectrum, time delay equal to two RF periods or 1.05 ns

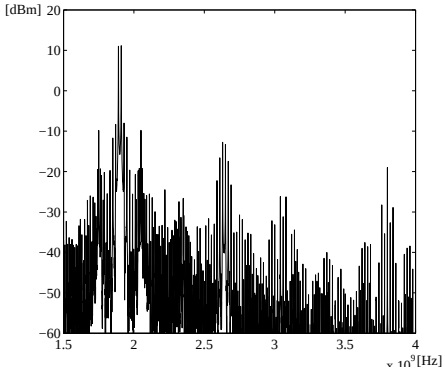

Figure 5.19. Class D polar amplifier spectrum, time delay equal to three RF periods or 1.6 ns

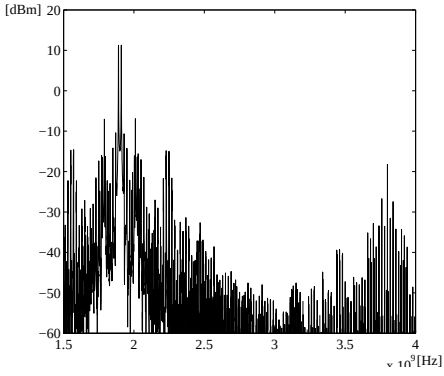

Figure 5.20. Class D polar amplifier spectrum, time delay equal four RF periods or 2.1 ns

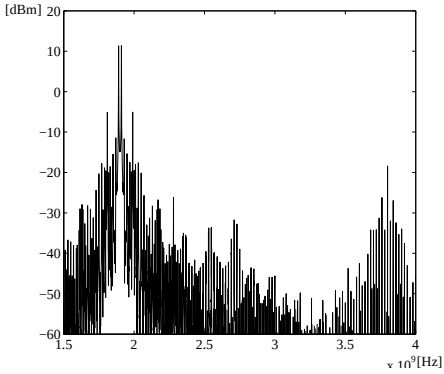

Figure 5.21. Class D polar amplifier spectrum, time delay equal five RF periods or 2.6 ns

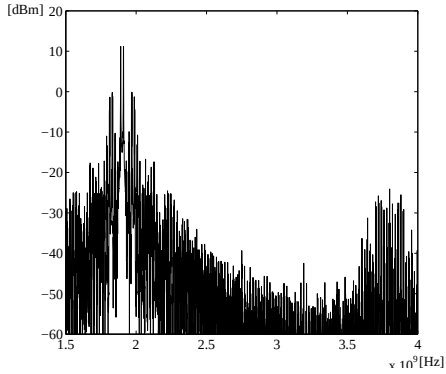

Figure 5.22. Class D polar amplifier spectrum, time delay equal six RF periods or 3.15 ns

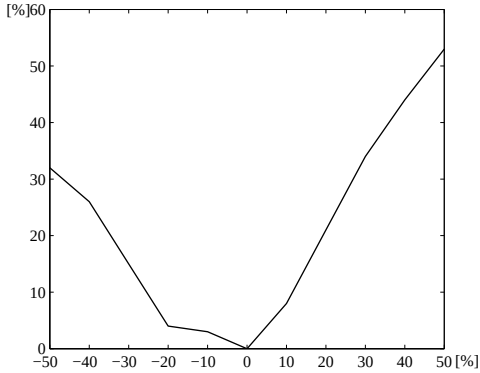

Figure 5.23. C/I degradation in percent versus LC-match inductor asymmetry in percent

The error in degrees a directly added to one of the voltage sources in the testbench. The results for several simulations are displayed in Figure 5.25. The vertical axis show the ratio between the fundamental tone and largest intermodulation product, which for all simulated values were third order. Over anything than a couple of degrees mismatch the linearity is rather poor. The third order intermodulation products have grown around 3 dB or roughly doubled with a phase error of 3°.

5.2.4 Results of Monte Carlo Analysis

To be able to discuss more realistically magnitudes of distortion *Monte Carlo* simulations have been performed. Device parameters are changed randomly and the strength of this kind of simulation is that one can predict performance after fab-

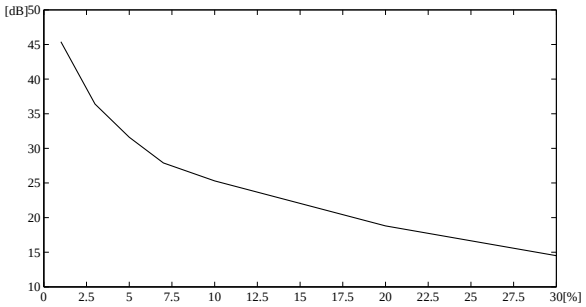

Figure 5.24. Inductor asymmetry for a LC-match in percent gives rise to reduction dynamic range

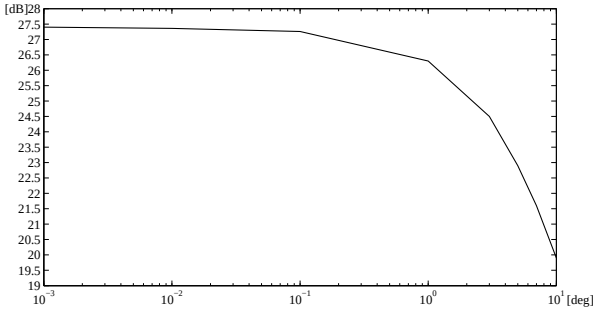

Figure 5.25. Rise in intermodulation due to phase mismatch

rication [48]. Performance metrics like output power and efficiency are assumed to not vary as much. The focus is set at watching how the third order modulation products vary with process variations. The outphasing relies on symmetry between paths and therefore the Monte Carlo analysis give some hints of realistic values of sensitivity between the two paths. The components that make up the matching networks are also considered in this analysis. The inductors are given a 5% uniform deviation of its nominal value, and the capacitors are assumed to be specified more precisely and has a uniform deviation of 1%.

As seen in Figure 5.26 the variations between one of the fundamental tones to the third order intermodulation products for the polar amplifier stays fairly constant in the analysis. In this analysis the audio frequency filter has not been accounted for even though an integrated version would have changed the bandwidth of the filter as well. If the bandwidth of the class S filter is more than two times the RF bandwidth in this simulation. The impact of the variations of the inductor and capacitor is assumed to change the filter insignificantly. The results

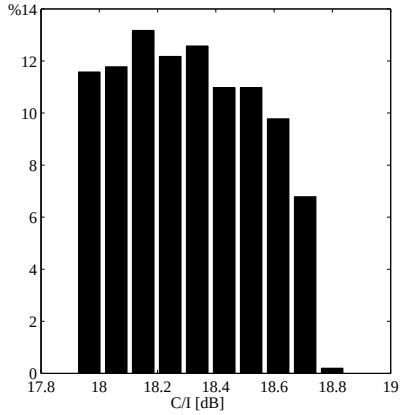

Figure 5.26. Carrier to interferer ratio with a two tone test as input to the class D polar amplifier

of the outphasing Monte Carlo analysis is shown below. The outphasing amplifier is clearly more sensitive than the polar amplifier but still over 50% of the iterations still fall within 0.5 dB. The dispersion is larger, over 2 dB compared to less than 1 dB for the polar topology. This is however not expected, that the differences are not that large anyway. The dynamic range of the outphasing amplifier

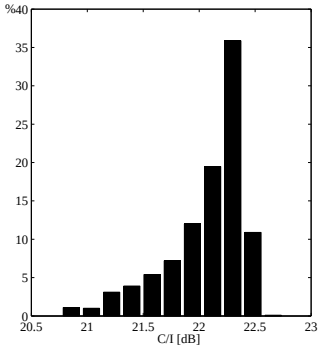

Figure 5.27. Carrier to interferer ratio with a two tone test as input to the class D outphasing amplifier

is very sensitive to any disturbances. That can be seen in 5.28. The variations are extremely large, around 60 dB. And the most iterations fall in the lower end of the plot, showing the sensitivity of the outphasing topology. A dynamic range over 40 dB for an amplifier with maximum output power of a little more than 25 dBm is probably not very realistic. More parameters would in a better simulation setup be accounted for. For example interconnects and other chip parameters are

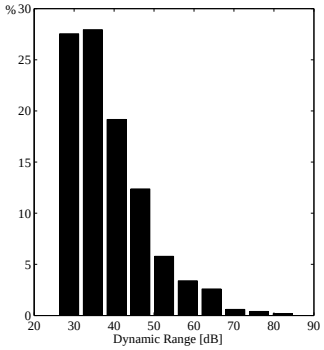

Figure 5.28. Dynamic Range variations with Monte Carlo analysis

in this ignored. And maybe most important the number of iterations are in these analysis set only to 1000, due to that transient analysis are very time consuming.

5.3 Class E

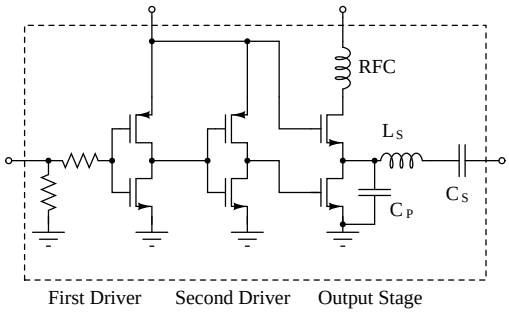

Figure 5.29. Circuit setup for the main class E amplifier

The second investigated topology is a class E amplifier. The same specifications apply as before, with an 150 mW of output power. The load now needs to be downconverted to [51]:

$$P_O = 0.0455\frac{(3.5620V_{DD})^2}{R_L} \Rightarrow R_L = 24\Omega \tag{5.22}$$

That the class E is capable of higher output powers than the class D already can be noticed from the above calculation. Roughly speaking, the class D needs to see a 6 times smaller load, whereas the class E only needs to convert the load

Table 5.2. Specification of class E CMOS 90nm Amplifier

	Name	Width [µm]	Inductance [nH]	Capacitance [pF]
Main	NMOS	1648		
Cascode	NMOS	3800		
	RFC		0.52	
	C_P			10
	C_s			49.7
	L_s			0.313
First driver	NMOS	442		
	PMOS	506		
Second driver	NMOS	100		
	PMOS	286		
Polar Matching	L		1.5	
	C			4.3
Outphasing Matching	L		2.15	
	C			6.38

downwards 2 times. The polar topology is corrected with 0.14 ns time delay in the phase path, since at this first setup do not have any filters in the amplitude path. As before the transistor sizes are optimized for a real load. The first optimization revealed that the drain voltage becomes very large, over six volts. Even though the transistors used have extra thick gate oxide to handle larger voltages, a cascode transistor is stacked on top of the main NMOS device to increase reliability. The main class E amplifier is shown in Figure 5.29. The optimizations are as before, based on high output power and efficiency, with the same weight applied to both. It is interesting to note that the total sum of the transistor sizes are much larger in the class E compared to the previous setup, the class D. A probable reason is that the class D efficiency degrades after a certain point of transistor widths, whereas the class E, (table 5.3) can have much larger transistor sizes without the same efficiency drop. Also, larger drive power is required by the class D because of the larger driver device sizes. After the optimization the maximum output power is a little over 25 dBm and a PAE over 46% The same kind of combiner is used for the outphasing and polar amplifier as for the class D simulations. Even though a lossless combiner is considered by some [14], [68] as not applicable to outphasing class E, due to the the variable loading will affect the amplifiers operation. For the sake of comparison this will be ignored because matched combiners introduce serious losses, and one of the advantages of the architecture would be lost.

5.3.1 Performance Results

In the Figures 5.30 and 5.31 the spectra's of the two tone test is displayed. The polar spectrum are have less unwanted tones. Of course this depends on that the timing has been corrected and the bandwidth of the amplitude modulator is infinite. So one conclusion compared to the class D version is that feedthrough is

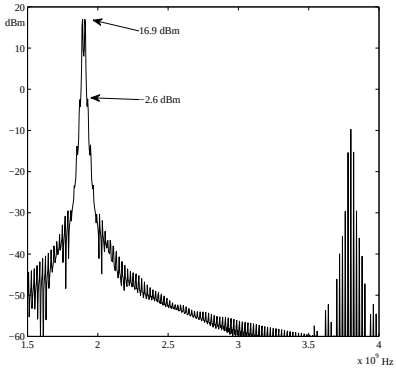

Figure 5.30. Spectrum at output for the class E polar amplifier

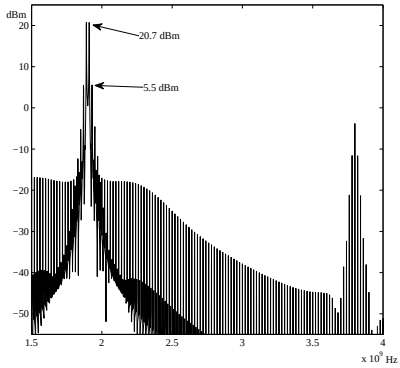

Figure 5.31. Spectrum at output for the class E outphasing amplifier

very small. The cascode transistor, while having a negative impact on efficiency, seem to have a positive impact on the linearity. The feedthrough through the input transistor are not directly coupled to the output. The choice of lossless

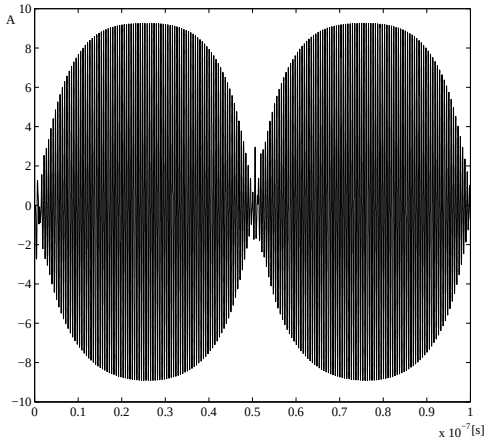

Figure 5.32. Transients of two tone test of for the class E outphasing

combining for the outphasing seem to interfere with linearity. As seen in the figures the spectrum is contaminated by unwanted spectral components. In Figure 5.32 the transient behavior corresponding the spectrum in Figure 5.31 show how the envelope is *squaring up*. In general, sinusoids showing this kind of distortion would have an increased odd order distortion. To find how the combiner alters the behavior of the class E amplifier the drain voltage is shown in Figure 5.33.

The arrow indicates increasing outphasing angle, which are 0, 80, 85, 90 degrees. So clearly for outphasing angles under 80 degrees the class E operation to be affected much. But especially when the two amplifiers outputs should supposedly fully cancel each other the class E action leaves nothing more but a sinusoid with double frequency to the fundamental.

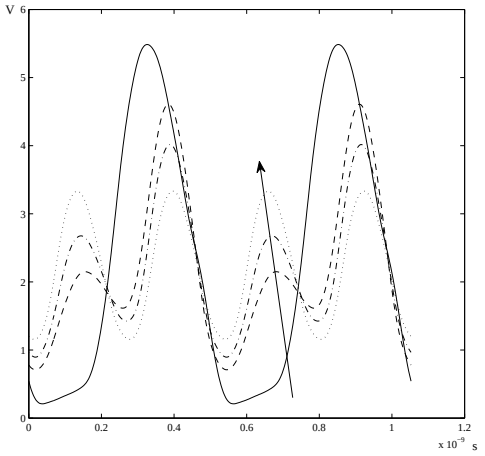

Figure 5.33. Transients at drain of an class E outphasing amplifier for different outphasing angles

5.3.2 Output Power

The output power show same behavior as the in the class D case. For normalized values on the power supply and outphasing angle at full output power the outphasing is able to put out almost 3 dB more compared to the polar amplifier, see Figure 5.34

5.3.3 Efficiency

Because of that the combiner affects the operation of the main amplifiers one could suspect that it is associated with losses. However the degradations are not as large, as seen in Figure 5.35. In fact, for large parts over the normalized supply voltage and outphasing angle it has actually better efficiency than the polar amplifier. The polar architecture have better peak efficiency which would be a result of, as with the class D, the losses involved due to heavy downconversion. But generally for the class E the difference in efficiency are rather moderate.

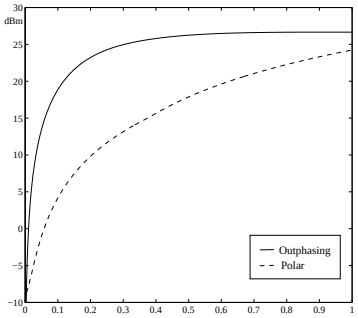

Figure 5.34. Output power versus normalized supply voltage and outphasing angle for the class E implementations

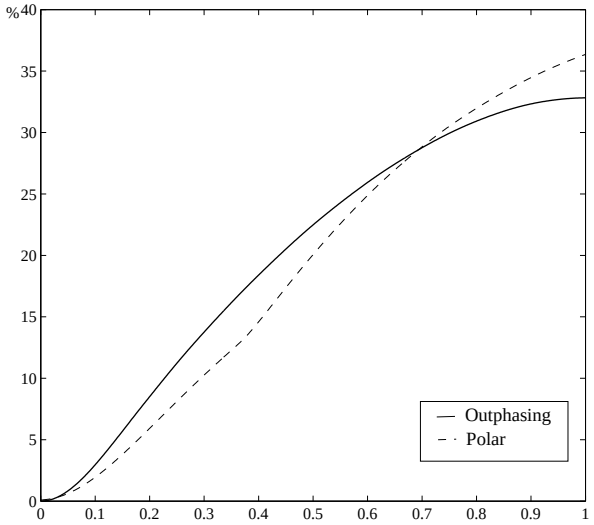

Figure 5.35. Drain efficiency versus normalized supply voltage and outphasing angle for the class E implementations

5.3.4 Results on Polar Linearity

Comparing the third order products in Figure 5.30 and 5.5 for the different amplifier classes the actual difference in carrier to interferer ratio is not very large. But the spectrum is much cleaner for the class E version which should depend on the lower feedthrough.

Envelope Bandwidth & Time Delay in Envelope Path

The envelope bandwidth and mismatch in timing can be considered as more of problems on the architectural level so maybe one can expect that there will be no major differences on how the these distortion factors will degrade class E linearity, versus the class D version. However for completeness this survey the results are displayed in Figure 5.36. The bandwidth of the envelope amplifier curve show the same behavior, with little performance degradation until the envelope bandwidth is in the range of 4:1 compared to the radio frequency bandwidth.

The timing mismatches behaves roughly the same, within delay of a up to a certain point the highest intermodulation products are not increasing. Then higher order products dominate, and contaminate the spectrum as shown in the figures for the class D version. The difference between the maximum and minimum C/I are around 6 dB, and as with the D amplifier really starts to degrade after 4 RF periods.

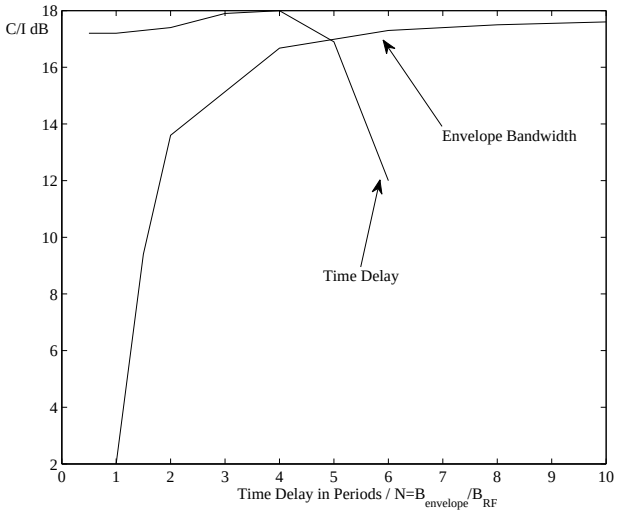

Figure 5.36. Effects of timing mismatch and how finite envelope bandwidth degrades the linearity of a class E amplifiers

5.3.5 Results on Outphasing Linearity

Effects of modulation depth

As seen, the disturbing effect the the outphasing action have on the class E amplifier seem to be of importance for larger outphasing angles. To test the impact for

different angles the two tone test is unsuitable for that purpose. The outphasing angle varies in its full range. With regular amplitude modulation where the carrier is not suppressed, one can choose how deep the amplitude modulation is suppose to be [7]:

$$S_{AM}(t) = A_c(1 + m \cdot sin(\omega_d t))sin(\omega_c t) \tag{5.23}$$

where m is the ratio between amplitude of the envelope and the carrier

$$m = \frac{A_d}{A_c} \tag{5.24}$$

So the components for outphasing will be:

$$S_i(t) = S_{AM}(t) + A_c(1 + m \cdot sin(\omega_d t))sin(\omega_c t \pm pi/2)\sqrt{\frac{1+m}{1+msin(\omega_d t)} - 1} \tag{5.25}$$

The maximum modulation angle used in this section by:

$$\alpha \quad = \quad 90 - cos^{-1}m \tag{5.26}$$

where the shift depends on that the combiner adds in-phase.

The AM signal is not really a good measuring stick for nonlinearities due to that it will be hard to measure between spectral components that is blended from the carrier with the tones blended from the the sidebands. The observed tone, the intermodulation product will come up at 1.93 GHz which is the same frequency where the fifth order intermodulation product between the carrier and one of the sidebands. So this kind of analysis, can only give a hint in what speed the linearity is deteriorating. And also cannot be compared against rest of the figures in this chapter. In Figure 5.37 fundamental to intermodulation product ratio obtained from transient simulations is shown. The carrier to interferer ratio is rapidly decreasing from almost 29 dB to less than 25 dB. The wavy behavior for higher outphasing angles can come from uncertainty with measuring. It seems that the class E linearity degradation depends on the outphasing angle. Even for small variations in the load conditions, significant intermodulation distortion is increased. However over a certain angle the carrier to interferer ratio degradation saturates.

Phase variations between paths

The see how the class E respond to a simulated mismatch between the inputs in phase an error introduced in one of the paths. The difference between the closest intermodulation product are shown in Figure 5.38. Even though the distortion components are larger in comparison to the class D version. The behavior are more or less the same. The real degradation starts at around 0.1 degrees. It seems that the class E is much more sensitive to mismatches in addition to already worse distortion compared to the amplifiers running in D operation.

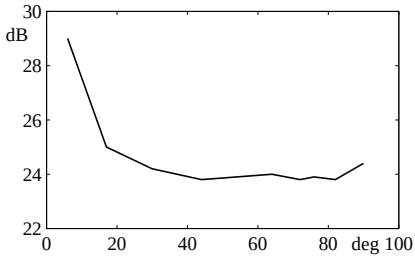

Figure 5.37. C/I (dB) for AM signals with different maximum outphasing angle

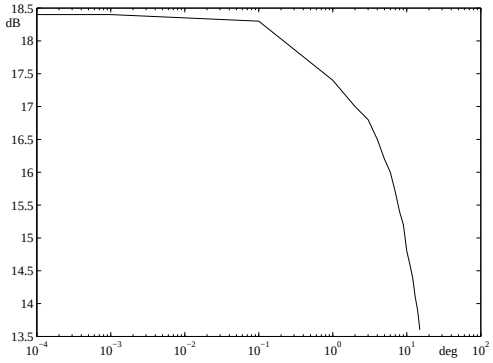

Figure 5.38. Class E outphasing carrier to interferer ratio versus angle mismatch

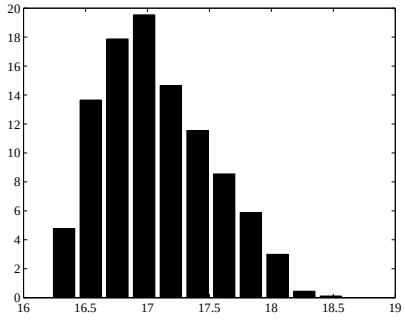

Figure 5.39. Monte Carlo analysis of carrier to interferer ratio for class E polar amplifier

5.3.6 Results of Monte Carlo Analysis

Monte Carlo analysis were performed on the same basis as for the class D topology. One thousand iterations to measure variations in carrier to interferer ratio. The transistors are varied on statistical measures from the manufacturer of the design kit. All passives are varied on a evenly distributed function. As before the inductors are varied 5% and the capacitors 1% from their nominal values. Due to the simulation time length of over one week for every simulation only a simulation for the polar architecture was performed. The result is shown in Figure 5.39. The dispersion is larger, around 2.5 dB, than for the polar class D amplifier, which had variations close to 1 dB. The large difference depends probably less on the transistor variations but to the larger count of passives which varies more in this simulation.

The simulations for dynamic range are performed in the frequency domain and therefore not as time consuming. So one can get a hint of the sensitivity of the class E outphasing. The results are shown in Figure 5.40. The worst case displayed shows around 20 dB of dynamic range. This is worse than the class D outphasing amplifier. Of these two simulations it seems that the class E amplifier is less robust than the class D, in these types of configurations. Of course this depends on if it is reasonable to assume that the integrated passives are that prone to large variations.

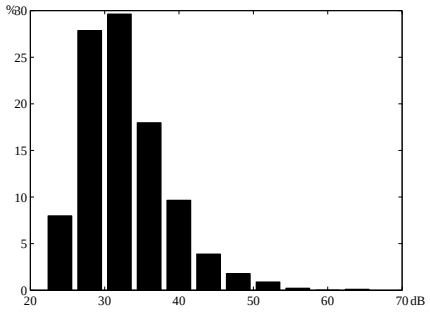

Figure 5.40. Monte Carlo analysis of dynamic range for class E outphasing

Chapter 6

Discussion & Conclusions

The last chapter of this thesis first gives a discussion regarding important performance metrics as well as a conclusion and a proposal of future research.

6.1 Discussion

6.1.1 Output Power & Power Combiners

In recent publications the polar architecture have, compared to outphasing much higher output powers. The polar architecture have examples with figures over 2 W, when examples of outphasing have output powers no higher than 160 mW, at least of those covered in Table 4.3. However not surprisingly, the simulations results show that for equally sized amplifiers, outphasing is capable of roughly 3 dB higher output power, for both classes of amplifiers. This depends of course that outphasing have two amplifiers which directly contributes with power to the load. One might argue that the sizing method used in this thesis favors outphasing. Another approach might have set a maximum chip area for the amplifiers to be sized within. Then the advantage would be for the polar amplifier because that the audio frequency amplifier is not accounted for.

The reasons for the large difference between the topologies in table 4.3 are twofold. First as seen, amplifiers in working in class E operation are capable of higher output levels than class D. Secondly, and the main reason is however that the polar types often use a distributed transformer with several amplifiers. Of the amplifiers listed in table 4.3 all outphasing use regular combiners, such as the LC or transmission line combiners. These cannot easily be put in configurations for high power output combining. None of the outphasing amplifiers in table 4.3 have used a transformer for lossless combining, which seems to be CMOS best choice for integrated combining for power levels more than a couple of hundreds of milliwatts. Especially transmission line combiners seem to be unsuitable for area concerns. Also the lumped transmission lines are either associated with large losses and inaccurate approximations. LC-balun versions might be an alternative

for differential configurations, however the author have not found any publications using them in outphasing configurations.

Even though the outphasing class E seem to be unsuitable due to the linearity simulations done in previous chapter, one cannot dismiss it without further investigations using real modulation formats. However it seems as if the easy dismissal of class E by some, is maybe a too harsh decision. Still, maybe the best chance of fulfilling all requirements of a modulation standard with outphasing are several differential class D used with a distributed transformer. Amplifiers working in class D, since it had best results of the linearity simulations in previous chapter, but the lower output power needs to be compensated for by using a distributed architecture.

6.1.2 Dynamic Range

The first simulations in previous chapter show that the dynamic range for the outphasing amplifier is almost infinite. For example shown in Figure 5.7 the whole dynamic range are not shown due to its large size. In the Monte Carlo analysis the results are more a lot less, a maybe more realistic figure would be 25-40 dB. These simulations were performed at circuit level, but in a real circuit the dynamic range would be further degraded by other issues. Asymmetric interconnects and disturbances from ambient circuitry could may have a significant effect of dynamic range.

The circuit feedthrough is the limiting factor of the dynamic range for all but the current source configurations of the polar technique. Even though two examples were described in Section 4.2.1 for enhancing the dynamic range, some objections to the proposed techniques can be pointed out. Especially since the phase information have multiple paths to the load, distortion can be introduced the same way as AM-PM distortion are added from feedthrough. For example, in Figure 4.4 there are in total four paths the input signal will travel through to the load; Through the matching networks and through the amplifiers. There is a small chance that all of these paths would have the same delay in time. The same way as a filter delay the signal heavily, an LC-matching network would do the same. So, when the signals add up in the combiner they all would have different phase. The sum at the output would contain several phase shifted terms, which would not be the case if there would only be one path to the load.

The polar architectures that do not use the common class S - class E topology do not display these problems with feedthrough, and have accomplished very high figures of dynamic range. However, as discussed in Section 4.2.2 those described in this thesis seem to have linearity problems. To conclude, from the simulations and discussed publications the problem with dynamic range, special measures have to be taken. For outphasing on the other hand, actual figures are hard to predict. However from the Monte Carlo analysis 20-35 dB do not seem unrealistic.

6.1.3 Efficiency

The LC combiner used in the simulations did not introduce significant losses in the class E outphasing amplifier. In fact the efficiency for both classes tested showed more or less the same behavior. The polar architecture had significantly better maximum efficiency for both classes, 15 % better efficiency for the class D, and 3-4 % for the class E configuration. For higher outphasing levels and lower supply voltages the values were reversed in favor of the outphasing technique. For low levels of the envelope the drivers in the polar version starts to dominate the power consumption, which cannot be neglected. The power consumption of the drivers, can be optimized by modulating the power supply but at the cost of linearity.

The type of combiner used with outphasing have a large impact on how the efficiency are for different outphasing angles. So, the efficiency can be altered to be higher at maximum output power, but this will reduce the efficiency for large outphasing angles. A better comparison would have taken in the effect of different combiners. For example, the more simple approach to power combining were used due to the difficulties involved in modeling transformers.

The simulations regarding the efficiency of the polar architecture have a linear relationship to the normalized supply voltage, see Figures 5.9 and 5.35. The efficiency is however much better for the class E version. As described earlier, these are overly optimistic, since the audio frequency amplifier are not considered. Also the author has not found any fully integrated class S - class E versions of the polar amplifier. Those considered have been current source configurations, or used a linear supply voltage modulator and reduced efficiency can probably be expected. Some techniques have been discussed to improve the efficiency, especially for low supply voltage levels. These often trade with linearity which make them less interesting. One strength of the polar architecture compared to outphasing in this context have to be that the optimizer did not have trouble finding solutions, which were significantly better than the outphasing class D counterpart.

6.1.4 Bandwidth

The bandwidth of the two tone test used in the simulations is very high compared to the majority of existing publications regarding the two discussed architectures. The common architecture of the polar topology are often not near these bandwidths for the envelope. As described in Chapter 2, for the switching noise to have an acceptable level, the switching frequency need to be more then ten times the bandwidth of the envelope. For the amplifiers in the simulations these would respond to a switching frequency over 2 GHz, if the envelope would be estimated to 200 MHz. As known, power dissipation relates to switching frequency linearly, so the power consumption would be very large for polar amplifiers with that high switching frequency. On the other hand, as lower the filter is set, the larger the components in the filter will be. Probably to large for integration. If the Butterworth filter in the simulations were to be implemented with N=2, which would have an envelope bandwidth of 40 MHz. According to tabled data the capacitor

would be 112 pF and then the inductor would be around 280 nH (with both source and load impedances set to 50 Ω)[65].

The largest envelope bandwidths covered in this thesis are around 20 MHz, see table 4.3. And as the envelope bandwidth are much larger than the actual RF signal [27] the RF bandwidth would be limited to very narrow band communications systems. It should be pointed out that these bandwidths are not accomplished with the class S modulator but with the current source configurations described in Section 4.2.2.

Even though some authors argue that outphasing is also destined for narrowband communications systems [27], some publications described in this thesis have explored the possibility for wideband communication. For example, at least one example in table 4.3 have over 40 dB ACPR over vast bandwidths as such 50 MHz. So it seems that outphasing can provide good cancellation of the unwanted terms, even though at least one of the publications have the amplifiers in separate chips, which one would assume easier would evoke asymmetries.

6.1.5 Cost

The cost in terms of area for the simulated amplifiers are roughly double for the outphasing amplifier, compared to the polar architecture. Then area of the audio frequency amplifier are not accounted for. If a linear amplifier is used the cost would be smaller than for a class S with an integrated filter. As described in previous section the integrated filter are bound to large. The outphasing amplifier will use more side components for signal generation, which is described in Section 6.1.7.

6.1.6 Distortion

Comparing the spectra's of the simulated amplifiers some differences and similarities can be pointed out. As expected both amplifiers performed best in their respective class where most of the research have focused on. The carrier to intermodulation ratio for the outphasing class D were 27.4 dB, compared to 19.5 for the polar class E. Maybe one cannot draw to many conclusions based on the big difference, the simulations were probably to ideal in its execution. And also, there is no way of knowing if there might be a better solution that the optimizer did not found. However one subtle difference can be pointed out; While outphasing relies fully on symmetry for good distortion figures, the polar topology needs to have some correction for optimal performance. The polar architecture cannot have an infinite envelope bandwidth since it would imply an infinite switching frequency. A trade between linearity and efficiency is present in the design. Even though these distortion corrections can be considered architectural flaws, there might be an advantage due the predictability of the bottlenecks of the architecture.

The outphasing technique show large variations in the carrier to interferer ra-

tio due to asymmetry. However, the results show even in the Monte Carlo analysis a few decibels better performance than the polar amplifier, in both its versions. Even though the these results can be expected to drop more in a finer detailed model, the polar amplifier still used timing correction and infinite bandwidth for the envelope amplifier.

6.1.7 Signal Generation

Both architectures described in Sections 2.2 and 2.3 are similar in the sense that both in their original publications depends on extraction of signals and combination. Signal generation by analog means have to be a disadvantage for the outphasing technique solely due to its need for larger amount of components. In the original publication [13] the signal generation required for example one mixer, two phase modulators, two phase delays and a high gain amplifier. Whereas an analog separator for the polar transmitter *only* would need an envelope detector and a limiter, which could be implemented as a variable gain amplifier [60]. For outphasing there exists other architectures how to generate the two constant envelope signals, but none as simple as compared to the polar amplifier is found by the author.

When using digital signal processors for generation of the signals the architectures are rather similar. As seen in Figure 2.5, the polar architecture needs two mixers, one phase shifter and one oscillator. The outphasing technique needs approximately the double amount of hardware, four mixers, two phase shifters and still one oscillator.

To see the amount of computations needed by the digital signal processor one can compare the equations 2.15 with 2.4 and 2.5. Ignoring the basic operands both share a square root computation. This is the only tougher computation needed by the outphasing topology except a phase shift due to the imaginary term. The polar also needs an arcus tangens operand to calculate the phase of the signal. So, it is hard to draw any conclusions on which of the architectures that should be preferred over the other.

6.1.8 Distortion Correction & Axillary Linearization Techniques

The analog generation of signals of the outphasing amplifier will make an axillary distortion technique harder to implement than a polar amplifier. In the examples discussed in Chapter 2, the outphasing distortion correction have been more intricate compared to the polar counterparts. For example the feedback approaches for the polar transmitter can be put around one of the paths of the architecture. The envelope feedback and phase feedback in Section 2.2.4 are examples of this strategy. This is possible due to that the signal is split into two parts where they are in some sense independent of each other. For the outphasing topology the signal in one branch cannot be separated from the output as easily. This can be seen

in the publications for distortion correction discussed previously in Section 2.3.4. Two of these algorithms described [3],[61] made use of a block *search algorithm* which one have to interpret as feedback to a digital circuit. That in turn will lead to extra hardware such as analog to digital converters. This reasoning have not accounted for predistortion but one can assume that implementation would be harder for outphasing due to some of the properties of the distortion sources in that architecture. The distortion factor relies mostly on mismatch which would be harder to characterize. The polar transmitters sources of distortion could more easily be estimated and measured when the branches are somewhat independent.

6.2 Conclusions

This survey has shown some differences and similarities between the polar and outphasing power amplifier architectures. While the polar architecture has been extensively studied, the outphasing have mostly been publications exploring the possibility to integrated solutions. The reason for this may be that the problems regarding outphasing amplifier seem to be hard to characterize. Of the simulations performed in this work the polar architecture had better maximum efficiency than the outphasing architecture with 15 % for the class D and 3-4% for the class E. However these simulations assumed an ideal audio amplifier. Also, the outphasing architecture had higher efficiency for high to medium power back off levels. The outphasing also have maximum output power with 3 dB for both classes of amplifier operation. With a two tone test the outphasing class D showed the highest carrier to interferer ratio of all simulations with 27.4 dB. The highest simulated carrier to interferer ratio for the polar architecture was the class E version with 19.5 dB. The outphasing amplifier seem to be much more sensitive to process variations and especially any asymmetries between the two signal paths the carrier to interferer ratio was still higher than for the polar versions. The class D outphasing amplifier had a dispersion of the carrier to interferer ratio between 20.7 - 22.5 dB in a Monte Carlo analysis. On the other hand the polar class D showed a carrier to interferer ratio between 18.0 - 18.6 dB. The drop in linearity is especially for the outphasing amplifier is significant. The drop with process variations are at least 6 dB for the outphasing amplifier when the polar amplifier the linearity drop is at smallest 1 dB and as largest close to 2 dB.

6.3 Future Work

There exist several possibilities of making the simulations more trustworthy. The maybe most obvious is to use better models than the ones used in this work. The inductors and capacitors could be modeled with more accurate models of integrated passives, instead as the author have done, with only resistive parasitics. Also the interconnects in this work is modeled as ideal conductors. A better comparison could also have been comparing on layout level with extracted parasitics. Also several other power combiners could have been evaluated for both architectures. This work have only tested one type of combiner, and the results may have

been different if other combiners were tested.

Even though the simulations showing the difference between the outphasing performance due to manufacturing parameters were somewhat depressing, an interesting idea would be to construct a fully integrated outphasing aimed for narrowband communications systems where research for the polar architectures have been extensive. To accomplish the high output power to comparable polar amplifiers, probably other processes which can tolerate higher supply voltages have to be used. With some tweaks the efficiency and output power could also be improved. As seen the for the class D amplifier the widths of the transistor would reach a limit before the performance got worse. For example the outphasing topologies had different drivers for both transistors to mitigate short circuit currents. Also, distributed transformers is could be used. Transformers are good combiners to use with outphasing, current cancellation for high outphasing angles would give good efficiency. The series combining transformer are maybe not a good choice for layout reasons. The closest transistor do not have to be in anti-phase, prohibiting use of virtual grounds. A parallel series transformer would be a better choice for easier layout, and would vouch for good efficiency.

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