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Strain relaxation of thin $\text{Si}_{0.6}\text{Ge}_{0.4}$ grown with low-temperature buffers by molecular beam epitaxy

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A double-low-temperature-buffer variable-temperature growth scheme was studied for fabrication of strain-relaxed thin $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer on Si(001) by using molecular beam epitaxy (MBE), with particular focuses on the influence of growth temperature of individual low-temperature-buffer layers on the relaxation process and final structural qualities. The low-temperature buffers consisted of a 40 nm Si layer grown at an optimized temperature of $\sim 400^\circ\text{C}$, followed by a 20 nm $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer grown at temperatures ranging from 50 to 550°C . A significant relaxation increase together with a surface roughness decrease both by a factor of ~ 2 , accompanied with the cross-hatch/cross-hatch-free surface morphology transition, took place for the sample containing a low-temperature $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer that was grown at $\sim 200^\circ\text{C}$. This dramatic change was explained by the association with a certain onset stage of the ordered/disordered growth transition during the low-temperature MBE, where the high density of misfit dislocation segments generated near surface cusps largely facilitated the strain relaxation of the top $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer. © 2009 American Institute of Physics. [DOI: 10.1063/1.3091266]

I. INTRODUCTION

With the rapid development of strain engineering in Si technology, the strain-relaxed $\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$) buffers on Si substrates as “virtual substrates” (VSs) have been highly demanded. They are crucial in introducing and controlling the strain in the device structures grown on top for desired electrical and optical properties. Such SiGe VSs have so far been widely used for high-speed strained Si and SiGe channel field-effect transistors.¹ There is also a potential for integration of III-V materials into Si.² Moreover, the emerging Si-based photonics technology, such as mid- and far-infrared Si/SiGe quantum cascade emitters,^{3–5} has also shown a substantial need for high-quality $\text{Si}_{1-x}\text{Ge}_x$ VSs, particularly with x ranging from 0.2 to 0.5. An ideal SiGe VS should possess the following major characteristics: (1) a uniform and high degree of strain relaxation, (2) a smooth surface with low roughness, (3) a high crystalline quality with low densities of dislocations and other extended defects, and (4) a low fabrication cost and the compatibility with the current processing technology.

In order to achieve a high degree of strain relaxation, the SiGe layer with a uniform composition, grown directly on Si at conventional growth conditions, must have a thickness significantly larger than the corresponding temperature-dependent critical thickness value. This relaxation process usually generates a high density of threading dislocations and a very rough surface for the relaxed SiGe layers,⁶ which, therefore, are not suitable for any practical use. In the past two decades, a considerable amount of effort has been made trying to solve this problem. Several growth schemes and fabrication techniques were proposed and studied, which included compositionally-graded SiGe growth,^{2,7} ion implanta-

tion during SiGe growth,⁸ incorporation of strain compliant buffer layers,^{9,10} post-growth annealing and intermixing,¹¹ low-temperature (LT) Si or/and SiGe buffer layers,^{12–15} etc. Among them, the technical approaches based on the concept of point defect injection and interaction with dislocations by using LT growth of a Si or SiGe buffer layer have attracted a large interest due to the simple process and the much lower demanded growth thickness. Upon experimental observations, several models of a large diversity have been proposed to address the mechanism of LT buffers for the strain-relaxation enhancement. For example, Li *et al.*¹³ speculated that there existed low energy sites in the LT buffer for dislocation nucleation, or that point defects could “trap” propagating dislocations; Kasper *et al.*¹⁴ suggested that the point defects may assist dislocation nucleation at an earlier stage and promote climbing of dislocations, resulting in a higher degree of relaxation with lower densities of threading dislocations; Luo *et al.*⁹ further demonstrated that the compliant effect of a LT-Si buffer layer also contributed to the resulted low-defect strain-relaxed SiGe VS with a smooth surface; Vyatkin¹⁶ lately proposed a model based on the atomic rearrangement of atoms and vacancies at the LT-Si/SiGe interface; and some other explanations as well. However, none of those were adequate enough to explain why the LT-buffer growth scheme has been unsuccessful in fabrication of high-quality $\text{Si}_{1-x}\text{Ge}_x$ VSs mainly with $0.4 \leq x < 0.6$.^{17–19} The relaxed SiGe VSs within this Ge composition range exhibited the maximal surface roughness and threading dislocation density,¹⁸ suggesting a much more complicated relaxation process.¹⁹ Therefore, a better understanding must be obtained in order to clarify the essential mechanism of the influence of LT growth on the strain-relaxation process.

Recently, Myronov and Shiraki²⁰ proposed and demonstrated a double-LT-buffer variable-temperature growth scheme consisting of a LT-Si layer, followed by the growth

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of a constant-composition SiGe thin layer with varied substrate temperature from low to high as the growth proceeded. The idea was to use the LT-Si buffer for “dislocation trapping” and the LT-SiGe part as a seed with a higher amount of point defects to enhance the relaxation. Their initial results showed for $\text{Si}_{0.34}\text{Ge}_{0.66}$ that at a certain LT-SiGe substrate temperature a dramatic increase in the strain relaxation was achieved accompanied with a surface roughness decrease, while the total SiGe layer was as thin as 50 nm. Using differential etching with modified Shimmel’s etchant, they estimated a threading dislocation density of $<1 \times 10^5 \text{ cm}^{-2}$ for the SiGe VSs grown at the optimum conditions. Moreover, the cross-hatch morphology of the final surface, which commonly appeared when using other growth methods, was not observed for any of the samples grown in their study. This approach is thus very attractive since it could be a potential solution to the aforementioned difficulty related to $\text{Si}_{1-x}\text{Ge}_x$ VSs with $0.4 \leq x < 0.6$. In the present work, an attempt was made with a similar growth scheme to fabricate $\text{Si}_{0.6}\text{Ge}_{0.4}$ VSs with thickness below 100 nm. In addition, comprehensive *in situ* and *ex situ* material characterizations were performed in order to gain more insights on the LT growth process for the SiGe alloy of this particular Ge composition.

II. EXPERIMENTAL DETAILS

In the present study, all samples were grown on 3 in. p-Si (001) substrates (resistivity 5–10 $\Omega \text{ cm}$). The growth was carried out by using a Balzers UMS-630 solid-source Si/Ge molecular beam epitaxy (MBE) system with a base pressure of $<5 \times 10^{-11}$ mbar and a pressure during growth of $<1 \times 10^{-8}$ mbar.²¹ The substrate heating power (in constant mode) was calibrated by using a thermal couple mounted onto the surface of a test Si wafer over the entire temperature range used in this study. The substrate temperature during growth was monitored *in situ* by a calibrated infrared radiation pyrometer (measurement range 300–800 °C). The transient behavior of the substrate temperature was also carefully studied before the growth experiments. All substrates were chemically cleaned involving HF dip and UV ozone surface treatment,²¹ and thereafter immediately loaded into the load-lock chamber of the MBE system. Throughout the entire growth process, the sample surface morphology was continuously monitored *in situ* by reflection high-energy electron diffraction (RHEED) with the incidence beam along the $\langle 110 \rangle$ azimuth.

In Ref. 20, Myronov and Shiraki originally used the LT-Si buffer trying to “trap” the dislocations that might be generated in the LT-SiGe buffer layer during relaxation. We expected that the LT-Si buffer, containing a certain amount of point defects, probably also contributed to the relaxation process to some extent through the aforementioned compliant effect and atom rearrangement at the Si/SiGe interface. It was experimentally demonstrated that for a LT-Si layer of certain thickness, there existed an optimum growth temperature at which the LT-Si layer could help relaxing the SiGe the most, while resulting in the best crystalline quality.⁹ A higher LT-Si growth temperature was not able to generate enough point defects for an efficient relaxation, while a lower one

FIG. 1. Schematic layer structures of grown samples. (a) Structure 1 for optimization of the LT-Si buffer substrate temperature. (b) Structure 2 for studying the influence of the LT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ buffer substrate temperature. The gaps introduced between adjacent layers represent growth interruptions for substrate temperature ramping and stabilization.

caused a high defect level in the SiGe layer. Therefore, the first type of structure [structure 1, as specified in Fig. 1(a)] contained only one Si buffer layer, which was grown in the temperature range of 200–550 °C in order to optimize the substrate temperature for the LT-Si buffer, LT_1 . Thereafter, a 70 nm high-temperature (HT) $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer was grown at a constant temperature of 550 °C on top of the LT-Si buffer. For further confirmation, the growth was repeated but with a much thicker HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer of 150 nm. The second type of structure [structure 2, as shown in Fig. 1(b)] was grown for studying the influence of the LT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ substrate temperature, LT_2 (ranging from 50 to 450 °C) on the final VS quality. The LT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ buffer thickness of 20 nm was chosen in such a way that it exceeded the thermal equilibrium critical thickness (~ 5 nm) for $\text{Si}_{0.6}\text{Ge}_{0.4}$ (Ref. 22) to initiate the strain relaxation. In order to improve the crystalline and surface quality at the topmost $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer and to complete the strain relaxation, the final 50 nm HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ was deposited at 550 °C, giving the total $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer thickness of 70 nm, which was slightly above the nonequilibrium critical thickness of ~ 50 nm for the chosen Ge content.²³

Prior to the growth, the substrate was first *in situ* annealed at ~ 800 °C for 10 min to sublimate the thin oxide layer on the substrate surface. The growth started with a 50 nm HT-Si buffer grown at ~ 700 °C in order to obtain a smooth growth basis with a high crystalline quality. For the samples with structure 1, the growth was interrupted for long enough time (13–17 min) to allow the substrate temperature ramping down and stabilizing at LT_1 . The 40 nm LT-Si buffer was grown at LT_1 , and then the growth was interrupted again to ramp up the substrate temperature and stabilizes it at 550 °C. Finally, a 70 or 150 nm HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer was grown at a constant temperature of 550 °C. For the samples with structure 2, the LT-Si buffer was grown in the same way as for structure 1 but all at 400 °C (this will be explained later). Afterward, a growth interruption was introduced to ramp and stabilize the substrate temperature at LT_2 . It deserves to be mentioned that the growth interruption time was over 15 min for the samples to be produced with $LT_2 < 300$ °C in order to ensure that the substrate temperature

TABLE I. Summary of growth parameters for samples grown in the present work.

Sample series	Sample label	LT-Si substrate temperature, LT_1 ($^{\circ}\text{C}$)	LT-Si _{0.6} Ge _{0.4} substrate temperature, LT_2 ($^{\circ}\text{C}$)	LT-Si _{0.6} Ge _{0.4} layer thickness (nm)	Thickness of HT-Si _{0.6} Ge _{0.4} layer grown at 550 $^{\circ}\text{C}$ (nm)
Structure 1					
S1-A	S1-A-550	550	...	...	70
	S1-A-400	400	...	...	70
	S1-A-300	300	...	...	70
	S1-A-200	200	...	...	70
S1-B	S1-B-450	450	...	...	150
	S1-B-400	400	...	...	150
	S1-B-300	300	...	...	150
Structure 2					
S2	S2-450	400	450	20	50
	S2-400	400	400	20	50
	S2-300	400	300	20	50
	S2-200	400	200	20	50
	S2-100	400	100	20	50
	S2-50	400	50	20	50

reached the desired values. When the LT-Si_{0.6}Ge_{0.4} growth was finished, the substrate temperature was quickly elevated and stabilized at 550 $^{\circ}\text{C}$ within 2 min without growth interruption, while the final 50 nm HT-Si_{0.6}Ge_{0.4} was grown. During the temperature ramping, special care was taken in order to prevent strong temperature overshooting over 550 $^{\circ}\text{C}$. All the growth experiments were carried out at a calibrated growth rate of 0.05 nm/s for both the Si and SiGe. Table I gives a summary of growth parameters for the samples grown in the present work.

The final surface morphology of grown samples was characterized using atomic force microscopy (AFM) immediately after removing samples from the MBE system. A Veeco Dimension 3100 was used in tapping mode in air ambient. The surface roughness was evaluated by the roughness r.m.s value obtained from an AFM image of $10 \times 10 \mu\text{m}^2$ scan size. The strain condition and Ge content of the SiGe layer were studied by means of two-dimensional (2D) reciprocal space mapping (RSM) of high-resolution x-ray diffraction (HRXRD) around Si (004) and (113) reciprocal lattice points. The HRXRD-RSM measurements were performed using a Philips X'Pert x-ray diffractometer (Cu $K\alpha_1$ radiation), with a hybrid Ge(220) monochromator (divergence $\sim 0.005^{\circ}$) and an asymmetric triple-axis analyzer. The strain-relaxation degree and Ge content of the SiGe were calculated following the method detailed in Ref. 24. The grown samples were further investigated using transmission electron microscopy (TEM). The cross-sectional TEM (XTEM) imaging was performed in a FEI Tecnai G² TF20 UT microscope equipped with a field emission gun operated at 200 kV, while the plan-view TEM (PVTEM) imaging was made using a Philips CM20 UT microscope operated at 200 kV which has smaller objective apertures for dark field imaging. The TEM specimens were prepared by mechanical thinning and low-angle ion milling until the electron transparency was reached.

III. EXPERIMENTAL RESULTS

A. Samples grown with structure 1

Figure 2 shows the typical RHEED patterns obtained at different stages during the growth of samples with structure 1. After removing the oxide layer on the substrate surface by

FIG. 2. (Color online) Typical RHEED patterns observed after (a) removing the thin oxide layer on the substrate surface, (b) the HT-Si buffer deposition, (c) growing the LT-Si buffer at $LT_1=400^{\circ}\text{C}$ for S1-A-400 and S1-B-400 samples, (d) growing the LT-Si buffer at $LT_1=200^{\circ}\text{C}$ for S1-A-200, the growth completed for (e) S1-A-200 samples and (f) S1-B-400 samples. Some black dots and stripes in the images are due to scratches in the fluorescent screen.

FIG. 3. (Color online) AFM images of $10 \times 10 \mu\text{m}^2$ size of (a) S1-A-400 sample and (b) S1-B-400 sample. The image edges are roughly aligned with surface $\langle 110 \rangle$ directions. The insets are images of $2 \times 2 \mu\text{m}^2$ size showing the detailed island morphology. (c) and (d) are line scan profiles from (a) and (b), respectively. The line scan directions were off from both surface $\langle 100 \rangle$ and $\langle 110 \rangle$ directions.

annealing at $\sim 800^\circ\text{C}$, a Si (001) 2×1 spotty pattern was observed as shown in Fig. 2(a), indicating a generally clean and flat surface. After deposition of the 50 nm HT-Si buffer, the 2×1 pattern became much sharper and more intense [Fig. 2(b)]. It can be concluded that an atomically flat surface with a high crystalline quality was obtained. After the growth of LT-Si buffer at different substrate temperatures LT_1 , the RHEED pattern gradually changed from a well-defined 2×1 spotty pattern for $LT_1 > 400^\circ\text{C}$ to a more streaky one [Fig. 2(c)] for $300^\circ\text{C} \leq LT_1 \leq 400^\circ\text{C}$ and eventually became a 1×1 bulk-like pattern when LT_1 reached 200°C [Fig. 2(d)]. This was a direct consequence of the decreased Si adatoms mobility at low substrate temperatures, which resulted in an evolution of the growth surface with increasing step density and eventually formation of three-dimensional (3D) islands. Shortly after starting the HT-Si_{0.6}Ge_{0.4} layer growth, the integral-order diffraction streaks split into spots vertically with a chevron-type feature and the half-order diffraction streaks appeared simultaneously to be bended. For all samples in the S1-A series, this kind of pattern remained after the capping growth of the 70 nm HT-Si_{0.6}Ge_{0.4} layer, as revealed in Fig. 2(e). The bending angle of the half-order diffraction streak, as well as the angle between the chevron arms and the Si [001] direction, was measured as $\sim 8^\circ$ in both cases, suggesting that these features might originate

from a high density of $\{105\}$ facets on the sample surface.²⁵ As the growth continued and the HT-Si_{0.6}Ge_{0.4} layer thickness was beyond 70 nm, the chevron-type feature slowly disappeared and ended up with a more 2×1 streak-like pattern for all samples in S1-B series, as depicted in Fig. 2(f).

The final surface morphology observed from AFM measurements exhibited very similar features for samples within each series. Figure 3 shows the representative AFM images of the S1-A-400 and S1-B-400 samples, where the typical cross-hatch pattern decorated with islands was clearly seen on both sample surfaces. It is well known that the cross-hatch pattern is strongly associated with a bunch of closely spaced or pileups of $60^\circ a/2\langle 110 \rangle$ misfit dislocations propagating along the in-plane $\langle 110 \rangle$ directions below the surface.^{26,27} The presence of the cross-hatch pattern was thus an evident sign of strain relaxation of the Si_{0.6}Ge_{0.4} layer. Moreover, the surface islands apparently showed the preference to be located along the cross-hatch lines. This was very similar to what was observed from the self-alignment of Ge quantum dots grown on relaxed SiGe VSs and explained by the nonuniformity of the strain field caused by the underlying dislocations.²⁸ The islands in Fig. 3(a) were much smaller and denser than those observed in Fig. 3(b). The majority of islands were elongated along the surface $\langle 100 \rangle$ directions and

FIG. 4. (Color online) (a) (004) and (b) (113) HRXRD-RSMs of S1-A-400 sample. (The diffraction intensity contours were in log scale.)

bounded by $\{105\}$ facets ($\sim 11^\circ$ side-wall angle as measured by AFM), as shown in the inset of Fig. 3(a). This was consistent with the RHEED observation. On the other hand, the islands in Fig. 3(b) were more randomly oriented with less defined side-wall planes, and they showed a tendency to coalesce with each other [Fig. 3(b), inset]. In consistence with the RHEED experiments, the resulted sample surface was more dominated by the long range cross-hatch pattern with a generally higher surface height variation. This difference was clearly evidenced by the line scan profiles shown in Figs. 3(c) and 3(d). As a consequence, the measured surface r.m.s roughness values from samples in S1-B series were universally higher than those in S1-A series, and a summary will be presented below. This kind of surface morphology evolution has been reported and explained as the result of the MBE growth process where a metastable SiGe film of high Ge content became plastically relaxed at an intermediate substrate temperature with a low growth rate.²⁹

HRXRD-RSMs showed that all S1 samples were partially relaxed with similar features in the maps but with different degrees of strain relaxation. Since the growth condition for the S1-A-550 sample could be regarded as that for the standard MBE growth process, the relaxation of this sample confirmed that the $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer thickness of 70 nm was larger than the corresponding nonequilibrium critical thickness reported in literature. Therefore, the choice of the total thickness of the $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer in the S2 series fulfilled the requirement for the present studies. Figures 4(a) and 4(b) are representative (004) and (113) RSMs of the S1-A-400 sample. No appreciable lattice plan tilt of the $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer from the Si substrate along the in-plane $\langle 110 \rangle$ directions was observed from the (004) RSM, which in fact was the case for all other samples as well. Hence, no correction was made for the $\text{Si}_{0.6}\text{Ge}_{0.4}$ peak position in (113) RSMs during calculations of the relaxation degree. HRXRD-RSMs confirmed that the Ge composition of the SiGe layers in all the samples grown in this study (including all samples with structure 2) was successfully controlled at 40 ± 2 at. %.

Figure 5 summarizes the strain relaxation and the corresponding surface roughness r.m.s values as a function of LT_1 for samples in the S1-A and S1-B series. Due to the doubled $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer thickness, it was not a surprise that samples

FIG. 5. (Color online) Strain relaxation and corresponding surface roughness as a function of LT-Si growth temperature LT_1 for all grown samples with structure 1. ● represents the data for samples in the S1-A series (with 70 nm HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$) and ■ for S1-B series (with 150 nm HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$).

in the S1-B series generally showed a much higher relaxation with higher surface roughness than those in the S1-A series. On the other hand, the $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer reached the highest relaxation at $\text{LT}_1 = 400^\circ\text{C}$ regardless of the layer thickness. This was consistent with the fact that the growth scheme of using LT-Si buffer was usually successful for $x \leq 0.3$ when the buffer was grown at $\sim 400^\circ\text{C}$.^{12,13,17} Experiments by using positron annihilation spectroscopy have proven that a Si layer grown at 400°C contained the highest point defect density.³⁰ However, a single LT-Si buffer clearly showed a limited capability for enhancing the relaxation of the $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer, as revealed in Fig. 5. For a 70 nm $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer, its relaxation could only be increased in the best case by $\sim 10\%$ (from $\sim 40\%$ to $\sim 50\%$) within the studied LT_1 range. In order to obtain a highly relaxed $\text{Si}_{0.6}\text{Ge}_{0.4}$ with $>70\%$ relaxation, one had to grow a much thicker SiGe layer at the cost of the surface roughness increase.

The TEM studies were focused on the S1-A-400 sample with $\text{LT}_1 = 400^\circ\text{C}$ and a 70 nm HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer which showed the highest relaxation in the S1-A series. Figure 6(a) is a typical bright field XTEM micrograph of this sample, where most of the defects were located at the LT-Si/HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ interface and below, but very few in the HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$. The defects were identified as being dominated by misfit dislocations and $\{111\}$ stacking faults. Within the viewing area of the specimen, no clear dislocation pile-ups or half loops were observed below the LT-Si/HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ interface, while these dislocation morphologies are commonly seen in compositionally-graded SiGe VSs due to the modified Frank-Read mechanism.^{31,32} The high magnification XTEM images, like the one shown in Fig. 6(b), further revealed that the majority of the extended defects were stacking faults primarily located right below the LT-Si/HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ interface running toward the Si substrate side, but only few of them propagated upward through the HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer and reached the top surface. The presence of $\{111\}$ stacking faults within the LT-Si buffer was the common feature in the SiGe VSs fabricated using the LT growth scheme, which was explained by the strain-

FIG. 6. [(a) and (b)] Bright field XTEM micrographs and (c) a dark field PVTEM micrograph with $g=[220]$ of S1-A-400 sample.

introduced vacancy rearrangement and aggregation near the LT-Si/HT-SiGe interface.^{16,33} Those stacking faults were suggested as the sources of dislocations or the products by separation of total dislocations into partial dislocations. PVTEM investigations revealed a regular cross-hatched misfit dislocation network at the LT-Si/HT-Si_{0.6}Ge_{0.4} interface, and the threading dislocation density was estimated to be in the order of $1 \times 10^7 \text{ cm}^{-2}$. In Fig. 6(c), the visibility of the dislocation lines along both in-plane $\langle 110 \rangle$ directions in the dark field PVTEM with $g=[220]$ clearly indicated that those misfit dislocations were of $60^\circ a/2\langle 110 \rangle$ type. Moreover, one can see some misfit dislocations closely bunched together. The cross-hatched 60° misfit dislocation network with bunched dislocations explained the observation of the cross-hatch pattern morphology in the AFM measurements.

B. Samples grown with structure 2

Based on the results shown in Sec. III A, $LT_1=400^\circ\text{C}$ was considered to be the most favorable choice for the following samples with double LT buffers. Consequently,

FIG. 7. (Color online) RHEED patterns observed at the end of the LT-Si_{0.6}Ge_{0.4} buffer growth for (a) S2-450 sample, (b) S2-300 sample, (c) S2-200 sample, and (d) S2-50 sample. RHEED patterns obtained after the growth was completed for (e) S2-200 sample and (f) S2-50 sample. Lines were drawn in (c) to illustrate the divergence angle of the diffraction spot intensity.

samples in the S2 series were grown with a constant LT_1 of 400°C , and only the substrate temperature for the LT-Si_{0.6}Ge_{0.4}, LT_2 , was varied between different samples.

After the deposition of the HT-Si buffer and successive 40 nm LT-Si buffer at $LT_1=400^\circ\text{C}$, the corresponding RHEED patterns were the same as shown in Figs. 2(b) and 2(c). When the LT-Si_{0.6}Ge_{0.4} buffer was completed at $LT_2 \geq 400^\circ\text{C}$ (S2-450 and S2-400 samples), chevron-type features were again observed in the RHEED pattern, as shown in Fig. 7(a). This was indicative of the presence of hut-cluster islands on the surface, like in the case for the S1 samples. When the LT_2 was 300°C , broad 2×1 streaks were observed in the RHEED pattern [Fig. 7(b)], which was a rather straight evidence that the islanding on the finishing surface of the LT-Si_{0.6}Ge_{0.4} buffer was much more suppressed. This was an expected result since the limited adatom mobility at a lower growth temperature could impede the formation of strain-driven 3D islands while increasing the generation of 2D surface terraces.

When growing the LT-Si_{0.6}Ge_{0.4} buffer at $LT_2=200^\circ\text{C}$, a 1×1 bulk RHEED pattern gradually developed. At the end of LT-Si_{0.6}Ge_{0.4} buffer growth, the diffraction spot intensity became diverged (meaning that the spots were in triangular shape) and diffuse, as depicted in Fig. 7(c). The intensity divergence angle away from the Si (001) normal was measured as $\sim 11^\circ - 15^\circ$, corresponding to the presence of surface $\{11\}$ facets with $l \geq 5$. As LT_2 decreased below 200°C , this kind of pattern appeared much earlier and the resulted 1×1 bulk patterns from the final LT-buffer surfaces were

more diffuse and diverged. The most diffuse and weakest RHEED pattern was obtained in the S2-50 sample with $LT_2 = 50^\circ\text{C}$, as shown in Fig. 7(d). After the HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ growth started, the surface conditions were quickly recovered for the samples with $LT_2 \leq 200^\circ\text{C}$, evidenced by the facts that the half-order RHEED diffraction streaks reappeared, accompanied with the simultaneous intensity increase for the integral-order spots. When the entire growth was completed, all the samples with $LT_2 \geq 300^\circ\text{C}$ generally showed the chevron-type RHEED pattern as the one in Fig. 2(e). Surprisingly, a rather straight 2×1 streaky pattern with a slight vertical-intensity-modulation was observed for the S2-200 sample [Fig. 7(e)], but a slight chevron-type pattern for the S2-100 and S2-50 samples. Figure 7(f) shows the RHEED pattern obtained from the final surface of the completed S2-50 sample, in which both the half-order streak bending angle and the half splitting angle of the chevron arms were measured to be $\sim 5^\circ$. The observations from the RHEED pattern evolutions suggested that for the samples with $LT_2 > 200^\circ\text{C}$, the growth basically proceeded in the same way as for the samples in the S1-A series. With decreasing LT_2 , the adatom mobility on the surface during the growth of LT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ buffer decreased correspondingly. Starting from $LT_2 = 200^\circ\text{C}$, a transition from the strain-driven islanding to the kinetic roughening of the surface, together with building up of $\{11\}$ terminated facets, was witnessed by RHEED. The diffuse diffraction spots also signified a degraded crystalline quality in the near surface region, presumably by a high density of defects. This process began at an earlier stage of the LT- $\text{Si}_{0.6}\text{Ge}_{0.4}$ buffer growth as LT_2 was further decreased. With the growth proceeded at $LT_2 < 200^\circ\text{C}$, the surface roughness continuously increased, followed by the enhanced formation of amorphous phase at the surface, resulting in obscured diffraction spots at the end of the buffer growth. Due to the quickly elevated substrate temperature during the growth of the HT- $\text{Si}_{0.6}\text{Ge}_{0.4}$, the adatom mobility increased with a much higher surface kinetic energy. The adatoms thus had a much higher probability to fill in the surface troughs and settle at the correct lattice sites on the surface, resulting in a smoother surface with an improved crystalline quality.

Samples in the S2 series were then characterized *ex situ* using AFM, HRXRD-RSM, and TEM. For samples grown with $LT_2 > 200^\circ\text{C}$ (i.e., S2-450, S2-450, and S2-300), the general features observed in the aforementioned *ex situ* measurements revealed a large similarity to those observed from samples in the S1-A series. Therefore, the specific results will not be repeated again in this section. However, dramatic differences were observed for the samples with $LT_2 \leq 200^\circ\text{C}$, which are detailed below.

One striking feature observed from AFM measurements on the samples with $LT_2 \leq 200^\circ\text{C}$ was a completely cross-hatch-free surface morphology, and the surface was dominated only by high densities of small islands and pits in irregular shape. This is illustrated in Fig. 8 for the AFM images obtained from S2-200 and S2-50 samples. Compared to the S1-A-400 sample with the same total $\text{Si}_{0.6}\text{Ge}_{0.4}$ layer thickness, the surface of the S2-200 sample was considerably smoother due to the absence of the cross-hatch pattern and

FIG. 8. (Color online) AFM images of $10 \times 10 \mu\text{m}^2$ size of (a) S2-200 sample and (b) S2-50 sample. The insets are images of $2 \times 2 \mu\text{m}^2$ size showing the detailed island morphology in (a) and (b), respectively.

much smaller amplitude of the surface height variation. For the samples with a lower LT_2 , the shape of islands and pits on the surface became more irregular, and the islands were more and more connected to each other but narrower in width (i.e., the total pit area increased). As an extreme example, the results of the S2-50 sample are shown in Fig. 8(b) and the inset therein.

Another interesting feature was noticed from the HRXRD-RSMs of samples with $LT_2 \leq 200^\circ\text{C}$. As indicated by arrows in Fig. 9, when LT_2 decreased to 200°C , an additional peak besides the Si and main $\text{Si}_{0.6}\text{Ge}_{0.4}$ peaks appeared in both (004) and (113) RSMs. In (113) RSMs those peaks and the Si peaks were located at the same Q_x positions,

FIG. 9. (Color online) [(a) and (c)] (004) and [(b) and (d)] (113) HRXRD-RSMs of S2-200 and S2-50 samples, respectively. The lines in (b) and (d) were drawn to illustrate the vertical alignment between the Si substrate peaks and the completely strained $\text{Si}_{0.6}\text{Ge}_{0.4}$ features indicated by arrows. (The diffraction intensity contours were in log scale.)

FIG. 10. Strain relaxation and corresponding surface roughness as a function of LT-Si_{0.6}Ge_{0.4} growth temperature LT_2 for all samples in the S2 series and S1-A-400 sample.

i.e., the corresponding material was totally constrained to fit with the Si lattice in-plane. Due to the interference of the intensity from the main Si_{0.6}Ge_{0.4} peaks, it was difficult to precisely determine the vertical position of those extra peaks (i.e., Q_y values) in both (004) and (113) RSMs, but most of the peak intensity was located approximately at the position corresponding to the fully-strained Si_{0.6}Ge_{0.4}. With further decreasing LT_2 , the intensity of the extra peaks became weaker, and finally only a small tail was left. One can clearly see this evolution process by comparing Figs. 9(a) and 9(b) with Figs. 9(c) and 9(d). This observation thus suggested that part of the Si_{0.6}Ge_{0.4} layer was completely strained when $LT_2 \leq 200$ °C, while the rest of it was strain-relaxed. The amount of strained Si_{0.6}Ge_{0.4} also decreased as decreasing LT_2 . Considering the fact that the epitaxial growth was generally maintained throughout the entire growth process according to RHEED experiments, a possible explanation is that the strained Si_{0.6}Ge_{0.4} was located near the LT-Si/LT-Si_{0.6}Ge_{0.4} interface, the relaxed part near the sample top surface, and the strain relaxation took place between these two parts within the Si_{0.6}Ge_{0.4} layer.

The relaxation of the Si_{0.6}Ge_{0.4} layer, together with the corresponding surface roughness r.m.s values for all samples in the S2 series, is summarized in Fig. 10. As a reference, data from the S1-A-400 sample were also included to present the growth condition with $LT_2 = 550$ °C. One can see that when LT_2 was in the range from 550 to 300 °C, the LT-Si_{0.6}Ge_{0.4} buffer generally had no significant influence on the final surface roughness and relaxation condition, while only a trend of slight decrease in the relaxation was observed. On the other hand, a dramatic enhancement in relaxation and suppression in surface roughness, both by a factor of ~ 2 , happened when LT_2 reached 200 °C. Note that this high relaxation degree of $\sim 80\%$ was only obtained when the total Si_{0.6}Ge_{0.4} layer thickness increased to ~ 150 nm in sample series S1-B, but with over two times higher surface roughness. Further decreasing LT_2 to < 200 °C, both the relaxation and the surface roughness were increased, ending up with $\sim 100\%$ relaxation and a very high surface roughness r.m.s value of ~ 5 nm at $LT_2 = 50$ °C. The general trend

FIG. 11. Bright field XTEM micrographs of [(a) and (b)] S2-200 sample and [(c) and (d)] S2-50 sample.

shown in Fig. 10 for our study was highly consistent with the results reported by Myronov and Shiraki in Ref. 20 using a similar growth scheme for Si_{0.34}Ge_{0.66}. A dramatic relaxation increase accompanied by a surface roughness decrease at $LT_2 = 200$ °C was observed in their study even though the layer thickness and the Ge composition of the SiGe layer were rather different in their case.

Figure 11 shows the XTEM images of the S2-200 and S2-50 samples, in which a significant difference in terms of dislocation distribution and microstructure was evidenced for the samples with $LT_2 \leq 200$ °C. In Fig. 11(a), a band of high density defects can be seen located near the LT-Si_{0.6}Ge_{0.4}/HT-Si_{0.6}Ge_{0.4} interface, from where many

FIG. 12. Dark field PVTEM micrographs of S2-200 sample with (a) $g=[220]$ and (b) $g=[\bar{2}20]$.

threading dislocations and $\{111\}$ stacking faults propagate into the HT-Si_{0.6}Ge_{0.4} layer and most of them reach the top surface [see Fig. 11(b) with a higher magnification]. Moreover, the lower part of the LT-Si_{0.6}Ge_{0.4} as well as the LT-Si region contained much less defects, which was rather different from Fig. 6(a). Only very few misfit dislocations and short segments of $\{111\}$ stacking faults were observed near the LT-Si/LT-Si_{0.6}Ge_{0.4} interface in a large viewing area. As LT₂ was decreased to 50 °C, almost the entire Si_{0.6}Ge_{0.4} was highly defective, while the LT-Si buffer was essentially defect-free, as shown in Figs. 11(c) and 11(d). The high magnification XTEM image in Fig. 11(d) clearly shows that the majority of defects were stacking faults on the $\{111\}$ planes. It also showed that the defective region was much closer to the LT-Si/LT-Si_{0.6}Ge_{0.4} interface, leaving only <2 nm of almost defect-free Si_{0.6}Ge_{0.4} above the LT-Si buffer. Even though the S2-200 sample showed a high relaxation and rather smooth surface, the defect density observed in XTEM was apparently too high ($>1 \times 10^7$ cm⁻²) for practical use.

Figures 12(a) and 12(b) are two dark field PVTEM images of the same area close to the LT-Si/LT-Si_{0.6}Ge_{0.4} interface for the S2-200 sample, with two orthogonal reflection vectors $g=[220]$ and $g=[\bar{2}20]$, respectively. In these images, a large number of defects were observed within the Si_{0.6}Ge_{0.4} layer. A similar type of irregular networks formed by randomly orientated short dislocations can be seen in both images. However, in the current imaging condition it was very difficult to identify the dislocation segments to be either misfit dislocations or threading dislocations due to their irregular shape and limited length. In addition, no regular cross-hatch dislocation network like in Fig. 6(c) was observed in the allowed viewing area of the specimen. The contrast visibility of dislocations oriented in random directions largely excluded the possibility for them to be of 90° pure-edge type. This irregular non-90° type dislocation network thus explained the absence of the cross-hatch surface morphology for the samples with LT₂ ≤ 200 °C in the AFM measurements.

IV. DISCUSSIONS

The measurement results of samples in the S2 series clearly revealed a growth-temperature-dependent transition when LT₂ decreased across 200 °C, characterized in three aspects: (1) a surface morphology change from cross-hatch to cross-hatch-free, (2) a significant strain-relaxation enhancement together with a surface roughness decrease, and

(3) the appearance of different defect distributions in terms of location and morphology. Although part of these observations was similar with that reported in Ref. 20, the experimental results therein on this type of transition were not very detailed, in particular no RHEED and TEM investigations were presented. Therefore, no specific explanation was provided for such a dramatic change in terms of the strain-relaxation mechanism.

Based on the results obtained using many different characterization techniques in this work, the strain-relaxation mechanism transition can be explained as follows. When LT₂ ≥ 300 °C, the strain-relaxation process was essentially the same as the one for samples without the LT-Si_{0.6}Ge_{0.4} buffer, i.e., through the nucleation and propagation of the conventional 60° misfit dislocations. In principle, lowering down LT₂ should increase the density of point defects and large open volume defects within the LT-Si_{0.6}Ge_{0.4} buffer. However, even at LT₂ = 300 °C those defect densities were not high enough to cause any fundamental change in the growth mode and material properties. The lattice-mismatch-induced strain energy was still accumulated at the LT-Si/LT-Si_{0.6}Ge_{0.4} interface, where the strain relaxation took place with the help of the LT-Si buffer upon the Si_{0.6}Ge_{0.4} layer thickness reaching a certain value. It was proposed and experimentally verified that the point/open volume defects in the LT-Si buffer played an important role in promoting the nucleation and propagation of dislocations for the overgrown Si_{1-x}Ge_x with $x \leq 0.3$.^{19,34–36} Since the substrate temperature LT₁ for the LT-Si buffer was the same for the samples grown in the S2 series, and the general quality of the buffer was similar according to RHEED observations, it may be expected for the LT₂ ≥ 300 °C cases that contribution by point defects in the LT-Si buffer to the dislocation nucleation and glide was, in principle, the same. On the other hand, using classical concept the dislocation nucleation rate and glide speed are both thermally activated kinetic processes, as which could be approximated by $\sim \exp(-E_a/k_B T)$,³⁷ where k_B is the Boltzmann constant, E_a is the activation energy for different processes, and T is temperature. When decreasing LT₂ from 550 to 300 °C, the total thermal energy given to the samples was reduced during the growth, which might explain the slight relaxation decrease shown in Fig. 10 for this LT₂ range.

With decreasing LT₂ to 200 °C and further below, the evolution of the *in situ* RHEED patterns during the deposition of the LT-Si_{0.6}Ge_{0.4} buffer was in an agreement with the reported observation corresponding to the ordered/disordered growth transition for Ge homoepitaxy on Ge(001) at a substrate temperature below 150 °C.³⁸ According to the defect accumulation and continuous breakdown models, there exists a continuous temperature-dependent increase in the concentration of lattice disorder.³⁹ Based on this concept and their experimental results, Bratland *et al.*³⁸ further defined seven specific surface stages during the epitaxy breakdown process: (1) atomic flat, (2) increased nucleation of surface 2D terraces, (3) formation of shallow islands and trenches, (4) development of deep cusps bounded by $\{111\}$ facets, (5) transformation of deep cusps into $\{111\}$ facets, (6) com-

mencement of amorphous growth at $\{111\}$ faceted cusps, and (7) complete amorphous growth.

In our case, the transition of the relaxation mechanism took place at $LT_2=200$ °C. Let us first consider what happened at this particular temperature. Based on the RHEED observations, the finishing surface of the LT-Si_{0.6}Ge_{0.4} can be described as in the condition somewhere between stage 4 and 5 in Bratland's definition. At that moment, the Si_{0.6}Ge_{0.4} layer thickness, in other words, the strain energy, was not yet large enough to trigger the relaxation at the LT-Si/LT-Si_{0.6}Ge_{0.4} interface, leaving the Si_{0.6}Ge_{0.4} just above that interface still completely strained. At the same time, however, the large stress located at the tips of surface cusps might already cause the nucleation of a high density of misfit dislocation segments at the surface vicinity.⁴⁰ During the final step where the HT-Si_{0.6}Ge_{0.4} capping layer was grown at a quickly elevated temperature, the HT-Si_{0.6}Ge_{0.4} would easily relax the strain on the pre-existing dislocation platform near the LT-Si_{0.6}Ge_{0.4}/HT-Si_{0.6}Ge_{0.4} interface, essentially without any contribution from the LT-Si buffer. This explained the coexisting features of both completely strained and highly relaxed Si_{0.6}Ge_{0.4} in HRXRD-RSMs.

Moreover, the propagation of short misfit dislocations by glide may either be blocked at the preformed facets or dissociated into partial dislocations through pre-existing $\{111\}$ stacking faults, resulting in a large number of threading dislocations and stacking faults running on the facet planes upward into the HT-Si_{0.6}Ge_{0.4}. Consequently, there was no formation of a regular network of long dislocations as shown in Fig. 6(c). The combination of these effects caused the irregular network of dislocation segments and the high density of extended defects observed in TEM studies. This also in turn led to a cross-hatch free surface morphology of low roughness observed in AFM, with shallow islands and pits on the final surface as the remnant of the rough starting surface for the HT-Si_{0.6}Ge_{0.4}. The significant enhancement of final relaxation degree for the HT-Si_{0.6}Ge_{0.4} can be explained by the high dislocation density since the total length of the dislocation per unit area could be still much larger than in the case where relaxation happened at the LT-Si/LT-Si_{0.6}Ge_{0.4} interface.

Further lowering of LT_2 led to ordered/disordered growth transition taking place earlier during the LT-Si_{0.6}Ge_{0.4} growth, so that the completely strained Si_{0.6}Ge_{0.4} material was thinner. When LT_2 eventually reached 50 °C, the LT-Si_{0.6}Ge_{0.4} surface was approximately at the transition stage 6 as defined before, in which amorphous growth just commenced. During the successive HT-Si_{0.6}Ge_{0.4} growth, the thin amorphous phase may recrystallize through solid phase epitaxy, resulting in a nearly 100% relaxation in the final Si_{0.6}Ge_{0.4} capping layer but with a high density of stacking faults as partial dislocations. Meanwhile, at such a low temperature, the very rough and faceted surface introduced at the initial stage by the ordered/disordered growth transition could not be recovered by the capping growth, so that the final surface roughness was the highest among the whole S2 sample series.

V. CONCLUSION

In conclusion, the overall experimental results thus indicate that a high degree of strain relaxation together with a low surface roughness could be obtained for a thin Si_{0.6}Ge_{0.4} layer, which was associated with a certain onset stage of the ordered/disordered growth transition during the deposition of LT-Si_{0.6}Ge_{0.4}. It was explained that the formation of cusps at this particular stage played an important role in promoting the nucleation of misfit dislocation segments at the surface vicinity that largely facilitated the strain relaxation. As long as the threading dislocation density can be controlled at a lower value, this double-LT-buffer variable-growth-temperature growth scheme could be a very promising technique to fabricate thin SiGe VSSs with Ge content up to 50 at. %. Or in another way, the technique may be useful for supplying a highly relaxed thin SiGe buffer as the template for further growth of the VS layer with a higher Ge fraction and an improved overall quality.

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