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ON REDUCTION OF SUBSTRATE NOISE IN MIXED-SIGNAL CIRCUITS

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On Reduction of Substrate Noise in Mixed-Signal Circuits

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ABSTRACT

Microelectronics is heading towards larger and larger systems implemented on a single chip. In wireless communication equipment, e.g., cellular phones, handheld computers etc., both analog and digital circuits are required. If several integrated circuits (ICs) are used in a system, a large amount of the power is consumed by the communication between the ICs. Furthermore, the communication between ICs is slow compared with on-chip communication. Therefore, it is favorable to integrate the whole system on a single chip, which is the objective in the system-on-chip (SoC) approach.

In a mixed-signal SoC, analog and digital circuits share the same chip. When digital circuits are switching, they produce noise that is spread through the silicon substrate to other circuits. This noise is known as substrate noise. The performance of sensitive analog circuits is degraded by the substrate noise in terms of, e.g., lower signal-to-noise ratio and lower spurious-free dynamic range. Another problem is the design of the clock distribution net, which is challenging in terms of obtaining low power consumption, sharp clock edges, and low simultaneous switching noise.

In this thesis, a noise reduction strategy that focus on reducing the amount of noise produced in digital clock buffers, is presented. The strategy is to use a clock with long rise and fall times. It is also used to relax the constraints on the clock distribution net, which also reduce the design effort. Measurements on a test chip show that the strategy can be implemented in an IC with low cost in terms of speed and power consumption. Comparisons between substrate coupling in silicon-on-insulator (SOI) and conventional bulk technology are made using simple models. The objective here is to get an understanding of how the substrate coupling differs in SOI from the bulk technology. The results show that the SOI has less substrate coupling when no guard band is used, up to a certain frequency that is highly dependent of the chip structure. When a guard band is introduced in one of the analyzed test structures, the bulk resulted in much higher attenuation compared with SOI. An on-chip measurement circuit aiming at measuring simultaneous switching noise has also been designed in a 0.13 μm SOI process.

ABBREVIATIONS

ADC	analog to digital converter
BGA	ball grid array
CBL	current balanced logic
C-CBL	complementary current balanced logic
CMOS	complementary metal-oxide-semiconductor
CSL	current steering logic
CSP	chip size package
DAC	digital to analog converter
DIL	dual in line
FEM	finite element method
IC	integrated circuit
IEEE	Institute of electrical and electronics engineers
JLCC	J-leaded chip carrier
LVDS	low-voltage differential signaling
MCM	multi-chip module
mil	milli-inch (1 mil = 0.0254 mm)
MOSFET	metal-oxide-semiconductor field-effect transistor
NMOS	negative channel metal-oxide-semiconductor
PCB	printed circuit board
PGA	pin grid array
PLCC	plastic leaded chip carrier
PLL	phase locked loop
PMOS	positive channel metal-oxide-semiconductor

PSRR	power supply rejection ratio
QFP	quad flat package
SFDR	spurious-free dynamic range
SNR	signal-to-noise ratio
SoC	system-on-chip
SOI	silicon on insulator
SSN	simultaneous switching noise
n	negatively doped silicon
p	positively doped silicon
n⁺	heavily negatively doped silicon
p⁺	heavily positively doped silicon
n⁻	lightly negatively doped silicon
p⁻	lightly positively doped silicon

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1

INTRODUCTION

This chapter gives the motivation for this thesis work together with a brief presentation of the main contributions. The organization of this thesis is also described.

1.1 Motivation

The development of microelectronics is heading towards integrating larger and larger systems on a single chip. In wireless communication equipment, e.g., cellular phones, handheld computers etc., both analog and digital parts are required. A circuit containing both analog and digital parts is referred to as a mixed-signal circuit. The operation time of portable equipment depends on the capacity of the battery and the power consumption. The capacity of a battery is limited by restriction of its size. Consequently, the power consumption should be minimized to achieve a maximal operation time. If several integrated circuits (ICs) are used in a system, a large amount of the power is consumed by the communication between the ICs. Furthermore, the communication between ICs is slow compared with on-chip communication. Therefore, it is favorable to integrate the whole system on a single chip, which is the objective in the system-on-chip (SoC) approach.

In mixed-signal SoC, signals are processed both in the digital and the analog domain. Unfortunately, integrating analog and digital parts on the same chip is cumbersome. One of the problems is that the digital circuits produce noise that affects the analog circuits. When the digital circuits are switching, they produce current spikes on the power supply lines. The current spikes together with the interconnect impedance between on-chip and off-chip, result in voltage fluctuations on the on-chip power supply lines. These voltage fluctuations are known as simultaneous switching noise (SSN). The noise produced in the digital circuits is spread through the silicon substrate to other circuits. The substrate noise degrades the performance of sensitive analog

circuits in terms of, e.g., lower signal-to-noise ratio (SNR) and lower spurious-free dynamic range (SFDR).

The complementary metal-oxide-semiconductor (CMOS) bulk technology has during the last decades been the dominating technology in many areas owing to its high cost effectiveness in comparison with other technologies. The silicon-on-insulator (SOI) CMOS has during the recent years become an increasingly interesting technology. The manufacturing cost of SOI is still higher than for bulk, but the relative difference in cost has decreased during the last years. The use of SOI is expected to increase in the future. In SOI, the active area is a thin-film of silicon, which is isolated from the substrate by a buried layer (e.g., silicon oxide). Isolating sensitive circuits using SOI in mixed-signal circuits may seem to be a very good idea, but the isolating layer is not a perfect insulator. The parasitic capacitance of the silicon oxide layer yields low impedance for high frequencies. Therefore, only low frequency components of the substrate noise are effectively attenuated in SOI.

The design of a clock distribution network in a high performance digital IC is challenging in terms of obtaining low power consumption, low waveform degradation, low clock skew and low SSN. Generally, the clock edges must be sharp which require large clock buffers, repeaters, and wide interconnects. Therefore, the design effort of the clock distribution net is high.

1.2 Contributions

In this section, the contributions of this thesis work are briefly introduced.

A noise reduction strategy that focuses on reducing the amount of noise produced in digital clock buffers is presented in this thesis. The strategy is to use a clock with long rise and fall times. This approach reduces both the high frequency components of the clock signal and the current peaks produced in the power supply lines. A robust D flip-flop, earlier presented in [44], is designed and investigated to be used in a test chip intended for evaluation of the strategy. Some considerations of how to design the D flip-flop are presented. Timing characteristics are presented for a wide range of fall times. The strategy to use long rise and fall times of the clock signal is also used to relax the constraints on the clock distribution net. With this method the design effort of the clock distribution net can be reduced.

A test chip has been designed and manufactured in a 0.35 μm CMOS process to evaluate the clocking strategy. The test chip contains two analog filters and

a digital filter. The digital filter has successfully been evaluated, showing that it is possible to use the clocking strategy in a real implementation. However, the noise reduction efficiency of using the strategy has not yet been thoroughly evaluated.

Comparisons between substrate coupling in SOI and conventional bulk are made by the use of simple models. The goal is to get an understanding of how SOI differs from bulk regarding the substrate coupling. The used models of the substrate are based on results achieved from the tool FEMLAB.

An on-chip measurement circuit aiming at measuring SSN has been designed and implemented in a 0.13 μm SOI CMOS process. A variable-reference comparator is used to capture the waveform of a periodic signal. Several passes are made where the waveform is compared with a different reference level in each pass. The comparator output is stored in a memory and is used to reconstruct the waveform when the capture is completed.

This thesis work has resulted in the papers [5]-[12], where [6], [9], [10], and [12] are appended in this thesis (paper I-IV). A paper manuscript is also appended (paper V).

1.3 Thesis Outline

In chapter 2, an introduction to substrate noise is given where the cause of substrate noise is explained. Examples of how analog circuits can be affected are also given. Substrate modeling is discussed in chapter 3. Examples of substrate noise reduction methods are given in chapter 4. The five appended papers are briefly presented in chapter 5. Finally, the papers are appended.

2

SUBSTRATE NOISE IN MIXED-SIGNAL CIRCUITS

In this chapter an introduction to substrate noise in mixed-signal circuits is given. First, a few examples are given of how analog circuits are affected by substrate noise that originates from digital circuits. Then, noise injection and noise reception mechanisms are discussed.

2.1 Substrate noise issues in mixed-signal circuits

In mixed-signal ICs both analog and digital circuits share the same substrate. When a digital circuit is operating, the voltages in the circuit nodes change rapidly levels and switching noise is produced. The noise is spread through the substrate and is received by other circuits. This noise is referred to as substrate noise. The performance of sensitive analog circuits is degraded by the substrate noise. Below, examples of how analog circuits are affected by substrate noise are given.

In a flash analog to digital converter (ADC), both analog and digital circuits are commonly integrated on the same chip. An N -bit flash ADC consists of $N - 1$ comparators where the outputs are connected to a digital circuit that converts the thermometer encoded output to a binary representation. One problem here is that the digital circuits generate substrate noise that disturbs the comparators, which can result in false output values [38]. The risk of false output values is especially high for the comparators with reference levels near the input level. When comparators have false outputs the ADC yields a reduced number of effective bits.

Substrate noise can also affect circuits used for synchronization, e.g., phase locked loop (PLL) circuits. The substrate noise is orders of magnitude larger than device noise in high-speed mixed-signal circuits [22]. The substrate

noise results in an uncertainty of the phase (i.e., jitter) of the synchronization signal. The jitter degrades the performance of all circuits that are connected to the PLL. In digital to analog converters, clock jitter results in a higher noise floor (i.e., lower SNR) and a distorted output signal giving a lower spurious-free dynamic range (SFDR) [3].

The effects of substrate noise in an analog differential architecture are analyzed in [30]. Here, a model of differential architecture is used, from where two interesting conclusions are drawn. The frequency components of differential noise appear directly at the analog output, but scaled with some gain factor. Common-mode noise is intermodulated with the differential analog input. Therefore, a frequency component that lays outside the analog signal band may, due to the intermodulation, fall into the analog signal band at the analog output.

2.2 Simultaneous switching noise

The parasitic inductance in the power supply interconnects between on-chip and off-chip, plays a big role in ICs. When digital circuits are switching, large current peaks are produced. The current peaks together with the parasitic inductance generate voltage drops on the on-chip power supply voltage. The voltage drop is

$$v_L(t) = L_{eff} \frac{di}{dt}, \quad (2.1)$$

where L_{eff} is the effective parasitic inductance of the power supply current path. To minimize the voltage drop the inductance is a target of minimization. Parasitic capacitances and typically also decoupling capacitors are present between the on-chip positive power supply node and the ground node. The sum of these capacitances may be modeled as a lumped capacitor C_{eff} . The capacitance C_{eff} together with the parasitic inductance L_{eff} form a resonance circuit with the resonance frequency

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{eff}C_{eff}}}. \quad (2.2)$$

When a current peak occur in the power supply, a damped voltage oscillation is seen [32]. This voltage fluctuation is known as simultaneous switching noise (SSN). On-chip decoupling capacitors are commonly used to form low impedance paths for reducing voltage fluctuations. When a decoupling capacitor is added, the SSN can be attenuated, but the added capacitor also lowers the resonance frequency as seen in (2.2). On-chip decoupling has earlier commonly been added as a lumped capacitor. Now, with circuits operating with higher frequencies it is preferable to distribute the decoupling capacitors over the whole circuit [3]. In the past, digital ICs was normally designed so that the resonance frequency of the on-chip power supply was well above the clock frequency to prevent an oscillation to grow during the clock cycles. Now, it is common with designs where the resonant frequency is well below the clock frequency. To prevent oscillations to grow, e.g., damping techniques based on adding resistance can be used [32] [27].

In digital designs, SSN can result in malfunction or degraded performance. In mixed-signal circuits the performance of analog circuits is degraded by the SSN that is spread through the substrate [4]. When a digital circuit is switching, the waveform and the frequency content of the power supply voltage are highly data dependent. This dependency is due to that the number of produced current peaks and the distribution of them in time, as well as the values of di/dt , depends on which circuits that are switching and when they are switching. The value of di/dt is in fact not only dependent on the switching circuits, but also on the impedance in the current path. In practice, if the number of simultaneous switching circuits is increased to the double, the SSN may increase to less than the double of the original SSN, which can be observed in [34].

2.2.1 Inductance

Inductance for a linear medium is calculated as

$$L = \frac{\Phi}{I} \quad (2.3)$$

[16], where I is the current in a closed loop and Φ is the magnetic flux through the area within the loop. Inductance can be divided into three contributions. The first is the internal inductance L_{int} , the second is the external L_{ext} , and the third is the mutual inductance L_{mutual} . The internal inductance is within the conductor. The external originates from the magnetic flux in within the closed loop. Mutual inductance comes from neighboring

magnetic fluxes that interact with the flux within the loop. The mutual inductance can either increase or decrease the effective inductance. The sum of the internal and the external inductance is often referred as self-inductance,

$$L_{self} = L_{int} + L_{ext}. \quad (2.4)$$

The sum of the self-inductance and the mutual inductance is referred to as the effective inductance of the current path,

$$L_{eff} = L_{int} + L_{ext} + \sum_j L_{mutual(j)}. \quad (2.5)$$

2.2.2 Inductance in power supply lines

In this section the inductance of wires are calculated from simplified examples. The wires are here assumed to be used for connecting a chip to a power supply.

Two wires in parallel

In Fig. 2.1, two wires with radius a , and distance d , are running in parallel. The wires are assumed to connect a chip to a power supply. To simplify calculations, the lengths of the wires are assumed to be long in comparison with the distance d . The currents are equal in magnitude in both wires but with opposite direction.

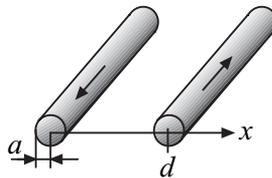


Figure 2.1: Two wires running in parallel.

The internal inductance per unit length is independent of the radius of the conductor and can be shown to be

$$L'_{int} = \frac{\mu_0}{8\pi} \quad (2.6)$$

[16], where $\mu_0 = 4\pi \cdot 10^{-7}$ H/m is the permeability of free space. Consequently, the internal inductance in the current path of the two wires is $L'_{int} = 0.1$ nH/mm. The external flux linkage, which is the total flux in the area in between the wires, is per unit length

$$\Phi' = \int_{s'} \mathbf{B} \cdot d\mathbf{s}' = \frac{\mu_0 I}{2\pi} \int_a^{(d-a)} \left(\frac{1}{x} + \frac{1}{d-x} \right) dx = \frac{\mu_0 I}{\pi} \ln\left(\frac{d}{a} - 1\right), \quad (2.7)$$

where s' is the area in between the wires. Hence, the external inductance per unit length can be expressed as

$$L'_{int} = \frac{\Phi'}{I} = \frac{\mu_0}{\pi} \ln\left(\frac{d}{a} - 1\right). \quad (2.8)$$

Hence, the total self-inductance per unit length of the two wires is equal to

$$L'_{self} = \frac{\mu_0}{\pi} \left(\frac{1}{4} + \ln\left(\frac{d}{a} - 1\right) \right). \quad (2.9)$$

In (2.9), it is seen that the ratio between the distance d and the radius a is critical. The self-inductance can be minimized by placing the interconnects as close to each other as possible.

Two pairs of wires

An interesting question is how the total inductance is affected when two pairs of interconnects are used instead of one pair of interconnects. If the distance between the two pairs of interconnects is large, the mutual inductance can be neglected. Consequently, the total effective inductance is simply the half of that in (2.9).

Four wires in parallel: First configuration

In Fig. 2.2, two pairs of interconnects that are placed adjacent to each other are shown. The distance between the interconnects is d and their radius is a . The interconnects labeled 1 and 3 are connected so that they have the same current direction. The interconnects labeled 2 and 4 are connected so that the currents have the opposite direction with respect to interconnects 1 and 3.

Owing to the symmetry the currents in the two outermost interconnects are equal. For the same reason, the currents in the two innermost interconnects

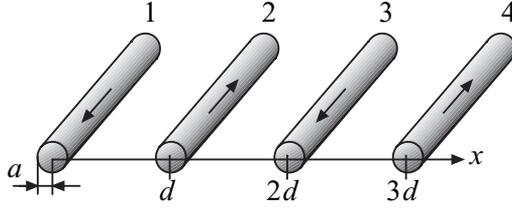


Figure 2.2: Four wires running in parallel.

are equal. Hence, we have two closed current loops with the internal wire distances of d and $3d$, respectively. The self-inductance per length unit of the inner current path and the outer current path are denoted L'_1 and L'_2 , respectively. Hence,

$$L'_1 = \frac{\mu_0}{\pi} \left(\frac{1}{4} + \ln \left(\frac{d}{a} - 1 \right) \right) \quad (2.10)$$

and

$$L'_2 = \frac{\mu_0}{\pi} \left(\frac{1}{4} + \ln \left(\frac{3d}{a} - 1 \right) \right). \quad (2.11)$$

Owing to the symmetry, the mutual inductance per unit length of the two loops may be calculated as

$$L'_{12} = \frac{1}{I} \int_{s'_{12}} \mathbf{B} \cdot d\mathbf{s}'_{12} = -\frac{\mu_0}{\pi} \int_{(d+a)}^{(2d-a)} \frac{1}{x} dx = -\frac{\mu_0}{\pi} \ln \left(\frac{2d/a - 1}{d/a + 1} \right). \quad (2.12)$$

The effective inductance per unit length of the paths are

$$L'_{1eff} = \frac{\mu_0}{\pi} \left[\frac{1}{4} + \ln \left(\frac{d}{a} - 1 \right) - \ln \left(\frac{2d/a - 1}{d/a + 1} \right) \right] \quad (2.13)$$

and

$$L'_{2eff} = \frac{\mu_0}{\pi} \left[\frac{1}{4} + \ln \left(\frac{3d-a}{a} \right) - \ln \left(\frac{2d/a - 1}{d/a + 1} \right) \right]. \quad (2.14)$$

The effective inductance of the four wires corresponds to two inductors in parallel with the value of L'_{1eff} and L'_{2eff} , respectively. Hence, the effective inductance per unit length of the four interconnects is

$$L'_{eff} = \frac{L'_{1eff}L'_{2eff}}{L'_{1eff} + L'_{2eff}}. \quad (2.15)$$

Four wires in parallel: Second configuration

Another configuration is shown in Fig. 2.3. Here, the interconnects labeled 1 and 2 are connected so that they have the same current direction. The interconnects labeled 3 and 4 are connected so that their currents have the opposite direction with respect to the currents in wire 1 and 2. We can solve the problem in the same way as the previous one, except that we have to consider that the current direction of the inner loop is changed. Therefore, we can reuse the previous calculations in (2.10) to (2.15) with the single exception that the sign in (2.12) is changed.

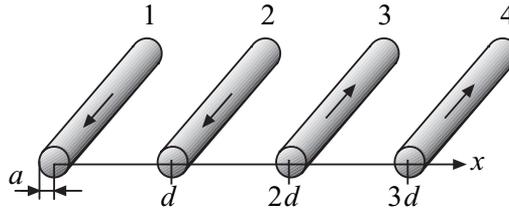


Figure 2.3: Four wires running in parallel: Second configuration.

In Table 2.1, the effective inductances are shown for the three cases corresponding to the illustrations in Fig. 2.1, Fig. 2.2, and Fig. 2.3, respectively. Three different values of d/a are used. It is seen that the effective inductance is some less than half of the original when four wires are used as in Fig. 2.2, instead of two wires as in Fig. 2.1. The effective inductance is significantly larger when using the assignment in Fig. 2.3 compared with the effective inductance for the assignment shown in Fig. 2.2. Hence, the effective inductance depends not only on the number of interconnects, but also on how the interconnects are placed. Consequently, doubling the number of pins for a power supply does not automatically result in an inductance reduced to the half of the original. However, it is a good strategy to place power supply interconnects so that the currents are in opposite directions in adjacent interconnects.

Inductance (nH/mm)			
	$d/a = 10$	$d/a = 20$	$d/a = 100$
Wires as in Fig. 2.1	0.98	1.28	1.94
Wires as in Fig. 2.2	0.47	0.61	0.93
Wires as in Fig. 2.3	0.69	0.86	1.21
Mutual inductance (Fig. 2.2 and Fig. 2.2)	0.219	0.248	0.271

Table 2.1: Effective inductance of current paths for three different examples and mutual inductance for the cases where four wires are used.

2.2.3 Skin effect

For high frequencies, the current in a conductor tends to be distributed in the outer area instead of being evenly distributed [16]. This results in higher resistivity due to the decreased conducting area. However, the internal inductance decreases for these frequencies, but still the inductance may be dominated by the external inductance formed by the current loop. Therefore, the effect of a decreased internal inductance may be small.

2.2.4 On-chip power supply distribution net

Even if the parasitics in the on-chip power supply distribution net tends to be rather small, they can still affect the on-chip SSN. The impedance from on-chip to off-chip can be made small if an advanced package is used in conjunction with many pins dedicated for the power supply. For high frequencies it is required to design the on-chip power supply distribution net with the emphasis on low inductance, low resistance, and sufficiently large decoupling capacitance. The need for carefully designed on-chip power supply distribution nets is expected to increase with technology scaling [29].

2.3 Packaging

The impedance from off-chip to on-chip differs between different types of packages. Generally, the inductive part of the impedance is the critical part. The lower inductance, the lower is the resulting power supply voltage drop for a given di/dt . Consequently, the choice of package is very important when considering SSN [19]. During the evolution of microelectronics, especially of high performance processors, the demand of low impedance packages has increased and have driven the development to low impedance packages.

A few distinctions between different packages can be made when considering how the package is connected to a printed circuit board (PCB). The package can either be put into a socket or directly soldered on the PCB. By putting the package into a socket instead of permanently soldering it (e.g., a processor on a motherboard), a higher flexibility is achieved with the cost of more parasitic capacitance and inductance. If the package is directly soldered on the PCB it could either be soldered on the top metal layer of the PCB (i.e., surface mounted) or mounted so that the pins of the package are put into holes through the PCB (i.e., pin-through-hole). The latter mounting style results in more parasitic inductance and capacitance. The required area on a PCB is smaller for a surface mounted package compared with a pin-through-hole package. Instead of packaging the silicon die it is also possible to connect the silicon die directly to a PCB via bonding wires or solder balls. One advantage is that the interconnects from the PCB to the chip can be kept very short and therefore the parasitics are low.

The dual in line (DIL) package has the pins on two opposite sides of a rectangular package. DIL packages is mounted with pin-through-hole. This kind of package has large parasitics both from the bonding wires and the long paths in the lead frame and the solder filled holes in the PCB. The lead pitch of a DIL package is typically 100 mil (1 mil = 0.0254 mm) or more. DIL is not suited for high performance circuits or when a small package area is required. Pin-through-hole packages have since the 1990s been less used in favor of surface mounted packages [20].

Plastic leaded chip carrier (PLCC) and J-leaded chip carrier (JLCC) are similar packages with some small difference in shape of pins and package corners. The pins are located at the sides of the rectangular package and the pitch is typically 50 mil. A PLCC or a JLCC package can either be put into a socket or surface mounted on a PCB. The parasitics of a JLCC or a PLCC package are smaller than in a DIL package. The parasitic inductance from on-

chip to off-chip differs between different pins. For example, consider the JLCC package shown in Fig. 2.4. Due to the distance between pin and pad, the pins in the middle have the least inductance and the pins at the corners have the largest inductance. Therefore, the pins in the middle should if possible be used for power supply lines. It is also important that pins dedicated for a higher frequency are not placed at the corners. The package shown in Fig. 2.4 was used for a chip designed during this thesis work. It has six adjacent pins dedicated for the power supply voltage to the digital core.

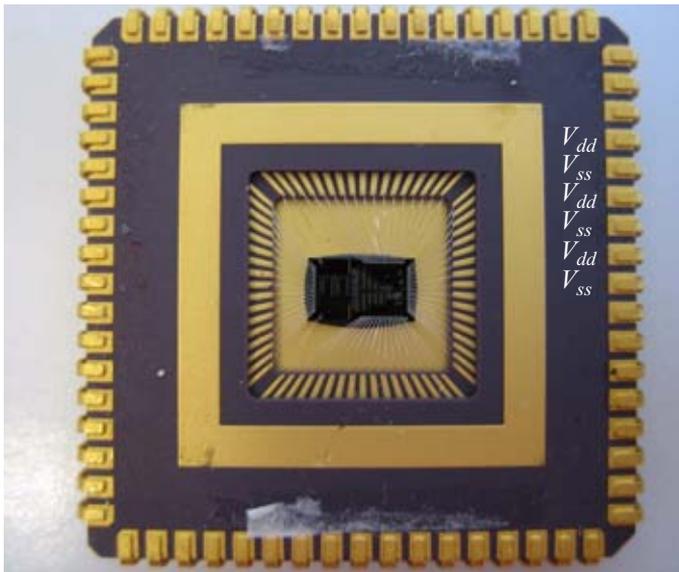


Figure 2.4: A test chip in a 68-pin JLCC package.

The Quad flat package (QFP) has the pins located at the perimeter of the package. QFP has less package size and smaller pin pitch than PLCC and JLCC [20]. Consequently, the parasitics are smaller in a QFP than in a PLCC or JLCC. QFPs can have up to about 300 pins.

A pin grid array (PGA) consists of an array of pins connected to a substrate on which the silicon die is attached with bonding wires or a flip-chip technique. This package is common for high performance microprocessors where a socket is used to enable a change of the processor. The pin count can be high and it is feasible to use more than 1000 pins.

Ball grid array (BGA) packages consists of an array of solder balls connected to a substrate on which the silicon die is attached with bonding wires or a flip-chip technique. The size of the package can be very small and the parasitics

are therefore also small. BGA packages are smaller in size and have less parasitics than PGA packages. If the package size is at most 20-30% larger than the chip, the package is said to be a chip-sized package (CSP).

In a multi-chip module (MCM) several silicon dies share the same package. In a conventional MCM, the dies are placed adjacent to each other and connected with bonding wires. Stacked chips are similar to MCM but with the difference that the chips are stacked on each other. With this approach it is possible to achieve a higher package density than with a conventional MCM.

2.4 Coupling through substrate contacts

The body of a transistor in a CMOS circuit is typically tied to a well defined bias voltage. Normally, the body of the PMOS transistor is connected to the positive power supply voltage and the body of the NMOS transistor is connected to ground. In a uniformly doped substrate, the body of the NMOS transistor is the substrate surrounding the transistor channel. The biasing contacts of the NMOS transistors are directly connected to the substrate.

Consider a design where a digital circuit and an analog circuit share the same substrate. In each gate in the digital circuit there is commonly at least one substrate contact. Therefore, the number of substrate contacts can be large in a digital design. Consequently, the digital ground has often a very low impedance to the substrate surface within the region of the digital circuit [21]. Therefore, any voltage fluctuation on the digital ground is also present in the substrate region of the digital circuit. This noise injection mechanism is normally the dominant one in digital integrated circuits [21]. If the substrate contacts in the analog circuit are connected directly to the analog ground, the substrate in the analog region has a low impedance to the analog ground. This causes the substrate noise, in the analog region, to be present on the analog ground. In this case, a sufficiently high power supply rejection ratio (PSRR) of the analog circuit is required to prevent lowered performance.

2.5 Capacitive coupling

The nodes in a circuit on a chip are capacitively coupled to the substrate by interconnects and parasitic pn-junctions. A capacitive coupling can both inject and receive substrate noise. However, the main contribution to substrate noise normally originates from the noise injected via substrate contacts [21].

2.5.1 Capacitive coupling of interconnects

On-chip interconnects are capacitively coupled to the substrate and adjacent interconnects as illustrated in Fig. 2.5. The capacitive coupling between the two interconnects and the substrate is modeled with three capacitors (C_1 , C_2 , and C_3). The capacitive coupling of an interconnect depends on, e.g., which metal layer the interconnect is located in, the length and the width of the interconnect and the distance to other objects (e.g., interconnects, diffusion areas, etc.). However, interconnects in the lower metal layers are more coupled to the substrate than interconnects in the upper metal layers.

Analog and digital circuits are normally placed in separate regions of the silicon. Therefore, direct coupling between analog and digital interconnects is seldom the case. The main coupling is through the substrate.

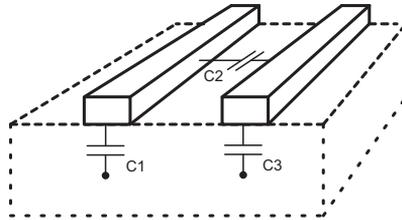


Figure 2.5: Capacitive coupling of two adjacent interconnects.

2.5.2 Capacitive coupling of pn-junctions

The different doping regions in MOSFETs form parasitic diodes. For example each pn-junction in an NMOS transistor forms a diode as illustrated in Fig. 2.6.

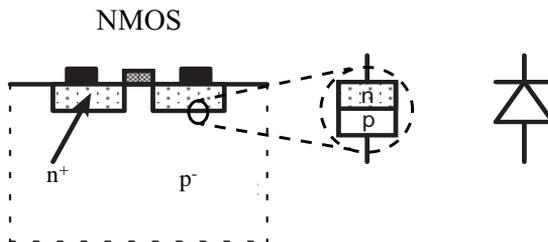


Figure 2.6: NMOS-transistor with parasitic pn-junctions.

In CMOS circuits the pn-junctions are normally reverse biased. The parasitic capacitance of a reversed biased pn-junction is nonlinear and voltage-dependent. This capacitance can be approximated to

$$C = \frac{A}{\left[\frac{2}{q\epsilon_{Si}} V_{bi} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) \right]^{1/2} \left(1 - \frac{V_D}{V_{bi}} \right)^m} \quad (2.16)$$

[4]. A is the area of the pn-junction, V_{bi} is the built in voltage, and V_D is the voltage over the diode. The doping levels for the p region and the n region are denoted as N_A and N_D , respectively. The gradient coefficient is denoted m , q is the elementary charge, and ϵ_{Si} is the permittivity of silicon. Due to the pn-junctions, both the drain and the source of a MOSFET are capacitively coupled to the bulk in CMOS circuits.

2.6 Body effect of MOSFET transistors

MOSFETs have four terminals as illustrated in Fig. 2.7. The drain current is mainly controlled by the gate source voltage. In analog circuits implemented in CMOS most of the transistors are commonly biased in the saturation region.

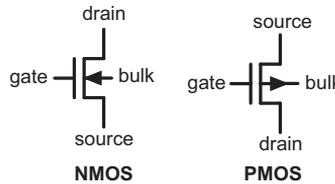


Figure 2.7: Symbols for NMOS and PMOS transistors.

A first order approximation of the drain current of a long channel NMOS transistor in the saturation region is

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{tn})^2 (1 + \lambda V_{DS}) \quad (2.17)$$

$$V_{tn} = V_{tn0} + \gamma (\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}). \quad (2.18)$$

In (2.17) and (2.18) it is seen that the drain current is affected by the threshold voltage, which is dependent of the source body voltage. This effect is known as the body effect. Any voltage fluctuation in the body of a circuit can due to the body effect result in a drain current fluctuation. Hence, the body effect in conjunction with substrate noise may degrade the performance of analog circuits.

2.7 Output drivers

To drive a digital output of an IC, cascaded inverters are commonly used as a driver. The output load consists of the parasitic capacitance of the bonding pad, the inductance and capacitance of the interconnect from on-chip to off-chip and the load on the PCB (e.g., wire trace plus the input of another IC). The current required to charge or discharge an off-chip load can be large, especially in the case of a high-speed communication. Consequently, the output drivers of a digital circuit generally produce a considerable amount of the total SSN [42]. Normally, the power supply lines for the output buffers are separated from the power supply lines for the chip core. The current paths of the output drivers differ much from the paths of the power supply to the chip core. The current path of a single ended output buffer is data dependent. While charging, the current path is through the positive on-chip power supply line and through the output load. Here, the current through the on-chip ground line is approximately zero. While discharging, the current path is through the ground supply line and through the output load. The currents in the power line and the ground line between the chip core and the PCB are always approximately equal. Therefore, the assignment of pins for power supply of single ended output buffers is more complicated than for the chip core. However, if a differential signaling is used for an output, the current path is always through the differential pair of interconnects.

2.8 Printed Circuit Board

Here a few aspects of the PCB design are discussed. The design of the printed circuit board is critical considering the switching noise. The PCB should provide stable power supply voltages where the voltage fluctuations are small.

2.8.1 Decoupling capacitor

A decoupling capacitor is commonly used to form a low impedance path for fluctuations on the power supply lines. With the use of decoupling capacitors the SSN on the PCB can be lowered. A rule of thumb of the placement of decoupling capacitors is that the higher resonant frequency a capacitor has, the closer to the IC it should be placed. An electrolyte capacitor, may be placed at a longer distance from the IC than a small surface mounted ceramic capacitor. On the second test PCB used in this thesis work, 22 ceramic capacitors were mounted near the test chip to decouple the power supplies for the digital part.

2.8.2 Inductance

To keep inductance low, a well known guideline is to keep current loop areas as small as possible. For example, each bit line from a chip to another chip must have a close current return path, otherwise the inductance originating from the loop will add inductance that slows down the propagation of the signal. Ringing of signals can also be a problem that comes into play due to the inductance of the path. Another important aspect is the radiated magnetic field, which may interfere with other signals on the PCB. Generally, the larger loop area the larger is the radiated magnetic field [17].

One approach to ensure that each signal or power line has a nearby current return path is to use a so called ground plane, which is a whole or almost a whole metal layer dedicated for ground. To prevent coupling between ICs separate ground planes can be used on the PCB. However, ICs that communicates with each other must have their ground planes properly electrically connected. Otherwise, the signals from one IC may float with respect to another IC.

2.8.3 Power planes on PCB

To ensure that the power supply lines on the PCB has a low inductance, a power plane can be used in conjunction with a ground plane. If the planes are placed in adjacent metal layers a capacitor with a high resonance frequency is formed corresponding to a high quality factor. The second test PCB used in this thesis work has four metal layers. The top and the bottom metal layers are used as ground planes. The two intermediate layers are used as signal layers and power planes.

In a high performance PCB, special metal layers are dedicated for the power supply. Here, the distance between the power supply metal planes is much smaller than the distance between signal layers. The smaller distance increases the capacitance and reduces the parasitic inductance which ensures a higher quality of the achieved decoupling [20].

3

SUBSTRATE MODELING

To estimate the coupling between different regions on a chip, a substrate model is required. A substrate model based on Maxwell's equations is shown. The method for modeling substrate used in this thesis work is also demonstrated.

3.1 Modeling of different substrate types

In conventional bulk processes, either a heavily doped substrate with a lightly doped epitaxial layer on top or a uniformly lightly doped substrate is used [37]. The heavily doped substrate may be modeled with less effort than a lightly doped substrate. The heavily doped silicon can be approximated to a single node due to its high conductance [41]. Therefore, the noise in highly doped substrate tends to be approximately uniform. However, the lightly doped substrate requires a higher modeling effort.

3.2 A substrate model based on Maxwell's equations

To predict the coupling between circuits that is on the same chip a reliable substrate model is required. The substrate height dimension is not negligible with respect to the area of the silicon. Consequently, the model of the substrate must be based on the three dimensions of the substrate. The basic Maxwell's equations can be used to find equations that can describe the substrate. However, a closed form solution does not exist as soon as geometries of different doping levels are included in the substrate or if different layers of the substrate have different doping levels [4]. For this reason, the substrate is divided into a number of smaller elements where each element is assumed to have a constant doping level. Hence, each element has a constant resistivity and a constant permittivity. The equations can then be

solved so that a model of an element is achieved. If the magnetic field is ignored, a simplified form of Maxwell's equations may be used on each element [40]

$$\varepsilon \frac{\partial}{\partial t} (\nabla \bullet E) + \frac{1}{\rho} \nabla \bullet E = 0. \quad (3.1)$$

E is the electrical field, ρ the resistivity, and ε is the permittivity of the silicon within the element. A cube shaped element with the volume V and the side $2d$ is shown in Fig. 3.1. The closed surface of the cube is denoted S .

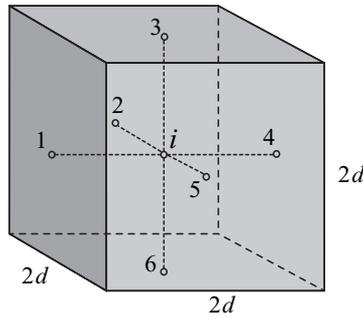


Figure 3.1: A cube shaped substrate element.

Gauss' law gives that the divergence of the electrical field in a point equals a constant [16]. Hence, the divergence in node i in the cube is

$$\nabla \bullet E = k. \quad (3.2)$$

We integrate $\nabla \bullet E$ over the volume V formed by the cube in Fig. 3.1, and then rewrite (3.2) as

$$\int_V \nabla \bullet E dV = \int_V k dV = 8d^3 k. \quad (3.3)$$

The divergence theorem [16] gives that

$$\int_V \nabla \bullet E dV = \int_S E dS. \quad (3.4)$$

Hence, (3.3) can be rewritten as

$$\frac{1}{8d^3} \int_S E dS = k. \quad (3.5)$$

Therefore,

$$\nabla \bullet E = \frac{1}{8d^3} \int_S E dS \quad (3.6)$$

The integral in (3.6) can be approximated as

$$\int_S E dS = \sum_{j=1}^6 E_{ij} 4d^2 \quad (3.7)$$

and the electrical field from node j to i can be approximated as

$$E_{ij} = \frac{V_i - V_j}{d/2} \quad (3.8)$$

[40]. Hence,

$$\nabla \bullet E = \frac{1}{8d^3} \sum_{j=1}^6 \frac{V_i - V_j}{d/2} 4d^2 = \sum_{j=1}^6 \frac{V_i - V_j}{d^2}. \quad (3.9)$$

Using (3.9) in (3.1) gives

$$\frac{1}{\rho} \sum_{j=1}^6 \frac{V_i - V_j}{d^2} + \epsilon \frac{\partial}{\partial t} \left(\sum_{j=1}^6 \frac{V_i - V_j}{d^2} \right) = 0. \quad (3.10)$$

We rewrite (3.10) as

$$\sum_{j=1}^6 \left[\frac{(V_i - V_j)}{R} + C \left(\frac{\partial V_i}{\partial t} - \frac{\partial V_j}{\partial t} \right) \right] = 0 \quad (3.11)$$

where $R = \rho/(2d)$ and $C = 2\epsilon d$ [40]. The resulting model is shown in Fig. 3.2, where each impedance from a surface to the middle node i , is

modeled as a resistor in parallel with a capacitor with the values of R and C , respectively. The expression in (3.11) corresponds to that the sum of the currents flowing into node i is zero.

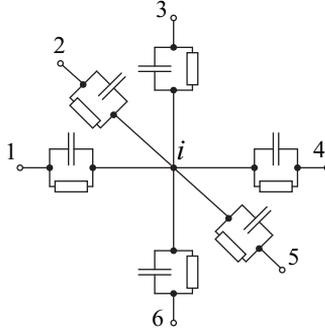


Figure 3.2: Model of a cube shaped substrate element.

When a substrate is divided into a number of elements, a mesh of resistors and capacitors is obtained. To achieve reliable results from the model, the mesh should be fine (i.e., small elements) in regions where the gradient of the doping level is high and also where the gradient of the electrical field is high. Due to the large number of nodes required in the model, it is not suited for hand calculations and therefore a simulator is required. By using a circuit simulator (e.g., SPICE) the coupling between different areas of the substrate can be analyzed. The areas of the substrate that are of interest are often called ports in the literature.

3.3 Substrate modeling with FEMLAB

Generally, the properties of a physical system can be described by partial differential equations as, e.g., in the previous section. A problem with this approach is that the equation system can be hard or impossible to solve analytically. In the finite element method (FEM) the objects are divided into a number of elements, where the equation system in each element can be numerically solved. The finite element method is used in the commercial tool FEMLAB [46], which can model and simulate physics in 3D. Here, a mesh of finite elements is generated and the partial differential equations of each element are then solved. In this thesis work FEMLAB was used to model lightly doped substrates.

3.3.1 Modeling example

In paper I and paper IV, FEMLAB is used to build models of substrates. In paper I, only the resistive coupling is considered (see section 3.4). In paper IV, both the resistive and the capacitive coupling are considered. The results achieved from FEMLAB are used to derive full models of the substrates consisting of resistors and capacitors. To demonstrate the used substrate modeling method, an example is given below.

Two circuits with surfaces of 50 by 50 μm located on a substrate is shown in Fig. 3.3. The substrate backside is assumed to be metallized. The silicon resistivity and the relative permittivity are assumed to be 20 Ωcm and 11.8, respectively. A mesh, of the substrate shown in Fig. 3.3, is generated using FEMLAB. The mesh is shown Fig. 3.4, where it can be seen that the mesh is made finer near the circuit areas than near the bottom of the substrate. The generated mesh consists of approximately $7 \cdot 10^4$ elements. To estimate the substrate coupling, a sinusoidal signal is applied on one of the circuits. The other circuit and the backside are grounded. In Fig. 3.5, the result of a simulation of the voltage potential in the generated mesh is shown. The currents (in complex form) obtained from the simulation are used to calculate the resistive and the capacitive coupling. A full model of the substrate coupling is shown in Fig. 3.6. Here, the capacitor and resistor values are $R_2 = 2.27 \text{ k}\Omega$, $R_3 = 6.31 \text{ k}\Omega$, $C_2 = 9.20 \text{ fF}$, and $C_3 = 3.31 \text{ fF}$.

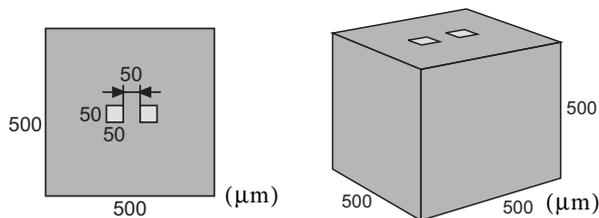


Figure 3.3: A lightly doped substrate with two circuit regions of 50 by 50 μm and a metallized backside.

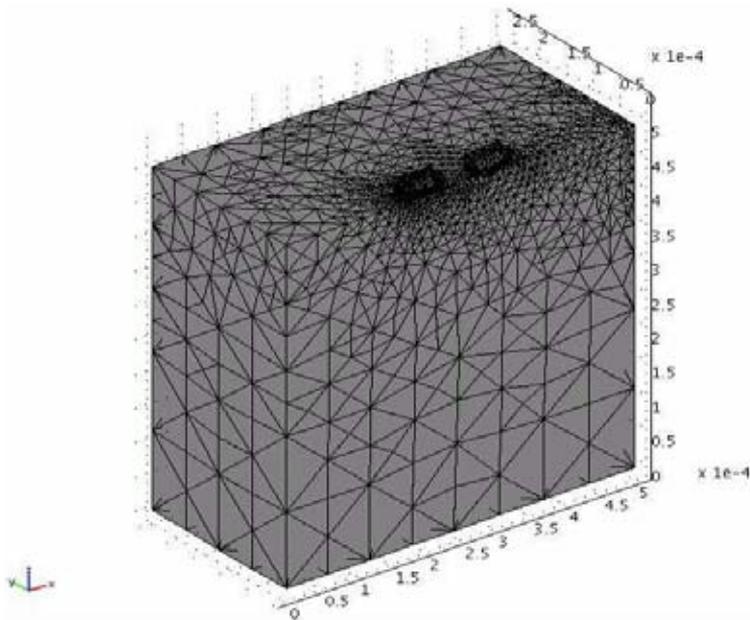


Figure 3.4: A generated mesh in FEMLAB.

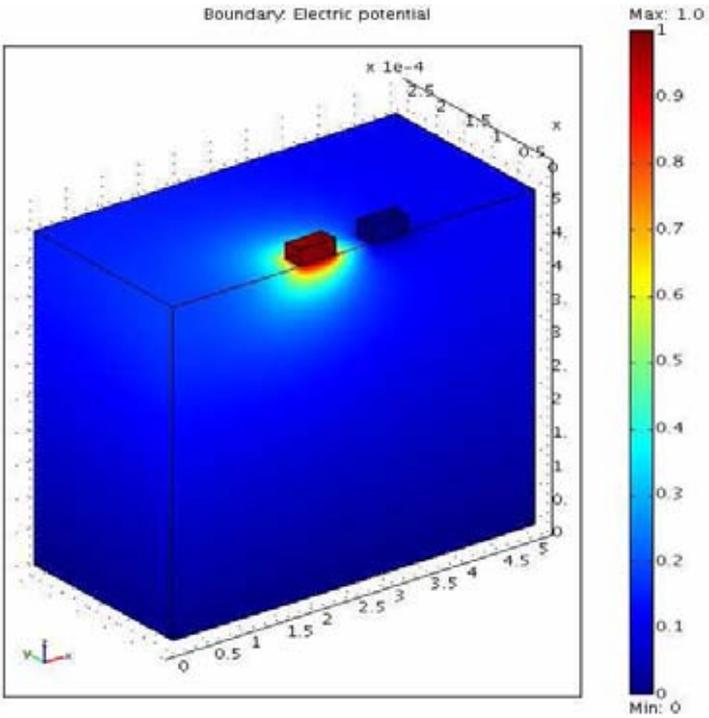


Figure 3.5: A visualized simulation result in FEMLAB.

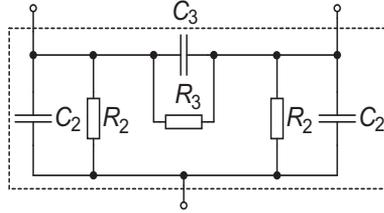


Figure 3.6: A full model of the capacitive and resistive coupling between the three nodes in Fig. 3.3.

3.4 Pure resistive substrate modeling

For low frequencies the substrate can be approximated as purely resistive, which is utilized in paper I. The substrate is mainly resistive for frequencies below the cut-off frequency

$$f_c = \frac{1}{2\pi\rho_{sub}\epsilon_{Si}} \quad (3.12)$$

where ρ_{sub} and ϵ_{Si} are the resistivity and the permittivity of the substrate, respectively [31]. Assuming a lightly doped substrate with a resistivity of $0.10 \Omega\text{m}$ leads according to (3.12) to that the substrate is mainly resistive for frequencies up to 15 GHz. If the capacitive coupling can be neglected the model is reduced to a resistive net. Consequently, the complexity of the net is reduced which may save simulation time.

4

SUBSTRATE NOISE REDUCTION METHODS

In this chapter an overview of noise reduction methods is given.

4.1 PCB with built in power supply decoupling

For high performance designs there are special PCBs with dedicated metal layers for the power supply. In this kind of PCB the distance between the power supply metal planes are much smaller than for the signal layers. This improves the amount of capacitance and decreases the parasitic inductance, which ensures a high quality of the decoupling. The same technique with power planes may also be used in the substrate of, e.g., a BGA package [18].

4.2 Low voltage differential signaling

Low-voltage differential signaling (LVDS) is an IEEE standard for digital signaling. This standard is mainly intended for high-speed communication between packages. By using low swing signaling (at most 400 mV) and also differential signaling the amount of radiated electromagnetic energy can be kept low [45]. The differential interface requires two dedicated pins for each signal. The shorter distance between the balanced interconnects, the lower is the effective inductance as described in section 2.2. At least four good properties are achieved with the LVDS compared with single ended signaling. First, with a lower effective inductance of the signal path, a higher data rate can be achieved. Second, a low inductance of the path yields a low magnetic flux through the loop, which results in a low radiated magnetic field. Third, with two signals making transitions with opposite polarities but equal values, the radiated electrical field is effectively reduced in comparison with a single ended signaling. The fourth is that, in a similar way as described in section

4.20, the differential signaling results in a higher noise rejection, which makes the signaling less sensitive for external noise.

One at least intuitively obvious cost of LVDS is the double number of required signal pins. In LVDS the current return path is always within the balanced pair. In the single ended case the current return path is normally via the ground pins. Consequently, single ended signaling requires a larger amount of ground pins than LVDS. The loop area is larger in single ended signaling. Hence, the maximum data rate is lower in single ended signaling than in LVDS.

4.3 Separate power supply lines

The power supply lines of digital circuits do always have voltage fluctuations during switching. Separate power supply lines are commonly used for digital and analog circuits to prevent the fluctuations from to be directly coupled to the analog circuits. Even if the power supply lines to an analog and a digital circuit originates from the same off-chip power supply source, it is still a good idea to separate them on chip. This is due to that higher impedance between the power supplies is achieved in this way. In the test chip used in this thesis work, separate power supply lines are used for the digital and the analog circuits.

4.4 Reduced power supply voltage

In [28] a mixed-signal test chip is evaluated. The chip contains a digital circuit and analog comparators. The experimental results show that when the power supply voltage is scaled down, the substrate noise is effectively reduced. Another gain is the reduced power consumption, which scales with V_{dd}^2 . The cost is the increased propagation delay, which may be compensated by, e.g., pipelining or interleaving [15]. Pipelining and interleaving both require some extra hardware, which also contributes to the noise. Hence, the gain of decreasing the power supply voltage on the substrate noise depends on what changes that has to be done in the architecture to still fulfill the requirement on speed.

4.5 Low impedance packaging

The choice of package is very important considering substrate noise. As described in section 2.2 the impedance differs between different types of packages. Generally, by choosing a low impedance package the amount of SSN is reduced. Instead of packaging the silicon die it is also possible to connect it directly to the PCB via bonding wires or solder balls. With this technique, the interconnects from the PCB to the silicon die can be kept very short and therefore the parasitics are low.

4.6 Separate packages

One method to avoid the substrate coupling is to separate the analog circuits from the digital circuits by simply placing them on separate chips in separate packages. Hence, the analog circuit does not suffer from the digital switching noise that is spread through the substrate. A drawback of using separate packages is that the communication between the packages consumes a considerable amount of power. To keep power consumption low, the number of packages should generally be kept as low as possible. The mounting area on a PCB increases as well when the number of packages is increased.

4.7 Multi Chip Module

In a multi-chip module (MCM) several silicon dies share the same package. With the use of an MCM it is possible to use separate silicon dies for, e.g., a sensitive analog circuit and a noisy digital circuit. In this way the substrate coupling is avoided. Another advantage is that the yield is larger for silicon dies of less area. In comparison with separate packages for analog and digital circuits the MCM yields lower power consumption and it occupies a smaller area on a PCB.

4.8 Lug pin

A lug pin is a wide pin that can be visualized as a number of adjacent leads in a leadframe where the spaces between the leads are filled with metal. The lug pin was intended to be a low impedance path for ground in leadframe

packages. The lug pin has low resistance, but the inductance is normally the critical part of the package impedance. However, compared with the case where power supply pins are placed so that the current flows are opposite in adjacent pins, the lug pin is not a good candidate for lowering SSN [35].

4.9 Double bonding

One technique that aims at reducing the impedance between on-chip and off-chip is double bonding. Instead of using one bonding wire from the on-chip pad to the off-chip interconnect (e.g., leadframe, a trace on pcb etc.) two bonding wires are used, which reduces the inductance [2]. Furthermore, the parasitic resistance is reduced to the half. This can be beneficial for high frequencies, where the resistance of a conductor increases with \sqrt{f} due to the skin effect [36].

4.10 On-chip decoupling

On-chip decoupling capacitors are commonly used to form low impedance paths for voltage fluctuations on the power supply lines. When a decoupling capacitance is added to digital power supply lines, the SSN can be drastically attenuated, but the added capacitance also lowers the resonance frequency. In the test chip used in this thesis work, the on-chip decoupling capacitor consists of regions where the different metal layers are used to form a capacitor. On-chip decoupling has earlier commonly been added as a single capacitor. Now, with circuits operating with higher frequencies it is preferable to distribute the decoupling over the whole circuit [3]. The decoupling may, e.g., be designed as a cell in a standard cell library or be included within each standard cell.

In [23], a simple circuit is used to eliminate the impedance peak at the resonance frequency of the on-chip power supply lines. The circuit consists of a resistor, a capacitor, and an inductance in series. The inductance and the capacitor are chosen so that the resonance frequency is placed at the same frequency as the impedance peak of the original power supply. In this way the original impedance peak can be removed. The resistor in the circuit makes it possible to avoid new peaks in the impedance characteristic, by carefully selecting a proper resistance.

4.11 Different clock latencies in different clock regions

In [13] a clock net is divided into four clock regions where each region has its individual and dedicated delay from the nominal clock. In this way the triggering clock edge appears at different time instances in the different regions preventing the switching of the circuits in respective region to start simultaneously. With this method, the resulting power supply current can be smoothed, which results in a lower SSN. Measurements on a test chip in [13] shows a reduction of SNN with more than a factor of 2. The technique may be effective if the timing constraints allow it to be used.

4.12 Timing and sizing of output buffers

Output buffers are main contributors to SSN. When an output change value the current peak can be high and dI/dt can be large yielding a high amount of SSN. To prevent output buffers from switching simultaneously the buffers may be designed with different propagation delays. This approach reduces the SSN. It is also important that the output buffers is not oversized yielding overly short propagation delay and rise and fall times. Oversized buffers yield more SSN.

4.13 Moving the frequency content of substrate noise

Instead of reducing the magnitude of the substrate noise it is in some cases possible to move the substrate noise to higher or lower frequencies. By moving the frequency components of the noise it may be possible to locate the critical components outside the analog signal band. However, even if the frequency components of the substrate noise is outside the signal band, the effects of the noise may still be seen in the signal band due to intermodulation as described in section 2.1.

4.14 Asynchronous circuits

In asynchronous circuits no clock is used. Due to the absence of a clock, asynchronous circuits have a favorable noise compared with synchronous circuits. The switching in asynchronous circuits tend to be more equally

distributed in time than in synchronous circuits. This results in a power supply current with smaller current peaks. In [14], one asynchronous and one synchronous processor are implemented in the same process technology. The circuit built using asynchronous logic yields very small peaks in the frequency spectra of the power supply current compared with the circuit built using synchronous logic.

4.15 Constant current logic

In constant current logic, the circuits are constructed with the target on making the power supply currents constant. The main idea is to steer currents so that only the paths change but not the magnitude of the currents. In practice, a constant current is impossible to achieve due to that the currents can not be perfectly balanced during switching.

In [1], simulations are made on extracted layouts of a conventional static on-chip, one current steering logic (CSL) circuit, one current balanced logic (CBL), and one complementary CBL (C-CBL). With the CMOS circuit as reference, the constant current logic circuits result in a noise reduction up to about 75%. The cost of this reduction is high in terms of higher power consumption, which may make the technique unsuitable for battery powered products. The constant current logic circuits also tend to occupy a larger silicon area than, e.g., static CMOS. However, if increased power consumption is afforded then this technique may be suitable.

4.16 Distance

One intuitively and straightforward approach to reduce the coupling between circuits is to place them with some extra distance in between. This is effective in lightly doped substrates where the impedance is significantly increased with the distance. The cost of increasing the distance between the circuits is the increased silicon area. In heavily doped substrates, increasing the distance between the circuits is inefficient as soon as the distance is more than four times larger than the thickness of the epitaxial layer [41]. This is due to that the p^+ layer has a relative high conductance and can therefore be approximated as single node. Consequently, the substrate noise is approximately uniform on the entire chip area [41]. The influence of distance on coupling is also briefly discussed in paper IV.

4.17 Guard ring

A guard ring provides a low impedance path to ground (or the positive supply), which lets the substrate currents to be lead to signal ground. Substrate noise can be reduced if a guard is inserted in between a noisy circuit and a noise sensitive circuit. If a lightly doped substrate is used, a guard can be effective. In the case of a heavily doped substrate the effect of guard rings is limited due to the highly conductive p^+ layer.

In CMOS processes a channel stop implant is normally used to prevent the substrate from forming a parasitic transistor channel [32]. However, the channel stop implant is highly doped and can be a significant part of the substrate coupling. By inserting an n -well in a p substrate the channel stop implant is interrupted by the higher resistivity of the n -well and the coupling is reduced [24].

A guard ring may consist of either p^+ substrate contacts tied to ground or n -wells tied to ground (or the positive supply). The effectiveness of p^+ substrate contacts is however better than n -well guards. With p^+ contacts, the guard is directly connected to the substrate. With an n -well as guard, the substrate region surrounding the guard is capacitively coupled to either ground or the positive supply. The impedance from the substrate via the pn-junction to the n -well and then through the n -well to the n^+ contact, is higher than the impedance from the substrate through the p^+ substrate contact. Therefore, the p^+ guard is to prefer but the channel stop implant should be interrupted by an n -well to reduce the substrate currents [24].

Separate pins should be dedicated for guards. Otherwise, the guards may increase the coupling between circuits. For example, if an analog guard ring is located some distance from the analog circuit and the guard is connected to the analog ground on-chip, then the noise at the location of the guard will easily be spread via the interconnects to the ground in the analog circuit.

In heavily doped substrates guard rings are ineffective for suppressing noise. The suppression that may occur when a guard is added mainly comes from that the interconnect impedance between on-chip and off-chip is decreased. A similar effect is achieved if the extra pins are dedicated for power supply instead of an area consuming guard.

In the test chip used in this thesis work, guard rings are used both for the digital circuit and the analog circuits. The guard rings have separate pins to achieve a low coupling between the guards.

4.18 Deep trench isolation

A deep trench isolation consists of a trench filled with undoped polysilicon. The trench serves as a high impedance wall in the substrate where any substrate current will be highly attenuated. The method has been proven to be effective up to 2 GHz in [39]. For frequencies above 2 GHz the isolation is degraded by the capacitive coupling through the trenches.

4.19 Silicon-on-insulator

In a silicon-on-insulator (SOI) technology a thin-film of silicon is placed on an isolating layer (e.g., silicon oxide) and under the isolating layer a substrate is used. With an ideal isolator no substrate coupling would exist in SOI. In reality, the isolator is not perfect and the thin film is capacitively coupled to the substrate. Therefore, substrate noise is effectively attenuated for low frequencies and higher frequencies are less attenuated [33]. The use of a thin-film of silicon instead of a conventional bulk results in reduced parasitic pn-junctions. The lower amount of parasitic capacitance yields faster and less power consuming circuits [26].

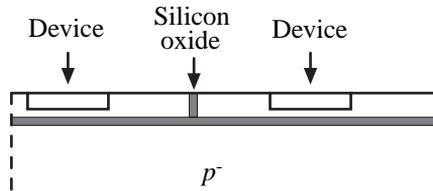


Figure 4.1: Silicon-on-insulator.

The effectiveness of increasing the distance between the circuits in SOI depends on what type of substrate that is used. Normally, a lightly doped substrate is used, which makes it possible to increase the impedance between two circuits by increasing the distance. Due to the isolating layer in SOI, guard bands can not be connected directly to the substrate as in the case of a bulk CMOS. In SOI, guard bands consist of regions where the thin-film is connected to ground. The parasitic capacitance between the thin film and the substrate is here acting as a decoupling capacitance. In paper IV, simplified comparisons between the substrate coupling in SOI and conventional bulk technology are made.

4.20 Differential architectures in analog circuits

In high performance analog circuits, fully differential signal paths are normally used. A high rejection of substrate noise can be achieved with this technique if the circuit is built in a symmetric manner. The symmetry of the circuit could in an ideal case result in that both signal paths are affected in the same way by the substrate noise. Hence, the noise is eliminated since only the difference between the signals is of interest in a differential architecture [25]. In reality, there are effects that limit the rejection of the substrate noise. For example, the differential signal paths on a fabricated chip are not equal due to component mismatches. The noise is not injected symmetrically due to asymmetries of the layout with respect to the noise propagation.

5

MAIN CONTRIBUTIONS

In this chapter the main contributions of the thesis work are presented together with brief introductions to the corresponding papers.

5.1 Strategy for reducing clock noise in mixed-signal ICs

Digital switching noise is of major concern in mixed-signal circuits due to the substrate coupling between circuits located on the same die. A significant noise source in this context is the digital clock network that generally has a high switching activity. Switching of the clock produces current peaks on the power supply lines causing SSN.

In paper I, we present a noise reduction strategy which focus on reducing the amount of digital switching noise that is produced due to clock buffers. The strategy is to use a clock with long rise and fall times. This strategy reduces both the high frequency components of the clock signal and the power supply current peaks produced by the clock buffers. Here, we use a special D flip-flop circuit that operates well with the clock. A test chip is designed where we can control the rise and fall time of the clock edges in a digital FIR filter, and measure the performance of a fifth-order analog active-RC filter. Simulations of a simple model of a substrate indicate that substrate noise with high frequencies are less attenuated than low frequencies. In this work an example shows that the longer rise and fall times of a digital buffer, the less substrate noise is seen in the analog region.

5.2 Design of circuits for a robust clocking scheme

The design of a clock distribution network in a digital IC is challenging in terms of obtaining low power consumption, low waveform degradation, low clock skew and low simultaneous switching noise. Generally, the clock edges must be sharp which normally require large clock buffers, repeaters, and wide interconnects.

In the work presented in paper II, we aim at reducing the design effort on the clock distribution net. This is done by using a clock buffer with reduced size and a D flip-flop circuit with relaxed constraints on the rise and fall times of the clock. With this approach, repeaters and wide interconnects in the clock distribution net are not required. Hence, the design effort of the clock distribution net is reduced. Some considerations of how to design a robust D flip-flop together with characteristics of the used D flip-flop are presented for a wide range of rise and fall times. According to simulations, the energy dissipation of the D flip-flop, implemented in a 0.35 μm process, increases with only 21% when the fall time of the clock was increased from 0.05 ns to 7.0 ns. Considering that smaller clock buffers can be used, there is a potential of power savings by using the suggested clocking strategy. Initial measurements on the test chip presented in paper I indicate that the strategy works.

5.3 Evaluation of a clocking strategy with relaxed constraints on clock edges

In the work presented in paper III, the strategy of using long rise and fall times on the clock to reduce the design effort is successfully evaluated throughout measurements on the fabricated test chip. The used test chip has earlier been presented in paper I and II. The actual rise and fall times of the clock on-chip, are estimated by measurements. The simulation and the measurement results of the clock edges show good agreement for long rise and fall times. The energy dissipation of the circuit increased 14% when the rise and fall times of the clock increased from 0.5 ns to 10 ns. The corresponding increase in propagation delay is less than 0.5 ns, i.e., an increase of 50% in propagation delay of the register. The results in this paper show that the clocking strategy works well.

5.4 Introduction to substrate noise in SOI CMOS ICs

In the SOI technology, the active area is a thin-film of silicon that is isolated from the substrate by a buried isolating layer (e.g., silicon oxide). The use of a thin-film instead of a conventional bulk results in smaller parasitic capacitances. This is mainly due to the less deep pn-junctions. The smaller parasitic capacitances yield faster and less power consuming circuits. Owing to the insulating layer, the coupling to the substrate is small for low frequencies.

In paper IV, simplified comparisons between the substrate coupling in SOI and conventional bulk technology are made. The focus is on the magnitude response from a digital circuit to an analog circuit. The results show that the SOI has less substrate coupling when no guard band is used, up to a certain frequency that is highly dependent of the chip structure. When a guard band is introduced in one of the analyzed test structures, the bulk resulted in much higher attenuation compared with SOI. One advantage of SOI is that a higher resistivity of the substrate can be used which increases the impedance of the substrate. Therefore, the substrate coupling is lowered up to the frequency where the capacitive coupling becomes dominant.

5.5 Programmable reference generator for on-chip measurements

SSN is generally the main contributor to substrate noise. Therefore, it is of interest to measure SSN in a digital circuit, e.g., when a SSN reduction method should be evaluated. To affect the digital circuit as little as possible an on-chip measurement circuit could be favorable.

In the work presented in paper V, we aim at measuring SSN with an on-chip measurement circuit. When a periodic signal is measured a simplified measurement circuit can be used. We use a variable-reference comparator to capture the waveform of a periodic signal. Several passes are made where the waveform is compared with a different reference level in each pass. The comparator output is stored in a memory and is used to reconstruct the waveform when the capture has completed. In this way it is possible to measure a waveform on-chip. A test chip has been designed in a 0.13 μm SOI CMOS process, and it is planned to be fabricated in a near future.

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Paper I

*A Strategy for Reducing Clock Noise
in Mixed-Signal Circuits*

E. Backenius, M. Vesterbacka, and R. Hägglund.

Proc. IEEE Midwest Symposium on Circuits and
Systems, Tulsa, Oklahoma, Aug. 2002.

A STRATEGY FOR REDUCING CLOCK NOISE IN MIXED-SIGNAL CIRCUITS

E. Backenius, M. Vesterbacka, and R. Hägglund

ABSTRACT

Digital switching noise is of major concern in mixed-signal circuits due to the coupling of the noise via a shared substrate to the analog circuits. A significant noise source in this context is the digital clock network that generally has a high switching activity. There is a large capacitive coupling between the clock network and the substrate. Switching of the clock produces current peaks causing simultaneous switching noise (SSN). Sharp clock edges yields a high frequency content of the clock signal and a large SSN. High frequency noise is less attenuated through the substrate than low frequencies due to the parasitic inductance of the interconnect from on-chip to off-chip.

In this work, we present a strategy that targets the problems with clock noise. The approach is to generate a clock with smooth edges, i.e. reducing both the high frequency components of the clock signal and the current peaks produced in the power supply. We use a special digital D flip-flop circuit that operates well with the clock. A test chip has been designed where we can control the rise and fall time of the clock edges in a digital FIR filter, and measure the performance of a fifth-order analog active-RC filter.

1. INTRODUCTION

A major problem in mixed-signal circuits is the noise injected into the analog circuits by the switching digital circuits, which is illustrated in Fig. 1. The noise is degrading the performance of the analog circuits [1]. In this paper we will present a strategy aiming at reducing the noise originating from the digital clock network. We will start by reviewing noise injection mechanisms, noise reception mechanisms and a few common techniques for reducing noise in mixed-signal circuits. The noise reduction strategy and a simple model of a mixed-signal circuit is presented. A test chip aimed at evaluating the proposed noise reduction strategy is presented. Finally we summarize the work.

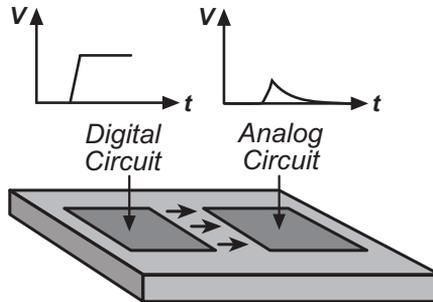


Figure 1: Noise injected into the analog circuit due to the switching of the digital circuit.

1.1 Noise injection mechanisms

The AC behavior of the pn-junctions between the MOS-transistors and the substrate is mainly capacitive [1]. Hence, a signal transition causes noise to be injected from the transistors into the substrate via the capacitive coupling. The noise is then spread in the substrate due to the conductivity of the substrate. Another source of noise is the interconnect, that also is capacitively coupled to the substrate. Hence, a transition in a digital node will be capacitively coupled to the substrate by both the pn-junctions and the interconnect in that node.

The switching of digital circuits produces current peaks, which results in fluctuations on the power supply lines due to the inductive behavior of the interconnect from on-chip to off-chip. This kind of noise is known as simultaneous switching noise (SSN). SSN in the power supply lines in digital circuits is directly injected into the substrate through the biasing substrate contacts.

The strong electrical field between drain and source in submicron transistors makes the carriers (electrons in nMOS, holes in pMOS) to acquire enough energy to become what is called hot. In nMOS devices these hot electrons impact the drain of the transistor and produce ionization and dislodging holes that are spread in the substrate [1]. The result is a current flowing from the bulk of the transistor into the substrate, leading to voltage fluctuations in the substrate.

1.2 Noise reception mechanisms

Since an analog circuit similarly to a digital circuit contains transistors, interconnect, and biased substrate contacts, the noise in the substrate will be received by the analog circuits via the same type of coupling as in the noise injection.

Another noise reception mechanism is the threshold voltage dependence of a transistor on the bulk-source voltage V_{BS} . When substrate noise reaches the transistor, the voltage V_{BS} is affected, and hence the drain current and the drain-source voltage V_{DS} . This is observed as noise in the analog signal.

1.3 Noise reduction techniques

In lightly doped substrates it is possible to reduce the substrate noise in the analog circuit by increasing the distance to the digital circuit. This is due to the increased impedance in the substrate. In heavily doped substrates, increasing the distance between the digital and the analog circuit is inefficient as soon as the distance is more than four times larger than the thickness of the epitaxial layer [2]. This is due to that the noise is spread via the highly conductive p^+ layer. A drawback of increasing the distance between the circuits is the increased area cost.

By inserting a guard ring between the circuits, the substrate noise can be suppressed if a lightly doped substrate is used. This is due to that a guard ring is a low impedance path to ground or V_{dd} . In the case of a heavily doped substrate the effect of guard rings is limited due to the highly conductive p^+ layer.

SSN may be reduced by the use of an on-chip decoupling capacitor. The design of the decoupling capacitor is critical due to the fact that a poorly sized capacitor can result in a resonant circuit with increased SSN. To prevent SSN at the analog power supply lines, it is common to separate the digital power supply lines from the analog. Even if a common supply voltage source is used, it is preferable to use separate pins when taking the parasitic impedance of the interconnect from on-chip to off-chip into account.

In a mixed-signal circuit it is recommended to use lightly doped substrates instead of heavily doped, due to the fact that noise is easily spread over the entire chip via the highly conductive layer of p^+ [1].

2. A STRATEGY FOR REDUCING CLOCK NOISE

Digital circuits commonly use a clock for global synchronization. When a large clock distribution network is used, the clock is strongly coupled to the substrate via the parasitic capacitance, and it will also require large drivers that are capacitively coupled to the substrate. When the clock buffer charge or discharge its large capacitive load, a large current peak is produced in the power supply line causing SSN. Hence, the distribution of the clock generates a considerable amount of the substrate noise that reduces the performance of the analog circuits.

With longer rise and fall times of the clock signal, the time derivative of the generated current peaks will decrease, resulting in lower SSN. The longer rise and fall times also yields a lower frequency content of the clock signal.

Therefore we propose a strategy for reducing the noise by the use of a clock signal with smooth clock edges, i.e. reducing both the high frequency components of the clock signal and the current peaks produced in the power supply. Reducing the rise and fall time of the clock, or ultimately using a sinusoidal waveform would achieve this. The proposed strategy requires a D flip-flop that can operate with long rise and fall times of the clock. Such a D flip-flop is presented in [4], which is used in this work. The efficiency of the strategy will be evaluated in a test chip that is currently being fabricated.

3. A SIMPLE MODEL OF A MIXED-SIGNAL CIRCUIT

A mixed-signal circuit consisting of an analog circuit and a digital circuit occupying equally large area is shown in Fig. 1. The biasing of the analog and the digital substrate is assumed to be uniform within their respective areas of the circuit. The substrate is also biased by a highly conductive backside contact. In the model of the substrate we only consider three nodes, namely the digital ground, the analog ground, and the backside contact. A standard 0.35 μm CMOS process with a lightly doped substrate is assumed. The thickness of the substrate is 725 μm and it is considered to be uniformly doped.

The substrate can be modeled as mainly resistive for frequencies from DC up to a cut-off frequency, f_c , which is defined as

$$f_c = \frac{1}{2\pi\rho_{sub}\epsilon_{Si}} \quad (1)$$

where ρ_{sub} and ϵ_{Si} are the resistivity of the substrate and the permittivity of silicon, respectively [3]. The resistivity of the substrate is $0.1 \Omega\text{m}$ which according to (1) leads to that the behavior of the substrate is mainly resistive for frequencies up to 15 GHz.

The finite element method is used to simulate the substrate. With the tool FEMLAB, a mesh of the substrate shown in Fig. 2 can be created. In our simulations, the generated mesh of the substrate consists of $8 \cdot 10^4$ nodes.

In Fig. 3, the model of the substrate, the parasitic inductances of the interconnect from chip to off-chip, and a clock buffer is shown. V_A is the voltage in the analog ground and V_D is the voltage in the digital ground. The three resistors form a full model of the resistive coupling between the three nodes of interest.

By a simulation in FEMLAB, the values of the resistors can be estimated to $R_1 = 13.8 \text{ k}\Omega$ and $R_2 = R_3 = 27.7 \Omega$. The package inductances L_1, L_2, L_3 and L_4 are all assumed to be 5 nH. The capacitances C_1 and C_2 are both equal to 2 pF.

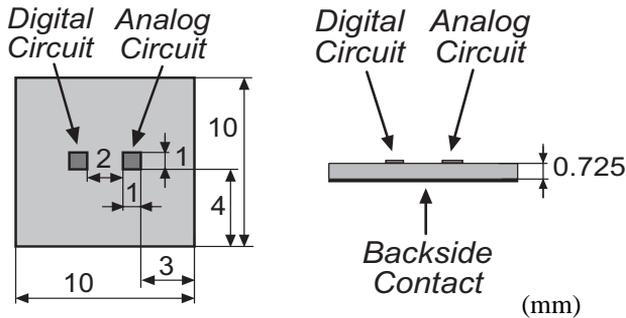


Figure 2: Substrate with a digital and an analog circuit.

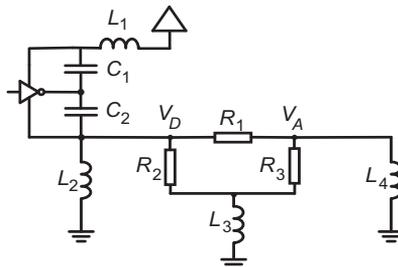


Figure 3: A simple model of a mixed-signal circuit.

The magnitude response from the digital ground V_D to the analog ground V_A is shown in Fig. 4. It is seen that a high frequency is less attenuated than a low frequency and that the noise increases with 40 dB per decade in the frequency range of 2 MHz to 300 MHz.

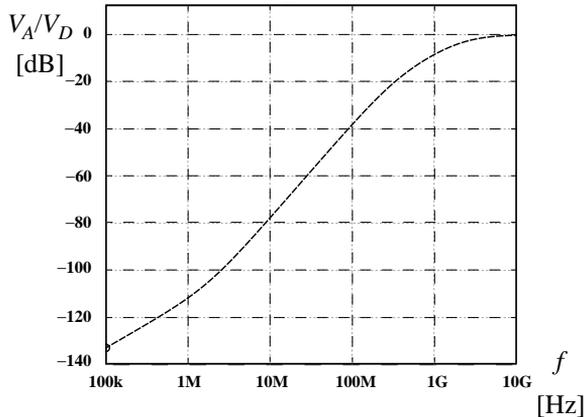


Figure 4: Magnitude response from the digital ground to the analog ground.

In Fig. 5 the root mean square (rms) value of the voltage at the analog ground is shown as a function of the rise and fall time of the clock signal. It is seen that the noise is approximately the reciprocal of the rise and fall time of the clock signal. In the result, only the contribution from switching of the clock net is considered. When switching logic is also taken into account the rms value of the voltage at the analog ground will be larger and the dependency of the rise and fall time of the clock signal will not be as large as shown in Fig. 5.

4. TEST CHIP

We have designed a test chip to evaluate the proposed strategy. The chip contains a digital circuit, a clock driver with programmable rise and fall time, and an analog circuit. The test chip is currently being manufactured in a 0.35 μm CMOS process with two poly layers and three metal layers. The substrate is a lightly doped p-substrate. Separate power supply lines are used for the analog and digital parts to avoid direct injection of SSN from the digital circuit into the analog circuit. The chip will be packaged in a JLCC 68 pin package.

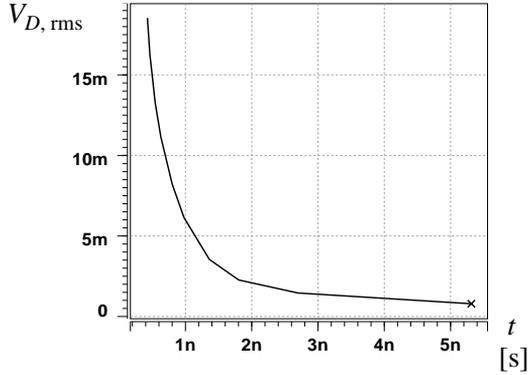


Figure 5: Root mean square of the voltage at the analog ground as a function of the rise and fall time of the clock signal.

4.1 The digital circuit

An FIR filter was chosen for the digital part of the test chip, since this is a common component in signal processing applications. The filter is a low pass filter of order 13 with an external word length of 16 bits, realized in direct form. Each delay element in the structure is implemented with 16 parallel D flip-flops. The addition and multiplication are implemented by hard wired shifts and a carry-save adder-tree which is an efficient implementation approach [5]. A pipelined ripple-carry adder implements the vector-merging adder (VMA), which is the final adder in the carry-save adder-tree. The number of full adders and D flip-flops are approximately 630 and 350, respectively.

With the use of pipelining of the carry-save tree the throughput of the filter could be increased. In this case we are interested of keeping the amount of D flip-flops at a reasonable level to have realistic results. The full adders in the carry-save adder tree are realized using static differential cascode voltage switch logic (DCVS).

The differential D flip-flop presented in [4] is chosen due to its robustness against long rise and fall times on the clock. The only difference between the D flip-flop in [4] and the D flip-flop in the test chip is that the multiplexer at the input is substituted by the two pull-down transistors M_0 and M'_0 as shown in Fig. 6.

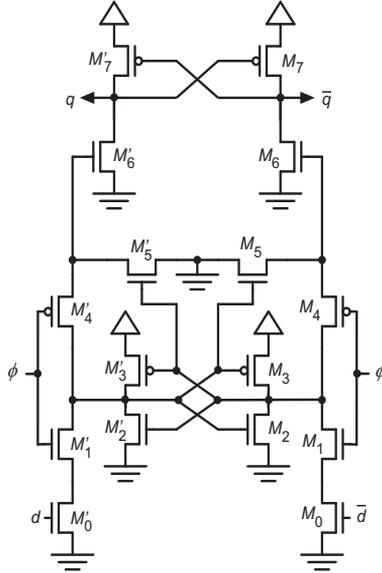


Figure 6: The robust differential D flip-flop.

Separate power supply pins are used for the digital output buffers and the digital filter. A guard ring, surrounding the digital filter, with a separate pin is also used.

4.2 The adjustable clock buffer

The last stage in the adjustable clock buffer consists of 256 unit buffers. The unit buffer is realized using a tri-state buffer where the pMOS and nMOS devices can be activated independently. Two binary vectors with a word length of 8 bits are used to control the number of active nMOS and pMOS devices. This makes it possible to individually adjust the rise and fall time of the clock signal.

4.3 The analog circuit

The analog circuit is a fifth-order low-pass leapfrog filter without finite zeros implemented in the active-RC technique. The filter is derived from a doubly resistively terminated LC ladder network to achieve low sensitivity for variation in the component values [6]. The integrators in the active RC filter consist of two operational amplifiers. In the filter, the inverting and non-inverting integrators are implemented with the proposed structures in [7]. The operational amplifiers are implemented as ordinary two-stage amplifiers with a common drain amplifier as an output buffer.

The cut-off frequency of the filter is programmable and can be adjusted off-chip by placing additional capacitors in parallel with the integrator capacitor. The range for the cut-off frequency is 1.5 to 3 MHz.

To reduce the effect of the substrate noise, the analog filter is shielded from the digital part utilizing p^+ guard rings connected to the analog negative power supply [8], [9].

4.4 Test setup

The test chip will be evaluated in a test setup where a DC voltage will be used as the input signal to the analog filter. The noise will be measured at the output of the analog filter. A series of measurements is planned to be performed where the rise and fall times of the internal clock connected to the digital FIR filter are varied. Also different clock frequencies for the filter will be tested.

5. SUMMARY

We have briefly described the noise injection and reception in mixed-signal circuits. Simulation of a simple substrate model yields that a high frequency is less attenuated in the substrate compared to a low frequency and that SSN generated by the clock buffer is in inverse proportion to the rise and fall time of the clock signal.

A strategy for reducing the noise caused by the digital clock was proposed. The strategy uses a clock with long rise and fall times, and a special D flip-flop that can operate with the special clock. Using longer rise and fall times decreases both the magnitude of high frequency components in the clock signal and the current peaks produced in the power supply. A test chip, containing an FIR filter and an analog filter, is currently being manufactured in a 0.35 μm CMOS process. Results from measurements on the fabricated circuits are expected in the near future.

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Paper II

*Design of Circuits for a Robust
Clocking Scheme*

E. Backenius and M. Vesterbacka

Proc. IEEE Mediterranean Electrotechnical Conf.,
Dubrovnik, Croatia, May 12-15, 2004.

DESIGN OF CIRCUITS FOR A ROBUST CLOCKING SCHEME

E. Backenius and M. Vesterbacka

ABSTRACT

The design of a clock distribution network in a digital integrated circuit is challenging in terms of obtaining low power consumption, low waveform degradation, low clock skew and low simultaneous switching noise. In this work we aim at alleviating these design restrictions by using a clock buffer with reduced size and a D flip-flop circuit with relaxed constraints on the rise and fall times of the clock. According to simulations the energy dissipation of a D flip-flop, implemented in a 0.35 μm process, increases with only 21% when the fall time of the clock is increased from 0.05 ns to 7.0 ns. Considering that smaller clock buffers can be used there is a potential of power savings by using the suggested clocking scheme.

1. INTRODUCTION

The design of a clock distribution network in a digital integrated circuit introduces severe challenges [1]. Generally the clock edges must be sharp which require large clock buffers. When a clock buffer charge or discharge its large capacitive load, a large current peak is produced in the power supply line causing high power dissipation and simultaneous switching noise (SSN) [2]. The noise will cause delay variations in the digital circuits and it will also disturb analog circuits, especially if they are located on the same silicon die [3]. By reducing the requirements on the rise and fall times of the clock, smaller clock buffers can be used and narrower wires may also be used in the clock distribution net.

In earlier work [4] we have aimed at reducing the substrate noise by the use of a clock with smooth clock edges, i.e., reducing both the high frequency components of the clock and the current peaks in the power supply. A D flip-flop [5] that can operate with a clock with long rise and fall times were used. That D flip-flop is also used in this work. The D flip-flop is negative edge-triggered and it uses a single-phase clock. The difference between the D flip-flop in [5] and the D flip-flop used in this work is that the multiplexer at the input of the master latch is here substituted by the two pull-down transistors

M_0 and M'_0 as shown in Fig. 1. The two cross-coupled inverters form the memory element of the static master latch. If the transistors M_2 and M'_2 are omitted a dynamic master latch is obtained instead. The slave latch is semi-static and is shown in Fig. 2. When the clock is low the slave latch is in a static state and when the clock is high the slave latch is in a dynamic state.

In this work we present a clocking scheme for digital circuits aiming at relaxing the constraints of the rise and fall times of the clock. The design of a D flip-flop that can operate with a clock with long rise and fall times and a clock buffer with adjustable drive strength are presented. We investigate how the performance parameters of the D flip-flop are affected by the rise and fall times of the clock, which is of interest from a design point of view, and present results from Hspice simulations and measurements on a test chip.

Some design considerations for the D flip-flop are presented in section II. The design of the adjustable clock buffer is presented in section III. Performance parameters based on simulations of the designed D flip-flop are presented in section IV. A test chip is described in section V together with results from measurements. Finally, the paper is concluded in section VI.

2. DESIGN OF THE D FLIP-FLOP

The design of the D flip-flop is critical due to that the transistors must be sized properly to operate correctly. For example, in the master latch, the pull-down net formed by M_0 , M_1 , M'_0 and M'_1 must be strong enough to pull down one of the inverters outputs below a certain voltage where the positive feedback of the cross-coupled inverters makes the circuit to change state. M_3 and M'_3 form the pull-up net. In Fig. 3, the voltages of the internal nodes n_1 and n_2 (indicated in Fig. 1), are plotted for different sizes of the pull-up net. The data input d changes value from low to high while the clock is kept high.

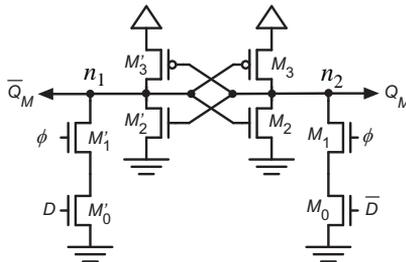


Figure 1: Master latch of the D flip-flop.

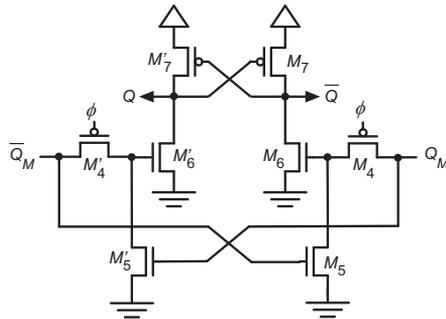


Figure 2: Slave latch of the D flip-flop.

The solid lines and the dashed lines correspond to the voltages of node n_1 and n_2 , respectively. In the first case, corresponding to the two waveforms labeled *a*, the pull-up net is too strong in comparison with the pull-down net, which results in that the voltage V_{n_1} is not reduced enough to force the latch into a new state. As soon the clock goes low, the memory element returns to its previous state. In the second case, corresponding to the waveforms labeled *b*, the pull-up net is weaker, which permits the memory element to change state. The waveform of V_{n_1} falls slowly between 0.5 ns and 1.2 ns. During this time the pull-up transistor M'_3 and the pull-down transistors M'_0 and M'_1 are on simultaneously, which results in a power consuming short-circuit current. When V_{n_1} falls below the threshold voltage of the inverters, V_{n_1} starts to drop more rapidly due to the positive feedback of the cross-coupled inverters. In the third case, corresponding to the waveforms labeled *c*, the pull-up net is weak enough to allow a fast discharging of n_1 , but yet strong enough to allow a fast charging of the complement node n_2 . Node n_1 is forced below the threshold voltage of the inverters quickly. Therefore, the effect of the positive feedback is hardly visible. In the last case, corresponding to the waveforms labeled *d*, the pull-up net is the weakest. The discharging is the fastest, but the charging of the complement node takes longer time than in case *c*. Of this four cases, case *c* should be targeted in the design since the master latch is updated in the smallest amount of time, yielding the smallest set up time of the D flip-flop.

3. DESIGN OF THE ADJUSTABLE CLOCK BUFFER

Our objective is to use a clock with relaxed constraints on the rise and fall times. From a design point of view it is required to know how the performance parameters of the D flip-flop are affected by the rise and fall

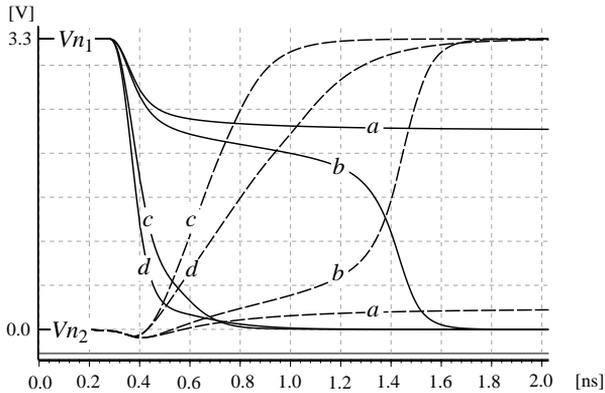


Figure 3: Simulated waveforms for different sizing of the master latch.

time of the clock. Therefore a clock buffer with adjustable driving strength is required. A straightforward design of a clock buffer can be obtained by using ordinary cascaded buffer stages except for the last buffer stage which is constructed of a number of parallel connected unit buffers. Each unit buffer can be realized using a tri-state buffer, which is shown in Fig. 4. The pMOS and nMOS devices can be activated independently, which makes it possible to individually adjust the rise and fall times of the clock.

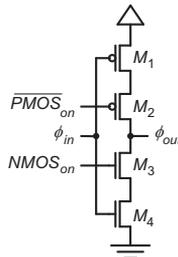


Figure 4: The unit buffer.

4. SIMULATION RESULTS

In this section the performance parameters of the D flip-flop are estimated from Hspice simulations for different cases of fall times of the triggering clock edge. The test set up consists of two identical cascaded D flip-flops. The measurements are performed on the first D flip-flop, whose data output is loaded by the data input of the second D flip-flop. The BSIMV3 models for

the AMS 0.35 μm technology with typical mean process parameters are used in the simulations. The power supply voltage V_{dd} is 3.3 V. However, the D flip-flop works well also with lower power supply voltages. The netlist used in the simulations was extracted from a layout of the D flip-flop.

The time from that the input data d rises or falls to 50% of V_{dd} to that the clock has fallen to 50% of V_{dd} is in the following denoted t_{dc} . The time from that the clock has fallen to 50% of V_{dd} to that the input d has propagated to the output q is denoted t_{cq} . The sum of t_{dc} and t_{cq} is denoted t_{dq} . Rise and fall times are measured on 10% and 90% of the supply voltage. The rise and fall times of the input data of the first D flip-flop are 0.18 ns.

4.1 Set Up Time and Propagation Delay

The set up time t_{su} is defined as the minimum time that the input data must be stable before the triggering clock edge, which in this case is the falling edge. The clock period T of a digital circuit must fulfill the relation

$$T \geq t_{su} + t_{cq} + t_{plogic} \quad (1)$$

where t_{plogic} is the worst case propagation delay of the logic in between the D flip-flops. The sum of t_{su} and t_{cq} in (1) determines how long time of the clock cycle that is occupied for the data propagation through the D flip-flop. Hence, from a performance point of view it is of interest to minimize $t_{su} + t_{cq}$.

In Fig. 5, t_{dc} , t_{cq} , and t_{dq} are shown as functions of t_{dc} , where the fall time of the clock $t_{f,clk}$ is set to 1.4 ns. The minimal time t_{dc} that results in a correct data output is 0.31 ns. However, this time of t_{dc} causes the circuit to go into a state where the circuit is close to metastability and failure. Further, the propagation delay from the triggering clock edge to the data output is in this case large. The closer the operation of the D flip-flop is to metastability, the longer is the propagation delay. t_{cq} reaches its minimum when t_{dc} is large, meaning that the input data is stable a long time before the triggering clock edge. The minimum value of t_{cq} is 0.30 ns and it is approximately reached as soon as $t_{dc} > 1.0$ ns. The sum of t_{cq} and t_{dc} , which is denoted t_{dq} , is the propagation delay of the D flip-flop. It is seen in Fig. 5 that t_{dq} has a minimum for a certain value of t_{dc} . This minimum is found where $dt_{cq}/dt_{dc} = -1$, which corresponds to that the D flip-flop operates on its optimum from a delay time point of view. We let this value of t_{dc} define the set up time t_{su} [6]. We denote the minimum value of t_{dq} as t_{dqmin} , which is obtained when $t_{dc} = t_{su}$. For the case shown in Fig. 5 we get $t_{su} = 0.39$ ns and $t_{dqmin} = 0.87$ ns.

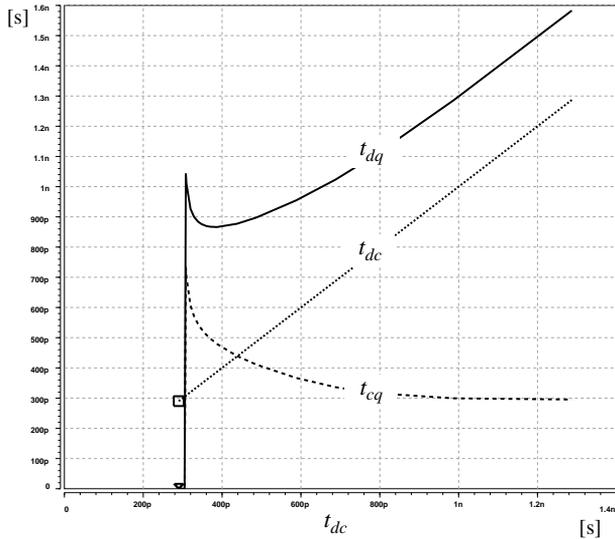


Figure 5: t_{dc} , t_{cq} and t_{dq} as functions of t_{dc} .

In Fig. 6, the set up time t_{su} and the minimal propagation delay t_{dqmin} are shown as functions of the fall time of the triggering clock edge $t_{f,clk}$. The range of the fall time of the clock is here from 50 ps to 14 ns. The minimal propagation delay t_{dqmin} is in this case 0.66 ns. When the fall time is increased 28 times to 1.4 ns, the minimum propagation delay t_{dqmin} increases with 32% to 0.87 ns. Further, if the fall time is increased from 50 ps to the more extreme fall time of 7 ns, t_{dqmin} increases with 72% to 1.18 ns. We see that t_{dqmin} increases when the fall time of the clock is increased. We also see that the increase in t_{dqmin} is modest even for a large increase of the fall time of the clock. The longer propagation delay, when using a longer fall time of the clock, is due to that the gate overdrive voltages of the clocked transistors do not reach their maximal values as quick as in the case of short rise and fall times. However, considering designs where the combinational circuit dominates the critical path, the impact of the increased propagation delay in the D flip-flops may be negligible.

4.2 Hold Time

The hold time t_h is defined as the minimum time that the data must be stable after the triggering clock edge when the input data just fulfills the requirement on set up time. The hold time t_h is affected by how close the D flip-flop is to metastability and failure for the used value of t_{su} . Hence, different values of set up time will result in different values of hold time for

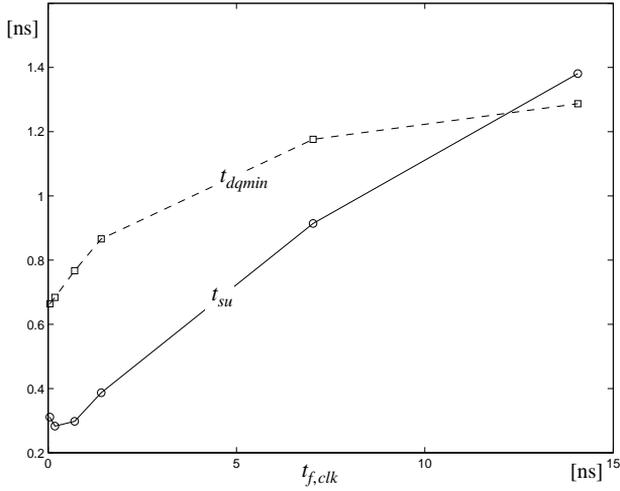


Figure 6: t_{dqmin} and t_{su} as functions of $t_{f,clk}$.

the same D flip-flop. Here we use the set up times that were found in the previous subsection. The hold time and the set up time form a window in which the data input must be stable to guarantee a proper function of the D flip-flop. In the previous subsection the input data was considered stable as long time after the triggering clock edge that the influence of a new data transition was negligible. The propagation delay t_{dq} is affected by the time that the input data is stable after the triggering clock edge. We choose to define t_h as the minimum time that the input data must be stable after the triggering clock edge to guarantee that the propagation delay t_{dq} does not increase more than 5% in comparison with t_{dqmin} . In Fig. 7 the hold time t_h for the case where $t_{dc} = t_{su}$ is shown as a function of $t_{f,clk}$. The hold time is in the range from -0.26 ns to 0.24 ns when $t_{f,clk}$ is varied from 50 ps and 14 ns.

4.3 Energy Dissipation

With a longer fall time of the clock edge, a longer time to read the input data into the master latch is required. This means that the two cross-coupled inverters take longer time to change state. While the cross-coupled inverters change state, short circuit currents occurs. Hence, longer fall time of the clock results in larger short-circuit currents in the master latch. The energy dissipation of the D flip-flop per clock cycle due to the load of the clocked transistors is about 0.17 pJ. The energy dissipation of the D flip-flop as a function of $t_{f,clk}$ is shown in Fig. 8, where it can be seen that the energy dissipation increases little with increased $t_{f,clk}$. For example, the energy

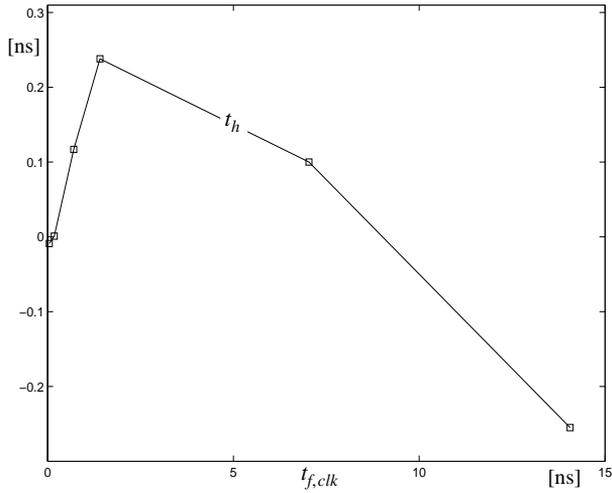


Figure 7: t_h as function of $t_{f,clk}$.

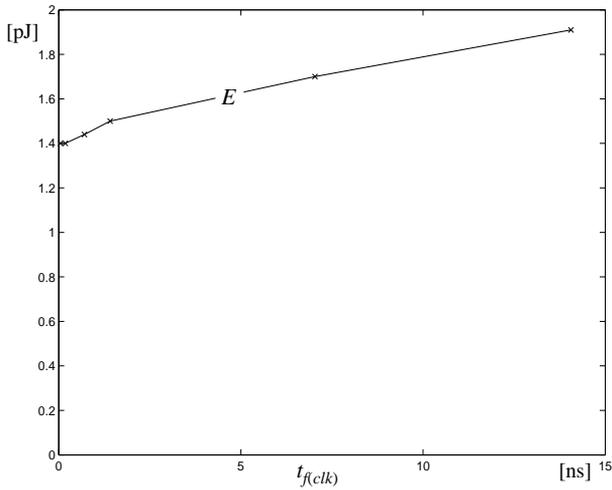


Figure 8: Dissipated energy E as a function of $t_{f,clk}$.

dissipation increases with only 21% when the fall time of the clock is increased from 0.05 ns to 7.0 ns. Considering that smaller clock buffers can be used in the clock distribution net, when longer rise and fall times are used, there is a potential of power savings in using the suggested clocking scheme.

5. TEST CHIP

A test chip has earlier been designed [4] where we use the D flip-flop described in section I and the adjustable clock buffer described in section III to implement a clock distribution network in a digital filter. The purpose of the test chip is to evaluate how a digital circuit and an analog circuit sharing the same substrate are affected by relaxed constraints on the rise and fall times of the clock. In this work we focus on the clock distribution in the digital part. The chip is manufactured in the AMS 0.35 μm CMOS process with two polysilicon layers and three metal layers. The substrate is a lightly doped p-substrate. An FIR filter was chosen for the digital part of the test chip, since this is a common component in signal processing applications. The filter is a low pass filter of order 13 with an input word length of 16 bits. The addition and multiplication are implemented by hard-wired shifts and a carry-save adder-tree [7]. A pipelined ripple-carry adder implements the vector-merging adder (VMA), which is the final adder in the carry-save adder-tree. The number of full adders and D flip-flops are approximately 630 and 350, respectively. The full adders are realized using static differential cascode voltage switch logic (DCVS) [8].

Measurements on the digital part on the test chip indicate that the clock scheme works well. For example, the digital circuit operates well even with a clock buffer that is so weak that the clock only reaches a swing of 60% of V_{dd} at a clock frequency of 74 MHz. The propagation delay of the critical path increases with 0.5 ns when the nominal rise and fall times of the clock are increased from approximately 0.5 ns to 10 ns.

6. CONCLUSIONS

An adjustable clock buffer and a special D flip-flop were designed. The circuit were aimed at relaxing the constraints on the rise and fall times of the clock in digital circuits. Simulation results indicated that the effect of long rise and fall times were mainly longer propagation delays. For example, when the fall time of the triggering clock edge is increased from 50 ps to 7.0 ns, the propagation delay increases with about 72% and the energy dissipation increases with 21%. Considering the sizing of the clock net and the smaller clock buffers that can be used, the relaxed clock scheme has a potential of power savings. Measurements on a test chip implies that it is feasible to design digital circuits with the presented clocking scheme.

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Paper III

*Evaluation of a Clocking Strategy with
Relaxed Constraints on Clock Edges*

E. Backenius and M. Vesterbacka

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2004.

EVALUATION OF A CLOCKING STRATEGY WITH RELAXED CONSTRAINTS ON CLOCK EDGES

E. Backenius and M. Vesterbacka

ABSTRACT

A strategy that aims at relaxing the design of the clock network in digital circuits is evaluated through simulations and measurements on a test circuit. In the strategy a clock with long rise and fall times is used in conjunction with a D flip-flop that operates well with this clock. The test circuit consists of a digital FIR filter and a clock buffer with adjustable driving strength. It was designed and manufactured in a 0.35 μm CMOS process. The energy dissipation of the circuit increased 14% when the rise and fall times of the clock increased from 0.5 ns to 10 ns. The corresponding increase in propagation delay was less than 0.5 ns, i.e. an increase of 50% in propagation delay of the register. The results in this paper show that the clocking strategy can be implemented with low costs of power and speed.

1. INTRODUCTION

The design of the clock distribution in a digital circuit can be challenging [1]. For example, the clock edges must generally be sharp, which require large clock buffers and wide interconnects in the clock net. The use of wider wires reduces the parasitic resistance, but it also increases the parasitic capacitance. When the clock buffer charge or discharge its capacitive load, a current peak is produced in the power supply line causing simultaneous switching noise (SSN), which is particularly cumbersome in mixed-signal circuits [2]. The clock distribution may generate a considerable amount of the digital switching noise that can degrade the performance of an analog circuit placed on the same die. When the clock path is long, repeaters can be used to lower the degradation of the clock waveform with an added cost of increased area and higher power consumption. The clock distribution does also contribute significantly to the total power consumption in many digital circuits due to that the clock makes two transitions every clock cycle and that the clock load generally is large.

The shapes of the clock edges affect both timing and power consumption. With smooth clock edges, smaller clock buffers can be used, which results in less internal load capacitance, smaller currents and less silicon area. With smaller currents in the clock distribution net narrower interconnects can be used which also reduces the capacitive load, but the required interconnect widths in the different paths in the clock net are still limited by timing constraints and the peak currents. However, compared with e.g. power supply lines the clock interconnects have less sensitivity for electromigration, due to the alternating current.

If long rise and fall times of the clock are used, a D flip-flop that can operate with this clock is required. To guarantee that a D flip-flop works properly, the input data must be stable within a time window defined by the set up time and the hold time [3]. The highest risk of violating the set up time is found in the registers that are placed at the end of the critical path. The highest risk of violating the hold time is found where registers are cascaded without logic in between. The longer rise and fall times of a signal, the longer time the voltage is in the range where both NMOS and PMOS transistors conduct simultaneously. Hence, longer rise and fall times of the clock result in a higher power consumption in the registers due to increased short circuit currents. The propagation delay does also increase due to that the gate voltage of a clocked transistor will not reach its maximal value as quick as in the case of short rise and fall times.

In earlier work [4] we have aimed at reducing the digital noise originating from the clock buffers by the use of a clock with smooth clock edges, i.e. reducing both the high frequency components of the clock and the current peaks produced in the power supply. A D flip-flop [5] that can operate with a clock with long rise and fall times was used. In [6] we presented the design of circuits for a robust clocking scheme.

In this work we present results from measurements on a manufactured test chip containing a digital filter where we use the D flip-flop presented in [5]. The measurements consider performance parameters as energy dissipation and minimal clock period as functions of the driving strength of the adjustable clock buffer. The clocking strategy is described in section II. In section III the test set up is described and in section IV the results from the manufactured test circuit are presented together with some simulation results. Finally, the work is concluded in section V.

2. CLOCKING STRATEGY

Our clocking strategy is to use a clock with long rise and fall times in conjunction with a D flip-flop that can operate with such a clock. With long rise and fall times of the clock, the constraints of the distribution of the clock are relaxed in terms of that smaller buffers can be used and that the need for repeaters and wide interconnects is reduced. In mixed-signal circuits there is a potential of reducing the digital switching noise, hence improving the performance of analog circuits.

3. TEST SET UP

To evaluate the clocking strategy a digital low pass FIR filter has been implemented. The filter is of order 13 with an external word length of 16 bits. The filter is realized in direct form [7], where the additions and multiplications are implemented by hard-wired shifts and a non-pipelined carry-save adder-tree [8]. The full adders in the tree are realized using static differential cascode voltage switch (DCVS) logic [9]. A pipelined ripple-carry adder implements the vector-merging adder (VMA), which is the final adder in the carry-save adder-tree. The number of full adders and D flip-flops are approximately 630 and 350, respectively.

In the vector merging adder there are cascaded registers with no logic in between which represent the highest risk for violating the hold time. The critical path of the digital filter corresponds to a certain path through the carry-save adder-tree. This path represents the highest risk for violating the set up time. Hence, results from measurements on the digital circuit should also be applicable on other digital implementations that use the same D flip-flop. The chosen D flip-flop [5] is shown in Fig. 1. It uses a single-phase clock and it can operate with long rise and fall times of the clock.

The clock buffer in the digital circuit has adjustable rise and fall times to evaluate effects of using long rise and fall times of the clock. The clock buffer consists of cascaded buffers of increasing size where the final buffer consists of 255 unit buffers. The PMOS and NMOS net in each unit buffer can be activated independently with the circuit shown in Fig. 2. If the NMOS net is enabled, the gate source capacitance of M_3 and the shared diffusion area of M_3 and M_4 will be added to the clock node. In the same way, gate capacitance and diffusion area will be added to the clock node when the PMOS net is enabled. Hence, the capacitive load of the clock node is dependent on the number of enabled NMOS and PMOS nets.

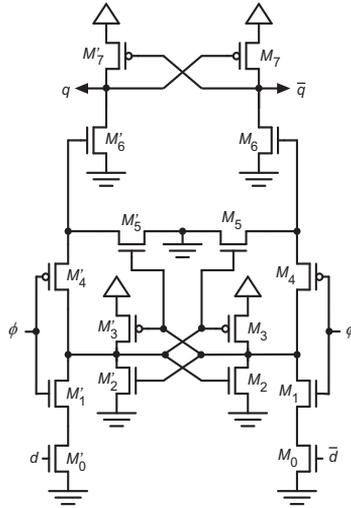


Figure 1: Differential D flip-flop.

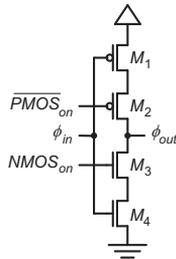


Figure 2: Unit buffer.

The actual rise and fall times (measured from 0% to 90% of final value) of the clock on chip can be estimated by measuring the energy dissipation of the clock node. The rise time is estimated by the following procedure. First the number of enabled PMOS nets are chosen. Then, a number of enabled NMOS nets are chosen so that the clock node always is fully discharged before it is recharged in each clock cycle. For long clock periods the clock node will have full swing (ranging from ground to V_{DD}). If the clock period time is decreased so that the energy dissipation of the clock decreases with 10%, then the swing of the clock is reduced to 90% of V_{DD} . This means that the clock is charged to 90% of V_{DD} after one half of the clock period time.

In the same way the fall time of the clock is estimated. However, when a short rise or fall time is measured, differences in the symmetry of the input of the unit buffers will highly affect the accuracy of the estimation. Further, when shorter clock periods are used the SSN dependence of the clock frequency

tends to be larger of the reason that the fluctuations on the power supply lines have not as long time to be smoothed out between the current peaks as when a longer clock period is used. For these reason the estimation method described here is expected to be applicable only for estimation of long rise and fall times.

With the purpose to measure the energy dissipation in the digital filter as function of the driving strength of the clock buffer, random vectors with four different transition activities were constructed. Here we define the transition activity α as the average number of transitions during one clock cycle. Each test case corresponds to 10^4 binary input vectors that are periodically repeated, where each input bit is independent of other input bits. The used transition activities are 0, 0.10, 0.20, 0.30, and 0.40.

In order to estimate how the propagation delay of the critical path is affected by the rise and fall times of the clock, the minimal clock period is measured for different cases of driving strengths of the clock buffer.

4. RESULTS

A test chip has been manufactured in a 0.35 μm CMOS process. The chip has an area of 11 mm^2 and a microphotograph of it is shown in Fig. 3. It contains a digital circuit, a clock driver with adjustable rise and fall time, and two analog circuits. Separate power supply lines are used for the analog and digital parts to avoid direct injection of SSN from the digital circuit into the analog circuits. The chip is packaged in a JLCC 68 pin package. A power supply voltage of 2.5 V was used.

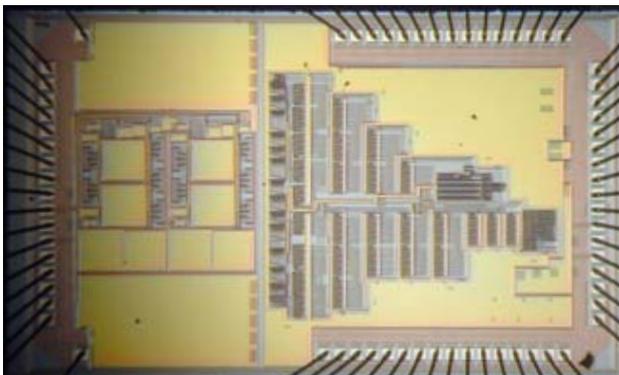


Figure 3: Microphotograph of the test chip.

4.1 Ranges of rise and fall times of the clock

The ranges of the rise and fall times of the adjustable clock buffer have been simulated in HSpice where the estimated parasitic impedances of the power supply lines have been included. In Fig. 4, the simulated and the measured rise time, as functions of the number of enabled unit buffers, are shown as the solid line and the dashed line, respectively. In Fig. 5, the simulated and the measured fall time, as functions of the number of enabled unit buffers, are shown as the solid line and the dashed line, respectively. The ranges of the rise and fall times estimated from simulations are from 0.5 ns to 25 ns and from 0.4 ns to 20 ns, respectively. The measured rise and fall times of the clock on the test chip shows good agreements with the simulation results for long rise and fall times.

4.2 Propagation delay

The propagation delay of the D flip-flop loaded by an identical D flip-flop is, according to Hspice simulations of a netlist extracted from the layout, about 0.94 ns for a fall time of the clock of 0.2 ns. If the fall time of the clock is increased to 10 ns the propagation delay increases to 1.9 ns, corresponding to an increase of 100%.

In Fig. 6, propagation delays of the critical paths of three test chips are shown as functions of the number of enabled unit buffers. The delay of the critical path is estimated by measuring the minimal clock period that the circuit can operate with. The respective propagation delays of the test chips varies less than 0.5 ns when the rise and fall times of the clock are within the range of about 0.5 ns to 10 ns. Considering the simulation results of the D flip-flop mentioned above, a larger variation in the propagation delay in the critical path could be expected.

In the case of two unit buffers enabled and a clock period of 13.5 ns (corresponding to 74 MHz), the clock has a decreased voltage swing that reaches only 1.5 V, which is 60% of the power supply voltage ($V_{DD} = 2.5$ V). With these long rise and fall times, the clock is approximately triangular wave shaped. The digital circuit even works when only one unit buffer is enabled, which correspond to rise and fall times of about 20 ns, but in this case the propagation delay increases to 15 ns.

4.3 Maximal clock pulse width

The D flip-flop is in a dynamic state when the clock is high which gives an upper bound on the pulse width of the clock. According to measurements on the test chip the upper bound on the pulse width is about 250 ns.

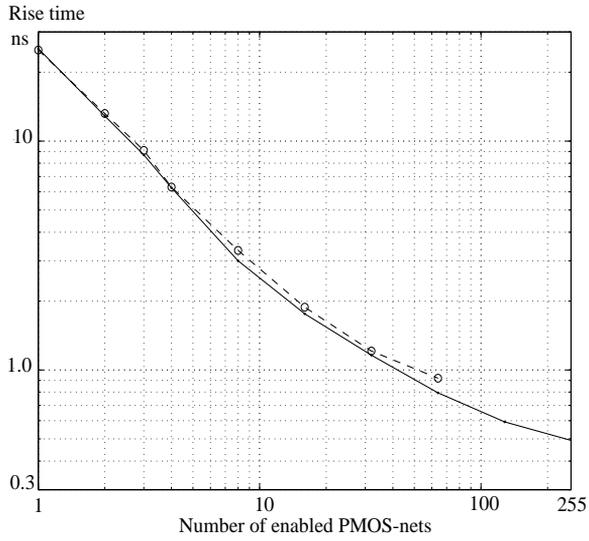


Figure 4: Simulated and measured rise time of the clock as functions of the number of enabled PMOS-nets.

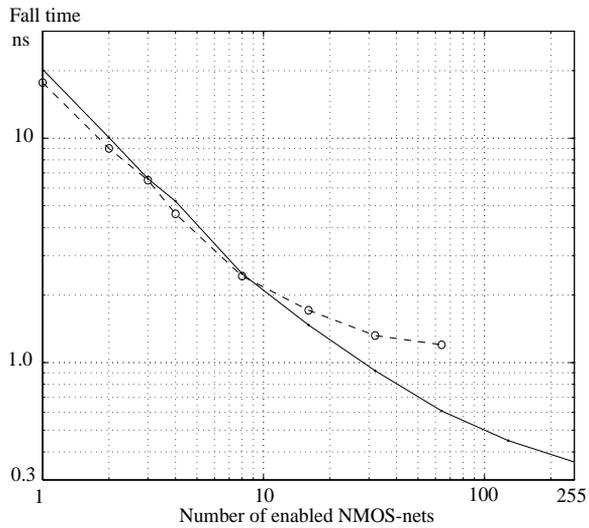


Figure 5: Simulated and measured fall time of the clock as functions of the number of enabled NMOS-nets.

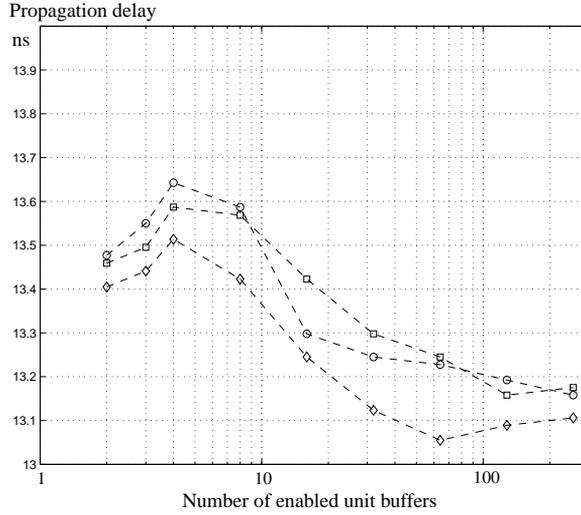


Figure 6: Propagation delay of the critical path as function of the number of enabled unit buffers.

If a normal clock is used where the pulse width is equal to the half of the clock period the minimal clock frequency is then 2 MHz. However, as long as the pulse width is no longer than 250 ns it is possible to choose an arbitrarily low clock frequency or even stop the clock.

4.4 Energy dissipation

The energy dissipation of the digital circuit, including the clock distribution, as function of the number of enabled unit buffers (N_{buff}) for different transition activities are shown in Fig. 7. The clock period used here is 20 ns. For $\alpha = 0$, the input of the digital filter is constant and the energy dissipation is in this case only due to the clock distribution (the contribute from leakage currents is 50 fJ which is negligible). The swing of the clock is less than V_{DD} for $N_{buff} < 4$, which results in a reduced dissipated energy. The increased dissipated energy seen for an increased number of enabled unit buffers for $N_{buff} > 4$ is mainly due to the diffusion capacitance and the gate source capacitance which are added to the clock node for each enabled unit buffer as described in section 3.. For $\alpha \geq 0.1$, the energy dissipation varies with N_{buff} due to both the short circuit currents in the D flip-flop and the variation in clock load.

In Fig. 8 the energy dissipation per clock cycle of the digital circuit excluding the clock distribution is shown. Here, it can be seen that the dissipated energy increases in the D flip-flops when a less number of unit buffers are used.

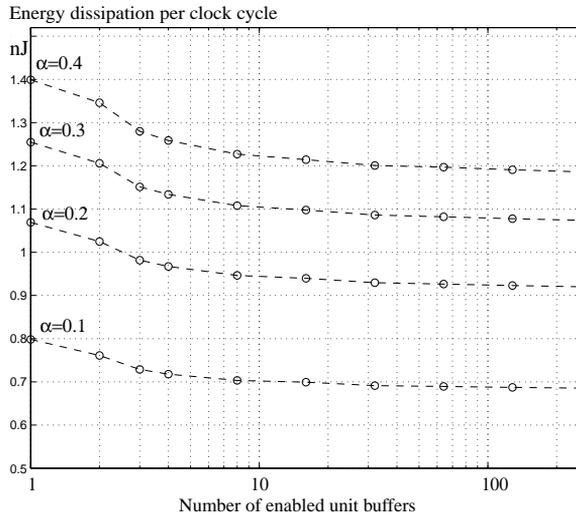


Figure 7: Energy dissipation per clock cycle of the digital circuit excluding the clock distribution as function of the number of enabled unit buffers.

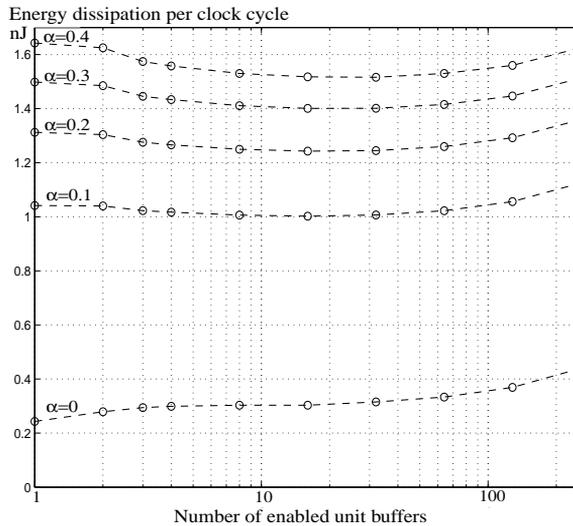


Figure 8: Energy dissipation per clock cycle of the digital circuit as function of the number of enabled unit buffers.

For example, the energy dissipation is increased with 11% when the number of unit buffers is decreased from 255 to 2 when $\alpha = 0.1$. According to simulation results, this corresponds to that the fall time of the triggering clock edge is increased from about 0.4 ns to 10 ns. For the case of $\alpha = 0.4$ the corresponding increase in energy dissipation is 14% which is the largest increase of the four cases of different transition activities.

The presented results from the test circuit indicate that the clocking strategy works well and that it can be implemented in digital circuits with a low cost of propagation delay and power consumption.

5. CONCLUSIONS

In this work effects of the shapes of the clock edges have been discussed. A clock distribution strategy that relaxes the constraints on the clock edges has been presented. According to simulations and results from the manufactured test chip, the clocking strategy works well. Simulation results indicates that if the rise and fall times of the clock are increased from about 0.5 ns to 10 ns, the propagation delay of the D flip-flop approximately doubles from 0.94 ns to 1.9 ns. Measurements on the test chip indicate that the propagation delay of the critical path in the implemented digital filter increases with 0.5 ns for the corresponding case. The energy dissipation was increased with at most 14% when the rise and fall times of the clock were increased from 0.5 ns to 10 ns. With the relaxed constraints on the clock edges the design effort can be reduced. There is also a potential of that the clocking strategy reduces the digital switching noise, hence the performance of analog circuits placed on the same die may be improved.

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Paper IV

*Introduction to Substrate Noise in
SOI CMOS Integrated Circuits*

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Sweden, June 14-16, 2005.

INTRODUCTION TO SUBSTRATE NOISE IN SOI CMOS INTEGRATED CIRCUITS

Erik Backenius and Mark Vesterbacka

ABSTRACT

In this paper an introduction to substrate noise in silicon on insulator (SOI) is given. Differences between substrate noise coupling in conventional bulk CMOS and SOI CMOS are discussed and analyzed by simulations. The efficiency of common substrate noise reduction methods are also analyzed. Simulation results show that the advantage of the substrate isolation in SOI is only valid up to a frequency that highly depends on the chip structure. In bulk, guard bands are normally directly connected to the substrate. In SOI, the guard bands are coupled to the substrate via the parasitic capacitance of the silicon oxide. Therefore, the efficiency of a guard may be much larger in a conventional bulk than in SOI. One opportunity in SOI is that a much higher resistivity of the substrate can be used, which results in a significantly higher impedance up to a frequency where the coupling is dominated by the capacitive coupling of the substrate.

1. INTRODUCTION

The conventional bulk CMOS technology has during the last decades been the dominating technology in many areas owing to its high cost effectiveness in comparison with other technologies. Silicon on insulator (SOI) has during the recent years become an increasingly interesting technology. The manufacturing cost of SOI is still higher than for CMOS, but the relative difference in cost has decreased during the last years and the use of SOI is expected to be increased in the future [1].

In silicon on insulator, the active area is a thin-film of silicon that is isolated from the substrate by a buried isolating layer (e.g. silicon oxide). The use of a thin-film instead of a conventional bulk results in smaller parasitic capacitances. This is mainly due to the less deep pn-junctions. The smaller parasitic capacitances yield faster and less power consuming circuits [2]. Owing to the insulating layer, the achieved quality factors of inductors are generally higher in SOI than in bulk.

There are some unwanted effects in SOI circuits that does not exist in bulk CMOS circuits. The special SOI effects that must be considered during a design depends not only on the design, but also on the chosen type of SOI-process [2]. However, in this work we focus on a conventional bulk substrate and a SOI substrate where the buried layer consists of silicon oxide.

In mixed-signal ICs, the integration of digital and analog circuits is a challenging task. The digital switching produces current peaks on the power supply voltage. The parasitic inductance of the interconnect from on-chip to off-chip together with the capacitance between the power supply nodes on-chip form a resonance circuit. Therefore, current peaks on the power supply lines result in fluctuations of the power supply voltage. This kin of fluctuations are known as simultaneous switching noise (SSN).

The digital circuits generate noise which is spread through the substrate and received by sensitive analog circuits. The propagation of noise through the substrate severely degrades the performance of analog circuits, e.g., lower signal to noise ratio (SNR) and lower spurious free dynamic range (SFDR). In the analog circuits, the frequency components of the substrate noise can be observed as either attenuated or amplified in the analog nodes. Substrate noise may also be intermodulated with analog signals, which results in appearance of new frequency components. Consequently, substrate noise that lays outside an analog signal band may, due to intermodulation, fall into the analog signal band [3]. Therefore, the coupling between different regions on a chip must be carefully analyzed during the design of a mixed-signal circuit.

Isolating circuits with the use of SOI may seem to be a very good idea, but the isolating layer is not a perfect insulator. The parasitic capacitance of the silicon oxide layer results in that higher frequency components are partially by-passed. Therefore, lower frequencies are effectively attenuated in SOI, while higher frequencies are less attenuated.

In Section 2., a brief description of the used modeling method is given. In Section 3., substrate noise in SOI and bulk are discussed together with test structures that are simulated and analyzed. In Section 4., conclusions are made.

2. SUBSTRATE MODELING

To compare bulk with SOI, reliable models of the substrates must be used. For this reason we use the tool FEMLAB, which use the finite element method to model 3D structures. In this tool we include the shape, the resistivity, and the permittivity of the substrates. In this way, both the resistive and the capacitive coupling through the substrates are modeled. The results

achieved in FEMLAB are used to derive full models of the substrates consisting of resistors and capacitors.

The substrates considered in this work have all the thickness of $500\ \mu\text{m}$. The silicon resistivity is assumed to be $20\ \Omega\text{cm}$, if nothing else is mentioned. The relative permittivity of silicon is assumed to be 11.8. The thickness of the buried oxide (i.e. the insulator) in SOI is $0.4\ \mu\text{m}$.

The capacitive coupling per area unit between the active area and the substrate in SOI is approximated to $C = \epsilon_r \epsilon_0 / d_{ox}$. The backside of the chip is assumed to be metallized and connected to ground. To take package impedance into account, inductors are added in series with resistors where the values are $0.20\ \text{nH}$ and $20\ \text{m}\Omega$, respectively.

In Fig. 1, a result of a simulation in 3D is shown where the difference in surface voltage potential is visualized. From the simulation, both the resistive and the capacitive couplings can be calculated by postprocessing the achieved data.

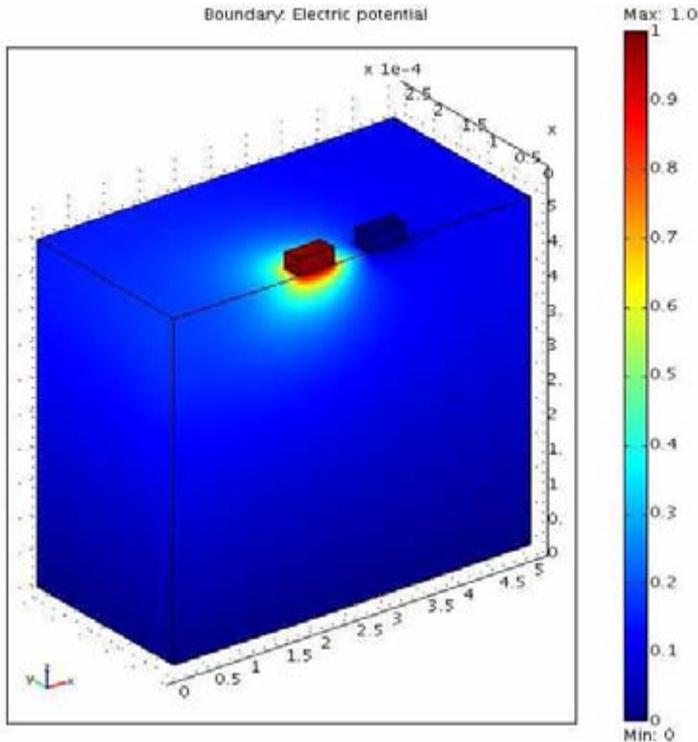


Figure 1: A simulation result in FEMLAB.

3. SOI VS. BULK

To compare SOI with bulk processes with a focus on substrate noise, different test structures are designed, modeled, and simulated. In each test structure a digital and an analog region are assumed to be placed on the same die. The magnitude response from the digital region to the analog region for each test structure are studied both for the case of bulk and SOI.

3.1 Two Different Test Structures

Two test structures are used to point out that the discrepancy in substrate noise in SOI and bulk are highly dependent on the chip structure. In Fig. 2, the two test structures are shown where two circuits are placed on each die.

The full RC model of the SOI test structure is shown in Fig. 3. The circuit in the dashed box is the full model of the substrate derived with FEMLAB. The inductors in series with resistors model the package impedance. In Fig. 4, the magnitude response from the digital region to the analog region is shown for the two test structures for both bulk and SOI. The coupling is significantly lower in SOI than in bulk for low frequencies, as expected. For test structure 1, the difference between SOI and bulk is small for frequencies above 2 GHz.

For test structure 2, the difference between SOI and bulk becomes small for frequencies above 500 MHz. The coupling for test structure 2 is significantly higher. The longer distance between the edges should give some extra impedance through the substrate, but on the other hand the larger areas of the

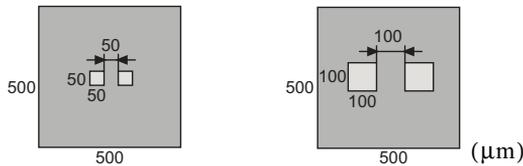


Figure 2: Two test structures.

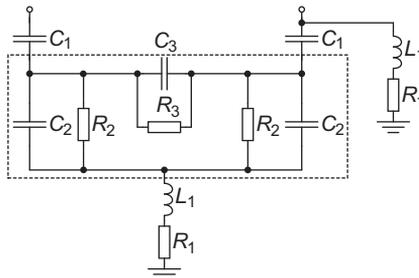


Figure 3: A full model of the SOI test structure.

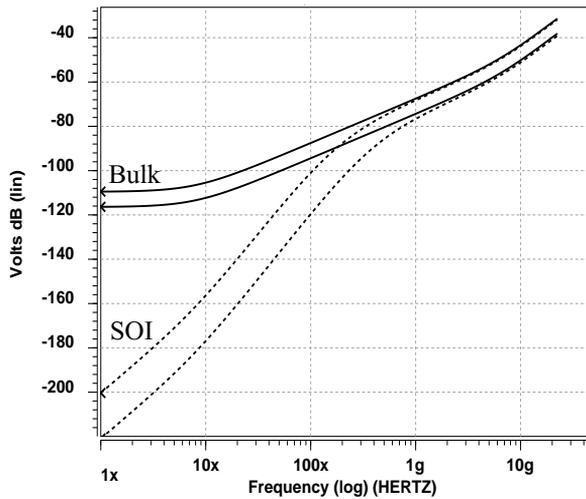


Figure 4: Magnitude responses from the digital to the analog region for two different test structures.

circuits increase the coupling significantly. From these two test structures we see that the frequency where the coupling is approximately equal for SOI and bulk is very dependent on the chip structure. Regarding the substrate coupling, it is interesting for the designers to know for which frequency bulk is comparable with SOI. If a conventional CMOS process may be used instead of a SOI process, money can be saved.

3.2 Distance for Increased Substrate Impedance

In lightly doped bulk substrates it is possible to reduce the substrate noise in the analog circuit by simply increasing the distance to the digital circuit. With an increased distance between the circuits, a higher impedance through the substrate is achieved. A drawback of increasing the distance between circuits is the increased cost in area. In heavily doped substrates, the substrate noise is almost uniform due to the highly conductive layer of p^+ . Increasing the distance between circuits in heavily doped substrates is inefficient as soon as the distance is more than four times larger than the thickness of the epitaxial layer [4]. However, in this work we only consider lightly doped substrates.

To investigate the influence of distance on the substrate coupling, three test structures are analyzed for SOI and bulk. The first test structure is shown in Fig. 5, where the distance between the two circuits is 0.2 mm and the sizes of them are 0.9 mm by 2 mm. The second and the third test structure have both the same circuit sizes, but the distances are here 0.1 mm and 0.4 mm, respectively. The corresponding chip areas for the three test structures are 3.8

mm², 4.0 mm² and 4.4 mm². In Fig. 6, the magnitude responses are shown for the three different cases of distance. It is seen that the distance significantly affects the coupling through the substrate. For frequencies of about 500 MHz and above, the influence of the distance is small. This effect originates from that the impedance through the inductors are high for these frequencies.

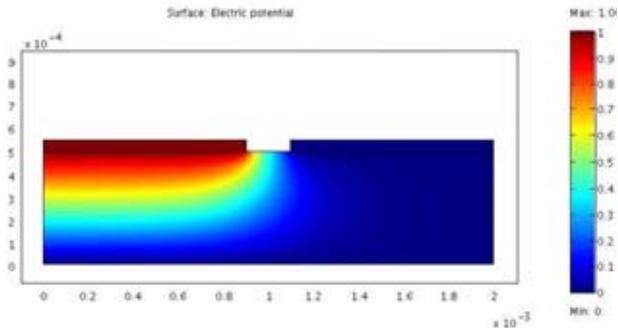


Figure 5: Two circuits with edge to edge distance of 0.2 mm on a 1.9 mm by 2.0 mm chip with wafer thickness of 0.50 mm.

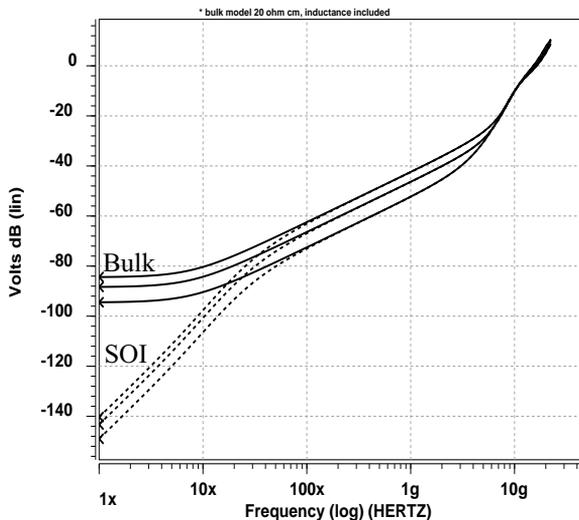


Figure 6: Magnitude responses from the digital to the analog region for three different distances.

3.3 Guard Band

In a bulk substrate, inserting a guard band between circuits can suppress the coupled noise if a lightly doped substrate is used. This is due to that a guard band works as a low impedance path to ground or V_{dd} . In lightly doped substrates, guard bands generally consist of substrate contacts. In the case of a heavily doped substrate the effect of guard bands is limited due to the highly conductive p^+ layer. Here, the substrate noise is almost uniformly distributed over the entire silicon area. Due to the insulator layer in SOI, substrate contacts can not be connected directly to the substrate. For this reason, guard bands in SOI CMOS IC's consist of regions where the thin-film is connected to ground. The parasitic capacitance between the thin film and the substrate is here acting as a decoupling capacitance where higher frequencies are damped. If a guard band is connected to the analog ground on the chip, all noise received in the guard will be seen at the analog ground. If a guard is connected to a digital ground, all digital ground noise will also be seen in the guard. For these reasons, guard bands should be connected to separate pins.

A guard is added in between the circuits in the test structure that was shown in Fig. 5. The resulting structure is shown in Fig. 7. The guard band has the width of $100\ \mu\text{m}$ and the length of $2\ \text{mm}$. The full model of the substrate coupling is shown in Fig. 8. As in previous test structures, inductors in series with resistors model the parasitic impedance of a package.

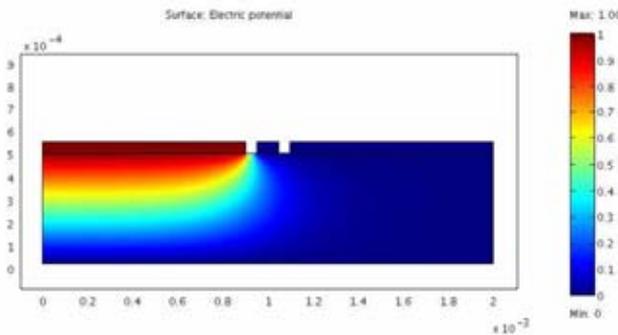


Figure 7: A guard band between two circuits.

The magnitude responses for the test structure with and without a guard band are shown in Fig. 9, where it is clearly seen that the SOI does not benefit as much as the bulk does from the use of a guard band. The reason for this is that the impedance from the substrate to the guard in SOI is capacitive and therefore lower frequencies see a large impedance. Higher frequencies are by-passed through the silicon oxide layer. A dip in the magnitude response

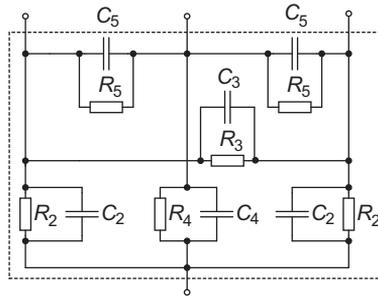


Figure 8: A full model of the substrate in the test structure using a guard band.

can be seen for the SOI in Fig. 9. This is due to the resonance frequency of the capacitor in series with the inductor. For frequencies higher than 2 GHz, the bulk has approximately the same coupling as SOI.

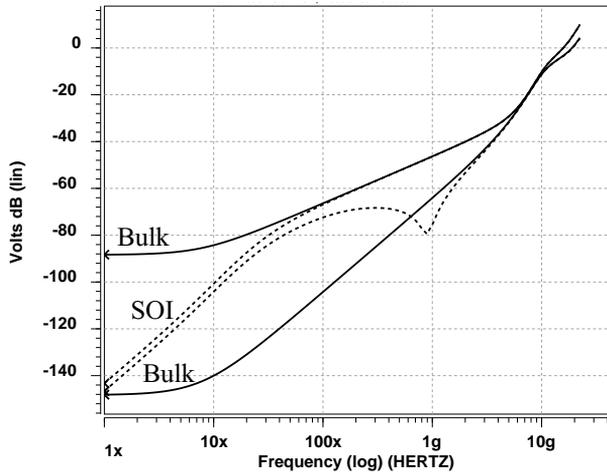


Figure 9: Magnitude responses for a test structure with and without guard band.

3.4 High Resistive Substrate

In conventional bulk processes the substrate is commonly used to bias the NMOS bodies. The substrate in SOI is not used for any biasing purposes. Therefore, much higher resistivity of the substrate can be used in SOI, which is beneficial for increasing the impedance in the substrate noise path [5]. Hence, the opportunity to use a higher resistivity substrate in SOI should translate to less substrate noise coupling up to some frequency where the capacitive coupling is dominating. In Fig. 10, the magnitude responses of the test structure shown in Fig. 5, are shown for 20 Ωcm , 200 Ωcm , and 200

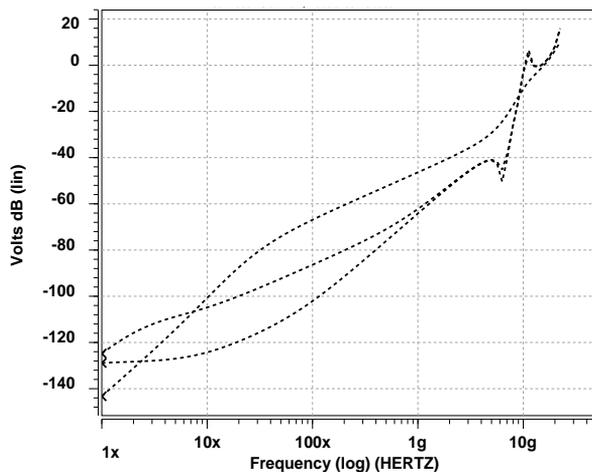


Figure 10: Magnitude responses for a test structure in SOI with resistivity of $20\Omega\text{cm}$, $200\Omega\text{cm}$, and $2000\Omega\text{cm}$.

Ωcm . It is seen that a higher resistivity of the substrate reduces the coupling. When the resistivity is increased from $20\Omega\text{cm}$ to $200\Omega\text{cm}$, the magnitude response is significantly decreased for the frequency range from 20 MHz up to 7 GHz. When the resistivity is further increased from $200\Omega\text{cm}$ to $2000\Omega\text{cm}$, the magnitude response is significantly decreased up to only 700 Mhz. This is explained by that the capacitive coupling is dominating for frequencies above 760 MHz for the resistivity of $200\Omega\text{cm}$.

3.5 Packaging and pin assignment

The magnitude response from one region to another region on-chip is highly dependent on the parasitic impedance of the die package. The impedance from off-chip to on-chip differs between different types of packages. Consequently, the choice of package is very important when considering SSN. By choosing a low impedance package, as for example a ball grid array (BGA) package, the amount of SSN in the digital circuit can be minimized. Furthermore, with a low impedance from the analog ground on-chip to the ground off-chip, the substrate noise in the analog region can be further attenuated.

Instead of packaging the silicon die it is also possible to connect the die directly to a PCB via e.g. solder balls or bonding wires. The advantage is that interconnects from the PCB to the silicon die can be kept very short and therefore the parasitics can be kept low. For a more in depth analysis of packaging we recommend[6].

A straightforward method to decrease the inductance of the power supply is to use several dedicated pins and by this way reduce the effective inductance. SSN can be further reduced, if the pins are placed so that adjacent interconnects have currents pointing in opposite directions which minimize the current loop areas.

4. CONCLUSIONS

In this work we analyzed the magnitude response from a digital region to an analog region for SOI and bulk for different test structures of substrates. Simulation results from two simple test structures indicated that SOI had significantly less coupling compared to bulk. This discrepancy in coupling between SOI and bulk was valid up to frequencies of 2 GHz and 500 MHz for the respective structures. Hence, the frequency where the coupling in SOI becomes approximately the same as that in bulk, is very dependent on the chip structure. Increasing the distance between the circuits was effective to decrease the substrate coupling in both bulk and SOI. The cost of increasing distance is mainly the increased area. One test structure was analyzed with and without a guard band in between the circuits. In bulk, the guard reduced the coupling between the two circuits more drastically than in SOI. In SOI, a substrate with a high resistivity can be used which decreases the substrate coupling up to the frequency where the capacitive coupling becomes dominating. The importance of a proper package and pin assignment for low substrate noise was also discussed.

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Paper V

*Programmable Reference Generator
for On-Chip Measurement*

E. Backenius, E. Säll, K. Ola Andersson, and Mark Vesterbacka.

Manuscript

PROGRAMMABLE REFERENCE GENERATOR FOR ON-CHIP MEASUREMENT

E. Backenius, E. Säll, K. Ola Andersson, and Mark Vesterbacka.

ABSTRACT

In this work, circuits for on-chip measurement and periodic waveform capture are designed. The aim is to analyze disturbances in mixed-signal chips such as simultaneous switching noise and the transfer of substrate noise. A programmable reference generator that replaces the standard digital-to-analog converter is proposed. It is based on a resistor string that is connected in a circular structure. A feature is that the reference outputs to the different comparators in the measurement channels are distributed over the nodes of the resistor string. Comparing with using a complete converter, the use of a buffer is avoided. Hence there is a potential reduction in the parasitic capacitance and power consumption as well as an increase in speed.

1. INTRODUCTION

Many applications benefit from low-cost, on-chip measurement capabilities that are used to evaluate the circuit performance. For example, a small measurement circuit could monitor the operation of the application, detecting or even correcting faults. In this work we aim at designing a measurement circuit for capturing the characteristics of disturbances like simultaneous switching noise and noise transfer in mixed-signal chips. A goal is that the implemented circuit should have low overhead in terms of hardware. Hence the use of a measurement circuit that operates at the full application speed is avoided. Instead we have designed a circuit for capturing a periodic waveform in multiple passes in the application nodes of interest. Examples on similar circuits are evaluations of delay and noise, early capture and multi-pass waveform capture [1][2][3]. The developed circuit will subsequently be used in our further research to mitigate problems related to noise generation and reception.

Our work as well as others' are typically based on measurement channels constructed from a variable-reference comparator depicted in Fig.1. As

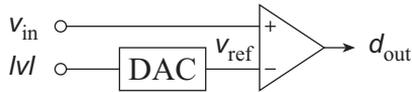


Figure 1: Variable-reference

shown, a comparator is used to compare the input v_{in} with a level v_{ref} that is programmed from the digital control word $|v|$. To capture the waveform of a periodic signal, several passes are made where the waveform is compared with a different reference level in each pass. The comparator output is stored in a memory and is used to reconstruct the waveform when the capture has completed. In an implemented circuit described towards the end of the paper, the result of the comparison will be stored in an off-chip memory, but it could of course be stored on-chip if the extra hardware required for the memory can be afforded.

In this work, we will in particular present a voltage reference generator circuit that replaces a standard digital-to-analog converter (DAC) in the measurement channels. The proposed circuit generates the voltage references directly from a special resistor string and uses the different nodes of the resistor string to obtain a distributed set of voltage references. The references can be used concurrently in the different channels. Hence the load on the resistor string is distributed and the buffer a standard DAC would have required can be eliminated. Another feature of the suggested approach is that the switches used to program the references are only connected directly to the voltage reference supply lines, hence eliminating further switches in the reference signal path.

The paper is organized as follows. In Section 2 the reference generator is presented. In Section 3 the design of a measurement circuit using the resistor structure described in 2 is presented. In Section 4, a test chip implemented in a 0.13 μ m SOI CMOS process is described, and the conclusions are given in the final Section 5.

2. REFERENCE GENERATOR

To be able to program a specific node of the resistor net to all the different reference voltages without switches in the reference signal path, we use a circular structure for the resistor string. The structure of this resistor net has earlier been used in a recent work [4] in the context of analog-to-digital conversion. In [4] the dynamic element matching technique was introduced in a flash analog-to-digital converter by using the circular, programmable structure to select different hardware paths over time for processing a certain

quantization level. This technique reduces the signal dependency of the errors, involving randomization in the program. In this work, we have reused the structure in a different context, i.e., to generate different reference levels to different measurement channels according to a deterministic program.

2.1 Circular resistor string

A well-known technique to design a monotonic DAC is to use a resistor string connected to a reference voltage supply at the ends [5][6][7][8]. To obtain programmability, a number of switches are connected to the different nodes in between the resistors that depending on binary input, connect one of the nodes to an output buffer.

In the approach used here, we instead use the circular structures illustrated in Fig.2. This approach yields simple hardware at the loss of monotonicity. There are N input pairs (s_{k+}, s_{k-}) , $k = 1, 2, \dots, N$ where the input reference voltage is applied with switches. There are also N output nodes r_i , $i = 0, 1, \dots, N-1$ that may be used as the programmable reference outputs. The structure in Fig.2 a) are used for odd N and the structure in b) for even N . By connecting the reference voltage to the different input pairs, all levels can be generated in all output nodes.

In Table 1, an example is given where all different possibilities of connections and the resulting output voltages are listed for $N=3$. To cycle between all levels for all outputs we can, e.g., connect the switches according to the sequence of cases I-V-III or IV-II-VI. Both these sequences allow us to connect switches to only half of the nodes.

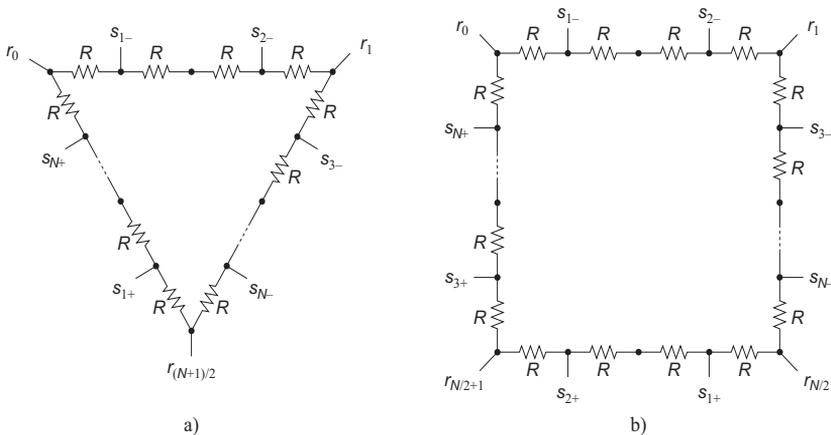


Figure 2: Circular resistor string with a) an odd and b) an even number N of output nodes and levels.

A formula for calculating the reference voltages of a net with a general number of levels N have been derived by transforming an equation describing a linear increase of the reference voltage with increasing node number. The transformations involved folding of the original equation into a periodic pattern by taking the fractional part and magnitude of the linear function with proper scaling and offsets. Connecting the voltage reference supply v_{ref} to input s_k for the first N levels, and the negative voltage reference 0 to input $s_{(k-N)}$ for the remaining N levels, the formula for calculating the output voltage reference in node i for $r_i(k)$ is

$$r_i(k) = 2v_{ref} \left| \frac{2k - 4i - 1}{4N} - \left\lceil \frac{2k - 4i - 1}{4N} - \frac{1}{2} \right\rceil \right|. \quad (1)$$

2.2 Reference generator structure

Adding switches to the different input pairs (s_{k+}, s_{k-}) obtain the programmability of the circuit. In Fig.3, a general generator structure has been outlined with a set of switches that connects the reference supply to the circular resistor string, and the reference outputs connected to a block of comparators. Note that the indices in Fig.3 do not agree with the notation above to simplify the drawing.

To the left in the drawing, there are N inputs denoted v_i that are connected directly to the comparators. Each comparator is connected to its own reference node in the circular resistor string. The comparators are designed to sample the comparison at times determined by the clock clk , which is distributed to the comparators. Programming the circuit is obtained by connecting the reference supply to the proper nodes in the resistor net with the switches in the bottom of the figure. Assuming the use of a CMOS implementation technology, the switches with connection to reference ground and supply can be implemented as nMOSFETs and pMOSFETs, respectively. Hence, a low impedance path is obtained.

Investigating the different choices of programming, it is seen that only half of the switches are required to implement all possible levels. Compare with the example given in Table 1. Hence, only N nMOSFETs and N pMOSFETs are required to generate all levels in all nodes. Which switches to keep do of course need to be selected during the design, but is not considered critical as long as all reference levels may be generated.

Connection			Reference voltage		
Case	0	v_{ref}	r_0	r_1	r_2
I	s_{1-}	s_{1+}	$\frac{1}{6}v_{\text{ref}}$	$\frac{3}{6}v_{\text{ref}}$	$\frac{5}{6}v_{\text{ref}}$
II	s_{2-}	s_{2+}	$\frac{3}{6}v_{\text{ref}}$	$\frac{1}{6}v_{\text{ref}}$	$\frac{5}{6}v_{\text{ref}}$
III	s_{3-}	s_{3+}	$\frac{5}{6}v_{\text{ref}}$	$\frac{1}{6}v_{\text{ref}}$	$\frac{3}{6}v_{\text{ref}}$
IV	s_{1+}	s_{1-}	$\frac{5}{6}v_{\text{ref}}$	$\frac{3}{6}v_{\text{ref}}$	$\frac{1}{6}v_{\text{ref}}$
V	s_{2+}	s_{2-}	$\frac{3}{6}v_{\text{ref}}$	$\frac{5}{6}v_{\text{ref}}$	$\frac{1}{6}v_{\text{ref}}$
VI	s_{3+}	s_{3-}	$\frac{1}{6}v_{\text{ref}}$	$\frac{5}{6}v_{\text{ref}}$	$\frac{3}{6}v_{\text{ref}}$

Table 1: Reference voltages for $N = 3$.

2.3 Control

A simple algorithm for controlling the switches is to loop through a number of cases in order. The control unit can be implemented with low complexity using a shift register with a circulating one that activates the switches in the determined order, or as a counter and a 1-of- N decoder.

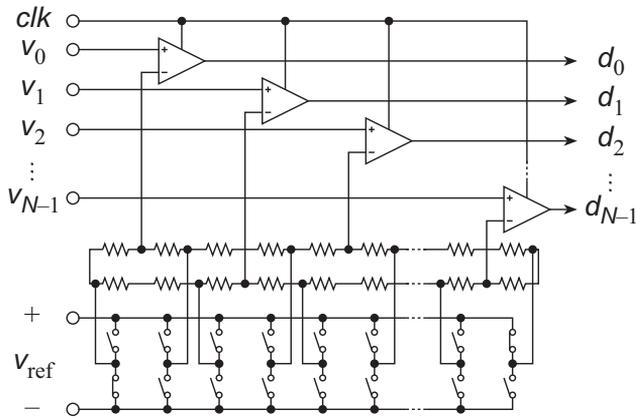


Figure 3: General structure of a reference generator connected to a comparator block.

3. ON-CHIP MEASUREMENT CIRCUIT

To illustrate the design and hardware required in an on-chip measurement circuit we have outlined an example circuit with $N=3$ and four captured samples describing the waveform of the three measured nodes. The hardware used in the example is given in Fig.4. As shown in the figure, there are four functional blocks; I, a comparator block; II the programmable reference generator; III the control unit providing the program and other control; and IV a simple data processing unit. Blocks I and II essentially follow the earlier description in Section 2, with elimination of MOSFETs that are not needed corresponding to the use of the case sequence I-III-V in Table 1. Block III, the control unit uses the approach with a counter and a decoder to program the switches. Besides producing the program sequence, it also produces the output *rdy* that is active high when the result becomes available from the data processing unit, and the binary output (o_1, o_0) that indicates what waveform sample that currently are output.

In the control unit, there is also an SR-latch that is used to capture a trigger-pulse on the input *tr*. After an active high trigger signal has been detected, four cycles of the free running clock *clk* will be forwarded to the internal circuits, causing one pass of comparisons to be performed and forwarded to the data processing unit. Note that in this simple outline, the trigger pulse and the external clock must be synchronized for the circuit to work properly.

Block IV, the data processing unit, collects comparison results and adds them to previous stored sample data in a shift register. As can be seen in the figure, the three inputs are connected to three identical subcircuits. The first Boolean operations in the subcircuit perform an addition between the input bit and a previously 2-bit sample in the shift register. This adder circuit has been

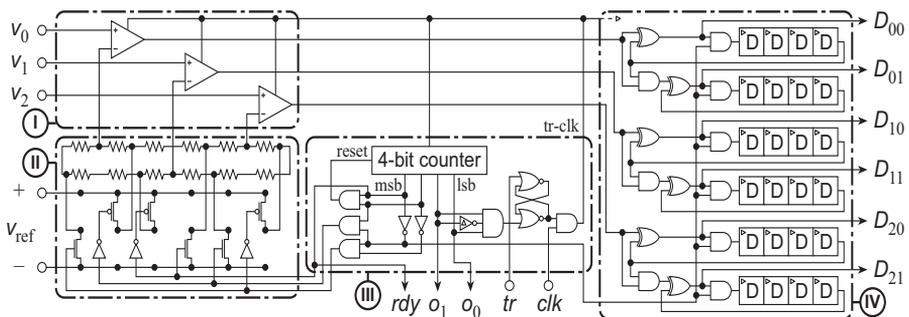


Figure 4: Principal design of 3-channel measurement circuit with functional blocks indicated: I comparator block, II reference generator, III control unit, and IV data processing unit.

simplified with respect to the short sample word length. Next, there is an AND gate that is used to clear the contents of the following shift register during the final pass, hence preparing for the next measurement. The output samples (D_{i1}, D_{i0}) are output during this pass as indicated by the state of (o_1, o_0) .

4. TEST CHIP

A test chip with $N=63$ has been implemented in a $0.13\ \mu\text{m}$ SOI CMOS process that is manufactured. There are two measurement channels that are connected to the power supply lines of a chain of buffers, aiming at characterizing the simultaneous switching noise of the configuration. A layout of the circuit is shown in Fig.5. The general structure in Fig.3 has been used without removing redundant switches. The control unit is implemented as a shift register with a circulating one. Subsequent data processing will be performed outside the chip. The measurement circuit occupies a core area of $0.48\ \text{mm}^2$, including the logic for controlling the reference generator, 126 switches and resistors, and two comparators. The total chip area is $2.4\ \text{mm}^2$.

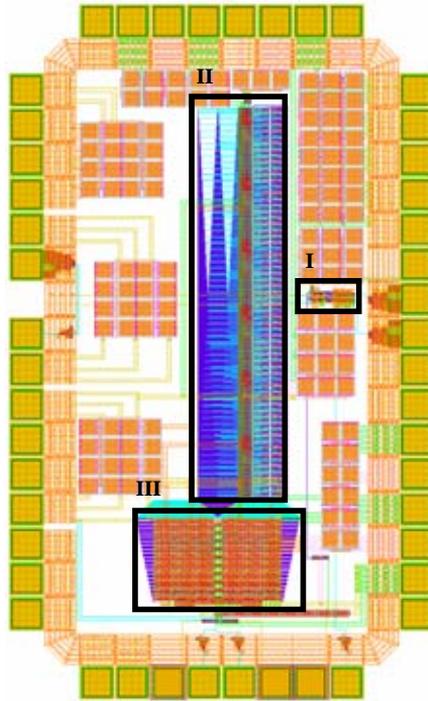


Figure 5: Chip layout with blocks indicated: I comparators, II reference, and III control.

5. CONCLUSIONS

The design of a measurement circuit was discussed, which used a special reference generator. The reference generator consisted of a circular resistor string programmed such that all outputs nodes in the resistor net could be distributed directly to a set of variable-reference comparators. The resulting measurement circuit uses multiple passes to capture the waveforms. Little hardware is required to implement the circuit, which is good for on-chip evaluation of an application. A test chip has been implemented to evaluate the approach.

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