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Reconfigurable and Broadband Circuits for Flexible RF Front Ends

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About the cover:

Top left picture: illustration of a highly linear, wideband RF front-end for multi-standard receivers that can withstand large blockers. 90nm CMOS chip micrograph on right. 0.2 μ m GaAs chip micrograph (left) and illustration of PROMFA concept with its three key functions.

Cover designed by author.

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Abstract

Most of today's microwave circuits are designed for specific function and special need. There is a growing trend to have flexible and reconfigurable circuits. Circuits that can be digitally programmed to achieve various functions based on specific needs. Realization of high frequency circuit blocks that can be dynamically reconfigured to achieve the desired performance seems to be challenging. However, with recent advances in many areas of technology these demands can now be met.

Two concepts have been investigated in this thesis. The initial part presents the feasibility of a flexible and programmable circuit (PROMFA) that can be utilized for multifunctional systems operating at microwave frequencies. Design details and PROMFA implementation is presented. This concept is based on an array of generic cells, which consists of a matrix of analog building blocks that can be dynamically reconfigured. Either each matrix element can be programmed independently or several elements can be programmed collectively to achieve a specific function. The PROMFA circuit can therefore realize more complex functions, such as filters or oscillators. Realization of a flexible RF circuit based on generic cells is a new concept. In order to validate the idea, two test chips have been fabricated. The first chip implementation was carried out in a 0.2 μm GaAs process, ED02AH from OMMICTM. The second chip was implemented in a standard 90nm CMOS process. Simulated and measured results are presented along with some key applications such as low noise amplifier, tunable band pass filter and a tunable oscillator.

The later part of the thesis covers the design and implementation of broadband RF front-ends that can be utilized for multistandard terminals such as software defined radio (SDR). The concept of low gain, highly linear frontends has been presented. For proof of concept two test chips have been implemented in 90nm CMOS technology process. Simulated and measurement results are presented. These RF front-end implementations utilize wideband designs with active and passive mixer configurations.

We have also investigated narrowband tunable LNAs. A dual band tunable LNA MMIC has been fabricated in 0.2 μ m GaAs process. A self tuning technique has been proposed for the optimization of this LNA.

Preface

This dissertation presents my research work during the period from June 2005 to May 2009, at the Division of Electronic Devices, Department of Electrical Engineering, Linköping University, Sweden. This thesis is mainly based on the following publications:

- **Paper 1: Naveed Ahsan**, Aziz Ouacha, Carl Samuelsson and Tomas Boman “Applications of Programmable Microwave Function Array (PROMFA),” in *Proceedings of the IEEE European Conference on Circuit Theory and Design (ECCTD 2007)*, pp. 164-167, August 26-30, 2007, Seville, Spain.
- **Paper 2: Naveed Ahsan**, Aziz Ouacha, Christer Svensson, Carl Samuelsson and Jerzy Dąbrowski “A Design Approach for Flexible RF Circuits Using Reconfigurable PROMFA Cells,” *manuscript submitted in Journal of Analog Integrated Circuits and Signal Processing*.
- **Paper 3: Naveed Ahsan**, Aziz Ouacha, Jerzy Dąbrowski and Carl Samuelsson “Dual band Tunable LNA for Flexible RF Front-End,” in *Proceedings of the IEEE International Bhurban Conference on Applied Sciences & Technology (IBCAST 2007)*, pp. 19-22, January 8-11, 2007, Islamabad, Pakistan.
- **Paper 4: Naveed Ahsan**, Jerzy Dąbrowski and Aziz Ouacha “A Self Tuning Technique for Optimization of Dual Band LNA,” in *Proceedings of the IEEE European Wireless Technology Conference (EuWiT), EuMW 2008*, pp. 178-181, October 27-28, 2008, Amsterdam, The Netherlands.

- **Paper 5: Naveed Ahsan**, Christer Svensson and Jerzy Dąbrowski “Highly Linear Wideband Low Power Current Mode LNA,” in *Proceedings of the IEEE International Conference on Signals and Electronic Systems (ICSES 08)*, pp. 73-76, September 14-17, 2008, Kraków, Poland.
- **Paper 6: Rashad Ramzan, Naveed Ahsan**, Jerzy Dąbrowski and Christer Svensson “A 0.5-6GHz Low Gain RF Front-end for Low-IF Over-Sampling Receivers in 90nm CMOS,” *manuscript submitted in IEEE Transactions on Circuits and Systems-II: Express Briefs*.
- **Paper 7: Naveed Ahsan**, Christer Svensson, Rashad Ramzan, Jerzy Dąbrowski, Aziz Ouacha, and Carl Samuelsson “A 1.1V 6.2mW, Highly Linear Wideband RF Front-end for Multi-Standard Receivers in 90nm CMOS,” *manuscript submitted in IEEE Journal of Solid State Circuits*.

The following publications related to this research are not included in the thesis:

- Carl Samuelsson, Aziz Ouacha, **Naveed Ahsan**, Tomas Boman “Programmable Microwave Function Array, PROMFA,” in *Proceedings of the IEEE Asia-Pacific Microwave Conference 2006 (APMC 2006)*, pp. 1787-1790, December 12-15, 2006, Yokohama, Japan.
- **Naveed Ahsan**, Aziz Ouacha and Jerzy Dąbrowski “A Tunable LNA for Flexible RF Front-End,” *Swedish System-on-Chip Conference (SSoCC06)*, May 4-5, 2006, Kolmården, Sweden.
- **Naveed Ahsan**, Aziz Ouacha, Carl Samuelsson and Tomas Boman “A Widely Tunable Filter Using Generic PROMFA Cells,” *Swedish System-on-Chip Conference (SSoCC07)*, May 14-15, 2007, Fiskebäckskil, Sweden.
- Shakeel Ahmad, **Naveed Ahsan**, Anton Blad, Rashad Ramzan, Timmy Sundström, Håkan Johansson, Jerzy Dąbrowski, and Christer Svensson, “Feasibility of Filter-less RF Receiver Front end,” *Giga Hertz Symposium 2008*, March 2008, Göteborg, Sweden.

I have also contributed in the following papers that are not related to this research:

- Ghulam Mehdi, **Naveed Ahsan**, Amjad Altaf, and Amir Eghbali “A 403-MHz Fully Differential Class-E Amplifier in 0.35 μ m CMOS for ISM Band Applications,” in *Proceedings of the IEEE East-West Design Test Symposium (EWDTS 2008)*, pp. 239-242, October 9-12, 2008, Lviv, Ukraine*.
- Rashad Ramzan, **Naveed Ahsan**, and Jerzy Dąbrowski “On-Chip Stimulus Generator for Gain, Linearity, and Blocking Profile Test of Wideband RF Front-ends,” *manuscript submitted in IEEE Transactions on Instrumentation & Measurement*.

* Best regular paper award

Contributions

The main contributions of this dissertation are as follows:

- Design of reconfigurable circuits using PROMFA concept. To demonstrate the viability of this approach, two test circuits have been implemented using 0.2 μ m GaAs and 90nm CMOS technology process.
- Design and implementation of a dual band tunable low noise amplifier in 0.2 μ m GaAs technology process. A self-tuning technique has been proposed for optimization of this LNA.
- Design and implementation of a wideband highly linear low noise amplifier in 90nm CMOS.
- Design, implementation and testing of a low power, highly linear wideband RF front-end for multistandard receivers in 90nm CMOS. The proposed front-end can withstand large blockers.
- Circuit implementation and testing of a wideband RF front-end with active mixer configuration for low-IF over-sampling receivers in 90nm CMOS.

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
CABs	Configurable Analog Blocks
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DR	Dynamic Range
DSP	Digital Signal Processor
EDGE	Enhanced GSM Evolution
FET	Field-Effect Transistor
FOM	Figure of Merit
FPAA	Field-Programmable Analog Array
FPGA	Field-Programmable Gate Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride

GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBT	Hetrojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IF	Intermediate Frequency
InP	Indium Phosphide
IP2	Second-Order Intercept Point
IP3	Third-Order Intercept Point
IIP3	Input Referred Third-Order Intercept Point
LNA	Low Noise Amplifier
MMIC	Monolithic Microwave Integrated Circuit
MBS	Mobile Broadband Services
MEMS	Micro-Electromechanical Systems
MESFET	Metal Semiconductor Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPW	Multi Project Wafer
NF	Noise Figure
NMOS	N-Channel Metal-Oxide-Semiconductor
OIP3	Output Referred Third-Order Intercept Point
PROMFA	Programmable Microwave Function Array
PMOS	P-Channel Metal-Oxide-Semiconductor
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RL	Return Loss
SAW	Surface Acoustic Wave
SDR	Software-Defined Radio
SFDR	Spurious Free Dynamic Range
SiC	Silicon Carbide

SiGe	Silicon Germanium
SNDR	Signal-to-Noise and Distortion Ratio
SPDT	Single Pole Double Throw
SNR	Signal-to-Noise Ratio
T/R	Transmit/Receive
UMTS	Universal Mobile Telecommunication System
UWB	Ultra Wideband
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
WLAN	Wireless Local Area Network
WPAN	Wireless Personal Area Network

Acknowledgments

It is indeed a moment of joy, as well as a bit of sadness that four years of exciting work has come to an end. I am very grateful to Allah almighty who has given me the strenght to carry out this job smoothly. The work presented here is not only just my effort but there is a lot of contribution and support from other people who deserve my warmest gratitude. Particularly, I would like to express my sincere gratitude to the following people who have always supported and encouraged me:

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Naveed Ahsan

Linköping, May 2009

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Part I

Background

Chapter 1

Introduction

“To realize the possible, the impossible has to be tried over and over again”.

Herman Hesse.

1.1 A Brief History of RF Technology

The success of today’s wireless communication technology and RFIC design is based on the enthusiastic efforts of brilliant scientists and creative engineers. In fact, the creative ideas and consequent commitment of these scientists made it possible for us to enjoy the technology benefits of today’s life. The following section will briefly discuss the key achievements in the area of wireless communications.

In 1800, Alessandro Volta demonstrated the existence of electric current and invented the battery. Later in 1820, Hans Oersted discovered that current and electromagnetic field are related. In 1864, James Maxwell described electromagnetic waves using his famous set of equations that serve as a base for wireless communication. In 1906, Lee De Forest designed a triode in a Vacuum tube, which was the first device that could amplify signals. Later in 1914, Edwin Armstrong developed the regenerative receiver and also in 1918 he invented super-heterodyne radio.

The idea of a semiconductor field effect transistor (FET) was launched and patented by Julius Lilienfeld in 1926. However, it took almost twenty years to develop an actual working semiconductor transistor. In 1947 John Bardeen, Walter Brattain and Walter Shockley at Bell Labs in California experimentally demonstrated the first working semiconductor transistor. Later in 1956, they received the joint Nobel Prize for their genius contribution [1]. At the same time, the German scientists Herbert Mataré and Heinrich Welker also invented a similar transistor [2]. A radio transceiver was successfully demonstrated using these transistors and later Mataré founded a company and launched first commercial radio product.

In 1958, Jack Kilby and Robert Noyce developed the idea of integrated circuits. With the integration of multiple devices on a single chip the size, weight and cost were significantly reduced. With photolithography it was possible to implement multiple layers with specific properties. Bell scientist John Atalla developed the MOSFET in 1960 based on Shockley's theories.

Wireless phone transmission via satellite started in 1965 and first WLAN transmission was performed by University of Hawaii in 1971. GPS (Global Positioning System) was developed in 1989. GSM-900 (Global System for mobile communication) was launched in 1991. WLAN standards (e.g. 802.11 a,b, etc) were defined in 1997 and UMTS (Universal Mobile Telecommunications System) was launched in 2003.

The very large scale integration (VLSI) technology has developed to the point where more than one billion transistors can now be integrated on a single die or chip. Recently, Intel introduced its new 2 Billion transistor microprocessor chip Tukwila [3,4]. It is the first quad-core member of the

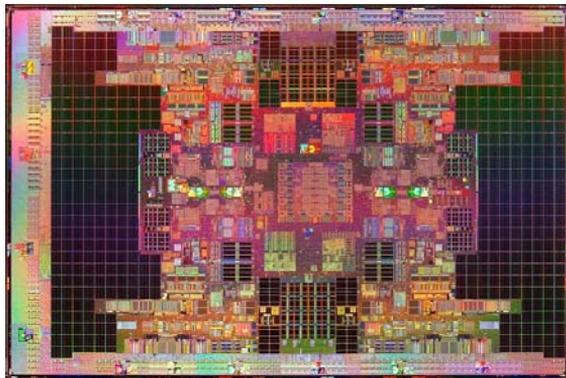


Figure 1.1 Tukwila's die micrograph (source: Intel)

Itanium® product family and the world's first processor to break the 2 Billion transistor mark. Tukwila's die size is $21.5 \times 32.5 \text{mm}^2$ using 65nm technology process with 2.046 Billion transistors (die micrograph shown in Fig 1.1). The first run of chipsets will reach speeds of up to 2GHz on 170W of power. Indeed, it is a remarkable growth in technology. In last few decades, the availability of mobile communication and personal computers to the commercial market was one of the prime reasons for this rapid growth.

1.2 Overview of RF Applications

Along with Military and Space applications there is a wide range of commercial applications that include wireless phones, networks, positioning and sensors. The major commercial market volume is in wireless phones followed by wireless networks and positioning. The availability of a mobile phone to an average consumer was the turning point of this growth. Approximately 1.15 Billion mobile phones were sold worldwide in 2007 [5]. Estimates indicate that in future this growth will increase due to more number of users and improved functionality of existing systems. The introduction of new functions such as Internet, GPS, Video and Audio streaming with high data rates have generated the need for improved functionality mobile phones. Cellular systems have evolved from first generation 1G to third generation 3G within a short span of time. The initial 1G cellular systems used analog frequency modulation and were operating in frequency bands around 450MHz and 900MHz. In 2G systems, the analog modulation schemes have been replaced by digital modulation schemes. GSM is the leading standard for 2G systems and used worldwide. The frequency of operation is around 900MHz and 1800MHz. However, in North America the frequency bands of 800MHz and 1900MHz are used. Modern GSM mobile phones operate in quad-band (i.e. 800, 900, 1800, 1900MHz). 2.5G standards such as GPRS (General Packet Radio Service) and EDGE (Enhanced Data Rates for Global Evolution), allow higher data rates. The maximum data rate specified in standard for GPRS and EDGE is 115Kbits/s and 384Kbits/s respectively. 3G standard, such as CDMA 2000 (Code Division Multiple Access 2000) and UMTS (Universal Mobile Telecommunication Service) provide further improvement in data rates. The standard indicates maximum data rates up to 2Mbits/s operating at 2.4GHz frequency band. Next generation standards aim to combine higher data rates with an increased level of reconfigurability. Multimode and multiband operation that can provide global roaming but at a low cost, and with low power consumption is the ultimate goal.

After cellular systems, wireless networks occupy most of the commercial market volume. WLANs (Wireless Local Area Networks) standards include important standards like 802.11a/b/g. WPANs (Wireless Personal Area

Networks) include Blue-tooth and UWB (Ultra-Wideband). Potential applications are high-speed short range communication, internet access, video streaming, traffic control, medical imaging, security systems and sensors. For data rates above 100Mbps MBS (Mobile Broadband Services) have proposed 27GHz to 60GHz band for millimeter wave WLANs. The 802.15.3 working group for WPAN aims to establish a standard with 7GHz bandwidth around 60GHz that will allow data rates above 1Gbits/s [6].

1.3 Development of MMIC Technology

A microwave circuit in which the active and passive components are fabricated on the same semiconductor substrate is referred as MMIC (monolithic microwave integrated circuit). The frequency of operation can range from 1GHz to well over 100GHz [7]. MMIC design is very different to conventional VLSI design, in which CAD offers a high degree of layout automation. The transmission line nature of interconnects on MMIC requires far more improvement from the designer in the layout process. Analog design still requires a “hands on” design approach in general therefore MMICs may have rather lower apparent circuit complexity than other integrated circuits however they are tough to design.

Development of MMIC started with the availability of high resistivity GaAs (Gallium Arsenide) material. In 1967, Plessey Optoelectronics and Microwave Ltd. launched first commercial device (4 μ m GaAs transistor). Later in 1968, Texas Instruments developed the first GaAs MMIC incorporating diodes and microstrip lines. The development of electron beam lithography allowed the first 1 μ m device to be produced in 1971. MMICs predominantly use GaAs for two key reasons:

- (a) GaAs has higher saturated electron velocity and low-field mobility than silicon, resulting in faster devices.
- (b) GaAs can readily be made with high resistivity, making it suitable substrate for high frequency passive components.

Therefore, GaAs completely dominated the first 15 years of MMIC development and even now the vast majority of MMICs are GaAs based.

The initial GaAs transistors were MESFETs, later the GaAs based pseudomorphic HEMT (high electron mobility transistor) offered much better performance. Circuits operating at 100GHz were reported with 0.1 μ m HEMT devices [8]. InP (Indium phosphide) based HEMTs showed excellent performance at extreme frequencies and amplifiers operating over 100GHz with very low noise figure have been reported [9,10]. Along with HEMT devices,

heterojunction bipolar transistor (HBT) based on GaAs and InP are useful for extreme high frequency circuits. Space and Military applications have been a major driving force behind MMIC technology. The adaptive phased-array antenna is one example of MMIC application where the cost and size has been reduced significantly.

1.4 Comparison of MMIC Materials

As discussed in previous section GaAs and InP were common materials for initial MMICs. However, with improvement in technology SiGe (silicon germanium) also became a good candidate for MMIC design. With technology scaling f_T and f_{max} of CMOS devices are touching extreme frequencies. Table 1.1 shows the predicted scaling of CMOS technology according to ITRS 2007 [11].

TABLE 1.1
PREDICTED SCALING OF CMOS TECHNOLOGY (ITRS 2007)

Year of production	2010	2013	2016	2019	2022
Technology process [nm]	45	32	22	16	11
Nominal V_{DD} [V]	1.0	1.0	0.8	0.8	0.7
T_{ox} [nm]	1.5	1.2	1.1	1.0	0.8
Peak f_T (NMOS) [GHz]	280	400	550	730	870
Peak f_{max} (NMOS) [GHz]	340	510	710	960	1160
$NF_{min @ 5GHz}$ (NMOS) [dB]	<0.2	<0.2	<0.2	<0.2	<0.2
1/f noise [$\mu V^2 \cdot \mu m^2 / Hz$]	90	60	50	40	30
I_{DS} for $f_T = 50GHz$ [$\mu A / \mu m$]	8	6	4	3	2
g_m / g_{ds} at 5.L _{min-digital}	30	30	30	30	30

Technology scaling has made CMOS much more attractive for high frequency circuit design. In recent years extensive work has been performed on CMOS RFICs and circuits operating around 60GHz have already been reported [12]. Key characteristics of different materials and a comparison of MMIC technologies are given in Table 1.2 [1]. Currently devices based on SiC (Silicon carbide) and GaN (Gallium nitride) are commercially available and have shown excellent performance particularly for high power amplifier applications. SiC and GaN are also considered promising candidates for future MMICs.

TABLE 1.2
KEY CHARACTERISTICS AND COMPARISON
OF MMIC TECHNOLOGIES

	Si	SiC	InP	GaAs	GaN
Electron mobility At 300°K [cm^2/Vs]	1500	700	5400	8500	1000 -2000
Hole mobility At 300°K [cm^2/Vs]	450	n.a.	150	400	n.a.
Peak electron velocity [10^7 cm/s]	1.0	2.0	2.0	2.1	2.1
Band gap [eV]	1.1	3.26	1.35	1.42	3.49
Critical break-down field [MV/cm]	0.3	3.0	0.5	0.4	3.0
Thermal conductivity [W/cm.K]	1.5	4.5	0.7	0.5	>1.5
Relative dielectric constant	11.8	10.0	12.5	12.8	9
Substrate resistance [Ωcm]	1-20	1-20	>1000	>1000	>1000
Number of transistors in IC	>1 billion	<200	<500	<1000	<50
Transistor type	MOSFET, Bipolar, HBT	MESFET, HEMT	MESFET, HEMT, HBT	MESFET, HEMT, HBT	MESFET, HEMT
Costs: Prototype /mass fabrication	High /Low	Very high /n.a.	High/ Very high	Low /High	Very high /n.a.
Ecological compatibility	Good	Good	Bad	Bad	Bad

1.4.1 Speed

The carrier drift velocity gives an insight regarding the speed of device. The carrier drift velocity is a function of applied electric field. Fig 1.2 shows the electron and hole drift velocities for both GaAs and Silicon. The figure indicates that velocity of electrons is higher than that of holes for low and moderate electric fields. Also approximately the peak electron velocity of GaAs is two times higher than that of Silicon. The hole velocity is higher in Silicon as compared to GaAs therefore complementary technologies featuring both type of

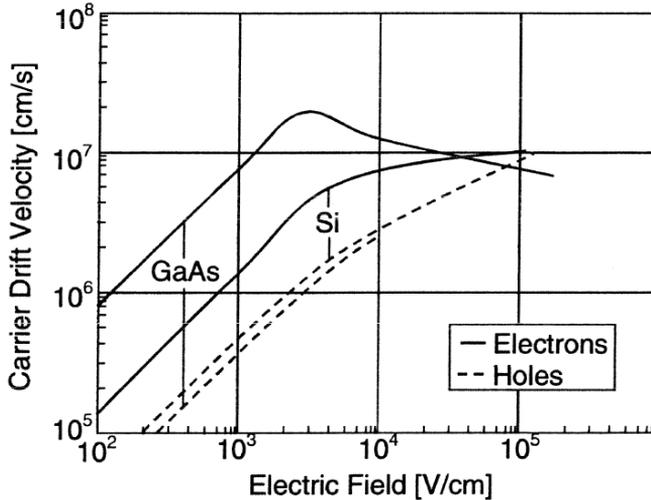


Figure 1.2 Drift velocity of electrons versus electric field, $T=300^{\circ}\text{K}$

carriers are applied. In contrary to Silicon the difference between electron and hole velocity is significant therefore complementary technologies are not feasible. Another important indicator of speed is mobility that is given by:

$$\mu = \frac{dv}{dE} \quad (1.1)$$

The mobility μ describes how fast the carrier velocity and the associated current can be varied with respect to an applied electric field E . The time required for carries to reach the maximum frequency is determined by the mobility. Fig. 1.3 shows the mobility of electrons and holes in Silicon and GaAs versus the level of impurities. The plot clearly indicates that compared to GaAs the electron mobility of Silicon based technology is lower. In addition, the mobility of electrons is higher than that of holes, almost 2.5 times higher in Silicon and more than 10 times higher in GaAs. Therefore, for high-speed applications, electrons rather than holes are usually applied as carriers. However, complementary technologies offer certain advantages in the design of analog and mixed-signal circuits, such as current reuse technique can be applied to reduce the overall power consumption. The linearity can also be improved by utilizing complementary technology as indicated by our research (**Paper 7**).

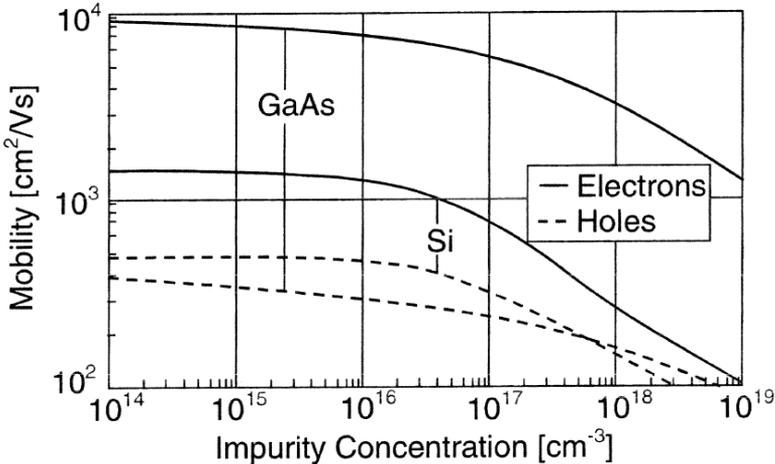


Figure 1.3 Mobility of carriers with respect to impurity concentration, $T=300^{\circ}\text{K}$

1.4.2 Integration

GaAs suffers from limited fabrication yield, typical transistor count in GaAs chips is around 1000. Silicon fabrication yield is much better and more than one billion transistors can be implemented on a single chip. Therefore, from SOC (system on chip) point of view Silicon is the only appropriate candidate. As a result, the commercial interest is very much in Silicon RFICs.

1.4.3 Cost

In today's consumer market there is a strong competition. Therefore, low-cost is the prime goal of IC manufacturers in order to capture the market. Usually, GaAs based technology has lower fixed cost than Silicon based technologies since less processing steps are required [1]. Hence, low volume prototyping costs for GaAs technology is relatively small. The fixed costs are mainly determined by the costs of lithographic masks. However, in mass fabrication, costs can be scaled down more significant for Silicon based technologies due to low variable fabrication cost per IC. Silicon material, which is based on quartz sand, is quite cheap. Therefore, for Silicon based technologies, lower material cost, large wafer size and high yield are the key factors that keep the mass fabrication cost low. Table 1.3 shows the comparison of IC fabrication costs for prototyping and mass fabrication for both technologies excluding the testing and packaging costs [1].

TABLE 1.3
APPROXIMATE IC FABRICATION COSTS

Technology	Prototyping cost (MPW)		Mass fabrication (100 wafer)
	Run cost (€)	1mm ² IC cost (€)	1mm ² IC (€)
0.2μm GaAs PHEMT $f_T = 80\text{GHz}$	12,000	80	< 1.0
90nm CMOS $f_T = 110\text{GHz}$	50,000	330	< 0.1

MPW: Multi Project Wafer, numbers estimated in 2006

1.4.4 Output Power

The speed of CMOS technology is achieved by aggressively downscaling of dimensions. As a consequence, at lower dimensions, the voltages have to be scaled as well to keep the electric field below a critical value. Hence, a major drawback of nanometric CMOS technology is the decrease of maximum possible RF output power.

III/V based technologies do not have to be scaled as aggressively as the Silicon counterparts due to the advantage in terms of speed. Therefore, generally, the supply voltage and associated RF output power is larger. Due to this advantage, mostly GaAs and InP based power amplifier ICs are still used in mobile phones [13].

SiC and GaN based power amplifiers are superior for high power applications as they can handle very high electric fields due to their large band-gap. In addition, their superior thermal conductivity is a big advantage.

1.4.5 Ecologic Compatibility

Considering the recycling or disposal of IC trash, the Silicon based technologies are compatible with environment, since it is based on the natural material quartz sand. Alternatively, GaAs and InP based ICs contains very poisonous materials like arsine and they are not directly compatible with the environment.

1.5 Future Trends and Challenges

Silicon CMOS technology is the leading technology and plays the most important role of today's IC market. The major reasons are low cost in mass fabrication and the excellent ability for highest level of integration. Reduced supply voltage with technology scaling is one drawback for analog circuit designers. As a consequence the analog circuit design in nanometric CMOS technology is challenging. Fig 1.4 shows an application spectrum and semiconductor devices likely to be used in that frequency range today [11]. Silicon technologies are gradually taking over the RFIC commercial market share from their counterparts due to low-cost chipsets. However, for Military and Space applications where extremely high frequency operation is required, GaAs and InP based devices will continue playing their dominant role. Due to the availability of high resistivity substrate in III/V based technologies, the passive components in these technologies offer much better performance. Therefore, they are suitable choice for extremely high frequency circuits. Fig 1.5

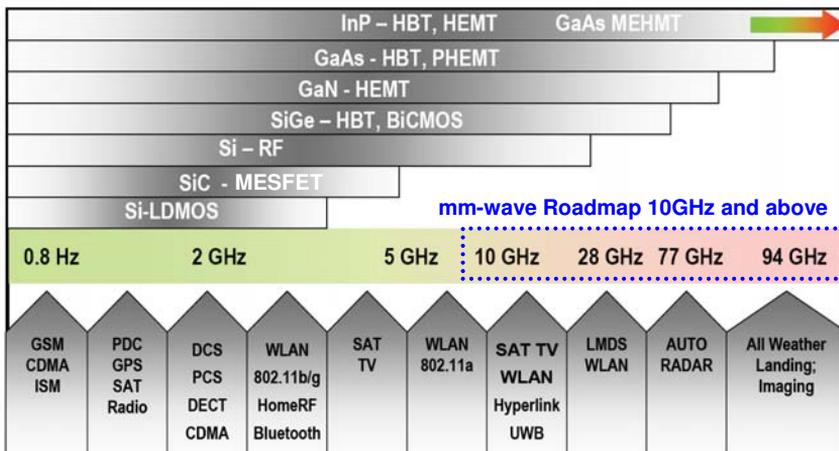


Figure 1.4 Application spectrum and semiconductor devices likely to be used today

shows the operating frequency of GaAs and InP based device [13]. Limited fabrication yield of III/V based technologies is a major drawback. Hence, from SOC point of view CMOS is the only appropriate candidate. The future wireless market interest is in CMOS as it provides the possibility to develop and mass-produce low cost chipsets. Radio transceivers for WLAN and GSM applications based on CMOS exclusively have already been reported [14,15].

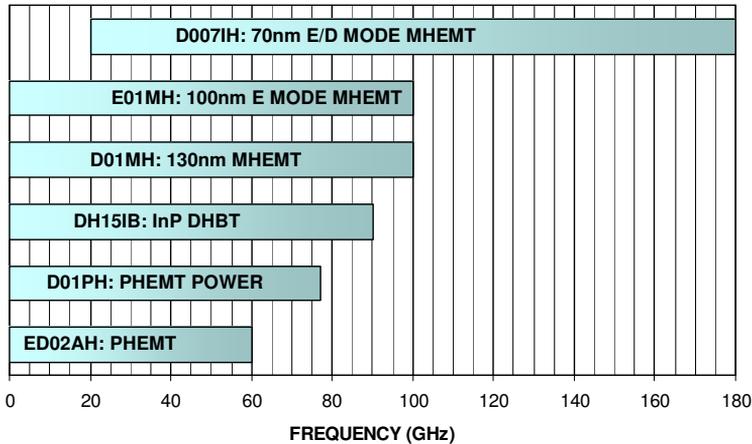


Figure 1.5 Operating Frequency of GaAs and InP based devices

1.6 Motivation and Scope of Thesis

The wireless market is growing at a fast rate; consequently, the RFIC market will continue its rapid growth. The main markets for RFICs involve wireless phones, network, positioning and sensors. There is a growing trend to merge several applications into one device. Therefore, there is a need for reconfigurable circuits. Advantages of reconfigurability are lower overall costs, smaller system size and high market potential.

Two concepts have been investigated in this thesis. The initial part presents the feasibility of a flexible and programmable circuit (PROMFA) that can be utilized for multifunctional systems operating at microwave frequencies. Design details and PROMFA implementation is presented in **Paper 1**. This concept is based on an array of generic cells, which consists of a matrix of analog building blocks that can be dynamically reconfigured. Either each matrix element can be programmed independently or several elements can be programmed collectively to achieve a specific function. The PROMFA circuit can therefore realize more complex functions, such as filters or oscillators. Realization of a flexible RF circuit based on generic cells is a new concept. In order to validate the idea, a test chip has been fabricated in a $0.2\mu\text{m}$ GaAs process, ED02AH from OMMICTM. Simulated and measured results are presented along with some key applications like implementation of a widely tunable band pass filter and an active corporate feed network. **Paper 2** addresses the CMOS implementation of PROMFA concept. A test chip has been implemented in a standard 90nm

CMOS technology process. A cell topology with low noise amplifiers have been utilized for this implementation. The test chip demonstrates that with dynamic reconfiguration the same circuit can perform various functions such as tunable oscillator, tunable band pass filter and a low noise amplifier. Chip measurement results indicate a good performance in all three configurations.

The later part of the thesis covers the design and implementation of broadband circuits for multistandard terminals such as software defined radio (SDR). One of the key components in the design of a flexible radio is low noise amplifier (LNA). Considering a multimode and multiband radio front-end, the LNA must provide adequate performance within a large frequency band. Optimization of LNA performance for a single frequency band is not suitable for this application. Narrowband tunable LNAs and wideband highly linear LNAs have been investigated. **Paper 3** and **Paper 4** presents the design and implementation of a dual band tunable LNA. For the optimization of this LNA a self-tuning technique has also been proposed. A dual band tunable LNA MMIC has been fabricated in 0.2 μ m GaAs process. **Paper 5** presents the design of novel highly linear current mode LNAs that can be used for wideband RF front-ends for multistandard applications. Technology process for this circuit is 90nm CMOS. **Paper 6** and **Paper 7** covers the design and implementation of wideband RF front-ends. Two test circuits have been implemented utilizing both active and passive mixer configurations. **Paper 6** presents a 0.5-6GHz low gain RF front-end for low-IF over-sampling receivers with an active mixer configuration. **Paper 7** presents a 6.2mW, highly linear, wideband RF front-end for multistandard receivers. The proposed front-end makes use of a highly linear LNA followed by a passive mixer. The front-end can also withstand large blockers. Simulation and chip measurement results are presented.

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Chapter 2

Radio Receiver Architectures

The main function of a receiver front-end is to receive the desired signal in the presence of undesired interferers (usually called blockers) and noise. Depending upon the scenario the received signal may be very weak if the transmitter is far away while at the same time the interferes may be quite strong. Detection of wanted signal in the presence of strong interferers is a challenging job. In addition to this, the wanted signal may also vary in strength due to different scenarios. Therefore, a wide dynamic range is also required. The key design specifications of a radio receiver include sensitivity, selectivity, blocker immunity, power consumption and most important for commercial market the cost. Considering a multimode and multiband radio receiver the front-end should provide the capability to operate the radio in multiple bands for various standards. The provision of GPS, WLAN along with multiband cellular operation to a single mobile phone is a typical commercial example. It is also necessary to limit the additional hardware, particularly; filters, resonators, oscillators, and frequency synthesizers. Therefore, design of a flexible RF front-end under these stringent requirements is challenging.

The initial part of this chapter provides an overview of traditional radio receiver architectures while the later part provides a discussion on flexible receiver architectures.

2.1 Super-Heterodyne Receiver

In 1918, Armstrong proposed the super-heterodyne receiver architecture. Most modern receivers still use similar approach for frequency downconversion with some refinements. The major advantages of a super-heterodyne receiver are its high sensitivity, excellent selectivity and good image rejection. Fig. 2.1 shows the block diagram of a classical super-heterodyne receiver. The received signal from the antenna is filtered by RF band pass filter, amplified by a low noise amplifier. The image frequency is filtered by an image reject filter and the signal is downconverted to a fixed intermediate frequency IF by means of a mixer. The channel select filter selects the desired channel and finally the wanted signal is digitized by an ADC followed by digital demodulation in DSP. Considering the Image problem, a large IF frequency is favorable to relax the requirements for the image rejection filter. A low IF on the other hand relaxes the channel filter requirement. Therefore, the choice of IF is a tradeoff between receiver selectivity and Image rejection. However, this tradeoff can be mitigated by using the dual super-heterodyne architecture [1]. Fig. 2.2 shows this architecture where two different IF frequencies are used. Image rejection is carried out at high IF while the channel selection is accomplished at low IF. Hence, the requirements of both filters can be relaxed simultaneously. For the first VCO, a constant frequency can be used and the frequency tuning is performed by the second VCO that operates at lower frequency. This architecture provides excellent selectivity along with good image rejection.

The major drawback of super-heterodyne receiver is its incompatibility with on chip implementation. Since high Q filters are required for image rejection, typically external SAW (Surface Acoustic Wave) filters are used as on chip implementation of such high Q filters is not feasible. Therefore, a single chip

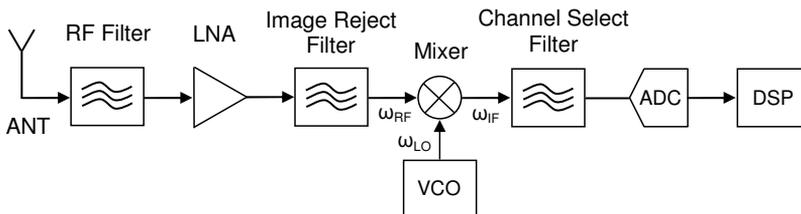


Figure 2.1 Super-Heterodyne receiver with single down-conversion

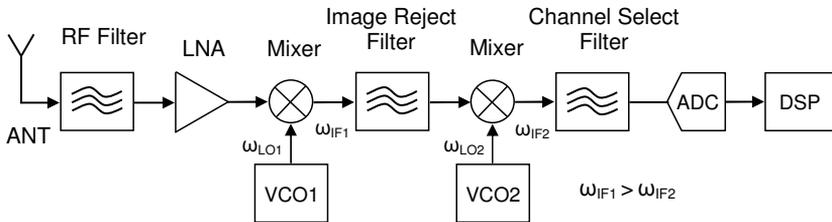


Figure 2.2 Super-Heterodyne receiver with double down-conversion

solution with this architecture is rather difficult to build also the receiver with off-chip components like the external filters consume relatively high power [2].

2.2 Homodyne Receiver

In a homodyne receiver the RF signal is directly downconverted to zero-IF frequency [3,4]. It is also called zero-IF or direct conversion receiver. Fig. 2.3 shows the architecture of a homodyne receiver. This architecture does not require an external high Q image reject filter. Also, the channel select filter can be a simple low pass filter. Therefore, fully integrated on-chip solution is feasible. Since IF frequency is zero, the sidebands allocated around the carrier frequency are translated to DC (0 Hz). For sophisticated frequency and phase modulation schemes, the information of both sidebands can be different, therefore, after conversion around DC, these sidebands can not be separated [5]. This can be prevented by using quadrature mixing with in-phase (I) and quadrature (Q) signals as illustrated in Fig. 2.3. Hartley and Weaver image reject techniques are most widely used. Both techniques are based on the idea of producing two paths having the same polarity for the desired signal, and the opposite polarity for the image signal. Finally, the combination of two paths recovers the desired signal and cancels the image signal [6]. The homodyne receiver shown in Fig 2.3 incorporates the Hartley image reject technique.

The homodyne receiver also has some disadvantages. Since the RF carrier and the local oscillator are at the same frequency, therefore, LO leakage to the mixer input can lead to self mixing resulting in a time-varying DC offset at the output of the mixer. This DC offset not only corrupts the wanted signal but also lead to a saturation of the following stages. As a consequence, the upper boundary of the dynamic range is significantly degraded. To avoid this problem DC offset cancellation circuits are used.

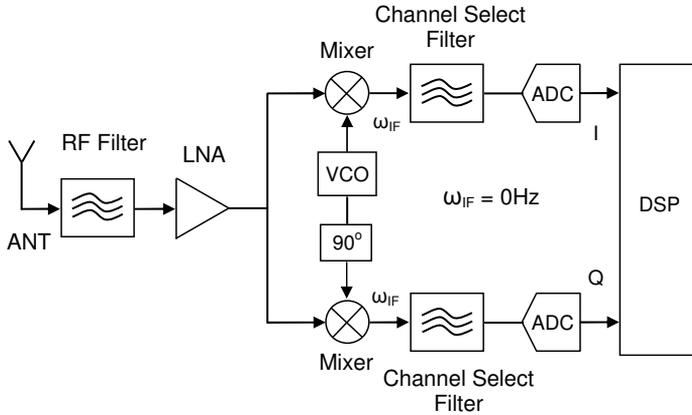


Figure 2.3 Homodyne receiver

The $1/f$ noise becomes significant at low frequencies. As the downconverted signal is around DC, therefore, $1/f$ noise becomes a problem and the wanted signal badly suffers. As a result, the lower limit of the dynamic range is degraded. Some techniques have been proposed to solve this problem [7,8].

The homodyne receiver is also sensitive to I/Q mismatch. The gain and phase errors between I and Q paths can severely degrade the image rejection. However, these errors are not considered significant as they can be corrected in the digital domain.

2.3 Low IF Receiver

Low IF receiver is a compromise between the heterodyne and super-heterodyne and it combines the advantages of both receivers. Fig. 2.4 shows the block diagram of a low IF receiver. Typically, the IF frequency is chosen to be one or two times the channel bandwidth [9]. Due to low IF frequency the channel filtering is relatively simple and all relevant filters can be implemented on-chip. The advantage of low IF receiver is that there is no problem of DC offset, LO leakage and $1/f$ noise. The image rejection can be performed by either Hartley or by Weaver quadrature downconversion technique.

Like homodyne receiver, the low IF receiver is also sensitive to I/Q mismatch. For fully integrated solutions with symmetrical designs, the gain and phase errors between I and Q paths are usually small. It is also possible to correct these errors in the digital domain therefore, practical implementations typically exhibit image rejection of more than 30dB [10].

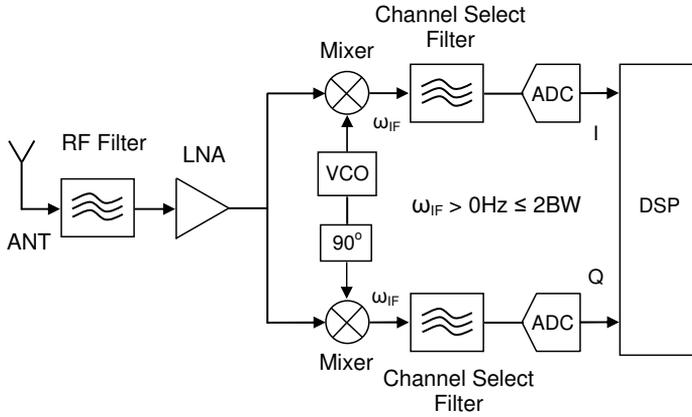


Figure 2.4 Low IF Receiver

2.4 Flexible Receiver Front-end

The choice of radio receiver architecture strongly depends on the system specifications and application. Digitalized radio receivers can offer more flexibility due to their powerful signal processing capability. With the availability of high performance ADCs the analog to digital conversion can be performed directly at RF frequency. Fig. 2.5 illustrates the architecture of a digitalized radio receiver that performs downconversion and demodulation in digital domain [11]. With this topology, the demodulation of multiple channels can be performed simultaneously by means of parallel DSP blocks. Therefore, a multistandard radio that can be reconfigured by software can be realized by this architecture. However, in practice, the ADC limits the dynamic range of such a receiver. Typically, ADCs for this high-speed operation consumes much more power therefore, this solution is not feasible for portable devices.

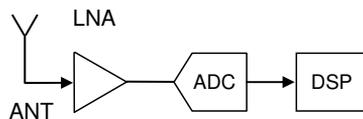


Figure 2.5 Digitalized Receiver with RF Analog to Digital Conversion

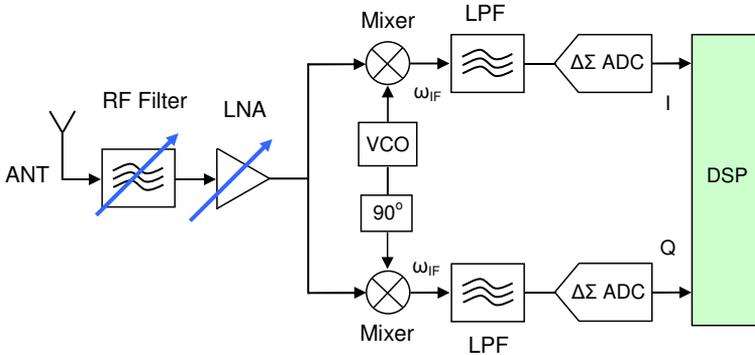


Figure 2.6 Flexible Receiver Frontend for Multistandard Radio

Another alternate approach is RF-Sampling Receiver. Various topologies have already been proposed [12-15]. The direct RF-Sampling technique provides great flexibility in the implementation of a reconfigurable radio [14].

As discussed in the previous section, the homodyne and low IF topologies are best suited for on-chip implementations. With multiband LNA and programmable filters, these architectures can be very flexible and hence they are popular candidates for multimode receivers. We have investigated the feasibility of a filter-less radio receiver front-end [16]. The channel selection in proposed architecture (Fig. 2.6) is performed digitally. The baseband signal is band limited by simple on-chip second order LPF that also helps in reducing the level of out of band blocker signals. The desired baseband signal (including adjacent channel blockers) is noise shaped by over-sampled $\Delta\Sigma$ -ADC. Both low pass and band pass $\Delta\Sigma$ -ADC topologies are feasible for this architecture. With this architecture, a relatively large dynamic range can be achieved. The RF filter requirements can also be relaxed and even it can be avoided if the following stages are highly linear. In operation, the proposed architecture is similar to [17] where a pseudodirect conversion topology is used for a multimode cellular radio. Like [17] it can either operate as a low IF receiver for narrowband standards such as GSM, EDGE etc. or as a zero IF receiver for wideband standards like WCDMA. Therefore, the proposed architecture offers a flexible on-chip radio receiver solution. However, the linearity requirements are extremely tough and the lower limit of the dynamic range may also degrade due to the thermal noise (KT/C) of the sampling capacitor at the input of ADC.

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Chapter 3

Programmable Microwave Function Array (PROMFA)

Most of today's microwave circuits are designed for specific function and special need. This conventional way of designing these high frequency circuits limits their ability to adapt to new demands and consequently it limits the flexibility of the whole system. There is a growing trend to have flexible and reconfigurable circuits. Circuits that can be digitally programmed to achieve various functions based on specific needs. With the recent advances in technology, these demands can now be met. Some efforts have been made with evolvable hardware, such as [1], where a mixer is automatically adjusted for best performance. The idea of having flexible RF systems with reconfigurable circuit blocks is becoming more and more popular. Various solutions have already been proposed for example: a flexible VCO based on tunable active inductor in [2], and a reconfigurable band pass filter for multifunctional systems in [3]. Some approaches of reconfiguration are based on MEMS (Micro-electromechanical systems), such as a reconfigurable power amplifier and a flexible low noise amplifier reported in [4-5].

FPA (Field Programmable Analog Array) is another approach for the implementation of reconfigurable circuits [6-11]. In this approach, two dimensional array of CABs (Configurable Analog Blocks) is utilized for the implementation of flexible filters. These CABs include digitally configurable transconductance amplifiers connected through a hexagonal interconnect network. Various filter configurations can be implemented by means of reconfigurable signal routing inside the array.

This chapter provides the details of PROMFA (Programmable Microwave Function Array) circuit which consists of a matrix of analog building blocks that can be dynamically reconfigured [12,13]. Either each matrix element can be programmed independently or several elements can be programmed collectively to achieve a specific function. The PROMFA circuit can therefore realize more complex functions, such as filters or oscillators.

3.1 PROMFA Concept

The concept is based on an array of generic cells. The idea is similar to a FPA approach, but for analog signals in the microwave region. A block schematic overview of such a system is illustrated in Fig. 3.1. Here the analog building blocks (PROMFA cells) are connected together, and to control the behavior of each analog cell digital control logic is placed between them. The individual PROMFA cells can be configured in a number of ways, for example as an amplifier, power splitter, power combiner, router etc. The array can therefore realize more complex functions, such as filters or oscillators. The PROMFA system utilizes a 2D mesh network topology which is also common routing topology used by digital network routers.

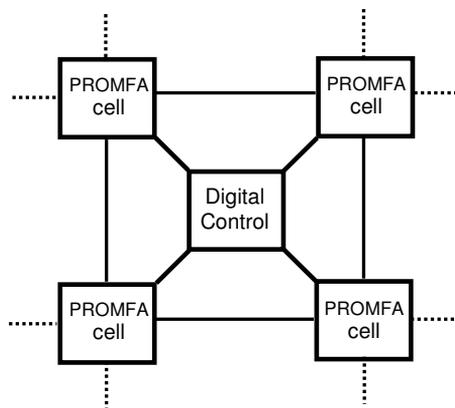


Figure 3.1 PROMFA concept illustrated by block diagram

3.2 Single PROMFA Cell

The PROMFA cell has several different possibilities to connect the four different ports to each other. Because of the symmetry of the cell, any port can be either an input or an output. The signal path can be either of pass-transistor type (simple switch) or amplifying depending on the biasing of the cell. This gives a number of different configurations. A single cell is described in the block schematic in Fig. 3.2. At each of the four ports, a transistor switch is placed to open or close the port. The transistor size is adjusted to achieve good matching both to other cells and to a 50 ohm system. The eight grey blocks are common source amplifier stages with transistor arrays. The white blocks are switching transistors, used for bi-directional signal paths. By activating different stages, the different functions can be realized [13].

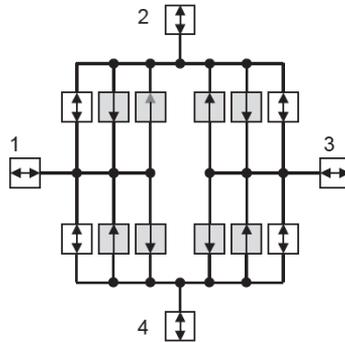
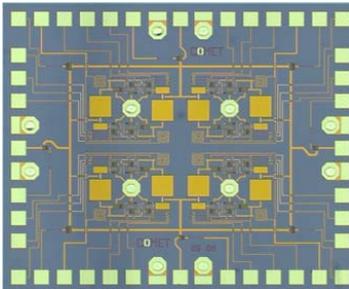
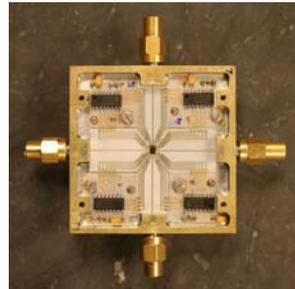


Figure 3.2 Block diagram of a single PROMFA cell



(a) Chip photo



(b) Test fixture photo

Figure 3.3 PROMFA chip photographs

Fig. 3.4 illustrates the PROMFA sub cell that includes a bi-directional amplifier stage and a bypass (pass-transistor switch). The input signal can be routed either through a direct path (pass-transistor) or through bi-directional amplifier stage. The bi-directional amplifier stage allows the possibility to amplify signal in both directions depending on requirement.

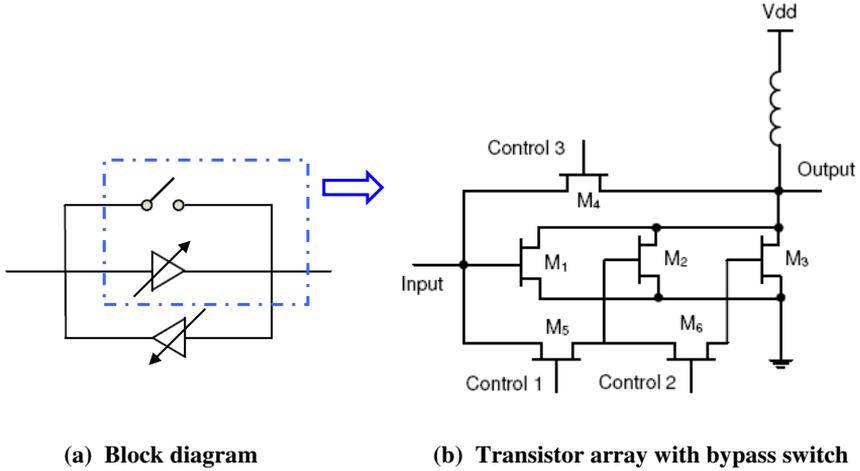


Figure 3.4 Illustration of PROMFA sub cell

The circuit is designed in such a way that it has symmetry that makes it a reciprocal network. Fig. 3.5 shows the measured gain of forward and reverse amplifier. This plot indicates the reciprocity of PROMFA cell. The forward and reverse amplifiers are not allowed to operate concurrently and based on requirement one of them is switched on at a time. Fig. 3.6 shows the comparison of simulated and measured results for amplifier gain and isolation. Fig. 3.7 shows the variation in input and output reflection coefficients versus frequency.

The amplifier transistor array also provides three possibilities of phases. The delay through an amplifier corresponds to a phase shift Φ that can be expressed as:

$$\Phi = \pi + 2\pi n = \omega_c \tau = 2\pi f_c \tau \quad (3.1)$$

Where τ is the amplifier time constant and given by:

$$\tau \propto \frac{C_L}{g_m} \quad (3.2)$$

It means that τ can be controlled by the variation of g_m . In addition, g_m is dependent on transistor width:

$$g_m \propto W_T \quad (3.3)$$

Therefore, different delays can be achieved by changing the width of transistor. The control transistors are used to get three phase possibilities Φ_1 , Φ_2 and Φ_3 . Fig. 3.8 shows the relative phase shift of transistor array amplifier with three possibilities. Fig. 3.9 shows the comparison of measured and simulated phase response for phase possibility Φ_3 . A single PROMFA sub cell only provides three possibilities. The results indicate that the relative phase shift has a reasonable flat response. The concept can be extended to get the other phase possibilities by connecting additional PROMFA cells.

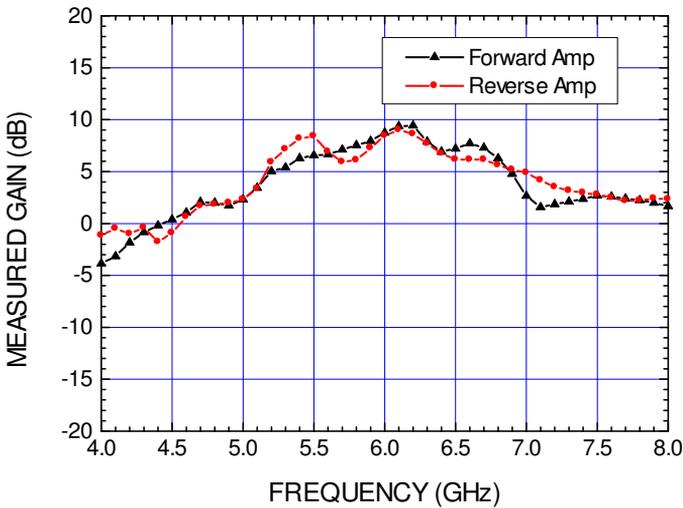


Figure 3.5 Measured gain of forward and reverse amplifier

Each PROMFA subcell requires seven control lines that includes three control lines for each transistor array and one for bypass. Four control lines are also needed for the port switches. Therefore, in total, 32 control lines are needed for a single PROMFA cell. For the first prototype, we have used four off-chip serial to parallel (S/P) converters each controlling one subcell. The chip is controlled through four serial lines using a computer based data acquisition card and Lab-View[®] software.

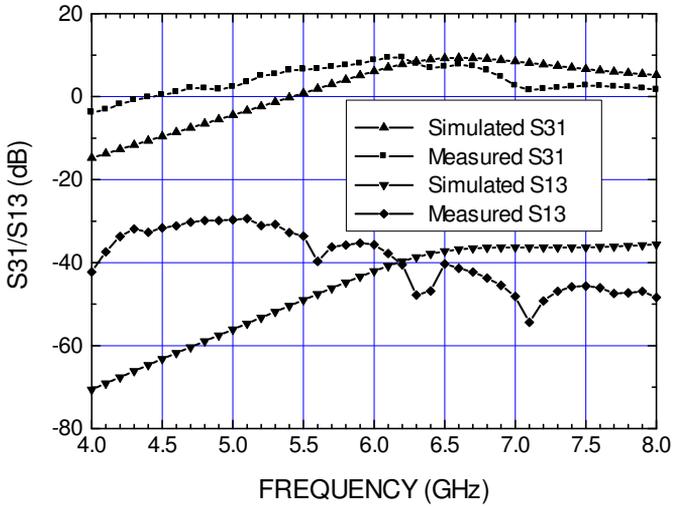


Figure 3.6 Measured and simulated response of PROMFA amplifier (Gain S31, Isolation S13)

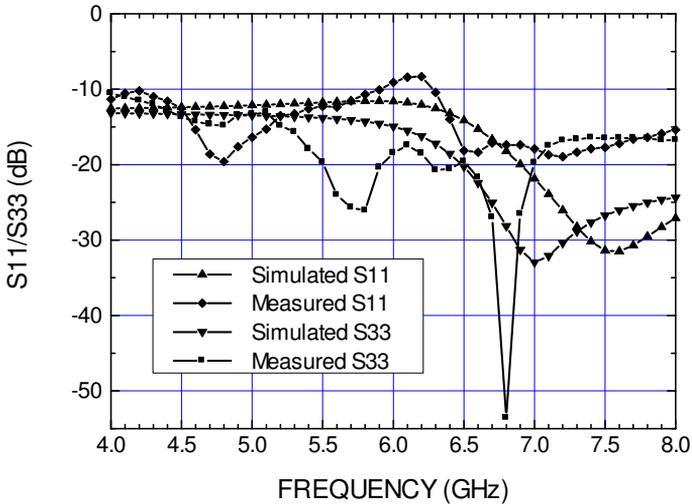


Figure 3.7 Measured and simulated response of input and output match

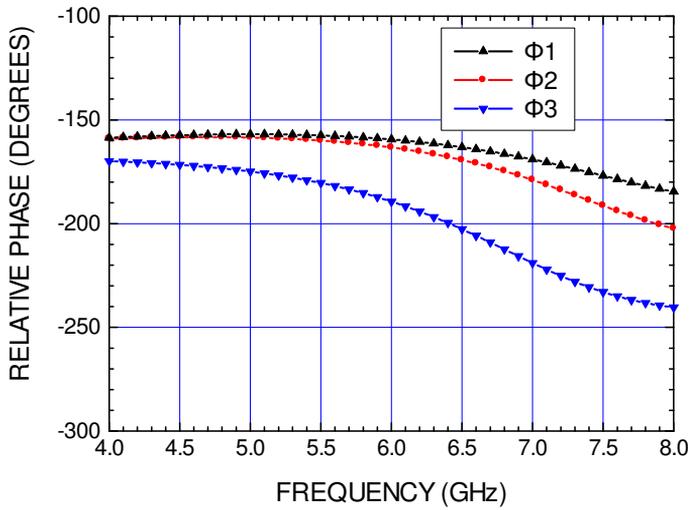


Figure 3.8 Relative phase shift of transistor array amplifier

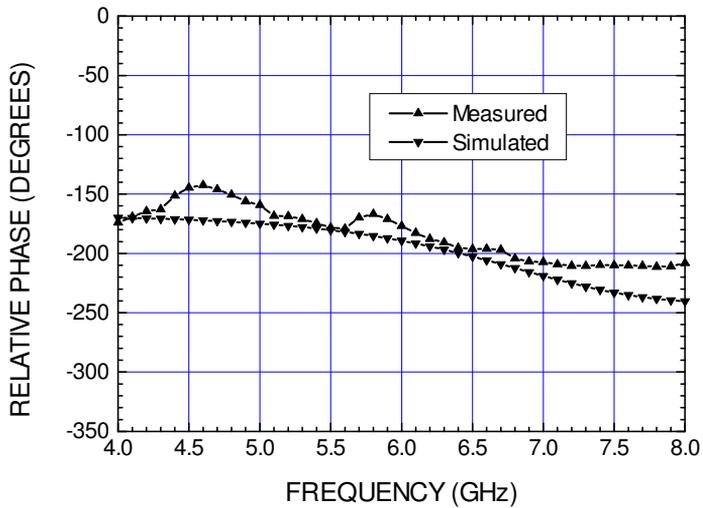


Figure 3.9 Measured and simulated response for phase possibility Φ_3

3.3 Tunable Band pass Filter

Active recursive band pass filters are very interesting for microwave applications. A traditional recursive band pass filter is accomplished according to the model in Fig. 3.10. This model is based on positive feedback, where some of the output is fed back to the input through a delay τ . The input coupling

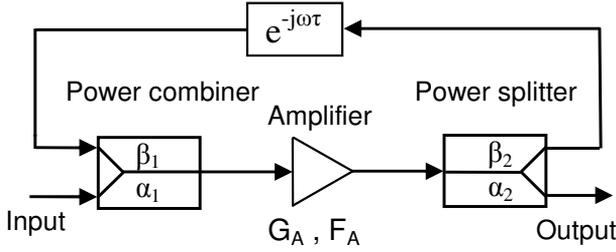


Figure 3.10 Block diagram of a recursive band pass filter

factor is denoted by α_1 while β_1 is the feedback coupling factor. Similarly α_2 and β_2 are coupling factors of the output power splitter. The amplifier gain and noise figure are denoted by G_A and F_A respectively. By varying the delay in the feedback loop, a phase shift is accomplished that changes the center frequency of filter [14].

The filter gain can be expressed as:

$$G_{fil}(\omega) = \left(\frac{\alpha_1 \alpha_2 G_A}{1 - 2\beta_1 \beta_2 S_{\beta_1} S_{\beta_2} G_A \cos(\omega\tau) + (\beta_1 \beta_2 S_{\beta_1} S_{\beta_2} G_A)^2} \right)^2 \quad (3.4)$$

where S_{β_1} and S_{β_2} are the transmission parameters (loss/gain) of power divider and power splitter path. At filter centre frequency (ω_o) the gain can be expressed as:

$$G_{fil}(\omega_o) = \left(\frac{\alpha_1 \alpha_2 G_A}{1 - \beta_1 \beta_2 S_{\beta_1} S_{\beta_2} G_A} \right)^2 \quad (3.5)$$

For a lossless and symmetrical power divider/combiner: $S_{\beta_1} = S_{\beta_2} = 1$ and $\alpha_1 = \alpha_2 = \beta_1 = \beta_2 = \sqrt{1/2}$, hence (3.5) reduces to:

$$G_{fil}(\omega_o) = \left(\frac{G_A}{2 - G_A} \right)^2 \quad (3.6)$$

The Q value can be evaluated by [15] :

$$Q = \frac{n\pi}{\arccos\left[\frac{4G_L - G_L^2 - 1}{2G_L}\right]}, \quad n = 1, 2, 3, \dots \quad (3.7)$$

where G_L is the loop gain and is given by:

$$G_L = \beta_1 \beta_2 S_{\beta_1} S_{\beta_2} G_A \quad (3.8)$$

The noise factor of the filter can be expressed as [15]:

$$F = 1 + \frac{1}{1 - \beta_1^2} \left[F_A - 1 + \beta_1^2 (1 - S_{\beta_1} + S_{\beta_1}^2 (1 - S_{\beta_2}^2)) + \left(\frac{(G_L - (\beta_1 S_{\beta_1} S_{\beta_2} G_A)^2)^2}{G_A^2 ((\beta_1 S_{\beta_1} S_{\beta_2} G_A)^2 - G_L^2)} \right) \right] \quad (3.9)$$

The active recursive filter can easily be implemented by using PROMFA cells. For a simple filter, only four cells are required that can perform the operation of power divider, power combiner, amplifier and a phase shifter. Fig. 3.11 illustrates a tunable filter based on 2x2 PROMFA cell. With the help of additional cells in the feedback loop, more phase possibilities can be exploited. Therefore, a widely tunable filter can be realized. Fig. 3.12 shows the simulated response of a tunable band pass filter implemented by generic PROMFA cells. This simulation makes use of the measured results of a single PROMFA cell. The plot indicates that a widely tunable filter can be realized. Just for the comparison of results, filter response at three frequencies 5 GHz, 6 GHz and 7 GHz is presented. The results also indicate that a widely tunable filter with

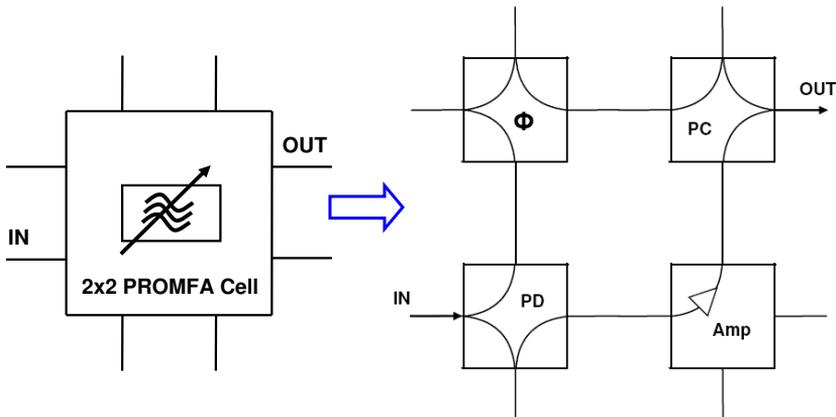


Figure 3.11 Illustration of tunable filter using 2x2 PROMFA cell

reasonable Q can be implemented with PROMFA generic cells. Table 3.1 shows a summary of tunable filter results.

The dynamic reconfiguration of PROMFA cells provides flexibility. Fig. 3.13 shows the configuration in which two T/R modules (transceivers) can share the same tunable filter based on 2x2 PROMFA cell.

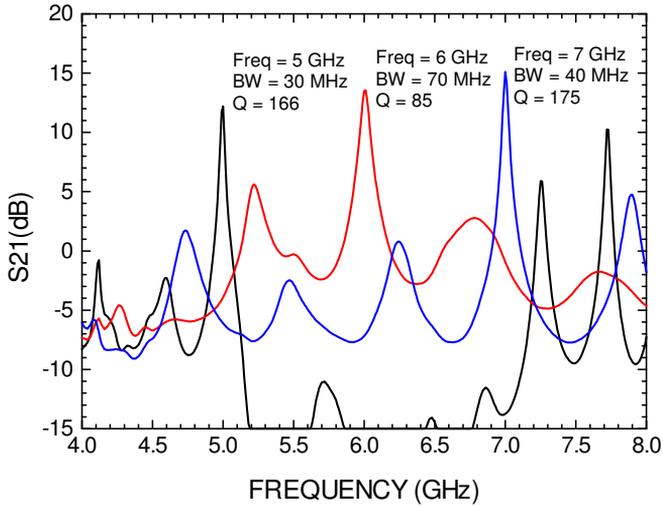


Figure 3.12 Simulated response of a tunable band pass filter based on measured results of a generic PROMFA cell

TABLE 3.1
SUMMARY OF TUNABLE FILTER RESULTS

Sr. No.	Freq. (GHz)	S21 (dB)	S11 (dB)	S22 (dB)	K	B
1	5	12.2	-9.7	-7.4	2.4	0.9
2	6	13.4	-6.6	-17.6	6.1	1.2
3	7	15.1	-6.9	-11.0	2.3	1.1

where $K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$, $\Delta = S_{11}S_{22} - S_{12}S_{21}$

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

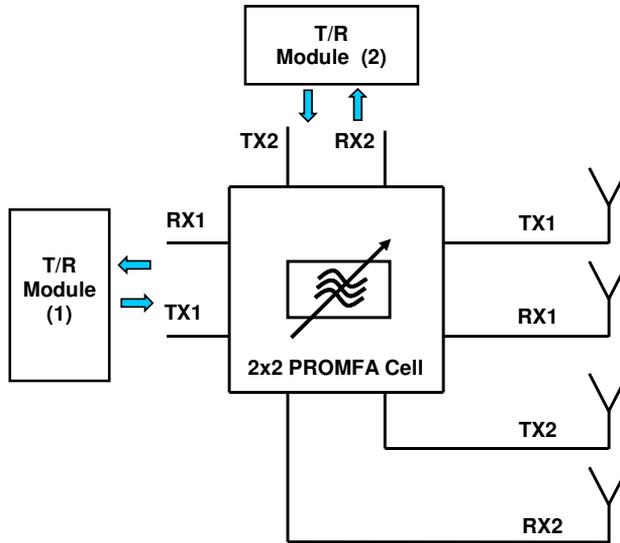


Figure 3.13 Two T/R modules sharing the same tunable filter

3.4 Other Applications

Another suitable application of PROMFA cell is in the implementation of beamforming networks. The reciprocity of PROMFA cell allows it to be an appropriate choice for this application. The corporate-fed arrays are mostly used for beam forming applications due to their versatility. Conventional networks make use of passive power dividers that have significant feed line losses. Active corporate feed network using PROMFA cells can be a suitable choice as it can reduce the feed line losses. Fig 3.14 shows the block diagram of an 8-element active corporate feed network using active PROMFA power dividers. The possibility of having a bidirectional amplifier makes it possible to use the same network as a receiver with active power combiners.

Another advantage of having generic cells in the beamforming network is that we can choose antenna elements depending on requirement. Especially in case of large arrays, it might be useful to have different possibility of active antenna elements. Fig. 3.15 shows the normalized linear array pattern with different antenna elements. As an example case normalized array pattern at 6 GHz with $N=16$, 8, & 4 is shown in Fig. 3.15.

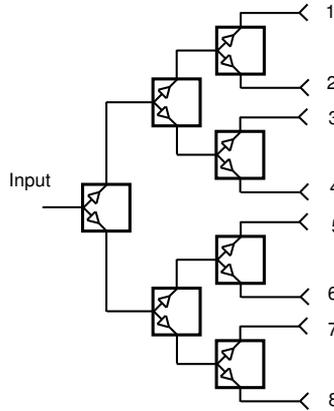


Figure 3.14 Block diagram of an active corporate feed network

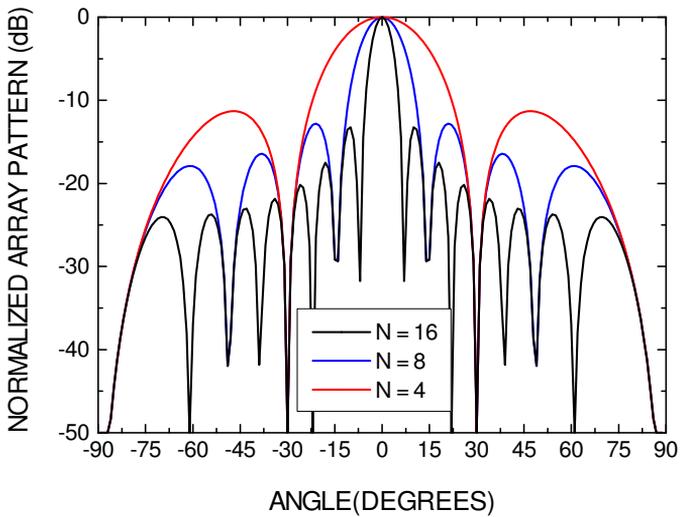


Figure 3.15 Normalized array pattern for different element selection ($d = 0.5\lambda$)

3.5 CMOS Implementation

The PROMFA approach provides one viable solution for flexible RF systems and its CMOS implementation has certain advantages. For example, a highly integrated solution with both analog and digital parts on the same chip, therefore, a low cost PROMFA circuit can be realized. The high level of integration in modern CMOS technology also provides the possibility of large PROMFA arrays which are rather difficult to implement in GaAs due to its limited yield.

The block diagram of a PROMFA cell utilized for CMOS implementation is shown in Fig. 3.16. This single cell architecture is similar to Fig. 3.2 but with out any port switches, instead it has isolation switches both at input and output of each amplifier. The single cell consists of four identical unit cells with low noise amplifiers in each unit cell. The circuit schematic of the unit cell amplifier is shown in Fig. 3.17. It is a common source cascode amplifier with a common drain feedback [16]. M_1 is the main amplifier transistor while M_2 is the cascode transistor. The common drain stage consisting of transistor M_3 and resistor R_F provides a wideband 50Ω input match. M_4 is a biasing transistor while C_1 , C_2 and C_3 are ac coupling capacitors. The voltage gain of the unit cell amplifier can be expressed as:

$$A_v = -g_{m1}R_L \quad (3.10)$$

The input impedance can be expressed as:

$$Z_{IN} = \frac{1 + g_{m3}R_F}{g_{m3}(1 + |A_v|)} \quad (3.11)$$

From (3.10) and (3.11) it is clear that amplifier gain is set by the common source stage while the input impedance by the common drain feedback stage. The

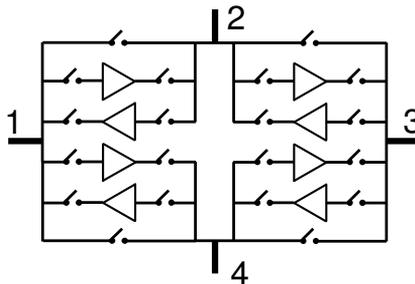


Figure 3.16 Block diagram of a PROMFA cell

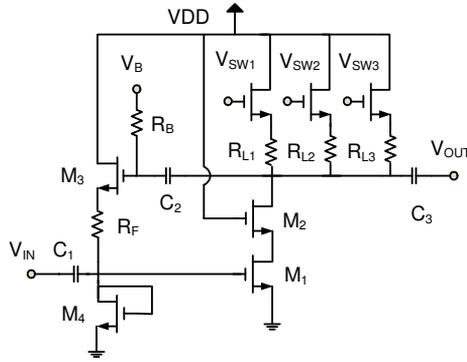


Figure 3.17 Schematic of unit cell low noise amplifier

common drain feedback stage also provides partial noise cancellation. The over all output noise is reduced by the correlated noise appearing from the feedback stage [14]. The noise from biasing transistor M_4 is not cancelled as it is outside the feedback loop. The noise factor of amplifier can be expressed as [16]:

$$F = 1 + \left(1 + \frac{1}{1 + |A_v|}\right)^2 \left(\frac{\gamma_1}{g_{m1} R_s}\right) + \frac{\gamma_3 g_{m3} R_s}{(1 + g_{m3} R_F)^2} + \gamma_4 g_{m4} R_s + \frac{R_F}{R_s (1 + |A_v|)^2} + \frac{R_L}{R_s (1 + |A_v|)^2} \tag{3.12}$$

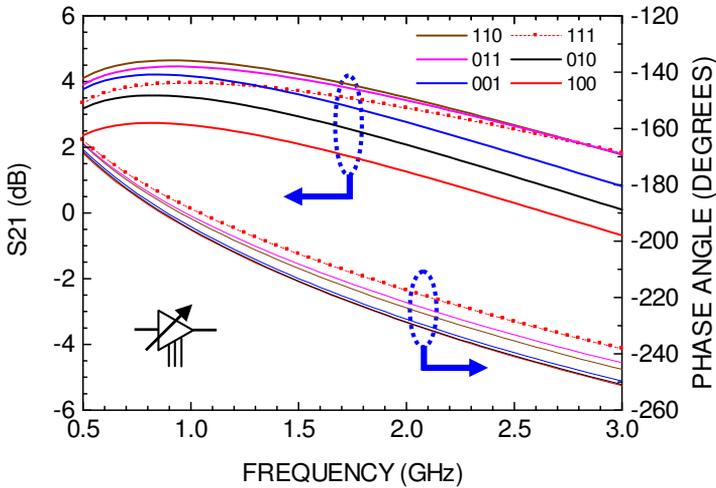


Figure 3.18 Variation in gain and phase with different control settings (single amplifier)

The circuit simulation results indicate that the amplifier (including series transistor switches) has a maximum NF of 2.65dB in 1-3GHz band. The proposed low noise amplifier has a switchable load. With a 3-bit digital control, various load configurations can be selected that provides flexibility to this architecture. The variation in gain and phase with different control settings is shown in Fig. 3.18.

3.6 Tunable Oscillator Configuration

The forward and reverse amplifiers of a unit cell can be activated simultaneously to realize a feedback oscillator. A simple model of a feedback oscillator is shown in Fig. 3.19. From the Barkhausen criteria we find the gain and phase conditions:

$$|H_1(j\omega_o)||H_2(j\omega_o)|=1 \quad (3.13a)$$

$$\Phi = \angle H_1(j\omega_o) + \angle H_2(j\omega_o) = 2\pi n \quad (3.13b)$$

where $n = 1, 2, 3, \dots$

Moreover the phase shift Φ can be expressed as:

$$\Phi = \omega_o \tau = 2\pi f_o \tau \quad (3.14)$$

where f_o is the oscillation frequency and τ is the amplifier pair time constant which can be expressed as [14]:

$$\tau \propto \frac{C_L}{gm} \quad (3.15)$$

from (3.14) & (3.15) we get;

$$f_o \propto \frac{gm}{C_L} \quad (3.16)$$

Equation (3.16) indicates that the oscillation frequency can be controlled by the variation in g_m . As g_m is dependent on $(v_{gs} - v_{th})$, this mechanism can be used to tune the oscillator frequency. In the proposed architecture this can be achieved by changing the bias voltage (V_B) of feedback transistor M_3 . Fig. 3.20 shows the variation in open loop phase response of the oscillator with different bias voltages. The proposed PROMFA unit cell oscillator also has the possibility of step tuning. Step tuning can be achieved by changing the state of 3-bit control switches in each amplifier. With load switching, it is also possible to introduce different phase shifts that will result in different oscillation frequencies. As the change in load impedance is relatively small, so the relative change in oscillator frequency with load switching is also small (e.g only 30MHz from 011 to 111 at an oscillator frequency of 1GHz).

For theoretical analysis of the phase noise a linear model approach is used [17]. The linearized model of the PROMFA unit cell oscillator is shown in

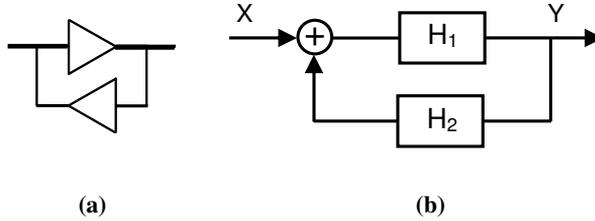


Figure 3.19 (a) Unit cell oscillator (b) Simple model of feedback oscillator

Fig. 3.21. R_L and C_L are load resistance and capacitance of each amplifier. The noise of each amplifier is modeled by current sources I_{N1} and I_{N2} . For a ‘startup’ gain $g_m R_L = 2$ and $\omega_o = 1/R_L C_L$, the open loop transfer function can be written as:

$$H(j\omega) = \frac{4}{(1 + j\omega/\omega_o)^2} \quad (3.17)$$

The open loop Q factor can be written as:

$$Q = \frac{\omega_o}{2} \left| \frac{dH(j\omega)}{d\omega} \right| = \sqrt{2} = 1.414 \quad (3.18)$$

while the noise shaping function can be written as:

$$\left| \frac{V_1}{I_{N1}} [j(\omega_o + \Delta\omega)] \right|^2 = \frac{1}{(\Delta\omega)^2 \left| \frac{dH(j\omega)}{d\omega} \right|^2} = \frac{1}{8} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \quad (3.19)$$

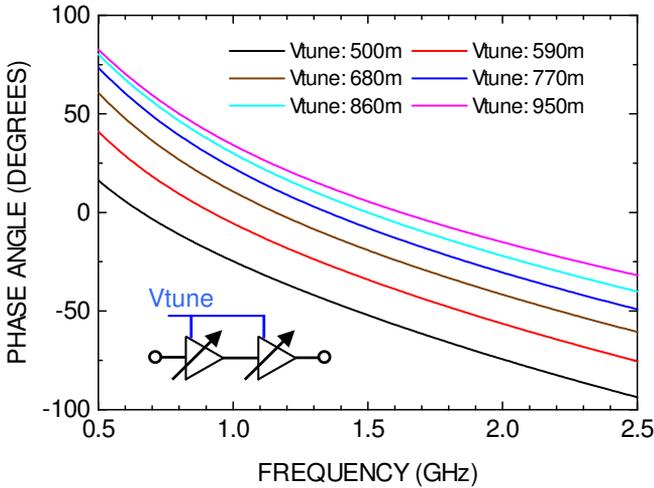


Figure 3.20 Variation in open loop phase response of oscillator with different control voltages (from simulations)

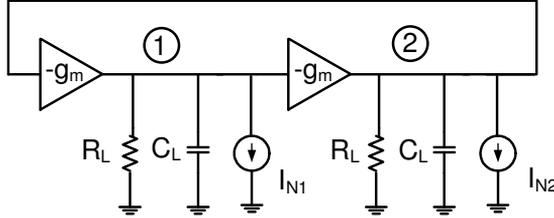


Figure 3.21 Linearized model of unit cell oscillator

As compared to cross-coupled LC oscillators this circuit topology has a lower Q value. Therefore, the proposed oscillator has a relatively higher phase noise. The PROMFA cell architecture and its dynamic reconfiguration capability provide the possibility of having a series of cascaded unit oscillators (Fig. 3.22). With harmonic combination of multiple oscillators the phase noise can be decreased [18]. Using the same linear model approach the open loop transfer function of four unit cell oscillators can be expressed as:

$$G(j\omega) = \left[\frac{H(j\omega)}{1-H(j\omega)} \right]^4 \quad (3.20)$$

The open loop Q factor value comes out to be 3.33 and the noise shaping function can be expressed as:

$$\left| \frac{Y}{X} [j(\omega_o + \Delta\omega)] \right|^2 = \frac{1}{44.5} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \quad (3.21)$$

Comparing (3.19) and (3.21) we can expect a phase noise reduction by a factor of 5.5 (i.e -7.45dB). This calculated value is also in agreement with our simulation results. The phase noise of a four unit cell oscillator can be expressed as:

$$L\{\Delta\omega\} = 10 \log \left[\frac{2FKT}{P_{sig}} \left\{ 1 + \frac{1}{44.5} \left(\frac{\omega_o}{\Delta\omega} \right)^2 \right\} \left(1 + \frac{\Delta\omega_{1/f}}{|\Delta\omega|} \right) \right] \quad (3.22)$$

where F is the amplifier noise figure and $\Delta\omega_{1/f}$ characterize the transistor 1/f noise. In a four unit cell oscillator, differential output signals can be obtained from adjacent ports (i.e 1&2 or 3&4). Fig. 3.23 shows the simulated frequency versus tuning voltage responses of a unit cell oscillator and a four unit cell oscillator. Fig. 3.24 shows the comparison of phase noise between a single unit cell and a four unit cell configuration. The plot indicates that the phase noise can be reduced with harmonic combination of multiple oscillators.

Paper 2 provides the details of simulation and chip measurement results. The chip measurement results indicate that a single unit cell oscillator can

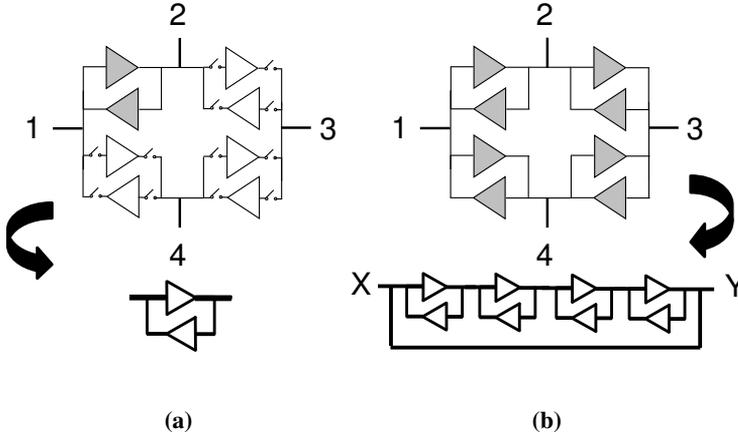


Figure 3.22 Different oscillator configurations in a PROMFA cell (a) Single unit cell oscillator (b) Four unit oscillators in a ring

achieve a wide tuning range within 600MHz to 1.8GHz frequency band with a measured phase noise of -94dBc/Hz at an offset frequency of 1MHz for the oscillation frequency of 1.2GHz. A single unit cell oscillator consumes 18mW at 1.2GHz while providing -8dBm power into 50Ω load.

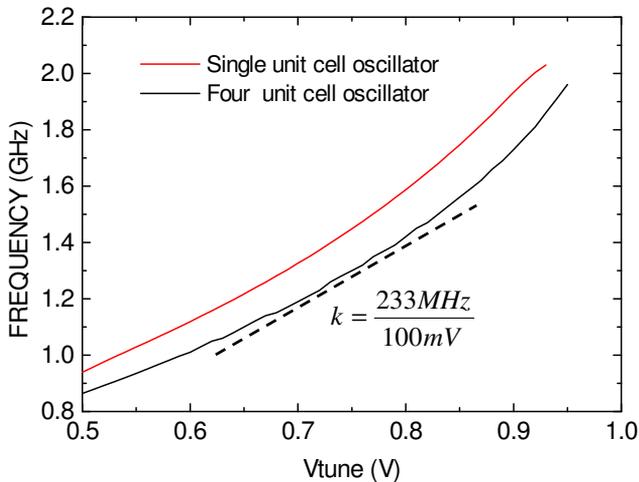


Figure 3.23 Oscillator frequency versus tune voltage

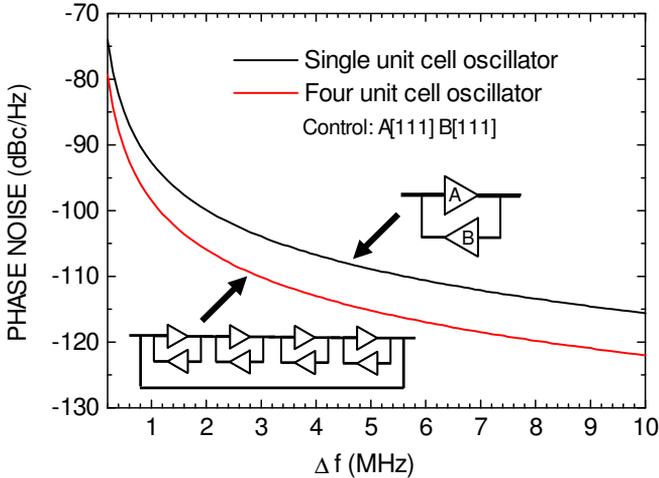


Figure 3.24 Phase noise response (Oscillator $f=1\text{GHz}$)

3.7 Tunable Filter Configuration

The active recursive filter can easily be implemented by using PROMFA cells. For a simple filter configuration, only a single unit cell is required. Like an oscillator configuration, the forward and reverse amplifiers of a unit cell can be activated simultaneously to realize an active recursive filter. The only difference is requirement for a reduced loop gain i.e $G_L < 1$ in order to guarantee a stable filter operation. From equation (3.8) with the assumption of a lossless and symmetrical power divider/combiner, the loop gain G_L can be evaluated as: $G_L = G_A/2$. For a stable filter operation, choosing $G_L = 0.9$, the required amplifier pair gain should be $G_A \leq 1.8$ i.e 5.1dB. The switchable load in a unit cell amplifier provides the possibility to reduce the loop gain by choice of appropriate load. Another advantage of the switchable load is the filter Q control. As indicated in (3.7) that the filter Q is also a function of loop gain, therefore, with a switchable load different Q values can be achieved. The center frequency of an active recursive filter can be changed by variation in the loop delay τ . Similar to an oscillator configuration, the loop delay can be controlled by changing the bias voltage of the feedback transistor M_3 . Therefore, a tunable band pass filter can be realized. Fig. 3.25 shows the simulated filter response with two different bias voltages. At each bias voltage, three different load

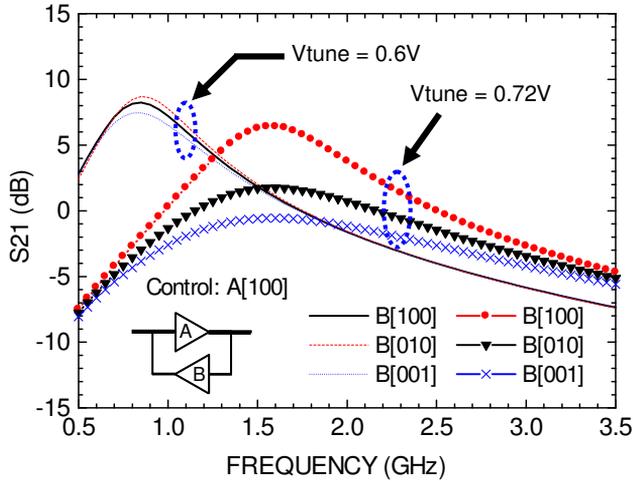


Figure 3.25 Simulated filter response

configurations of the reverse amplifier are shown. The plot indicates the Q control with load switching and the frequency tuning with change in bias voltage. Simulations indicate that a single unit cell filter is tunable within 600MHz to 1.6GHz frequency band. Cascaded filter stages provide a higher filter Q but at the cost of more power consumption.

Fig. 3.26 shows the 90nm CMOS chip micrograph with two unit cells. A single unit cell has an active chip area of 0.091mm^2 including coupling capacitors. The test board utilizes a four layer PCB with a standard FR4 substrate material. A summary of measured results for all three configurations is given in Table 3.2. The chip measurement results are promising and indicate that this circuit has a good performance in all three configurations. Further details of chip measurement results are provided in **Paper 2**.

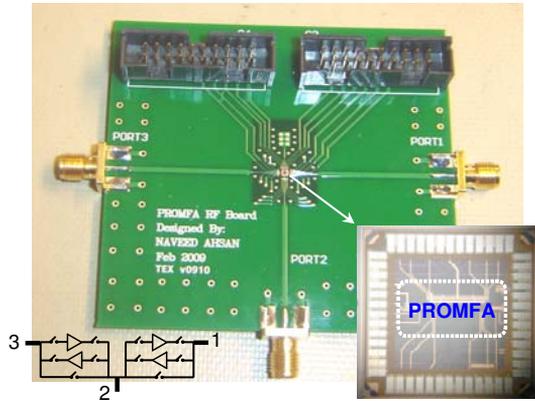


Figure 3.26 Test fixture photograph showing 1mm² chip mounted on FR4 PCB

TABLE 3.2
SUMMARY OF MEASURED RESULTS

Configuration	Measured Results (single unit cell)
LNA	Gain _{typical} = 4dB NF _{min} = 2.65 3dB BW = 2.7GHz 1dBC _P @ 1GHz = -8dBm IIP3 @ 1GHz = +1.1dBm P _{DC max} = 8.8mW
Tunable Filter	Tuning Range = 600MHz-1.2GHz S ₂₁ @ 1.1GHz = 5.6dB Q @ 1GHz = 1.6 P _{DC} @1GHz = 13mW
Tunable Oscillator	Tuning Range = 600MHz-1.8GHz Phase Noise @ (1.2GHz, Δf=1MHz) = -94.7dBc/Hz P _{OUT} @ 1.2GHz = -8dBm P _{DC} @ 1.2GHz = 18mW

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Chapter 4

Multiband LNA Design

The LNA is a key component in the design of a flexible radio. The main purpose of LNA is to amplify the input signal without adding much noise. The input signal can be very weak, so the first thing to do is strengthen the signal without corrupting it. Therefore, the main design considerations are noise figure, gain, input match, linearity, and power consumption. In addition to low noise performance, the LNA must also remain linear even when strong signals are being received. In particular, the LNA must maintain linear operation when receiving a weak signal in the presence of a strong interferer (blocker), otherwise intermodulation distortion and cross modulation may occur. In the worst case the strong interferer may swamp out the desired weak signal and hence causing desensitization of the receiver. Considering a multimode and multiband radio front end, the LNA must provide adequate performance within a large frequency band. Optimization of LNA performance for a single frequency band is not suitable for this application. The process variations is another problem for onchip implementations. Flexible LNA architectures that are tolerant against process variations are needed for future wireless systems.

The initial part of this chapter discusses the design considerations and implementation of narrowband tunable LNAs, while the later part provides the details of design and implementation of low power, highly linear wideband LNAs.

4.1 Overview of Multiband LNAs

The initial multiband wireless receivers were implemented with one front-end for each band. With the increase in number of standards, this approach is not cost effective as it consumes a large chip area. For low-cost solutions, reuse of circuit blocks is necessary. Some of the multiband LNAs have utilized inductor reuse technique to save the chip area [1-3]. Concurrent dual band LNA approach gives the possibility to use the LNA in both bands simultaneously [4]. Widely tunable LNAs based on recursive technique have also been reported [5-6]. However, achieving low noise figure and good linearity from recursive LNAs is still a challenge. Another solution for multiband and multimode radio is to utilize a wideband LNA architecture. Various solutions have been proposed [7-9]. For wideband LNAs, achieving very low noise figure with good linearity is also challenging.

In order to meet the demands of future wireless systems, flexible architectures are also needed that can adopt according to requirement. Especially, circuits that are tolerant against process variations and can perform self optimization for optimal performance are needed.

4.2 Design Specifications

The main design parameters for an adequate LNA design include noise figure, gain, input match, linearity, and power consumption. Gain and noise figure are typical small signal parameters. As discussed previously, the main purpose of LNA is to amplify the input signal without adding much noise. The total noise figure of the cascaded system as given by 4.1 (Friis formula) indicates that the overall noise figure is dominated by the noise from the initial stages. Also, the large gain for initial stages helps in minimizing the overall noise figure [9].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_N - 1}{G_1 G_2 \dots G_{N-1}} \quad (4.1)$$

Therefore, in a receiver chain the overall noise figure is dominated by LNA noise figure. Hence most of the design effort is put on LNA to achieve a low noise figure.

The input match is another important design specification. The most commonly used standard impedance level is 50Ω. In a receiver chain, usually LNA is placed after an RF filter which is designed for a 50Ω system. The filter transfer characteristics are very sensitive to the quality of termination [10]. Therefore, it is mandatory to match the LNA input impedance to standard 50Ω. The mismatch between filter and LNA could easily destroy the filter function

and hence severely degrade the receiver performance. The mismatch is usually expressed by RL (Return loss) and defined as [11]:

$$RL = -10 \log \left(\frac{P_r}{P_i} \right) = -20 \log |\Gamma_{IN}| \quad (4.2)$$

where P_i = Incident power, P_r = Reflected power and Γ_{IN} is defined as:

$$\Gamma_{IN} = \frac{Z_{IN} - Z_o}{Z_{IN} + Z_o} \quad (4.3)$$

where Z_{IN} is the input impedance and Z_o is the characteristic impedance of transmission line which is usually 50Ω .

In addition to gain, noise figure and input match, linearity is another important design specification. The LNA must also remain linear even when strong signals are being received. Particularly, the LNA must maintain linear operation when receiving a weak signal in the presence of a strong interferer. The consequences of nonlinearity are intermodulation distortion, cross modulation and in the worst case desensitization. The most commonly used measures of linearity are 1-dB compression point (1-dBC_p) and the third order intercept point (IP3). Fig. 4.1 and Fig. 4.2 illustrates the definitions of these two linearity measures. The small signal gain of an amplifier is usually obtained with the assumption that harmonics are negligible. However, with the increase in signal amplitude the amplifier gain begins to vary as it leaves its linear region. The input signal level that causes the small signal gain to drop 1 dB from its linear curve is referred to as 1-dB compression point.

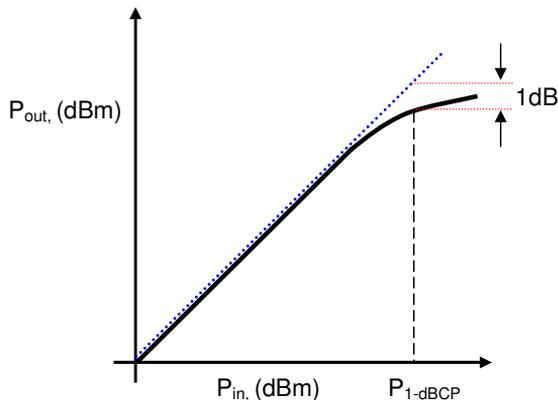


Figure 4.1 Illustration of 1-dB compression point (1-dBC_p)

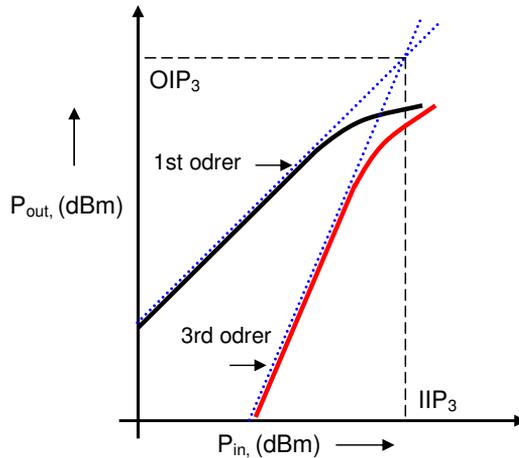


Figure 4.2 Illustration of third order intercept point (IP3)

When two signals with different frequencies are applied to a non linear system, the output in general exhibits some components that are not harmonics of the input frequencies. These components are called intermodulation products. Particularly the third order intermodulation products are more harmful as they directly fall inside the wanted channel. Fig. 4.3 illustrates this situation where wanted channel is corrupted by third order intermodulation products. In order to characterize the third order nonlinearity, third order intercept point (IP3) is defined. The third order intercept point is a theoretical point where the amplitudes of the intermodulation tones at $(2\omega_1 - \omega_2)$ and $(2\omega_2 - \omega_1)$ are equal to

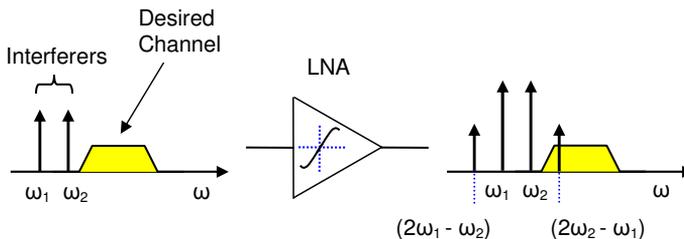


Figure 4.3 Corruption of wanted signal due to intermodulation products

the amplitudes of the fundamental tones at ω_1 and ω_2 . Typically the IP3 of LNA is measured by performing a two tone test. From the measured data the slopes of fundamental and third order intermodulation product are extrapolated to get the IP3 value. In a receiver chain the IP3 of cascaded stages can be expressed as:

$$\frac{1}{IP3} \approx \frac{1}{IP3_1} + \frac{G_1}{IP3_2} + \frac{G_1 G_2}{IP3_3} \dots + \frac{G_1 G_2 \dots G_{n-1}}{IP3_n} \quad (4.4)$$

Equation 4.1 and 4.4 indicates that while designing a receiver chain the distribution of gain to maintain low NF and high IP3 simultaneously is contradictory, therefore, a compromise is required for an adequate design.

The receiver noise floor at $T = 290^\circ\text{K}$ can be expressed as:

$$\text{Noise Floor} = -174\text{dBm} + 10\log(B) \quad (4.5)$$

and the receiver sensitivity is defined as:

$$\text{Sensitivity} = -174\text{dBm} + 10\log(B) + NF_{dB} + SNR_{\min} \quad (4.6)$$

The dynamic range (DR) is generally defined as the ratio of the maximum input level that the circuit can tolerate to the minimum input level at which the circuit provides a reasonable signal quality. In a radio receiver design, spurious free dynamic range (SFDR) is defined that takes into account the effects of third order non linearity. SFDR can be expressed as:

$$SFDR = \frac{2(IIP3_{dBm} - F)}{3} - SNR_{\min} \quad (4.7)$$

where $F = -174\text{dBm} + NF + 10\log(B)$.

4.3 Design of Tunable LNAs

Considering a flexible multimode radio receiver, tunable and switchable LNAs are promising candidates and their use can relax some of the requirements from the digital baseband circuit. Widely tunable LNAs based on recursive technique provide the advantage of wideband tuning, however, achieving low noise figure and good linearity from recursive LNAs is still a challenge. Another approach for multiband operation utilizes switchable LNAs [12-14]. Some of the flexible LNAs are MEMS based such as reported in [13,14].

We have designed and implemented a flexible LNA MMIC that can be switched between two bands [15,16]. The LNA also provides the possibility of tuning within each band. The test chip consists of two fully integrated narrow-band tunable LNAs along with SPDT switch. For power saving one LNA can be switched off. The technology process is $0.2\mu\text{m}$ GaAs offered by OMMICTM.

The schematic of a tunable LNA used for the dualband architecture is shown in Fig. 4.4. The circuit is based on inductively degenerated common-source cascode amplifier. The output stage makes use of another common source buffer amplifier. This architecture provides a large gain with very low NF and a good input match. An extra source inductor at the buffer stage gives improvement in stability and output match. Tuning is incorporated into the LC loads and implemented by on-chip transistor varactors.

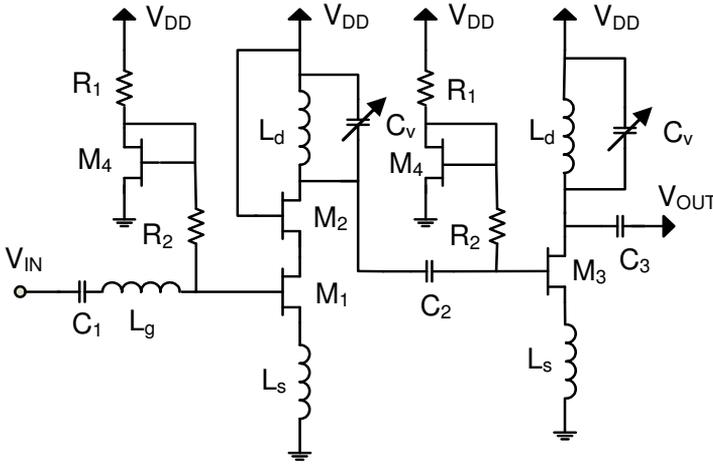


Figure 4.4 The schematic of a tunable LNA

The input impedance of an inductively degenerated common source amplifier is given by:

$$Z_{IN} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + L_s \frac{g_{m1}}{C_{gs}} \quad (4.8)$$

at resonance frequency ω_o , Z_{IN} can be expressed as:

$$Z_{IN} = L_s \frac{g_{m1}}{C_{gs}} \quad (4.9)$$

The noise factor can be written as:

$$F = 1 + \frac{\gamma}{g_{m1} Q_{in}^2 R_s} \quad (4.10)$$

where $R_s = 50\Omega$, γ is technology dependent factor and Q_{in} is given by:

$$Q_{in} = \frac{1}{R_s} \sqrt{\frac{L_g + L_s}{C_{gs}}} \quad (4.11)$$

The two stage amplifier gain can be expressed as:

$$A_v \approx (g_{m1} g_{m3}) Z_{\tan k1} \cdot Z_{\tan k2} \quad (4.12)$$

The tuned LC tank has a resonance frequency ω_c given by:

$$\omega_c = \frac{1}{\sqrt{L_d C_V}} \quad (4.13)$$

The LNA tuning voltage changes the varactor capacitance C_V , consequently the LC tank resonance frequency is changed. The details of design and implementation are discussed in **Paper 3**. The chip measurement results are provided in **Paper 4**. These results are promising and indicate that a relatively good performance over the two bands can be achieved by the proposed architecture. The implementation of varactor in tuned LC tank provides flexibility and a reasonable tuning can be attained within each band. This technique can also be used to tolerate the process variation in inductances. Tuning gives an extra advantage to compensate for these variations, also referred to as on-chip calibration.

One drawback of this technique is that the tuning range is limited by varactor capacitance. For wideband tuning large ΔC_V is required that is rather difficult to achieve from transistor varactors. We have achieved a capacitance ratio of 2.4 and 2.2 for low band and high band varactors respectively. Therefore, the frequency tuning range is less than 500MHz in both bands.

Paper 4 also presents a self-tuning technique for the optimization of this dual band LNA. With this tuning technique, the LNA can perform self-calibration for the optimal performance. A possible shift in resonance frequency due to process and temperature variations can be compensated by this method. The proposed self-tuning technique is implemented by using a simple RF detector at the LNA output. Based on the DC value provided by this detector the LNA is tuned for a maximum gain through the tuning loop, which incorporates ADC, digital base-band and DAC. Fig. 4.5 shows the block diagram of this self tunable LNA.

The schematic of RF detector is shown in Fig. 4.6. The transistor M_1 operates in weak inversion. The small size of M_1 ensures high input impedance at higher frequencies. The capacitor C_2 keeps the output voltage constant. Since M_1 is biased in weak inversion and R_3 is relatively large, the bias current I_b is almost constant. The difference between I_b and $I_d + I_{R1}$ is provided by the

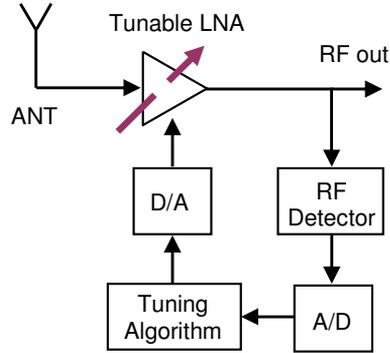


Figure 4.5 Block diagram of self tunable LNA

capacitor C_2 . Resistors R_1 and R_2 are very large so the respective change in their current is less significant. Consequently, during the positive half-cycle a certain amount of charge is removed from capacitor C_2 . As a result, the output voltage decreases. During negative half-cycle the drain current I_d decreases. Since the bias current I_b is roughly constant, the capacitor C_2 should charge increasing the DC output voltage. However, due to non-linear characteristic of M_1 and also different time constants during the positive and negative half cycle, the increase in capacitor charge is smaller than the decrease in the previous positive half-cycle. Therefore, with increase in RF input level the corresponding detector DC output voltage decreases.

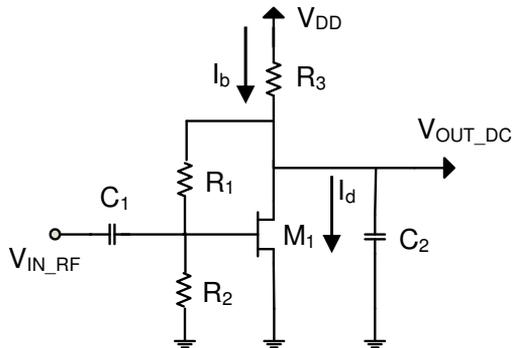


Figure 4.6 Schematic of RF detector

A mathematical relation between ADC and DAC resolution has been established and verified by system level simulations that results in the worst case tuning error of $A_{LSB}/2$. The relation can be expressed as:

$$0.27\alpha k_f^2 V_{LSB}^2 < A_{LSB} < 3.73\alpha k_f^2 V_{LSB}^2 \quad (4.14)$$

where A_{LSB} = ADC step, V_{LSB} = DAC step, k_f = tuning gain, and α is a constant.

For the 4-bit configuration with 50 mV ADC resolution, the worst case tuning error corresponds to the LNA gain error of 0.4dB while typical error values are much smaller. However, the tuning error can easily exceed $A_{LSB}/2$ if the upper bound in (4.14) is violated. The chip measurements and simulation results are promising for practical implementations of the presented technique.

4.4 Design of Wideband Highly Linear LNAs

Wideband LNAs are also suitable choice for a wireless receiver with multiband and multistandard operation. Usually, a wideband LNA is preceded by a broad RF band-pass filter covering all required carrier frequencies. The main obstacle for such a solution is the large linearity requirement. In a narrow-band design, out of band blockers are significantly reduced by the passive RF filters. In a wideband design, these blockers will instead reach the LNA and mixer, thus requiring them to manage the full blocker power. Blockers may have a power of up to 0dBm (such as in the GSM specification). In conclusion, we need to manage input blocker signals of up to 0dBm, simultaneously with the reception of a useful signal with maximum sensitivity. As a result, a 1dB compression point of at least 0dBm (or, more strictly, small desensitization at 0dBm), and sufficiently low intermodulation are needed. Also, there is very little room for voltage gain. 0dBm at 50Ω corresponds to a peak-to-peak voltage of 0.62V, which occupies nearly all voltage headroom in a modern nanometer CMOS process with a supply voltage around 1V. Conventional high gain RF LNAs are thus excluded, as they will have a too large voltage swing on their output.

We have proposed a wideband, low power and highly linear LNA in **Paper 5** [17]. The circuit operates in current mode to avoid hitting the limits given by the supply voltage. The current output is assumed to drive a current mode mixer followed by appropriate baseband circuitry. To implement the LNA, an inverter-like CMOS circuit is chosen for its inherent symmetry making it easier to manage a large input voltage swing. The common gate structure is used to achieve wideband input matching. A circuit schematic of the proposed differential wideband LNA is shown in Fig. 4.7. This novel architecture consists of a pair of NMOS and PMOS common gate amplifiers in each branch, sharing the same load. L_1 , L_2 are off-chip inductors while C_{C1} , C_{C2} are AC coupling

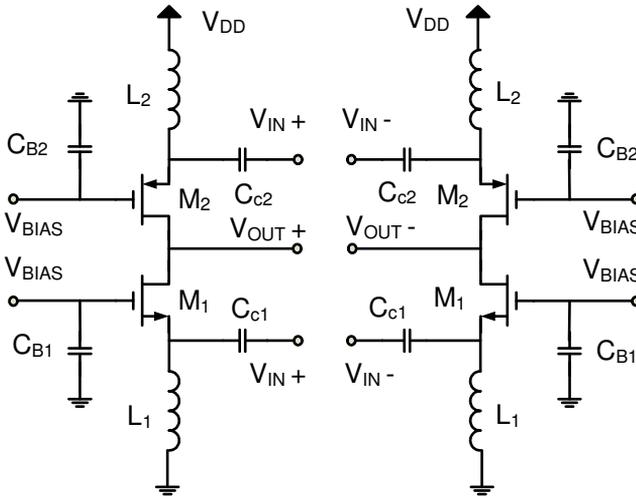


Figure 4.7 Schematic of differential wideband LNA

capacitors with value much larger than C_{gs} . One prime advantage of this architecture is that the transistors M_1 and M_2 share same bias current. The input impedance as given in (4.15) indicates that the broad-band 50Ω matching can be achieved with approximately half bias current as compared to a simple common gate circuit. This helps in minimizing the overall power consumption. Also the effective transconductance is roughly two times larger than in simple common gate amplifier. The architecture also provides the possibility to bias the transistors either symmetrically for Class A or Class AB operation, or asymmetrically.

$$Z_{in} = \frac{1}{g_{m1} + g_{m2}} \quad (4.15)$$

$$G_m = g_{m1} + g_{m2} \quad (4.16)$$

Considering an on chip multistandard radio receiver, there is a stringent requirement for high linearity and usually for low power consumption as well. Particularly, for battery operated devices low power consumption is mandatory for long battery lifetime. In a typical CMOS LNA, there is a tradeoff between linearity and power consumption. So far reported highly linear LNAs [18-20] use cancellation techniques in order to increase IP3. The result is a high IIP3 value but no improvement in the compression point. In the proposed LNA, the complementary characteristics of the NMOS and PMOS transistors can be

utilized for cancelling the first and second derivative of g_m (g'_m and g''_m) in a wide range of input voltages [17,21,22]. As our objective is to utilize a large part of the available voltage headroom for our signal, this is essential. This is in contrast to other solutions utilizing g''_m cancelling utilizing subtraction between two signal paths, which cancels the g''_m term only in a limited voltage range [23].

Basically, the 3rd order nonlinearity component mainly originates from the transistor I-V characteristics. The simple Taylor series expansion of I_{DS} is given by:

$$I_{DS} = g_m V_{gs} + g'_m V_{gs}^2 + g''_m V_{gs}^3 + \dots \tag{4.17}$$

The same nonlinearity reflects in the load current that can be expressed as follows:

$$I_L = g_1 V_{IN} + g_2 V_{IN}^2 + g_3 V_{IN}^3 + \dots \tag{4.18}$$

where $g_1 = \partial I_L / \partial V_{IN}$, $g_2 = \frac{1}{2!} (\partial I_L^2 / \partial V_{IN}^2)$ and $g_3 = \frac{1}{3!} (\partial I_L^3 / \partial V_{IN}^3)$.

In **Paper 5**, we have analyzed the large signal behavior of g_2 and g_3 for various bias scenarios and calculated g_2 and g_3 for the dynamic bias points. For this purpose a DC model of the circuit was used and the voltage V_{IN} was swept around the original bias point. For circuit level simulations we have used

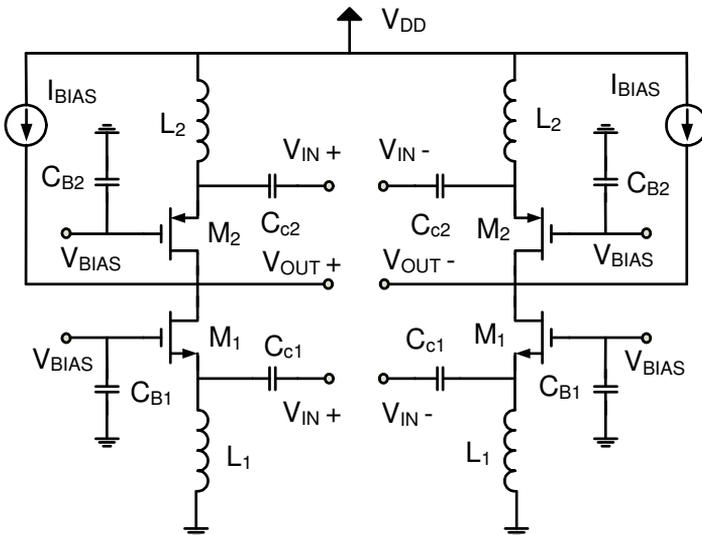


Figure 4.8 Asymmetric biased wideband LNA

standard 90nm CMOS design kit. In the first case, the amplifier transistors are biased just above V_T (*weakly driven*) and for the second case, they are biased in deep saturation (*overdriven*). In the third case, the transistors are asymmetrically biased. Fig. 4.8 shows the schematic of an asymmetrically biased amplifier. Fig. 4.9 illustrates these biasing scenarios.

The details of simulation results are provided in **Paper 5**. The chip measurement results are given in **Paper 7**. The simulation and chip measurement results are very promising and indicate that the proposed architecture is a suitable choice for a highly linear multistandard radio receiver where the linearity and dynamic range requirements are extremely tough.

Table 4.1 shows a comparison of results of this work with already published state-of-art wideband and ultrawideband LNAs. For the comparison of different topologies, we have utilized the figure of merit (FOM) that includes linearity and is given by [24]:

$$FOM = \frac{IIP3_{average}[mW]Gain_{average}[abs]BW[GHz]}{P_{DC}[mW](F_{average} - 1)} \quad (4.19)$$

As indicated in Table 4.1, the proposed LNA performance is comparable to state-of-art highly linear and low power designs. Typical distortion cancellation LNAs only provide improvement in IIP3, however the inverter-like architecture also has a higher value of $1dBC_P$. The measured input referred $1dBC_P$ is

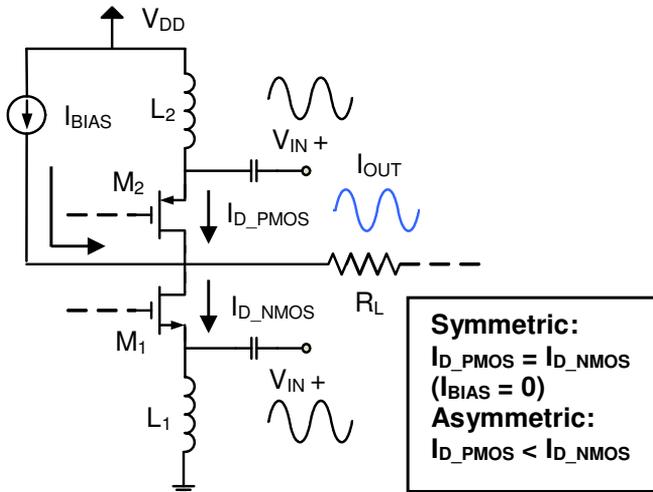


Figure 4.9 One branch of LNA illustrating various biasing scenarios

+4.2dBm at 2GHz. Therefore, this architecture is a suitable for front-ends that can withstand large blockers. Further details are given in **Paper 7**.

TABLE 4.1
CMOS WIDEBAND LNA COMPARISON

	CMOS Process	3dB BW (GHz)	S21 (dB)	NF (dB)	IIP3 (dBm)	Pdc (mW)	Area (mm ²)	FOM
[24]	0.13 μ m	1.5~8.1	8.6~11.7	3.6~6	11.7~14.1	2.62	0.58	261.6
This work	90nm	0.5~7	4.3	2.6~3.8	16.2	6.2	0.055	108
[27]	65nm	2~8	12	2.5	12	18	-	107.4
[28]	0.13 μ m	0.1~6.5	17~19	3~4.2	1	12	-	33.2
[9]	0.13 μ m	1~7	17	2.4	-4.1	24.5	0.019	6.4
[25]	0.13 μ m	1.5~2.5	5.2	3.0	10.5	12.6	0.66*	2.9
[26]	90nm	2~11	9~12	5~6	-4	16.8	0.7	0.9

*Area including bonding pads

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Chapter 5

Wideband RF Front-end Design

The growing number of wireless standards demand for flexible radios that can operate in any band in order to meet various standards. The current approach for multistandard radio utilizes multiple receivers optimized for narrow frequency band. From power consumption point of view, this approach is not feasible. To realize the concept of a software defined radio (SDR), the most economical approach is to use a single RF front-end utilizing wideband LNA and mixer [1]. Wideband front-ends are becoming more popular due to the recent developments in the area of multiband antenna and tunable SAW filters as they provide a more compact and low power solution [2]. Another design challenge for wideband front-end is the stringent linearity requirement, due to large numbers of in band interferers, and the intermodulation caused by the blockers [3]. In a narrowband design, the out of band blockers are significantly reduced by RF band pass filters. However, in a wideband design, the front-end must handle signals in a wide frequency range including strong blockers.

This chapter provides discussion on broadband, highly linear RF front-ends. Two test circuits have been implemented consisting of active and passive mixer configurations.

5.1 Front-end with Active Mixer

As shown in Fig. 5.1, we propose an RF front-end that consists of an active mixer with enhanced conversion gain (total front-end gain is still moderate or low) and broadband impedance matching followed by 1st-order LPF. The mixer transconductance transistors are split into an NMOS-PMOS pair as shown in Fig. 5.2. This provides a better linearity due to the fact that some of NMOS generated non-linear components are neutralized by their MOS generated counterparts. The bias current through the mixer switching pair M5-M6 and PMOS transistor M2 is reused in M1, which results in lower power consumption and hence improved gain/power ratio. The common-drain stage (M3, M4, & R1) provides the wideband 50 Ω input impedance match. The cross-coupling capacitors C_{BW} between the input and the drain of M1 partly neutralize the input capacitance. This improves the bandwidth and the input matching at high frequency [4].

The simplified model of single ended front-end is shown in Fig. 5.3. Since only one transistor of the symmetric switching pair M5-M6 is on at any point in time therefore, mixer-switching stage can be modeled as a single fully on transistor with load resistor R_D for gain calculations. In its forward path an inverter stage (equivalent to mixer transconductance transistor) transistors M1 and M2 are biased independent of each other to amplify the input signal. This is contrary to the common practice where common source stage with load resistor is used in forward path in wideband LNAs [4][5]. The bias current of the PMOS transistor M2 is reused in the NMOS transistor M1. Furthermore, the capacitive coupling of gate of M2 to the input (using C2) also contributes to the overall

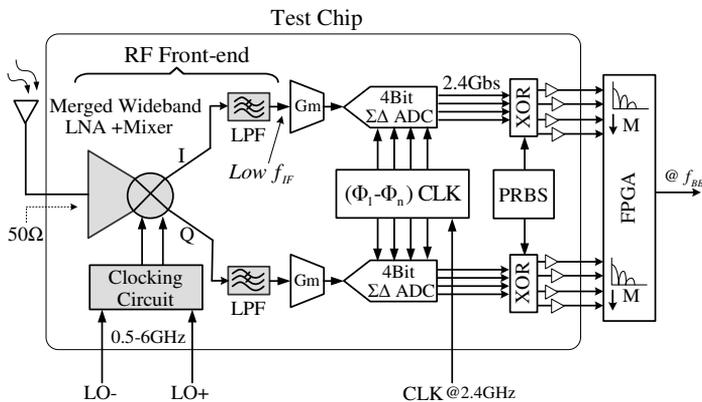


Figure 5.1 Block diagram of wideband Low-IF RF receiver front-end

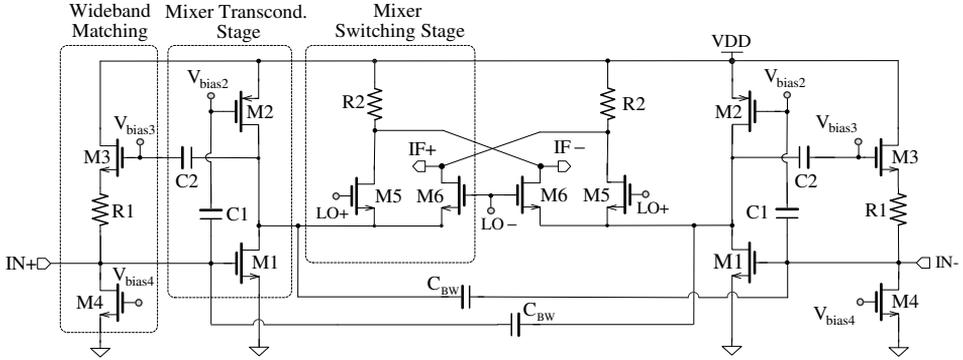


Figure 5.2 Simplified circuit diagram of wideband differential RF front-end

gain. The loading affect of M3 can be ignored since its size is much smaller compared to the size of inverter pair M1-M2. The gain of the single ended front-end shown in Fig. 5.3 can be expressed as:

$$A_v = -(g_{m1} + g_{m2}) \left[\frac{1}{g_{ds1} + g_{ds2}} \parallel \frac{1 + R_D g_{ds5}}{g_{m5} + g_{ds5}} \right] = -G_m R_{OUT} \quad (5.1)$$

where,

$$G_m = g_{m1} + g_{m2} \quad (5.2)$$

and for $g_{ds5} \ll g_{m5}$

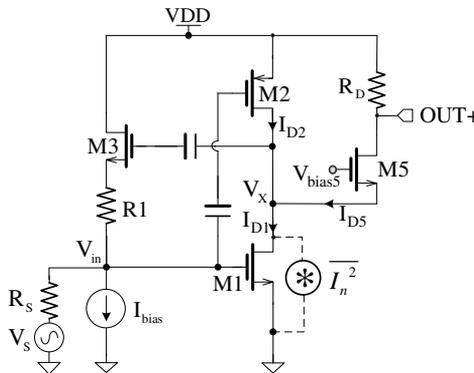


Figure 5.3 Simplified circuit diagram of left half of differential RF front-end

$$R_{OUT} = \left[\frac{1}{g_{ds1} + g_{ds2}} \parallel \frac{1 + R_D g_{ds5}}{(g_{m5} + g_{ds5})} \right] = \frac{1}{g_{ds1} + g_{ds2} + g_{m5}} \quad (5.3)$$

The common-drain feedback stage consisting of M3-M4 and R1 provides wideband 50Ω (100Ω differential) impedance match. The linearity of the common-drain feedback stage improves by connecting resistor R1 at the source of transistor M3. This in turn improves the S11 flatness over the frequency range of interest. The approximate input impedance is given by:

$$Z_{in} = \frac{1 + g_{m3} R_1}{g_{m3} (1 + G_m R_{OUT})} = \frac{1 + g_{m3} R_1}{g_{m3} (1 + |A_v|)} \quad (5.4)$$

Theoretically, the channel noise of transistors M1, M2, M3, and R1 is partially cancelled [4]. As shown in Fig. 5.3, the input signal is amplified by inverter pair M1-M2, whereas the channel thermal noise of transistor M1 denoted by the dotted line undergoes subtraction at node V_X . The channel thermal noise current (I_n^2) produces a noise voltage $I_n^2 r_{o2}$ (r_{o2} is the output resistance of M2) at node V_X . A portion of the same voltage passes through M3 and appears at the gate of transistor M1 where it is amplified and inverted. This out-of-phase noise voltage adds with the noise voltage $I_n^2 r_{o2}$ at node V_X . Since these two noise voltages are correlated, the output noise is partially canceled. The level of cancellation depends upon the forward gain, feed-back, and input impedance as well as the location of the noise source [4].

The basic motivation to use the inverter pair M1-M2 replacing the mixer transconductance transistor is to improve the linearity of the complete front-end.

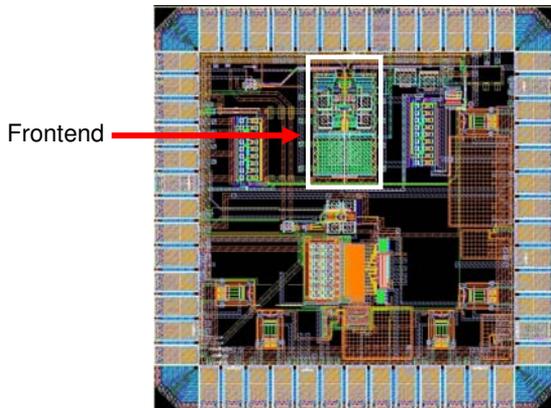


Figure 5.4 90nm CMOS chip micrograph

The input NMOS transistor M1 ($W/L=160\mu\text{m}/0.09\mu\text{m}$) is biased at its optimum gate-source voltage of 360mV with $I_D = 8\text{mA}$. The input PMOS transistor M2 ($W/L=60\mu\text{m}/0.09\mu\text{m}$) is biased at optimum gate-source voltage of 560mV with $I_D = 5\text{mA}$. At these bias points, the 3rd-order derivative of the transistors DC-characteristic is close to zero [6]. Therefore, the IP3 of this front-end is better compared to the popular approach when resistor is used instead of the PMOS transistor M2. The details of simulation and chip measurement results are given in **Paper 6**.

5.2 Front-end with Passive Mixer

The current approach for multi-standard radio utilizes either multiple receivers, each optimized for a single, narrow frequency band, or multiple narrow-band passive filters followed by one or several wideband receivers. The key limitation to these solutions is the need for multiple narrow-band passive filters [2]. These filters are expensive and space-consuming. The most economical approach is to use a single, wideband LNA and mixer followed by analog baseband [1]. This could be preceded by a broad RF band-pass filter covering all required carrier frequencies. The main obstacle for such a solution is the large linearity requirement on the RF front-end [3]. In a narrow-band design, out of band blockers are significantly reduced by the passive RF filters. In a wideband design, these blockers will instead reach the LNA and mixer, thus requiring them to manage the full blocker power. Blockers may have a power of up to 0dBm (such as in the GSM specification). In conclusion, we need to manage input blocker signals of up to 0dBm, simultaneously with the reception of a

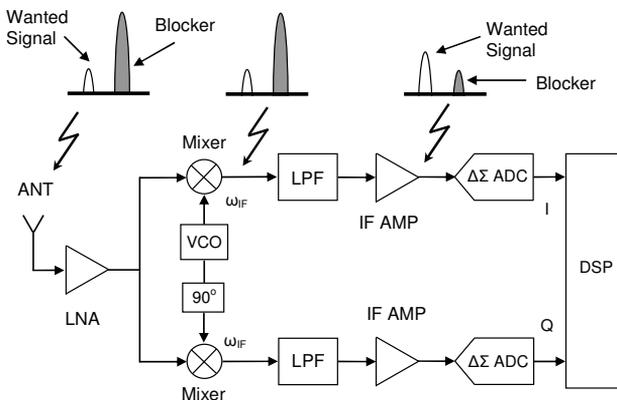


Figure 5.5 Block diagram of multiband receiver utilizing highly linear RF front-end

useful signal with maximum sensitivity. As a result, a 1dB compression point of at least 0dBm (or, more strictly, small desensitization at 0dBm), and sufficiently low intermodulation are needed. Also, there is very little room for voltage gain. 0dBm at 50 Ω corresponds to a peak-to-peak voltage of 0.62V, which occupies nearly all voltage headroom in a modern nanometer CMOS process with a supply voltage around 1V. Conventional high gain RF LNAs are thus excluded, as they will have a too large voltage swing on their output.

We propose a different approach with a low gain LNA. Fig. 5.5 shows the block diagram of a multiband receiver utilizing the proposed RF front-end. In the proposed design, a wideband LNA and mixer provides low gain and high linearity in order to accommodate strong blockers and still maintain high sensitivity. The baseband low pass filter is then utilized to prevent the full power of out of band blockers to reach the IF amplifier, so the IF amplifier will provide the necessary gain for weak signals. In this solution, the low gain of the RF front-end will increase the noise requirements on the IF amplifier. Finally, the useful signal, together with the attenuated blockers, is sampled and converted to digital form with a $\Delta\Sigma$ AD-converter. The presence of an oversampled ADC not only helps in maintaining a large dynamic range but also relaxes the analog filter requirement [7]. An alternative solution could be to have the $\Delta\Sigma$ AD-converter to accommodate the full dynamic range (blocker and weak signal) by omitting both the low pass filter and the IF amplifier [8].

A circuit schematic of the proposed differential wideband RF front-end is shown in Fig. 5.6. The architecture consists of an inverter-like common gate low

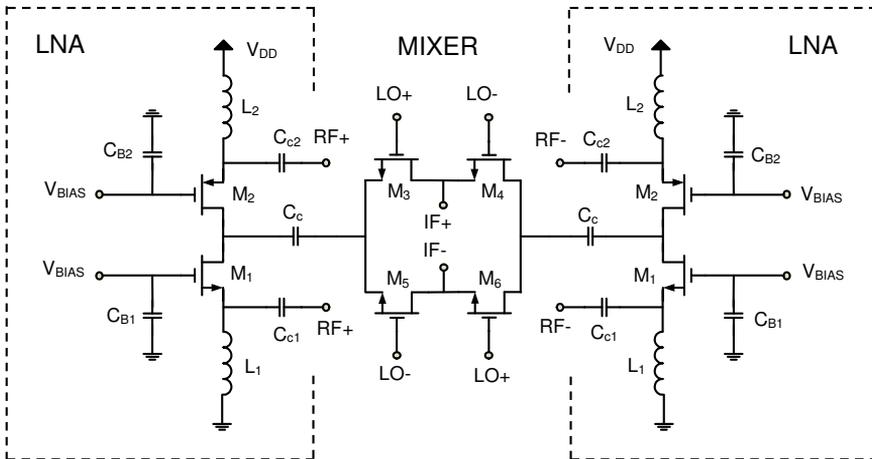


Figure 5.6 Schematic diagram of proposed wideband RF Front-end

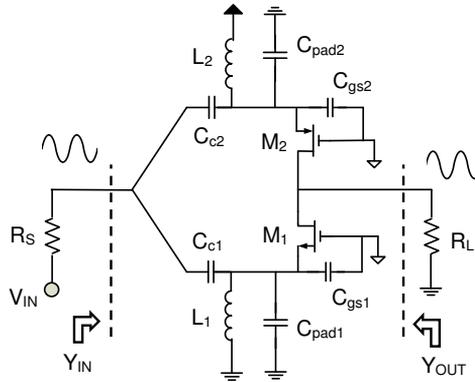


Figure 5.7 One branch of differential inverter-like CG-LNA showing important parasitic capacitances

noise amplifier (CG-LNA) followed by a passive ring mixer. For wideband and ultra-wideband applications, the CG-LNA configuration is more popular due to its simple and robust input matching. In addition, it has good linearity, low power consumption and good input output isolation [3,9]. The noise figure of a common source low noise amplifier (CS-LNA) is generally superior to that of CG-LNA, however, lower noise figure is often achieved through higher power consumption [10]. Another advantage of CG-LNA is its better noise performance for higher operating frequency ratios ω_o/ω_t , where ω_o is the operating frequency and ω_t is the transistor transit time frequency, as its induced gate noise is only a weak function of ω_o/ω_t , while the CS-LNA's noise is proportional to ω_o/ω_t [10]. Earlier studies have indicated that current reuse techniques are very useful for low power designs [11,12]. A lower noise figure with less power consumption can be achieved by g_m -boosting technique [10].

However in a capacitor cross-coupled CG-LNA, the input gate source voltage is doubled which limits the linearity. We propose a differential wideband LNA consisting of a pair of NMOS and PMOS common gate amplifiers in each branch, sharing the same load. L_1 , L_2 are off-chip biasing inductors while C_{C1} , C_{C2} are AC coupling capacitors with values much larger than C_{gs} . One prime advantage of this architecture is that the transistors M_1 and M_2 share same bias current. From Fig. 5.7, the input admittance can be expressed as:

$$Y_{IN} \approx (g_{m1} + g_{m2}) + s(C_{pad1} + C_{pad2} + C_{gs1} + C_{gs2}) + \frac{1}{s(L_1 + L_2)} \quad (5.5)$$

The off-chip biasing inductors have large values, therefore the input impedance is mainly dependent on transistor effective transconductance ($G_{m,eff}$).

$$Z_{IN} \approx \frac{1}{g_{m1} + g_{m2}} = \frac{1}{G_{m,eff}} \quad (5.6)$$

The input impedance as given in (5.6) indicates that the broad-band 50Ω matching can be achieved with approximately half bias current as compared to a simple common gate circuit. This helps in minimizing the overall power consumption. Also the $G_{m,eff}$ is roughly two times larger than in simple common gate amplifier. The output admittance can be expressed as:

$$Y_{OUT} \approx (g_{ds1} + g_{ds2}) + s(C_{dg1} + C_{dg2}) \quad (5.7)$$

Ignoring the gate noise, the noise factor can be expressed as:

$$F = 1 + \frac{\gamma}{\alpha} \left[\frac{1}{G_{m,eff} R_s} \right] \quad (5.8)$$

where $\alpha = G_{m,eff} / (g_{d01} + g_{d02})$. When the input is matched (i.e. $G_{m,eff} R_s = 1$), the noise factor is $F = 1 + \gamma/\alpha$. However, considering practical specifications, the input match and noise figure tradeoff can be exploited in order to have a lower noise figure with an acceptable mismatch. Increasing $G_{m,eff}$ will result in a lower noise figure at the cost of more power consumption. However, the current reuse technique makes this power penalty insignificant. In our implementation, the transistors M_1 ($W/L=15\mu\text{m}/0.09\mu\text{m}$) and M_2 ($W/L=45\mu\text{m}/0.09\mu\text{m}$) with nominal drain bias current of 2.8mA, provide $g_{m1} = 13.66\text{mS}$ and $g_{m2} = 15.24\text{mS}$. Therefore, $G_{m,eff} R_s = 1.445$, and $Z_{IN} = 34.6\Omega$, while the corresponding $S_{11} = -14.8\text{dB}$, which means that only 3.3% of the incident power is reflected. With this input matching condition the noise factor can be expressed as: $F = 1 + 0.692\gamma/\alpha$. Hence, an overall LNA noise figure close to 3dB can be achieved.

Another, advantage of this inverter-like architecture is its improved linearity. The complementary characteristics of the NMOS and PMOS transistors can be utilized for cancelling the first and second derivative of g_m (g'_m and g''_m) in a wide range of input voltages [9,13,14]. As our objective is to utilize a large part of the available voltage headroom for our signal, this is essential. This is in contrast to other solutions utilizing g''_m cancelling utilizing

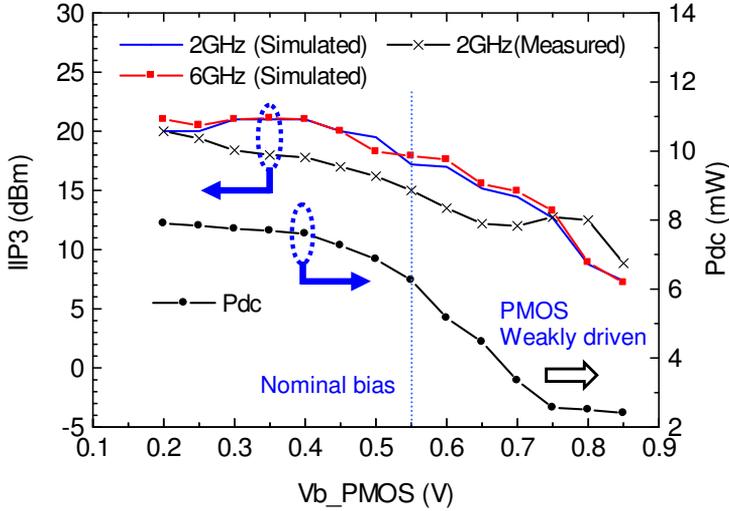


Figure 5.8 LNA IIP3 response versus PMOS bias voltage

subtraction between two signal paths, which cancels the g_m^* term only in a limited voltage range [15]. The result is a high IIP3 value but no improvement in the compression point, as can be seen from the measured curves in [15,16].

Basically, the 3rd order nonlinearity component mainly originates from the transistor I-V characteristics. The simple Taylor series expansion of I_{DS} is given by:

$$I_{DS} = g_m V_{gs} + g_m' V_{gs}^2 + g_m^* V_{gs}^3 + \dots \quad (5.9)$$

The same nonlinearity reflects in the load current that can be expressed as follows [9]:

$$I_L = g_1 V_{IN} + g_2 V_{IN}^2 + g_3 V_{IN}^3 + \dots \quad (5.10)$$

where $g_1 = \partial I_L / \partial V_{IN}$, $g_2 = \frac{1}{2!} (\partial^2 I_L / \partial V_{IN}^2)$ and $g_3 = \frac{1}{3!} (\partial^3 I_L / \partial V_{IN}^3)$. We have analyzed the

large signal behavior of g_3 for various bias scenarios and calculated g_3 for the dynamic bias points. A detailed discussion on biasing scenarios and simulation results are given in [9]. Chip measurement results also validate our approach and indicate that the proposed architecture provides high linearity in a wide frequency band. Fig. 5.8 shows the variation in LNA IIP3 and power consumption by change in PMOS bias voltage. The plot indicates that overdriven transistors are more linear at the cost of more power consumption. The plot also indicates that the IIP3 is not sensitive to bias variations, therefore,

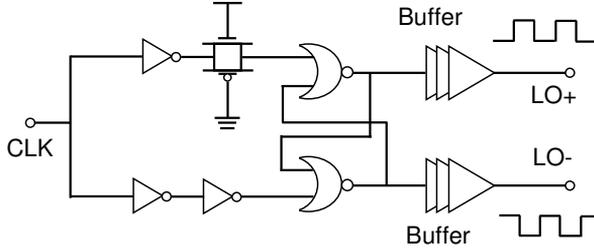


Figure 5.9 Circuit diagram of LO driver

as compared to other distortion cancellation architectures the proposed circuit is more robust. The measured result shows that the IIP3 varies between +8dBm and +20dBm while the corresponding power consumption varies between 2.4mW and 7.9mW.

We have chosen a passive ring mixer configuration for our implementation. The motivation behind this topology is its relatively high linearity along with low $1/f$ noise. Moreover, it does not consume any DC power as compared to an active mixer. Earlier studies have indicated that with low input swing, the input voltage dependent $1/f$ noise at the mixer output is quite low. The random duty cycle variations of the LO clock is a prime contributor of $1/f$ noise [17,18]. As compared to active mixer implementations the relative level of $1/f$ noise in a passive mixer is much lower. For theoretical noise analysis, we can express the output noise power spectral density (PSD), excluding the contribution from load as follows:

$$S_{n,out} = 2\tau [4kT(R_S + 2R_{SW})] \left[\frac{R_L}{R_S + R_L + 2R_{SW}} \right]^2 \quad (5.11)$$

Where $\tau = \Delta T/T$ is the effective duty factor of the LO clock and R_L , R_S , R_{SW} stand for the load, source and transistor switch on-resistance, respectively. The power conversion gain of the mixer can be expressed as:

$$G_p = \frac{4}{\pi^2} \sin^2(\pi\tau) \left(\frac{R_L}{R_S + R_L + 2R_{SW}} \right)^2 \quad (5.12)$$

acknowledging that for a rectangular waveform with ± 1 amplitude and a duty factor of τ , the first harmonic amplitude is $\frac{4}{\pi} \sin(\pi\tau)$. In passive mixer implementations, transistors with large overdrive are preferred for good linearity and noise figure [19] that is modeled here by the full swing rectangular

waveform. Based on this we can calculate the single sideband noise factor (F_{SSB}) of a passive ring mixer as follows:

$$F_{SSB} = \frac{2S_{n,out}}{G_p \times 2S_{n,R_s}} \quad (5.13)$$

where $S_{n,R_s} = 4kTR_s$ and the factor 2 accounts for the image bands. Hence, we find:

$$F_{SSB} = \frac{2\tau}{\sin^2(\pi\tau)} \left[\frac{\pi^2}{4} \left(1 + \frac{2R_{sw}}{R_s} \right) \right] \quad (5.14)$$

where $R_L = R_s$ is assumed. It can be observed that (5.14) achieves a minimum for clock duty factor, $\tau = 0.35, \dots, 0.4$, which reduces the F_{SSB} by a factor of 0.88 (i.e 0.5dB) as compared to $\tau = 0.5$.

For our implementation, we have chosen NMOS switching transistors (M_3 - M_6) with optimum size ($W/L=100\mu\text{m}/0.09\mu\text{m}$) that provides a low NF with improved linearity. The mixer transistors are driven by a differential non-overlapping clock. Fig. 5.9 shows a circuit diagram of the LO driver. For a lower noise, we have optimized the circuit using a 40% duty cycle clock (i.e: $\tau = 0.4$). In our implementation, $R_{sw} = 3\Omega$ and for $R_s = 50\Omega$ the calculated value of mixer noise figure under these condition is $F_{SSB} = 3.9\text{dB}$ which is close to the value obtained from simulation, i.e. 4.15 dB. Fig. 5.10 and Fig. 5.11 show the simulated time domain LO clk waveforms at 2GHz and 5GHz respectively.

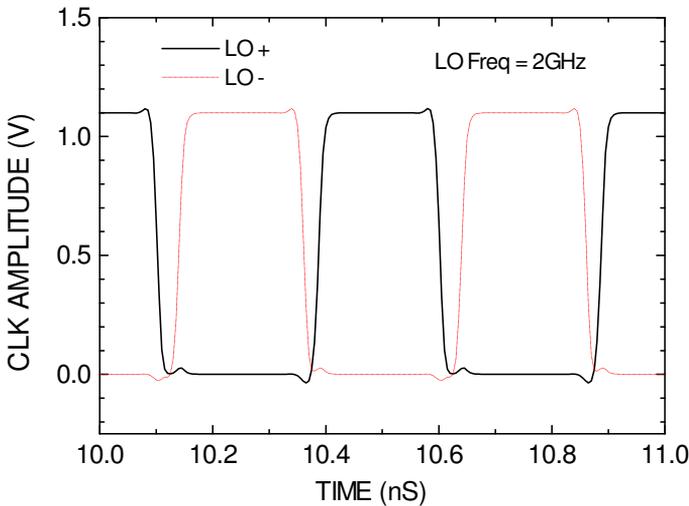


Figure 5.10 LO clk waveform at 2GHz

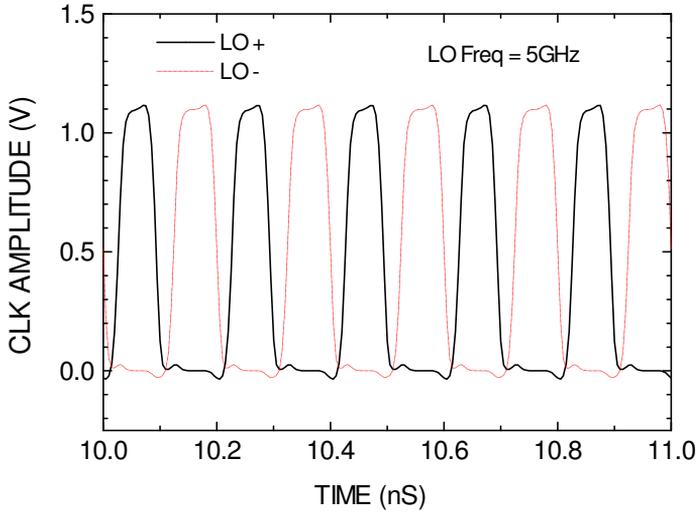


Figure 5.11 LO clk waveform at 5GHz

Fig. 5.12 shows the variation in G_P and F_{SSB} with clk duty factor τ . The result indicates that the optimum value τ of is between 0.35 and 0.4 for a lower noise figure. Fig. 5.13 shows the chip layout, chip micrograph and the test fixture. The photograph of chip measurement setup is shown in Fig. 5.14. The details of chip measurement results are provided in **Paper 7**.

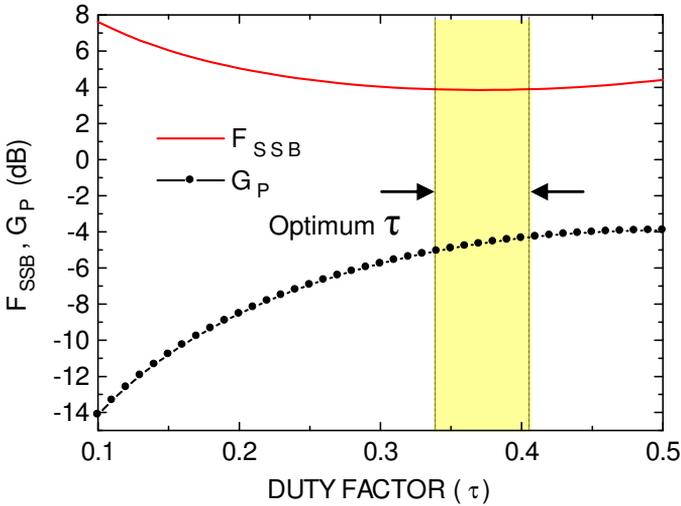


Figure 5.12 Variation in G_P and F_{SSB} with clk duty factor (G_P for $R_L \gg R_S$)

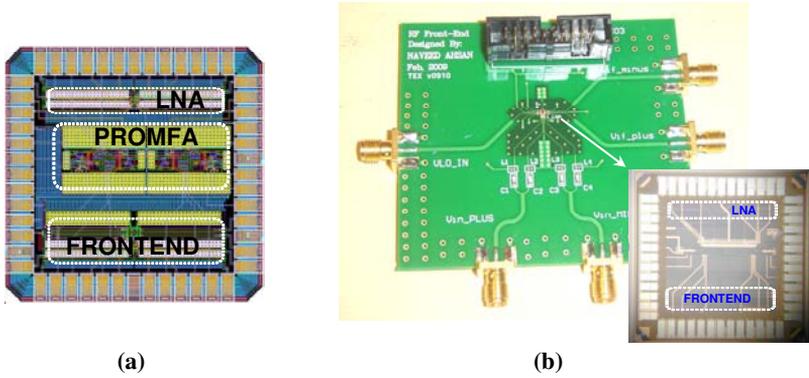


Figure 5.13 (a) Chip layout (b) Test fixture and chip micrograph

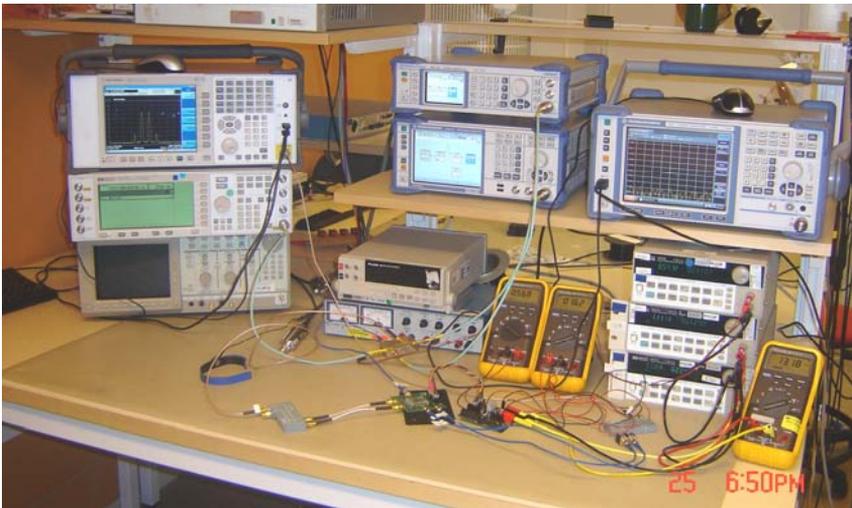


Figure 5.14 Photograph of chip measurement setup

5.3 Performance Comparison

Table 5.1 shows a comparison of results of our work with recent publications. The chip measurement results indicate that the front-end with passive mixer configuration has proven to be more useful. The NF performance of this front-end is comparable to others but achieved with much lower power. The IIP3 of this architecture is much better and to the best of our knowledge there is no reported CMOS RF front-end that can manage 0dBm blockers. Therefore, the proposed architecture is the only reported work that tackles the problem of large blockers.

TABLE 5.1
PERFORMANCE COMPARISON WITH RECENT PUBLICATIONS

	Front-end with passive mixer	Front-end with active mixer	[2]	[20]	[21]
Technology	90nm	90nm	90nm	90nm	65nm
P (mW)	6.2	23.6	9.8	76	39
Freq Range (GHz)	0.5 – 6	0.5 - 6	0.1 – 3.85	2 – 5.8	2 – 8
Bandwidth (GHz)	5.5	5.5	3.75	3.8	6
Voltage Gain _{max} (dB)	4.5	10	20	22	23
NF _{min} (dB) @ IF(MHz)/RF(GHz)	6.25 (10/2)	7 (30/1.5)	8.4 (70/2.1)	12 (10/5)	4.5 (100/4.5)
1dB-CP (dBm)	+1.5	-14	-12.83	- 20	
IIP3 (dBm)	+11.73	+2.5	–	- 4	- 7
IIP2 (dBm)	+26.2	+40	–	–	18
Pin_Blocker (dBm) @ΔIF=120MHz	0	-10	-	-	-
S11 (dB)	<- 8.8*	<- 8*	<- 10	<- 15	<- 8
Vdd (Volt)	1.1	1.1	1.2	2.7	1.2
LO-RF Isolation @6GHz (dB)	48	38	–	–	–
Active Area (mm ²)	0.086	0.049	0.88	0.2	0.09

* S11 including microstrip lines on FR4 PCB.

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

We have investigated the feasibility of a flexible and programmable circuit PROMFA. The presented concept has a great potential for the implementation of flexible RF and microwave circuits. The idea of having flexible RF systems with reconfigurable circuit blocks is becoming more and more popular. PROMFA approach is one feasible option in this regard. A single chip with multiple PROMFA cells is capable of performing different tasks depending on requirements. We have demonstrated the feasibility of tunable oscillators, tunable filters and a low noise amplifier by configuring individual PROMFA cells. The possibility of dynamic reconfiguration is a big advantage and it gives a lot of flexibility to the whole system. Measured and simulated results of both test circuits indicate reasonable performance in all three configurations. However, the overall performance of a single application optimized circuit will always be superior to a flexible and multifunctional circuit.

Modern radio receivers require multiband and multistandard operation. We have presented the design and implementation of tunable and wideband highly linear LNAs that are suitable choice for these applications. The chip

measurement results indicate that varactor tuned LNAs have a low noise figure with good linearity. However, the tuning range is limited by varactor capacitance. The chip measurement results of wideband LNA are very encouraging and indicate that the proposed architecture is a suitable choice for a highly linear multistandard radio receiver where the linearity and dynamic range requirements are extremely tough.

The idea of a low gain RF front-end has been presented. The proposed architectures are very well suited for wideband receivers with stringent linearity requirements. The front-end configuration with passive mixer has shown excellent performance in terms of linearity with very low power consumption.

6.2 Future Work

The proposed PROMFA approach has shown great potential for the implementation of flexible RF circuits. The concept is not limited to a certain technology or architecture. It can be implemented with different technology process and with different architectures. Therefore, the concept of flexible circuit implementations using reconfigurable blocks will be useful for future multifunctional systems.

As mentioned in previous section that varactor tuned LNAs have a limited tuning range. The varactor quality factor (Q) also decreases with the increase in capacitance. Tuning technique that can maintain the high Q value will be more adequate. MEMS based low loss RF switches can be one feasible option for the implementation of switchable LNAs. However, considering a multiband and multistandard receiver wideband LNAs offer more adequate solution. Unlike tunable and switchable LNAs their circuit implementation is not complicated. Therefore, wideband highly linear LNAs have a great potential for multistandard receivers.

The proposed low gain front-end architectures are also well suited for broadband and highly linear receivers. A complete receiver utilizing proposed highly linear front-ends with oversampled $\Delta\Sigma$ ADC would be a viable solution for software defined radio.