

DESIGN AND IMPLEMENTATION OF COMPARATOR FOR SIGMA-DELTA MODULATOR

Examensarbete utfört i Elektroniksystem
vid Linköpings Tekniska Högskola

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Noor Aizad

Reg nr: LiTH-ISY-EX--06/3826--SE

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ABSTRACT

Comparator is the main building block in an ADC architecture. Main purpose of the comparator is to compare a signal with a reference signal and produce an output depending on whether the input signal is greater or smaller than reference. Many architectures for comparators exist for various purposes. In this thesis, Latched comparator architecture is used for sigma delta modulator. This particular design has two main characteristics that are very important for sigma delta application. First characteristic is the cancellation of memory effect which increases the speed and reliability of the system and the second is, with this architecture, high sensitivity can be achieved.

The design and implementation of latched comparator for sigma delta modulator is presented in this thesis work. Various non-linearities and performance parameters are discussed in detail. Practical implementation and circuit design issues are highlighted to achieve maximum sensitivity along with reasonable speed and accuracy.

ACKNOWLEDGMENTS

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1

INTRODUCTION

1.1 OVERVIEW

1.1.1 DYNAMIC LATCH

A dynamic latch is defined as the memory unit that stores the charge on the gate capacitance of the inverter. A simple dynamic latch is shown in figure 1.1.

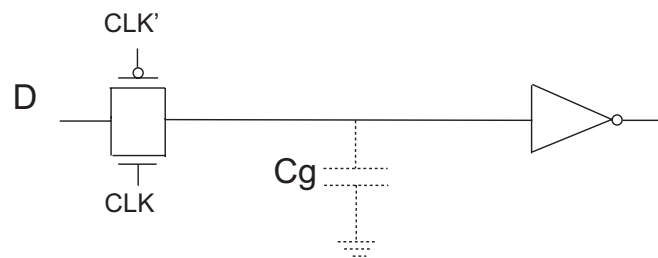


Figure 1.1: Simple dynamic latch.

The circuit is driven by a clock. During one phase of the clock ($clk = 1$) when the transmission gate is closed, the latch acts transparent, and the inverter is directly connected to the input. In the other phase of the clock ($clk = 0$), the transmission gate opens and the inverter's output is determined by the storage node.

Setup and hold times determined by the transmission gate must be taken into

consideration in order to ensure proper operation of the latch i.e adequate level of voltage is stored on the gate capacitance of the latch.

1.1.2 PRE-AMPLIFIER

The pre-amplifier used in this design is a simple common source differential amplifier with PMOS transistors as active loads. Pre-amplifier is followed by a small circuit which is basically used for two main functions. First it is used to avoid the kick back effect from the latch to the input signal which is made possible by using two NMOS transistors which operate on the clock. Kick back is the noise observed at the input signal which is produced due to high voltage variations at the regenerative nodes of the latched and is coupled to the input through the parasitic capacitance of the transistors. The second purpose of using the kick back protection circuitry is to create charge imbalance in the latch when it switches from reset mode to regeneration mode.

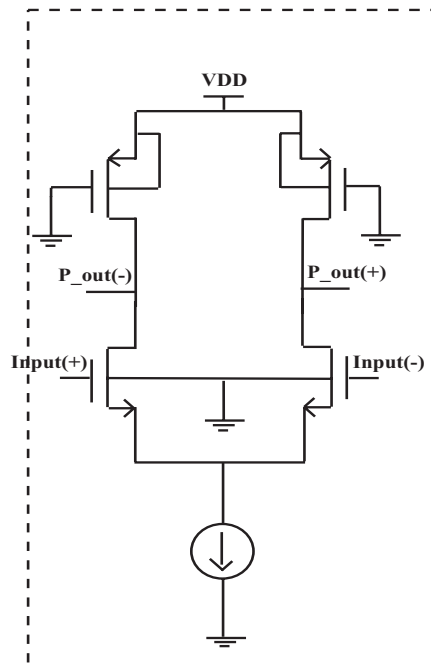


Figure 1.2: Pre-amplifier circuit diagram.

1.2 COMPARATOR ARCHITECTURE

The comparator [1] uses the regenerative structure of a dynamic latch. It consists of two inverters connected back to back with each other forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch.

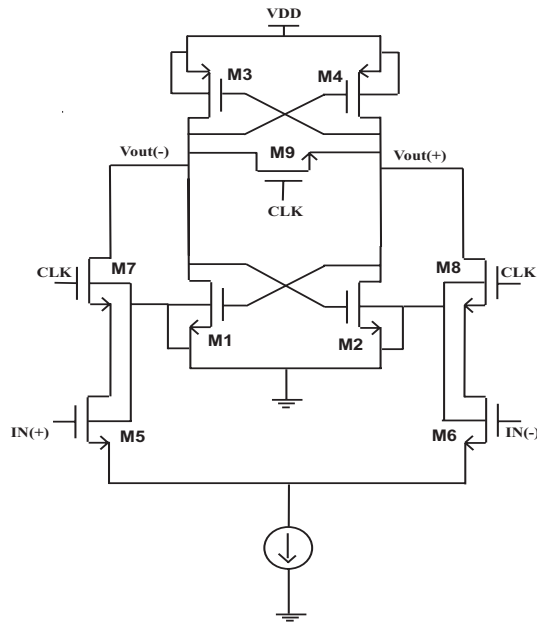


Figure 1.3: Comparator.

1.2.1 COMPARATOR OPERATION

The comparator senses the charge imbalance produced by the input at the pre-amplifier and reacts to that imbalance to create desired digital voltage levels at the output. In this manner this comparator can also be called a current comparator. The whole operation of comparison is divided into two phases of the clock. In the first phase when the clock is high, the switch transistor closes and short-circuits both the outputs of the comparator and set them to certain DC voltage level around mid point of VCC. In the same phase the pre-amplifier creates charge imbalance at the differential nodes of the latch. In the second phase, the pre-amplifier is disconnected from the comparator and the

short-circuiting transistor is also switched off. Now the comparator (or the inverter pair) amplifies the charge imbalance into digital voltage levels on the differential nodes.

1.2.2 SPECIFIC REGENERATIVE STRUCTURE

The following parameters were taken into consideration before finalizing the specific chosen architecture for the latch.

1) SPEED:

A comparator with only two inverters connected to each other in a closed loop makes the regenerative structure very fast. Primarily because of the simplicity of the circuit as only 4 (two NMOS - PMOS pair) transistors are used in the inverter combination. This reduces the parasitic capacitance and hence high comparison speed can be achieved.

2) RAIL - TO - RAIL OUTPUT:

As in most of the other designs of the latches, there is always a biasing transistor connected to the source of the NMOS in the regenerative loop. This raises the VOL for the latch and hence minimum value close to the VSS cannot be achieved. In this chosen architecture, the biasing transistor is eliminated and self biasing techniques are used to attain required voltage levels and therefore rail to rail output is closely achieved.

3) RESET:

During the reset phase, the switching transistor short circuits the latch's outputs and the output is set to a point approximately equal to $1/2 V_{CC}$. The advantage for this characteristic feature is that in the second phase the regenerative loop can easily shift the output to the corresponding digital levels as determined by the charge imbalance. This also increases the speed and performance of the comparator. In other comparator designs, the latch is usually set to a floating state in the reset mode, so then chances of correct evaluation decreases as the outputs are not short-circuited to same DC level. This leads to a memory effect in the latch.

1.3 BASIC FUNCTIONALITY

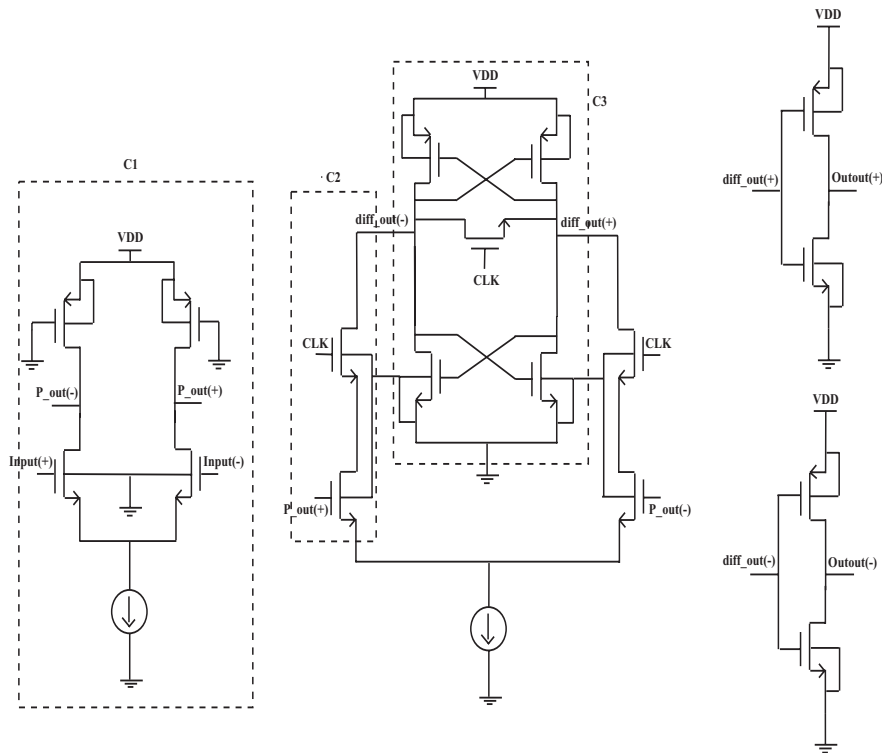


Figure 1.4: Complete circuit diagram of the latched comparator.

$V_{in}(+)$ and $V_{in}(-)$ are the two input signals for the pre-amplifier C1. The change in these two signals is amplified by the pre-amplifier. From the pre-amplifier, the amplified voltage difference is transferred to the gates of the circuit C2. C2 is a small circuit that creates charge imbalance in the latch and minimizes the kickback noise effects from latch to the pre-amplifier. The latch operates in two phases; reset and regeneration. In the Reset phase the charge imbalance is created on the differential nodes of the latch proportional to the variation in the input signal. In regeneration mode, the voltage imbalance on the nodes is amplified to the rail-to-rail digital levels by the NMOS and PMOS regeneration loops.

2

NON-LINEARITIES AND PERFORMANCE PARAMETERS

2.1 KICK BACK

Almost all the analog to digital converters use various architectures of latched comparators. The latched comparator regenerates the input signal to a full scale digital level. These high voltage level variations at the regeneration nodes are coupled to the input of the comparator through parasitic capacitance of the transistors and disturbs the voltage level of the input signal. This effect is called kick-back. There exits numerous solutions to this problem [2], few of which are described as follows:

2.1.1 ISOLATION TRANSISTORS

This kind of design of comparator incorporates a set of NMOS transistors that isolates the input signal from the regenerative output nodes, where the voltage variations are large. Hence, this results in low kick back noise. The comparator designed in this work also includes this feature. The disadvantage of using this technique is that it adds parasitic load to the output of the latch, which reduces the operational speed of the latch.

2.1.2 PRE-AMPLIFIER

The most common solution to reduce the kick back effect is to add a pre

amplifier before the comparator. This would increase the power consumption but speed and gain of the system can be increased.

2.1.3 NEUTRALIZATION

This technique is applicable to those circuits in which the differential inputs are directly connected to the regenerative nodes. Voltage variations on the regenerative nodes cause the disturbance on the input due to non-zero impedance of the pre-amplifier mainly caused by C_{gd} . Adding capacitance equal to C_{gd} between drain and bulk of input transistor would cancel the noise because the voltage variations as complimentary due to differential signal.

2.1.4 SAMPLING SWITCHES

Inserting sampling switches before in the differential input of the latch reduces the kick back and also can be used in some cases where sampling is required.

2.2 CLOCK FEED THROUGH

In the latched comparator architecture that is used in this work contains a single phase clock. This clock is used to set the differential nodes of the comparator to mid point of VCC to clear the memory effect during reset mode. Also this clock signal is connected to the isolation transistors. These transistors disconnect the input signal from the regenerative nodes of the latch during regeneration phase. Switching of the clock produces distortion on the input signal. The following figure 2.1 shows the parasitic capacitive coupling path of the transistors through which clock feed through effect is observed

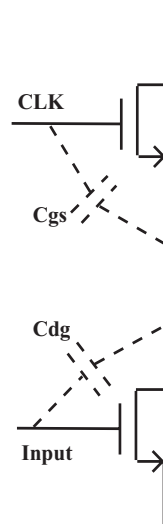


Figure 2.1: Parasitic capacitance coupling.

In the following figure 2.2, an undistorted sinusoidal signal is shown as a reference for the clock-feed through effected input signal.

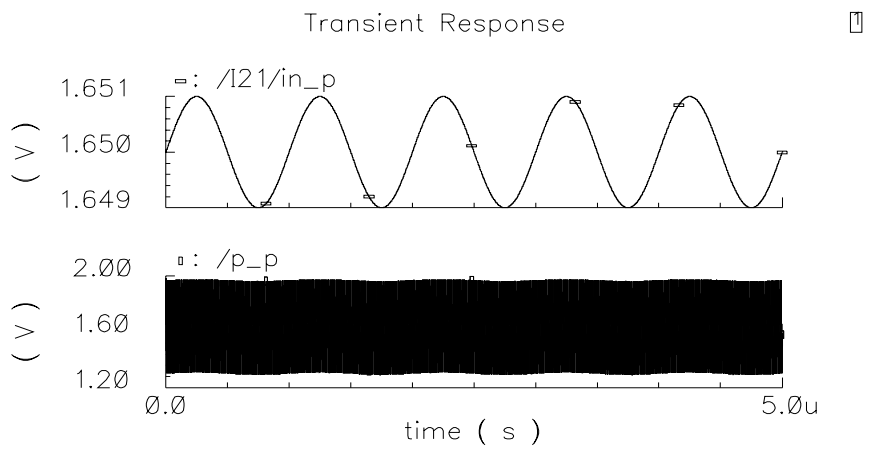


Figure 2.2: Clock feed through.

2.3 META STABILITY

Normally the output of the inverter has two stable states; either VCC or ground. If the input is set to a mid point, e.g., ' V_m ', then ideally the output should also be held at the mid point. This mid point is called "metastable" point. At this point the inverter has maximum gain. If the input is slightly deviating (' $V_m + dV$ ' or ' $V_m - dV$ ') from the ' V_m ' level, then the output quickly sets either to the supply voltage or to ground. The sensitivity of the inverter is determined by these two factors: 1) gain, and 2) what magnitude of ' dV ' does it require to switch its output to corresponding digital voltage level.

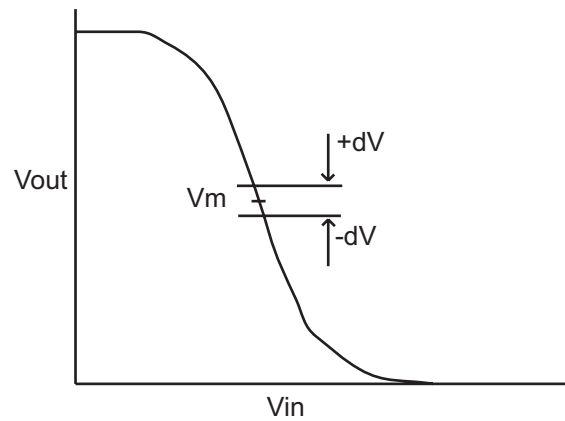


Figure 2.3: Voltage transfer characteristics of inverter.

In the above figure, the band between ' $+dV$ ' and ' $-dV$ ' indicates the area for the input voltage for which the output is uncertain for its logic level. In this region, due to noise or other disturbances, the output can easily be switched to wrong logic level that is not corresponding to input. This band is basically the bottle neck for the comparator designs. Reducing this metastable band increases the reliability and performance of the comparator.

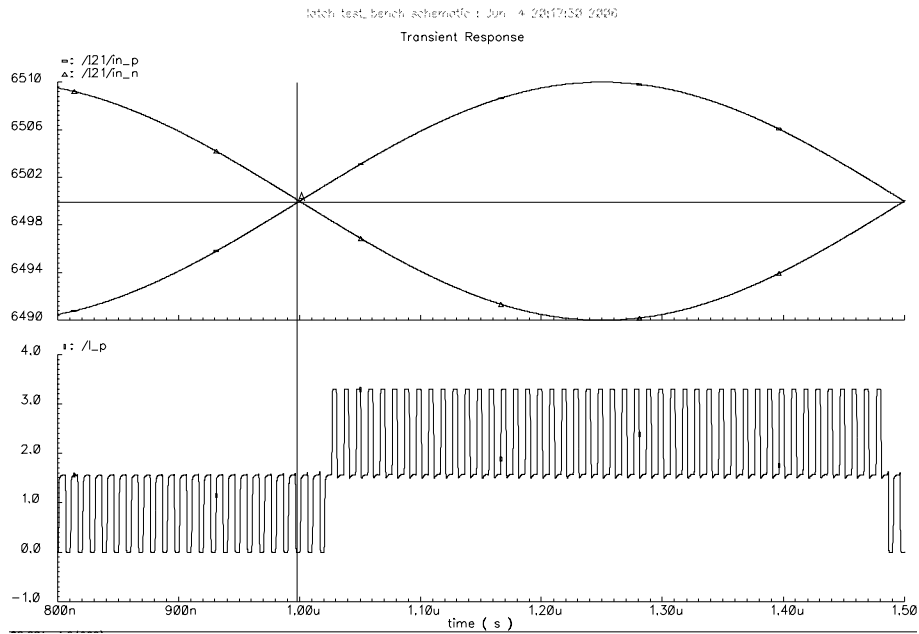


Figure 2.4: Comparator offset simulation.

2.4 COMPARATOR OFFSET

Due to unsymmetries and paracitics in the design, the comparator will exhibit an input-referred offset. The above diagram is the simulation result showing the effects of comparator offset and how it effects the output of the comparator. In this particular case, the width of the ‘reset switching capacitor’ was slightly changed and it increased the offset error. In the ideal situation, the output should switch as soon as the input differential sinusoids cross each other, but due to the offset error, the accuracy is effected. Other than this ‘reset switching capacitor’, there are other factors like the bias current, the width of NMOS/PMOS transistor of the regenerative loop and input isolation transistors of the comparator that effect the offset error of the circuit. However, when used in the sigma-delta modulators, the effect of comparator offset is in general suppressed by the noise-shaping loop and is therefore not as important as comparator memory effects and metastability.

2.5 SPEED OF THE COMPARATOR

Speed of the comparator is highly dependant on the regenerative time constant of the latch. We can model the latch with two inverters connected in the loop with positive feed back configuration as shown in figure 2.5.

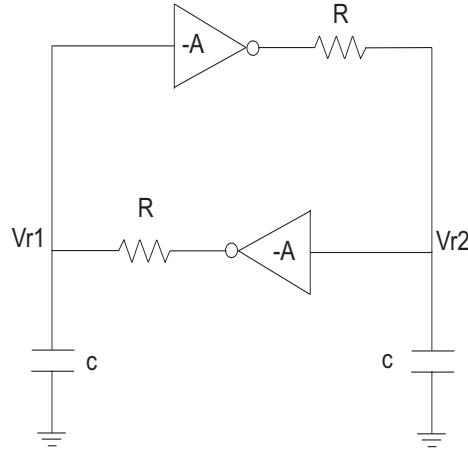


Figure 2.5: Model for a comparator.

The regenerative nodes are marked as Vr1 and Vr2. These nodes are capable of converting small voltage difference to a full logic level. The time required for the amplification is dependant on the initial voltage difference 'Vdiff' which is produced by the pre-amplifier in the form of slight charge disturbance during reset phase. The time required for regeneration is given as:

$$t_{comp} = \frac{(RC)}{A-1} \ln\left(\frac{(Vdiff)}{Vdd}\right)$$

(2.1)

where 'A' is the small signal gain of the inverters. From this equation [3], it can be observed that the time for comparison depends upon time constant RC, gain of the inverter and initial voltage difference.

2.6 MEAN TIME TO FAILURE

Mean time to failure is an estimation of the average time until a component first failure or disruption of the first operation is observed. As demonstrated in [3],[4] If the time given to make a decision is T , and the input follows the uniform distribution between the range '-Vdiff' to 'Vdiff', then the probability that the comparator will not amplify to full logic levels can be written as:

$$P\left(t_{comp} > \frac{T}{2}\right) = e^{(-1)\left(\frac{T}{2}\right)\left(\frac{1}{RC}\right)(A_0 - 1)} \quad (2.2)$$

Using the above equation of probability, mean time to failure can be calculated as:

$$MTF = \frac{1}{F_s(P)} \quad (2.3)$$

where, 'Fs' is the sampling frequency of the latch and 'P' is the probability that the comparator will not amplify to full logic levels. In this thesis work, the inverter is modelled as a latch. As inverter is a single pole system, therefore the MTF formula can be further simplified as:

$$MTF = \frac{e^{\frac{(\pi)(F_{unity})}{F_s}\left(1 - \frac{1}{A_0}\right)}}{F_s} \quad (2.4)$$

3

SMALL SIGNAL MODELS FOR THE COMPARATOR

3.1 SSM FOR PRE-AMPLIFIER

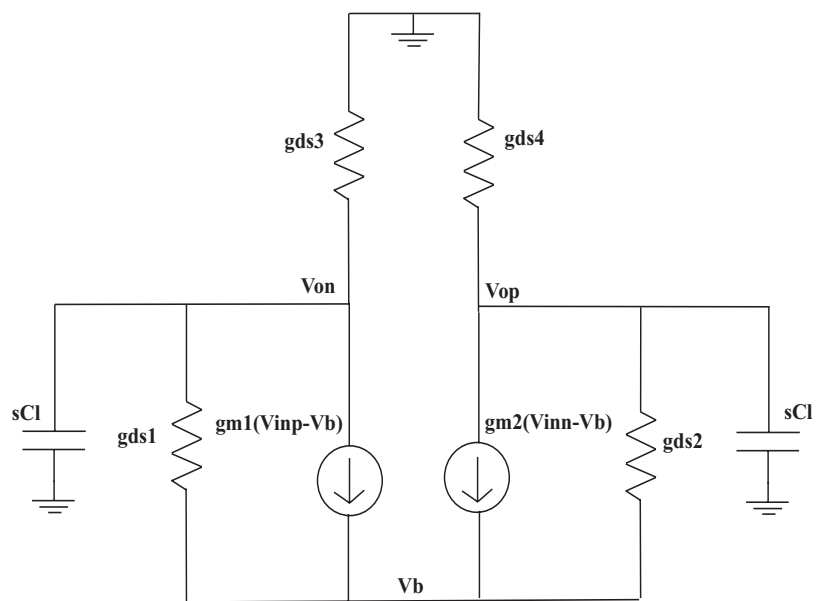


Figure 3.1: Small signal model for pre-Amplifier.

Applying KCL on the circuit, the following equations can be derived for corresponding voltage nodes:

At Von:

$$(V_{on})g_{ds3} + (V_{on} - V_b)g_{ds1} + (V_{inp} - V_b)g_{m1} + (V_{on})(sCl) = 0 \quad (3.1)$$

At Vop:

$$(V_{op})g_{ds4} + (V_{op} - V_b)g_{ds2} + (V_{inp} - V_b)g_{m2} + (V_{op})(sCl) = 0 \quad (3.2)$$

At Vb:

$$(V_{on} - V_b)g_{ds1} + (V_{op} - V_b)g_{ds2} + (V_{inp} - V_b)g_{m1} - (V_{inn} - V_b)g_{m2} = 0 \quad (3.3)$$

Assuming $g_{ds1}=g_{ds2}$ and $g_{m1}=g_{m2}$, then the gain of the Pre-Amplifier is Calculated to be:

$$A = \frac{g_{m1}}{g_{ds1} + g_{ds3} + sCl} \quad (3.4)$$

And the DC gain is given as:

$$A_0 = \frac{g_{m1}}{g_{ds1} + g_{ds3}} \quad (3.5)$$

3.2 SSM FOR KICK BACK CIRCUIT

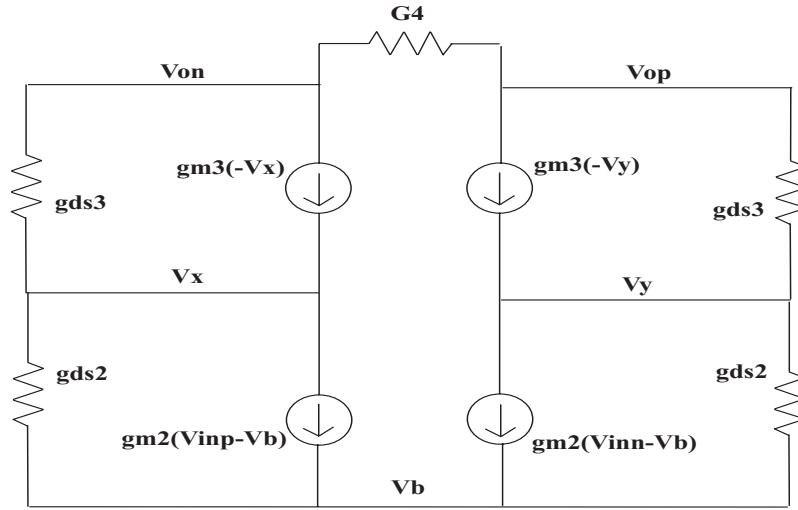


Figure 3.2: Small Signal Model for Kick back protection circuitry.

Small signal analysis on this part is carried out for the reset phase of the latch when all the switching transistors are turned 'ON'. During this reset phase, the voltage difference from the pre-amplifier creates a charge imbalance on the regenerative nodes of the comparator through this protection circuitry. This stage has its own gain which is added along with the gain of the pre-amplifier after which the charge imbalance is created on the nodes of the comparator. In this way the effect of the gain of this protection circuit is added to the overall gain of the comparator.

By applying KCL to the small signal model of this circuit, the following equations can be written:

At V_{op} :

$$(V_{op} - V_{on})G4 + gm3(-Vy) + (V_{op} - Vy)gds3 = 0$$

(3.6)

At Von:

$$(V_{on} - V_{op})G_4 + gm_3(-V_x) + (V_{on} - V_x)g_{ds3} = 0 \quad (3.7)$$

At Vx:

$$gm_3(-V_x) + (V_{on} - V_x)g_{ds3} - gm_2(V_{inp} - V_b) - (V_x - V_b)g_{ds2} = 0 \quad (3.8)$$

At Vy:

$$gm_3(-V_y) + (V_{op} - V_y)g_{ds3} - gm_2(V_{inn} - V_b) - (V_y - V_b)g_{ds2} = 0 \quad (3.9)$$

The DC gain can be written as:

$$A_0 = \frac{((gm_2)(g_{ds3} + gm_3))}{(g_{ds2})(g_{ds3}) + 2(G_4)(g_{ds2} + g_{ds3} + gm_3)} \quad (3.10)$$

3.3 SSM FOR THE LATCH

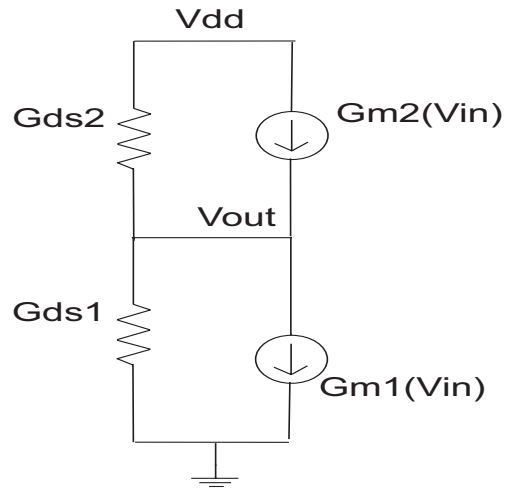


Figure 3.3: Small signal model of an inverter modelled as latch.

We are interested in calculating the gain of the latch. In the regeneration phase of the comparator, the latch simply acts as a circuit of loop inverters. So for small signal analysis, we can model the latch as an inverter and calculate its gain by applying KCL on the small signal model circuit.

At V_{out} :

$$-V_{out}(g_{ds1}) = V_{out}(g_{ds2} + sC_l) + V_{in}(g_{m1} + g_{m2}) \quad (3.11)$$

$$A = \frac{(V_{out})}{(V_{in})} = -\frac{(g_{m1} + g_{m2})}{(g_{ds1} + g_{ds2} + sC_l)} \quad (3.12)$$

DC gain can be written as:

$$A_0 = \frac{gm1 + gm2}{gds1 + gds2} \quad (3.13)$$

first pole of the latch can be derived as:

$$A = \frac{A_0}{1 + \frac{s}{p_1}} \quad (3.14)$$

By substituting the values from eq 3.12 and eq 3.13 in eq 3.14, we get:

$$p_1 = \frac{(gds1 + gds2)}{Cl} \quad (3.15)$$

3.4 OVER-ALL GAIN

The overall gain of the comparator is the product of gains of all the three stages:

$$A_{total} = A_{pre} \times A_{kickback} \times A_{latch} \quad (3.16)$$

4

DESIGN DETAILS

4.1 PRE-AMPLIFIER

Pre-amplifier design consists of a simple common source differential amplifier. Following the pre-amplifier is a circuit used to create charge imbalance and minimize the kick back effect from the comparator to the input signal.

4.1.1 BIASING TECHNIQUE

The pre-amplifier is combination of two differential pairs of NMOS transistor with PMOS transistors acting as active loads. PMOS are connected in a pseudo logic configuration to make it operate in a linear region. The main objectives for proper biasing are that we achieve a high bandwidth, high cut-off frequency, approximately $V_{CC}/2$ DC biasing at the output, and a DC gain of around 10 dB. According to the following formula of gain:

$$A = \frac{(gm1)}{gds1 + gds3 + sCl} \tag{4.1}$$

which is derived from the small signal model analysis, the current through the circuit was properly adjusted to achieve desired DC gain. The above equation can be further simplified to give the relation between gain and biasing current

$$A = \frac{\left(\sqrt{2\mu \left(\frac{W_1}{L_1} \right) I_d C_{ox}} \right)}{I_d(\lambda_3 + \lambda_1) + sCI} \quad (4.2)$$

$$A \propto \frac{1}{\sqrt{I_d}} \quad (4.3)$$

Keeping the sizes of the transistors optimized allowed the circuit to have less parasitic capacitance which increased its cut-off frequency. Increasing the size of the load PMOS takes the DC biasing close to VCC and increasing the size of NMOS bring the DC level close to ground. Through this sizing strategy of the transistors, the output DC biasing was also set around VCC/2. The purpose of setting the output close to VCC/2 is to make the latch operate properly in its metastable region where maximum gain of the comparator could be achieved.

4.1.2 SIMULATION RESULTS

The final design of the pre-amplifier used in the latched comparator has a DC gain of 16dB, unity gain frequency of 953 MHz and -3dB cut-off frequency of 145 MHz.

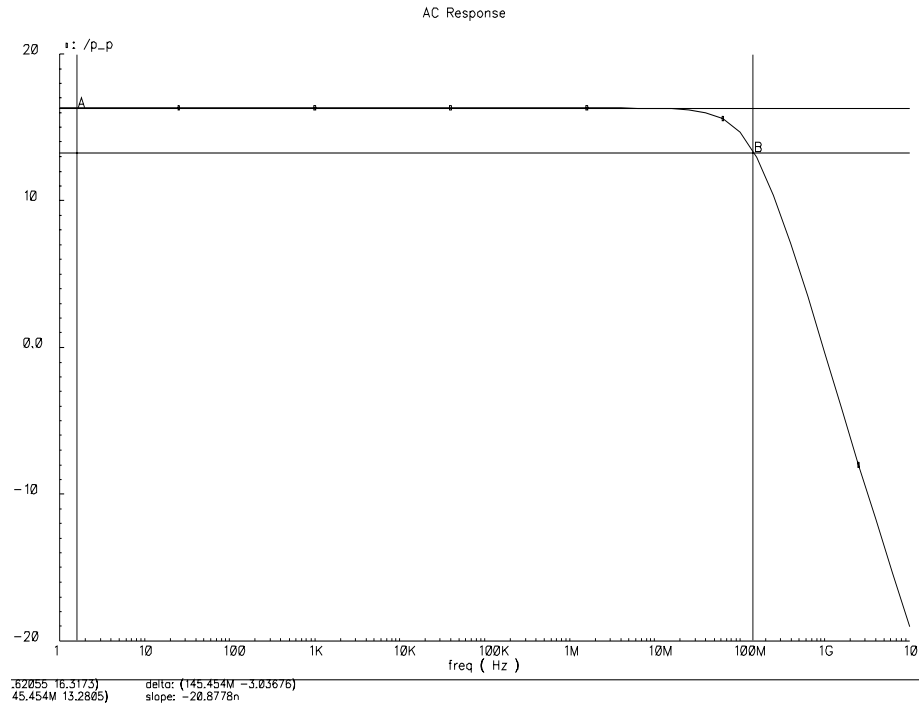


Figure 4.1: Gain and -3dB cutoff frequency for Pre-Amplifier.

4.2 LATCH DESIGN DETAILS

The Latch is the most sensitive part in the comparator design.

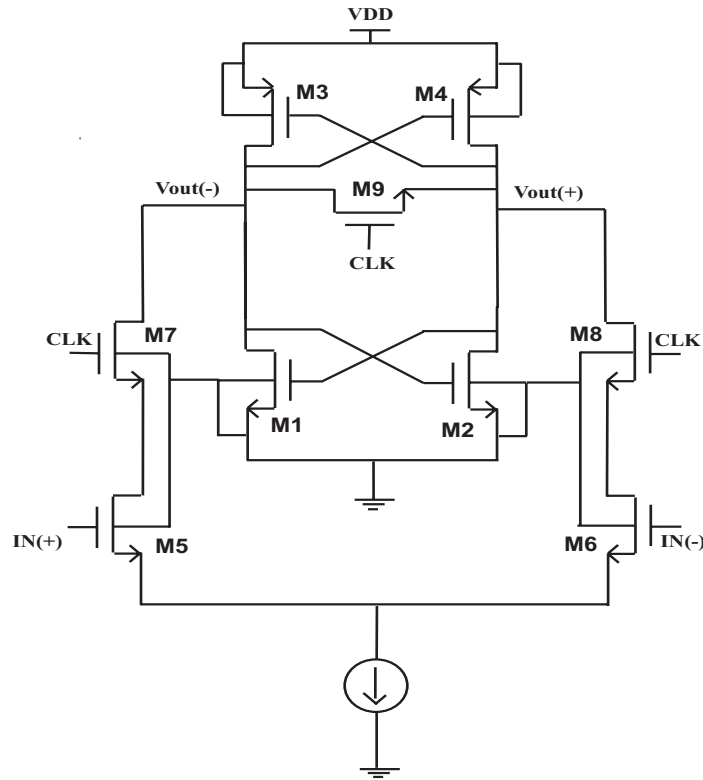


Figure 4.2: Comparator schematic.

4.2.1 COMPARATOR DESIGN AND TRANSISTOR SIZING

Step-1:

The cross coupled inverter pair was first separately designed. Each inverter follows the typical rule of CMOS inverter transistor sizing i.e. the size of PMOS is almost equal to three times size of NMOS. Then the sizes of these transistors were optimized so that the DC biasing is kept a little bit more than the mid point of supply voltage. Also the widths of the transistors were kept minimum size i.e. 0.35 μm to cater for speed as a digital design. The sizes of the transistors were adjusted in a manner that the circuit remains self biased.

Step-2:

Now the inverter pair was connected to the charge imbalance creating circuitry which consist of transistor M5-M8. A switching NMOS transistor M9

is connected between the differential output nodes of the latch. When the extra circuitry is connected to the cross coupled inverter pair, then it pulls down the DC operating point of the latch, that is why initially it was set a bit above mid point to VCC. So, after connecting the rest of the transistor i.e M5-M10, the final DC operating point got around mid of supply voltage. It is necessary to keep this voltage point because during the reset phase the outputs are short-circuited to this voltage level just when entering into the next phase of regeneration, then at this voltage level, the latch has the maximum gain which can be observed from voltage transfer curve of an inverter.

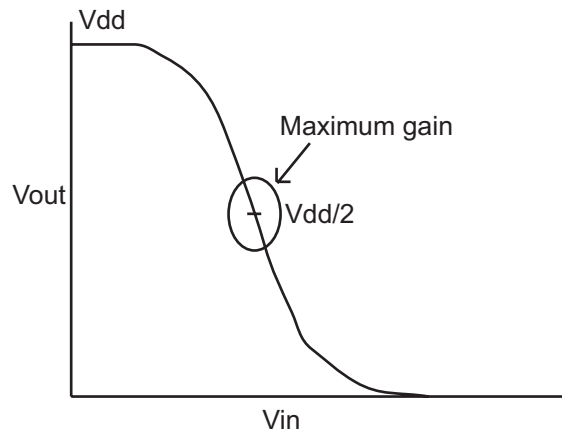


Figure 4.3: Voltage transfer curve for a typical inverter.

4.2.2 TWO PHASE OPERATION

Reset and regeneration are the two phases for one comparison cycle of the comparator. In the reset phase, VCC is applied at the gates of the transistor M9, M7 and M8. M9 short circuits the differential nodes where as M7 and M8 provide a connection of input to the differential nodes of the latch.

1) RESET PHASE:

Reset phase is regarded as the duration when clock is high. In this phase M7 and M8 are switched 'ON', connecting the output of the pre-amplifier to the differential nodes of the latch through transistor M5 and M6 respectively. Also the transistor M9 is switched 'ON' which short circuits the node Vout(-) and Vout(+) to a DC level of 1.65 Volts. The significance of having this reset phase is, first, that the differential nodes are set to a certain DC value which

removes the memory effect in the latch and, secondly, that the charge imbalance is created at the differential nodes of the latch.

2) REGENERATION PHASE:

Regeneration phase starts as soon the clock turns from high to low. In this phase the M7, M8 and M9 turn OFF and then the inverter pair moves the either of the Vout(+) and Vout(-) nodes to VDD or GND depending upon the charge imbalance created due to the difference in the input signal. The speed of voltage transition depends upon the gain of the inverter, biasing current, and sizes of the transistors.

4.2.3 EFFECT OF TRANSISTOR SIZES ON THE PERFORMANCE

1) TRANSISTOR M1-M4:

Transistors M1-M4 constitute the cross-coupled inverter pair structure which forms the main regenerative loop for the latch. Their sizes for length and width are kept minimum for least capacitive effects, and W/L ratio is kept as for an ideal inverter. Sizes are further optimized to set the metastable trip point of the inverter to half of the supply voltage.

2) TRANSISTOR M9:

This switching transistor M9 short circuits the latch's differential nodes to a common DC level. An advantage of increasing its width is that it brings the DC level on both nodes close to each other but on the other hand, increasing the width also increase the charge injection which degrades the sensitivity of the latch, as shown in the following figure 4.4 and figure 4.5.

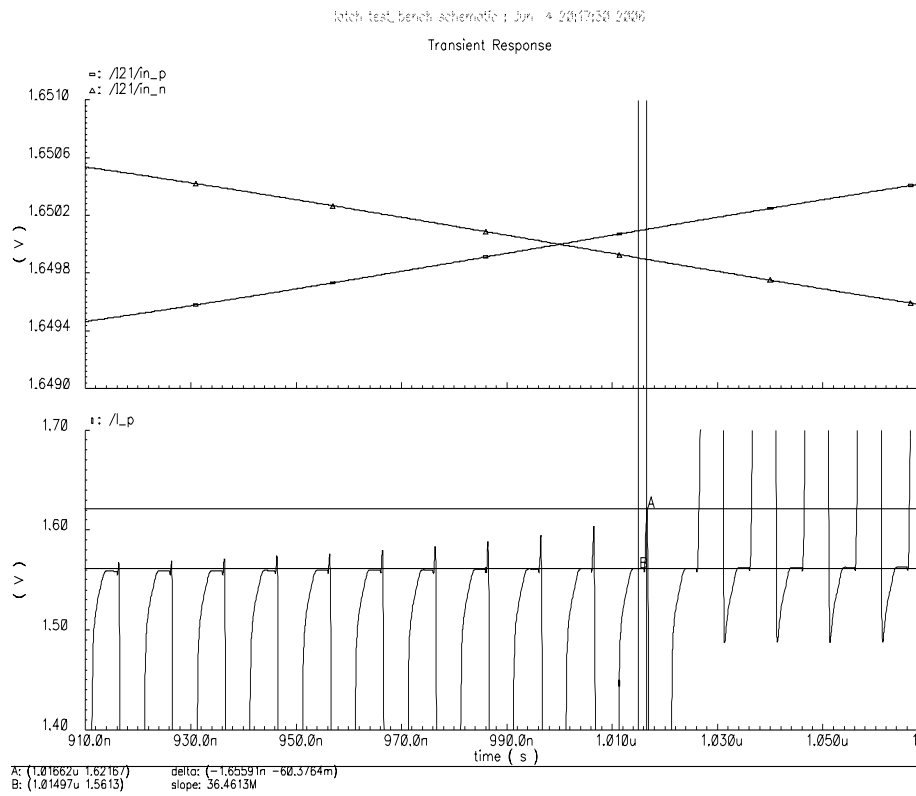


Figure 4.4: Effects of charge injection, width of M9=2.1um.

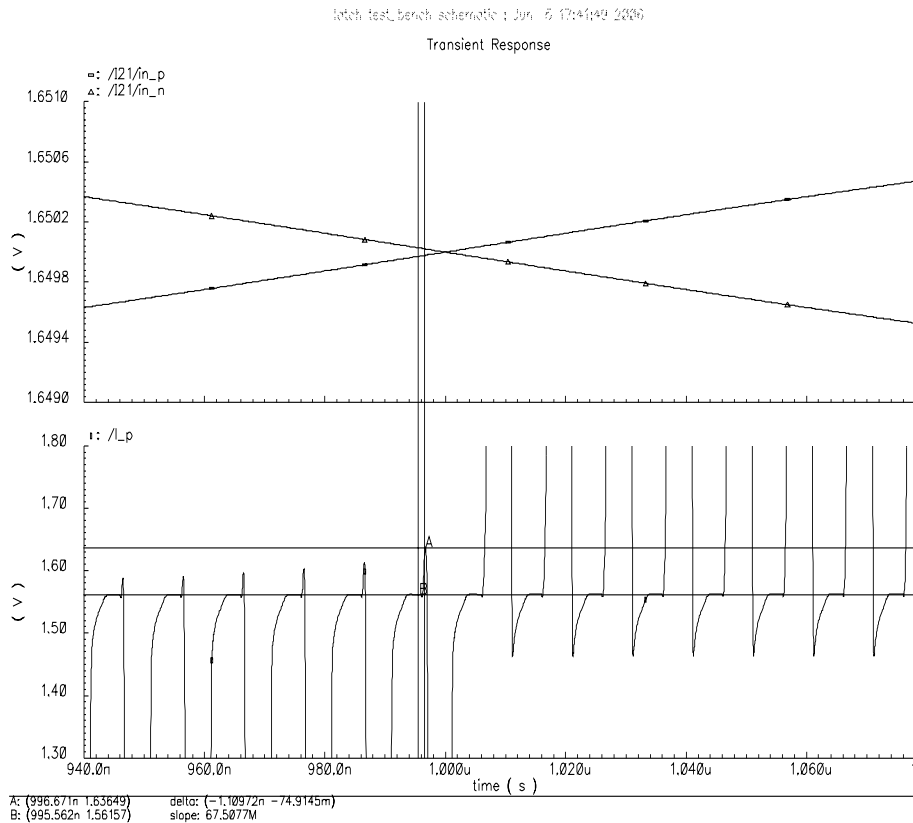


Figure 4.5: Effects of charge injection, width of M9=2.7 μ m.

From the above figures it is clear that charge injection increases by increasing the width of transistor M9, but on the other hand it improves the accuracy of the comparator. So, there exists a trade-off between charge injection and accuracy of the comparator. Ideally the width of M9 should be adjusted to a value where we can achieve minimum charge injection and reasonable accuracy.

3) TRANSISTOR M7 and M8:

These transistors are used to avoid the clock feed through and kickback effects from the latch to the input. Width of these transistors also effects the performance of the latch. If the width is increased, it adds to the equivalent capacitance on the nodes of the latch and increases the effect of clock feed

through on the input; resulting in degradation in sensitivity of the latch. If the width is decreased, then input signal has to be increased otherwise charge imbalance on the latch is not properly created.

4.2.4 GAIN AND BANDWIDTH OF COMPARATOR

The comparator is modelled as an inverter and on the output has been loaded by the capacitance of 2.1fF that is present at the regenerative node of the comparator.

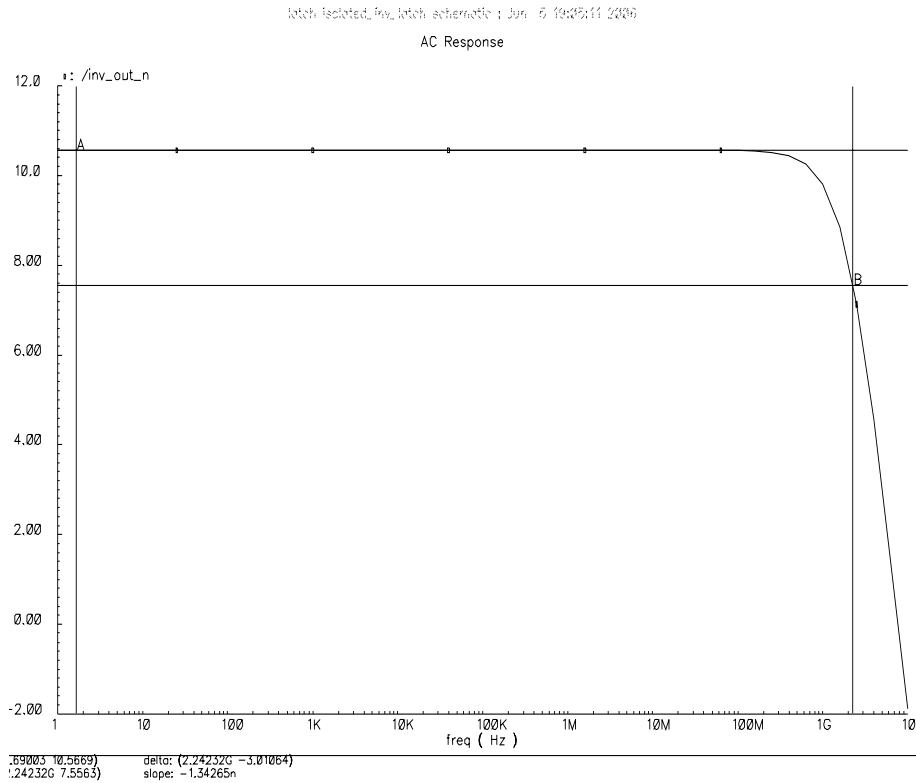


Figure 4.6: Gain and bandwidth of inverter used in the latch.

The input DC biasing for the inverter is kept 1.56 V which is same as the reset voltage on the regenerative nodes of the comparator. From this configuration, the results are obtained as follows: Gain is 11dB, -3db frequency is 2.2GHz, and output resistance is calculated to be 28 KOhms.

5

CONCLUSION

5.1 SENSITIVITY

The current design of the latched comparator is able to respond on the differential voltage difference of around 2uV peak to peak at the input of the circuit. Any value less than 2uV is not detectable by comparator. The maximum sampling frequency observed through simulations is 125 MSps for a 50% duty-cycle of the sampling clock. If the duty-cycle is increased to 70%, the sampling frequency can be increased to 200 MSps, keeping all other parameters the same. This is due to the fact that the latch part of the comparator is very fast and this makes it possible to have a quite short regeneration phase, i.e., a short time for which the clock signal is low. With a duty-cycle larger than 50%, the time for resetting the latch to the mid-point is increased, necessary for increased sampling frequency operation.

It is observed that the inverter used in this thesis work has the maximum gain at the metastable point which is at 1.65V. But in the design, the inverters of the regenerative loops are biased at 1.561V at the reset phase. Although biasing the inverter at 1.561 V gives relatively less gain, the sensitivity of the latch is improved. At 1.65V biasing, the latch's sensitivity is degraded, compared with the current configuration, where the sensitivity is 2uV. Raising the biasing to 1.65V reduces the power consumption and increases the speed but reduces the sensitivity, so therefore there exists a trade-off between power consumption, speed and sensitivity.

5.2 MTF CALCULATION

Since the comparator is intended to be used in sigma-delta modulator loops, memory effects and metastability is of primary interest. The mean time to failure is therefore one of the important design parameter for the latch. Using eq 2.4 and eq 3.16, MTF is calculated to be nearly infinite. This is due to the high bandwidth of the latch.

5.3 DESIGN PARAMETERS AND PERFORMANCE

From the simulation results of the latched comparator, the following design and performance parameters were calculated:

Power consumption	4.58mW
Mean time to failure	Infinite
Maximum Sampling frequency	125MHz @ 50% duty-cycle 200MHz @ 70% duty-cycle
Input sensitivity	2uV (differential)
Pre-amplifier DC gain	16dB
Pre-amplifier unity gain Frequency	953MHz
Pre-amplifier -3dB cutoff Frequency	148MHz
Kickback stage gain	-6.9dB
Latch DC gain	11dB
Latch output resistance	28KOhms
Latch -3dB cutoff Frequency	2.2GHz
Latch unity gain Frequency	7.6GHz
Input DC offset	1.65V

Table 5.1. Performance and design parameters.

5.4 FINAL SIMULATION RESULTS

The following results are obtained when a differential sinusoidal signal and a ramp signal is applied as an input to the latched comparator.

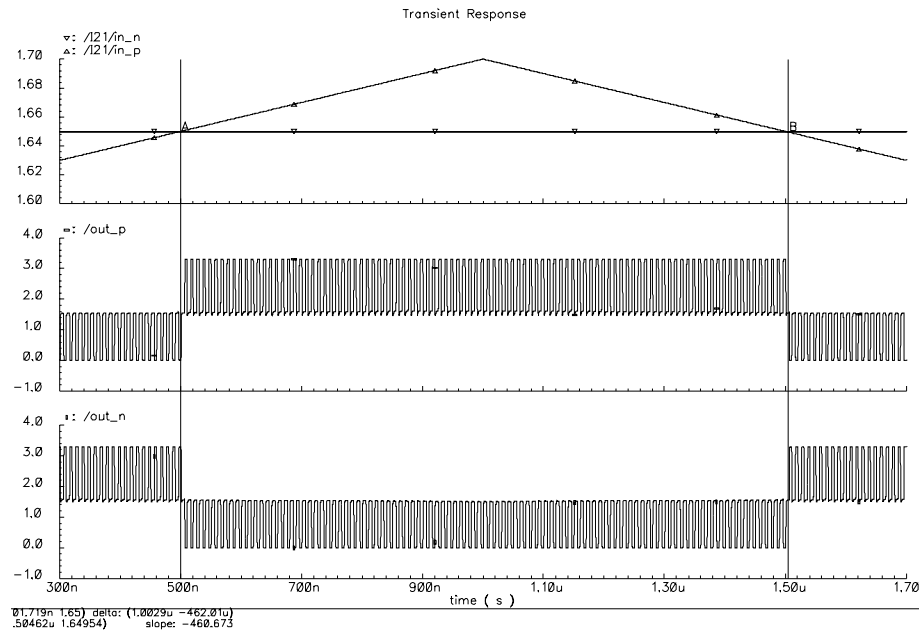


Figure 5.1: Simulation result when ramp signal is applied as input.

In figure 5.1, the two comparator inputs are connected such that one input is a reference signal which is kept constant and other is the ramp. As soon as the ramp magnitude becomes greater than the reference, the output switches to positive side (1.56 V to 3.3 V). The output is sampled by a sampling clock of 100 MHz and during reset phase, the output is set to a DC value of 1.54 V.

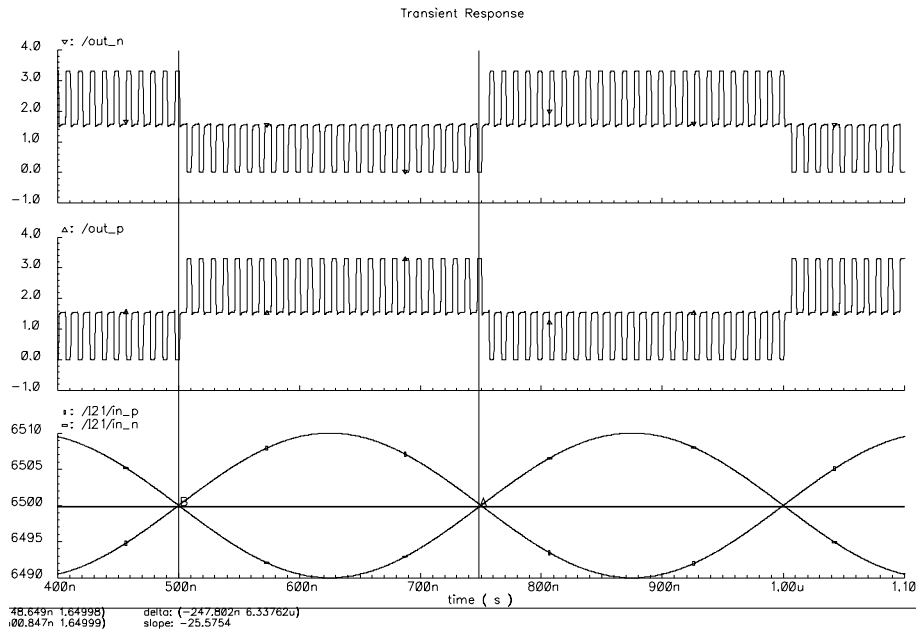


Figure 5.2: Simulation result when sinusoidal signal is applied as input.

In figure 5.2, the input is given as a differential sinusoid signal. The output here also changes its orientation depending upon the input.

5.5 SPEED OF THE DESIGNED COMPARATOR

By analysing the frequency response of the pre-amplifier and the latch, it is evident that the system can be operated at much greater frequencies than 100 MHz. However, currently the speed is limited to sampling frequencies up to 100 MHz. Here the bottle neck for the speed is the kick back protection circuit. As observed from simulation of the circuit, the unity-gain frequency of the preamplifier and the kick back protection circuit together is some 360 MHz which limits the sampling speed of the comparator. Therefore it can be concluded that if this circuit can be modified, then speed of the current architecture of latched comparator can be increased.

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APPENDIX

Latch Design:

The following design parameters were used during circuit implementation of the latched comparator.

Transistors	Size - (Width/Length) um
M1	1.5/0.35
M2	1.5/0.35
M3	4.8/0.35
M4	4.8/0.35
M5	14/1
M6	14/1
M7	0.7/0.7
M8	0.7/0.7
M9	2.7/0.35

A schematic of the comparator is shown in the figure below.

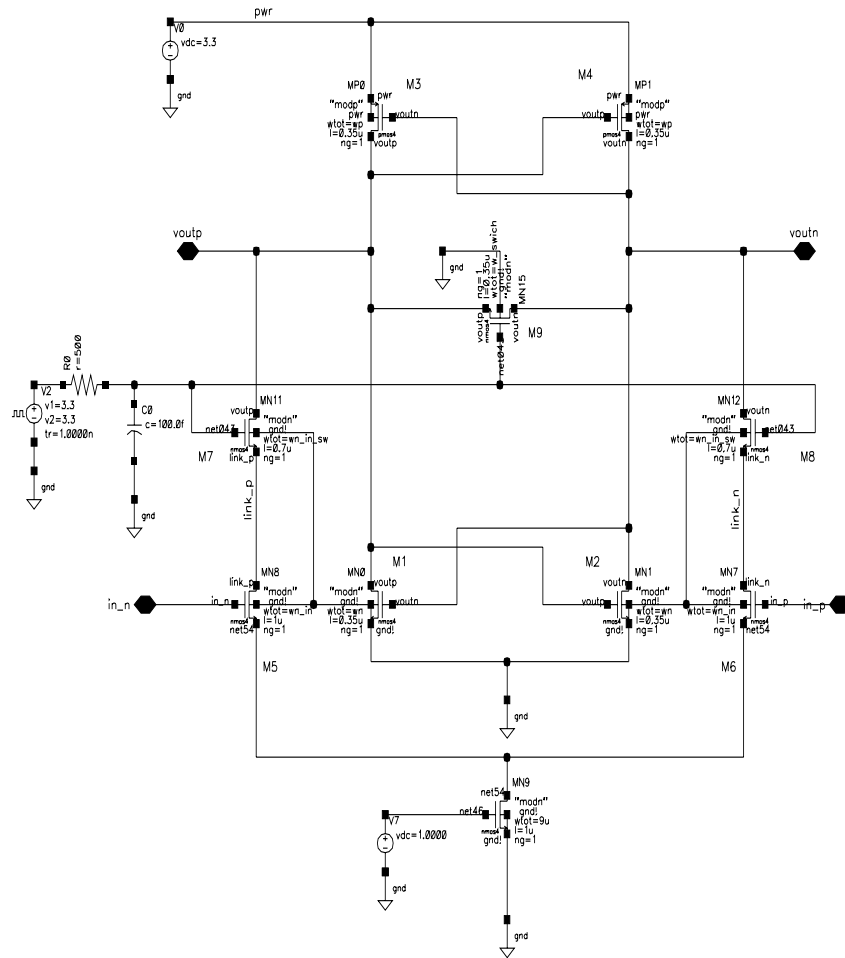


Figure A. Schematic view of the comparator.

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