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Low-Power Multi-GHz Circuit Techniques for On-chip Clocking

Martin Hansson

Linköpings universitet
INSTITUTE OF TECHNOLOGY

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Department of Electrical Engineering
Linköpings universitet, SE-581 83 Linköping, Sweden
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Abstract

The impressive evolution of modern high-performance microprocessors have resulted in chips with over one billion transistors as well as multi-GHz clock frequencies. As the silicon integrated circuit industry moves further into the nanometer regime, three of the main challenges to overcome in order for continuing CMOS technology scaling are; growing standby power dissipation, increasing variations in process parameters, and increasing power dissipation due to growing clock load and circuit complexity. This thesis addresses all three of these future scaling challenges with the overall focus on reducing the total clock-power for low-power, multi-GHz VLSI circuits.

Power-dissipation related to the clock generation and distribution is identified as the dominating contributor of the total active power dissipation. This makes novel power reduction techniques crucial in future VLSI design. This thesis describes a new energy-recovering clocking technique aimed at reducing the total chip clock-power. The proposed technique consumes 2.3x lower clock-power compared to conventional clocking at a clock frequency of 1.56 GHz.

Apart from increasing power dissipation due to leakage also the robustness constraints for circuits are impacted by the increasing leakage. To improve the leakage robustness for sub-90 nm low clock load dynamic flip-flops a novel keeper technique is proposed. The proposed keeper utilizes a scalable and simple leakage compensation technique. During any low frequency operation, the flip-flop is configured as a static flip-flop with increased functional robustness.

In order to compensate the impact of the increasingly large process variations on latches and flip-flops, a reconfigurable keeper technique is presented in this

thesis. In contrast to the traditional design for worst-case process corners, a variable keeper circuit is utilized. The proposed reconfigurable keeper preserves the robustness of storage nodes across the process corners without degrading the overall chip performance.

Preface

This licentiate thesis presents my research during the period June 2003 through December 2005 at the Electronic Devices group, Department of Electrical Engineering, Linköping University, Sweden. The following papers are included in the thesis:

- **Paper 1 - Martin Hansson** and Atila Alvandpour, "A Low Clock Load Conditional Flip-Flop", in *Proceedings of IEEE International System-on-Chip Conference*, pp. 169-170, Santa Clara, California, USA, September 2004.

- **Paper 2 - Martin Hansson**, Atila Alvandpour, Steven K. Hsu, and Ram K. Krishnamurthy, "A Process Variation Tolerant Technique for sub-70 nm Latches and Flip-Flops", in *Proceedings of the 23rd IEEE NORCHIP Conference*, pp. 149-152, Oulu, Finland, November 2005.

- **Paper 3 - Martin Hansson** and Atila Alvandpour, "Power-Performance Analysis of Sinusoidially Clocked Flip-Flops", in *Proceedings of 23rd IEEE NORCHIP Conference,* pp. 153-156, Oulu, Finland, November 2005.

- **Paper 4 - Martin Hansson**, Behzad Mesgarzadeh, and Atila Alvandpour "1.56 GHz On-chip Clocking with 2.3X Clock Power-Saving in 130 nm CMOS", manuscript to be submitted.

My research has also included involvement in projects that has generated the following papers falling outside the scope of this thesis:

- Robert Malmqvist, and **Martin Hansson**, "SiGe BiCMOS LNA's and Tunable Active Filter for Future Wide-Band Multi-Purpose Array Antennas", in *Proceeding of the national conference GigaHertz*, Linköping, Sweden, November, 2003.

- **Martin Hansson**, and Atila Alvandpour, "Crosstalk Analysis Considering Power and Delay on Interconnects", in *Proceedings of the 21st IEEE NORCHIP Conference*, pp. 196-199, Riga, Latvia, November, 2003.

- Peter Caputa, Henrik Fredriksson, **Martin Hansson**, Stefan Andersson, Atila Alvandpour, and Christer Svensson, "An Extended Transition Energy Cost Model for Buses in Deep Submicron Technologies", in *Proceeding of the 14th International Workshop on Power and Timing Modeling, Optimization and Simulation*, pp. 849-858, Santorini, Greece, September, 2004.

- Robert Malmqvist, **Martin Hansson**, Carl Samuelsson, Mattias Alfredson. "Some Important Aspects on the Design of Active Microwave Filters using Standard RF Silicon Process Technologies", in *Proceeding of the 34th European Microwave Conference*, pp. 941-944, Amsterdam, The Netherlands, October, 2004.

Abbreviations

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
FF	Flip-Flop
FO	Fan-Out
IEEE	The Institute of Electrical and Electronics Engineers
ITRS	International Technology Roadmap for Semiconductors
LC	Inductance-Capacitance
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSFF	Master-Slave Flip-Flop
MUX	Multiplexer
NMOS	N-channel Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide-Semiconductor
RC	Resistance-Capacitance
RF	Radio-Frequency

RLC	Resistance- Inductance-Capacitance
SOC	System-on-Chip
SR	Set-Reset
TG	Transmission-Gate
VCO	Voltage-Controlled Oscillator
VLSI	Very-Large Scale Integration

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There are several persons that deserve credit for making it possible for me to write this thesis. I would especially want to thank the following persons:

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Martin Hansson
Linköping, February 2006

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Introduction

Chapter 1

Introduction

1.1 Brief History Outlook on Technology Scaling

During the last five decades the microelectronic industry has evolved tremendously, and the last 10 years of aggressive scaling have moved integrated circuits from the micrometer regime down to nanoscale regime. Transistors are now being manufactured with gate-lengths well below 100 nm. From the late sixtieth the amount of transistors on a single chip has exploded from mere hundreds of devices to over one billion transistors per chip. In 1965 Gordon Moore published his famous paper [1], in which he predicted that the number of components per integrated circuit for minimum cost would increase by two every year. This prediction was updated 10 years later predicting that the number of devices should double every second year from then on, popularly refereed to as Moore's Law [2]. These predictions have since then inspired the microelectronic industry to strive for increased complexity and lower fabrication costs of integrated circuits. Up until now Moore's predictions have turned out to fairly accurately predict the future, which can be illustrated in form of the microprocessor evolution in the last four decades seen in Figure 1.1. From the first Intel microprocessor 4004 to the present Pentium 4 processor sold today the number of transistors has roughly doubled every two years [3] [4]. Without the

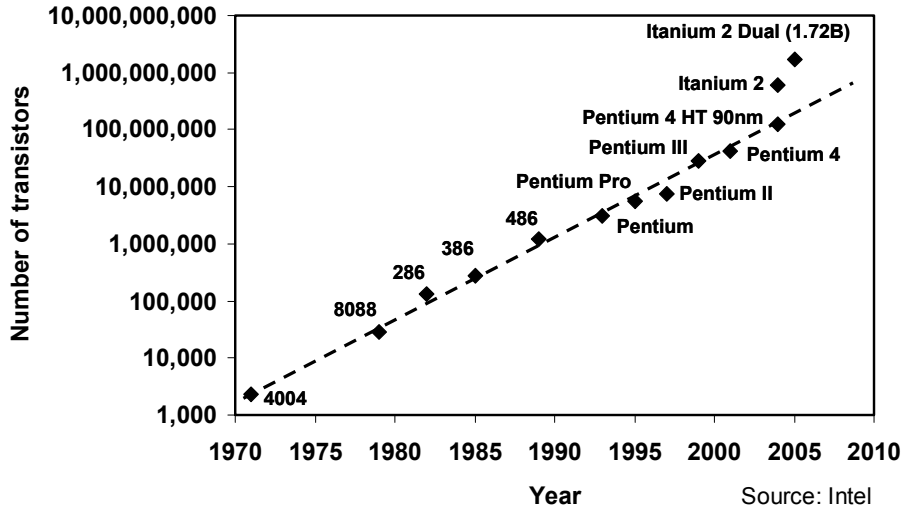

Figure 1.1: 35 years evolution of Intel® microprocessors [3].

incredible progress of integrated circuits high-technology achievements like Internet, portable computer, and mobile phones would never been able to be realized, and the evolution of integrated circuits will certainly continue to increase in importance in the high-technology society [5] [6].

1.2 Motivation and Scope of this Thesis

With roughly two years between every new technology node there seem to be no end for continuing CMOS scaling in the near term [7]. However in order to take advantage of the scaling there are several challenges that need to be addressed. Increasing standby power dissipation, growing parameter variation in CMOS processes, and increasing clock power dissipation all have emerged as potential show-stoppers for continuing progress in VLSI circuit design.

The continuing scaling of gate-oxide thickness and threshold voltages to improve transistor performance leads to a dramatic increase of leakage power dissipation, which contributes to a large portion of the total power dissipation [8]. In order to maintain the total power dissipation at reasonable levels there is an urgent need for novel and clever design techniques to compensate and reduce the leakage currents. Apart from increasing power dissipation due to leakage also the robustness constraints for circuits are impacted by the increasing

leakage, which emphasize the need for leakage tolerant design techniques in future VLSI designs. In **Paper 1** a low clock load conditional transmission-gate flip-flop is presented, aimed at reducing on-chip clock power consumption for high-performance applications. The proposed flip-flop utilizes a scalable and simple leakage compensation technique, which injects additional leakage current in opposite direction to the destructive leakage. Hence the technique compensates the worst-case leakage currents for dynamic flip-flops. During any low frequency operation, the flip-flop is configured as a static flip-flop with increased functional robustness. Chip measurements show a 25 % clock power reduction compared to a conventional static flip-flop.

Due to shrinking geometries of CMOS devices the number of atoms in the transistor channels reduces. Manufacturing imperfections that leads to statistical deviation from the mean number of dopant atoms will cause large process parameter variations, which in turn increase the spread in performance and power dissipation for VLSI designs. Variation tolerant circuit techniques are therefore needed in order to reduce the effect of growing device parameter uncertainties [8]. **Paper 2** describes a sub-70 nm circuit technique that compensates the impact of the increasingly large process variations on latches and flip-flops. In contrast to the traditional design for worst-case process corners, the proposed technique utilizes a variable keeper circuit that preserves the robustness of storage nodes across the process corners without degrading the overall chip performance. Power and delay improvements of 7 % and 12 % respectively have been observed for wide static MUX-latch circuits in a 65 nm CMOS technology. The proposed technique furthermore enables functional flip-flops utilizing weak uninterrupted keepers leading to over 9 % local clock power reduction without performance degradations.

Finally, power dissipation related to the clock generation and clock distribution is identified as one of the dominating contributors to the total active power dissipation. Resent power analysis for a high-performance dual-core microprocessor have showed that the clock distribution accounts for more than 25 % of the total core power [9], and even numbers as high as 70 % have been reported [10]. Hence, low power clocking techniques for on-chip clocking are extremely important in future digital VLSI design. Sequential designs are the basis for almost all digital VLSI systems of today and the number of clocked elements like flip-flops and latches will certainly continue to increase as complexity continues to grow [11]. This will cause the power related to the clock to increase even further.

Energy-recovering clocking techniques using on-chip sinusoidal clock-generators are considered as potential candidates to considerably reduce the total clock power dissipation. However, in order to take advantage of the large clock

power reductions of novel clocking techniques, power-dissipation in flip-flops and latches can not be allowed to increase dramatically. **Paper 3** presents a study on the impact on power and performance of six conventional flip-flops due to sinusoidal clock-signals, generally generated by energy-recovering clock drivers. The results indicate that the dominating effects in the flip-flops are latency and power-dissipation penalties compared to using a conventional clocking technique. This needs to be considered when using an energy-recovering clocking technique.

Finally **Paper 4** describes a successful experiment of a novel 1.56 GHz on-chip LC-tank resonant clock oscillator, which directly distributes and drives 2x896 conventional flip-flops without intermediate buffers. Detailed power measurements of a test-chip in 130 nm CMOS show that the resonant clocking network have 2.3x lower clock power dissipation compared to the conventional clocking at 1.56 GHz, which represented the best power-performance numbers presented to date. The total power reduction is 20 % even though including the power penalty introduced in the flip-flops, further proving the potential of the energy recovering clocking technique.

1.3 Organization of this Thesis

This thesis is organized into three parts:

- Part I - Introduction
- Part II - Low-Power Multi-GHz Clocking
- Part III - Papers

Part I, provides the background for the concepts used in the papers. In Chapter 2 the basic MOS devices and the impact of scaling on power and performance are discussed. An extensive background to leakage power is also given. This is followed by a brief discussion of process variation. Finally clocking and synchronization are treated, which includes clock distribution, latches, and flip-flops.

In Part II, a summary of the discussions and results from the included papers is given. Chapter 3 provides a background of some common low clock load techniques for conventional master-slave flip-flops. A summary of the leakage compensation technique presented in **Paper 1** is also given in Chapter 3 together with a summary of the proposed process variation tolerant circuit techniques presented in **Paper 2**. Chapter 4 provides the background for the resonant clocking technique presented in **Paper 4** together with a summary of results from both **Paper 3** and **Paper 4.**

Finally in Part III the papers, included in this thesis, are presented in full.

1.4 References

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Chapter 2

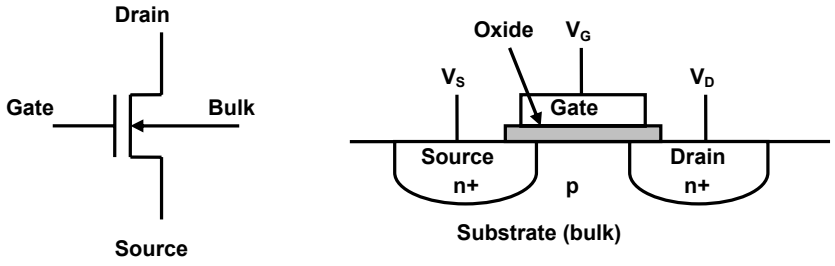
Background

2.1 CMOS Technology

The extraordinary evolution in microelectronics would not have been as impressive if it where not for the invention of MOS devices, and lately CMOS circuits. CMOS devices have grown to become without comparison the most commonly used devices in VLSI circuits and the workhorse of the entire digital electronics industry [1].

2.1.1 The MOSFET Device

Schematic and cross section views of an NMOS transistor are shown in Figure 2.1. An MOSFET is a voltage controlled device with four terminals; drain, source, gate, and bulk. The gate commonly implemented in heavily doped polysilicon is separated from the bulk by a thin gate-oxide. The bulk represents the doped Si-substrate in which the transistors are manufactured. If a positive voltage relative the substrate is asserted on the gate terminal an electric field is created between the gate and the substrate. This will attract electrons to gather in the positively (p) doped region between the negatively (n) doped source and drain. When the applied voltage is larger than a certain threshold voltage (V_{th}) the concentration of electrons is high enough to invert the region between the drain and source. A channel then forms between the drain and source terminals



NMOS schematic symbol NMOS cross section

Figure 2.1: Schematic and cross section views of an NMOS transistor.

[2], thus increasing the conductivity between the source and drain. This property of being able to control the conductivity between two terminals with the gate voltage is what makes the MOS transistors attractive as a switch in digital circuits. The voltage asserted on the fourth terminal, bulk, modulates the performance and parameters of the device. The complementary device to the NMOS transistor is called PMOS. The PMOS transistor is implemented in an n-doped well with p-doped drain/source regions, which gives the complementary functionality compared to the NMOS. Circuits implemented with both types of transistors are referred to as CMOS circuits [1].

2.1.2 Impact of Scaling on Transistor Performance

Silicon technology scaling leads to several positive effects on the performance of the MOS devices. When the device dimensions are reduced the total gate capacitance (C_{gate}) will also scale with the same factor. The intrinsic delay of a MOS transistor is described by equation (2.1), which represents the minimum switching time for an unloaded transistor [1]. The characteristic on-resistance (R_{on}) of a transistor is defined by the power supply divided by the saturation current. Both these properties are scaled with the same ratio, which yields that R_{on} to the first order will remain constant when the technology scales. For every new technology-node dimensions are scaled roughly 30 %. Hence the performance of the transistor will rapidly improve with scaling [1].

$$\tau_{gate} = C_{gate} \cdot R_{on} \tag{2.1}$$

2.1.3 Power Dissipation in CMOS Circuits

Generally the power dissipation of a simple CMOS inverter (seen in Figure 2.2) can be divided in dynamic power and static power [1] [3]. The two main sources

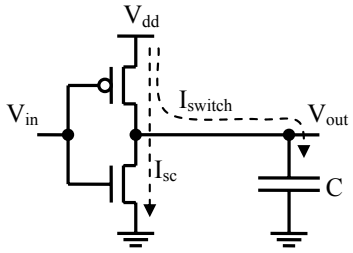


Figure 2.2: Schematic of a basic CMOS inverter, including switching and short-circuit currents.

of dynamic power are switching power and short circuit power, while the static power dissipation emanates from leakage currents in various forms. Leakage will be more extensively covered in section 2.2.

Switching power is described by the relation in (2.2), where C is the load capacitor that is charged, f_{clk} is the clock frequency with which the gate switches, V_{dd} is the power supply, and α is the switching activity ratio, which determines how frequently the output switches per clock-cycle.

$$P_{switch} = \alpha \cdot f_{clk} \cdot C \cdot V_{dd}^2 \tag{2.2}$$

The short-circuit power is due to the direct path between the power supply and ground that forms briefly when both PMOS and NMOS transistors conduct current simultaneously. Equation (2.3) describes the short-circuit power dissipation for a simple CMOS inverter, where β is the gain factor of the transistors, τ is the input rise/fall time, and V_{th} is the threshold voltage of the transistors, which are assumed to be symmetric [4]. The short-circuit power will increase in cases where the input rise/fall times to the gates are large compared to the output rise/fall times. For a well sized static CMOS gate the short-circuit power can be kept below 10 % of the switching component [3].

$$P_{sc} = \frac{\beta}{12}\left(V_{dd} - 2V_{th}\right)^3 \cdot \tau \cdot f_{clk} \tag{2.3}$$

2.2 Leakage and Leakage Power

As shown in Figure 2.3 leakage will be an increasing contributor to the overall power dissipation in the future [5] [6] [7]. There are several leakage mechanisms that contribute to the total leakage for CMOS circuits both in active mode and in steady-state. Figure 2.4 shows the three main leakage mechanism that are

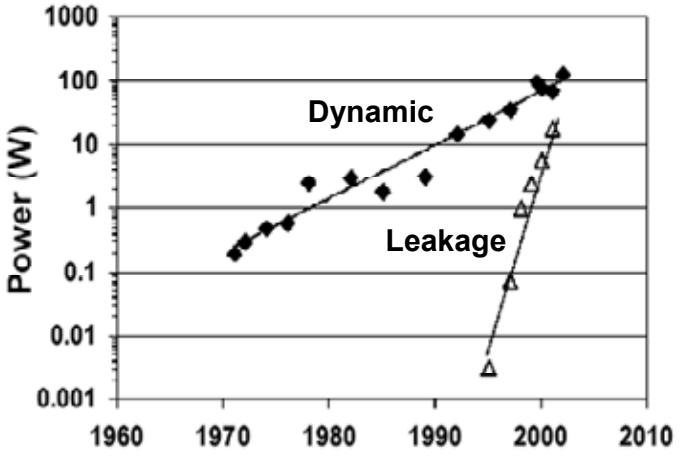


Figure 2.3: Dynamic versus leakage power for microprocessors [5].

present in a MOS transistor under normal operating conditions. These are subthreshold leakage (I_{sub}), gate leakage (I_{gso}, I_{gc}, I_{gb}, I_{gdo}), and reversed junction leakage (I_{junc}) [6].

2.2.1 Junction Leakage

Junction leakage emanates from the reverse-biased diode that is formed by the drain and source well junctions. There are mainly two contributors to the reversed bias pn-junction leakage; (1) minority carrier diffusion and drift near the depletion region edge; (2) electron-hole pair generation in the depletion region of the reversed pn-junction. The resulting leakage current from both of

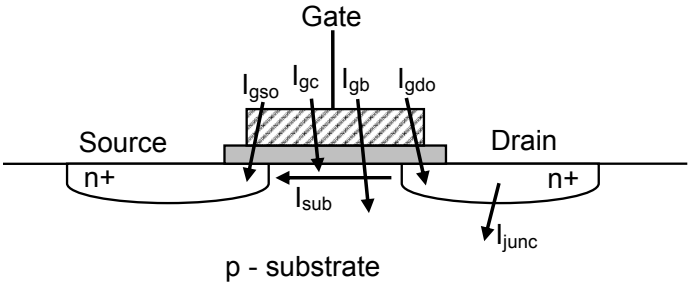


Figure 2.4: Main leakage components for a MOS transistor.

these effects depends on the junction area and the doping concentration of the diffusion regions [6].

An additional junction leakage effect called band-to-band tunneling can occur if both the n and p regions in the MOS device are heavily doped. If the reverse-biased junction is asserted a high electric field electrons are able to tunnel from the valence band in the p-region to the conduction band in the n-region. In order for this tunneling to take place the voltage drop over the junction need to be larger then the band-gap [7].

2.2.2 Subthreshold Leakage

Subthreshold leakage or weak inversion conduction is the region of operation where the gate-source voltage of the transistor is below the threshold voltage. The current transport between the source and drain terminals of the MOS transistor is due to diffusion of carriers along the surface instead of due to drift as in the active region, which yields an exponential relation to the gate voltage similar to that of a bipolar device [6].

For short-channel devices when the drain and source are close to each other, the voltage on the drain terminal will cause the drain depletion region to interact with the source depletion region. This causes the effective source potential barrier to decrease, which reduces the threshold voltage. This effect is called drain induced barrier lowering (DIBL) and leads to further increase in subthreshold current [6] [7].

If the bulk-to-source junction is reversed biased the depletion region in the bulk region of the transistor widens. This will increase the threshold voltage and this effect is called body-effect. Hence one way to reduce the subthreshold leakage is to alter the body-bias voltage for the transistors [6].

VLSI circuits usually operate at elevated temperatures due to the heat generated by the large power dissipation. Figure 2.5 shows how the sub-threshold leakage current (I_{subth}) increases with increased temperature. This greatly impacts leakage power dissipation and robustness of VLSI designs during operation.

Weak inversion conduction of a MOS transistor can be modeled as:

$$I_{subth} = \mu_0 C'_{ox} \frac{W}{L_{eff}} (v_T)^2 e^{1.8} \cdot e^{1/mv_T(V_G - V_S - V_{th0} - \gamma V_S + \eta V_D)} \left(1 - e^{-v_{DS}/v_T}\right) \qquad (2.4)$$

where V_{th0} is the zero bias threshold voltage, v_T is the thermal voltage, and m is the subthreshold swing coefficient. The body effect is modeled with γV_S, and the DIBL effect is modeled with the parameter η [6].

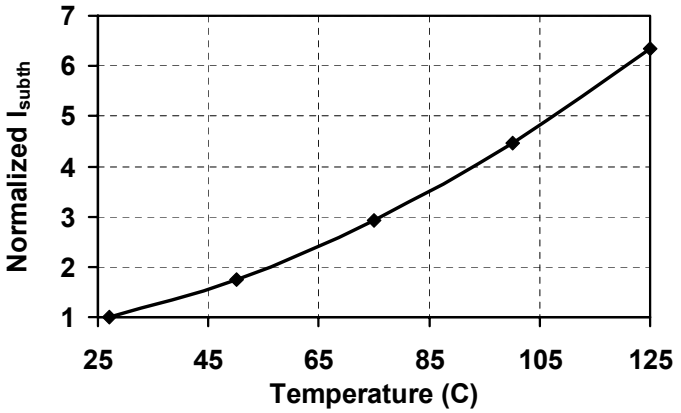


Figure 2.5: I_{subth} versus temperature for a 130 nm CMOS process.

2.2.3 Gate-Tunneling Leakage

When the physical gate-oxide thickness is reduced the field strength between the gate and the substrate increases. Electrons or holes in the substrate are then able to directly tunnel through the gate-oxide. This direct tunneling can be modeled with the following current density expression:

$$J_{DT} = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 exp\left(-B\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{\frac{2}{3}}\right)\Big/\frac{V_{ox}}{T_{ox}}\right) \tag{2.5}$$

where V_{ox} is the voltage over the gate-oxide, T_{ox} is the gate-oxide thickness, and ϕ_{ox} is the barrier height for the tunneling particle. A and B are physical parameters where A is proportional to $1/\phi_{ox}$ and B is proportional to $1/\phi_{ox}^{3/2}$ [8] [9] [10].

The gate tunneling current is composed by several components, which will contribute more or less to the total gate leakage current depending on the operation mode of the transistor. I_{gso} and I_{gdo} are tunneling currents from the gate to the drain/source overlap regions, while I_{gb} is the gate-to-substrate leakage current and I_{gc} is gate leakage to the channel [8] [9] [10]. For an NMOS transistor in the on-state the gate-to-channel leakage will be dominated by electrons tunneling from the conduction band in the inversion layer through the gate-oxide to the gate. Electrons accumulated in the overlap regions also tunnels from the conduction band in the accumulation region to the gate. For the PMOS transistor in on-state the gate-to-channel leakage and drain/source-gate overlap

leakage are instead due to holes tunneling from the valence band in the channel and accumulation regions to the gate [8] [9] [10]. The mechanism behind gate-to-substrate tunneling for both PMOS and NMOS is electron tunneling from the conduction band during accumulation, and electron tunneling from the valence band during depletion and inversion [8] [10]. The gate leakage currents associated with PMOS transistors are considerably smaller than for the NMOS due to the larger barrier height that the holes in the valence band experience when tunneling to the gate [8] [10].

From equation (2.5) it is clear that the gate leakage currents are greatly impacted of the physical gate-oxide thickness. To combat the gate leakage while still obtaining lower effective oxide-capacitance, oxides manufactured with high-k materials would be needed. High-k materials make it possible to manufacture physically thicker oxide layers, while improving the electrical properties of the gate-oxide. Intel announced 2003 that they plan to introduce high-k materials by the introduction of their 45 nm technology node [11].

2.3 Process Variation

Process variations are deviations from the intended circuit or device parameters. Integrated circuits will be impacted by two different types of variations. Environmental variations occur during operation of the circuit, changing the device parameters due to temperature, power supply, and activity differences across the chip. Physical variations are stochastic deviations that impact the circuit and device parameters during the manufacturing of chips. This could be among other things, difference in channel lengths and width, gate-oxide thickness, and channel doping concentration [12] [13].

From a circuit designer point of view changes in electrical parameters for transistors and interconnects, due to physical or environmental variations are important. Statistical variations in process parameters such as channel length and width, gate-oxide thickness, and threshold voltage greatly impact the device properties. Among all transistor parameters, threshold voltage constitutes an extremely important parameter both for the driving strength of the transistors (i.e. delay) and the ability to turn off properly (i.e. leakage currents). The variation in threshold voltage can lead to 20x die-to-die variations of leakage currents while the spread in performance leads to 30 % spread of clock frequency for a microprocessor [13], which is illustrated in Figure 2.6. The threshold voltage variation arises from several sources, where random dopant fluctuations in the channel, is one of the most important. This effect increases with scaling due to the shrinking number of dopant atoms in the channel [14].

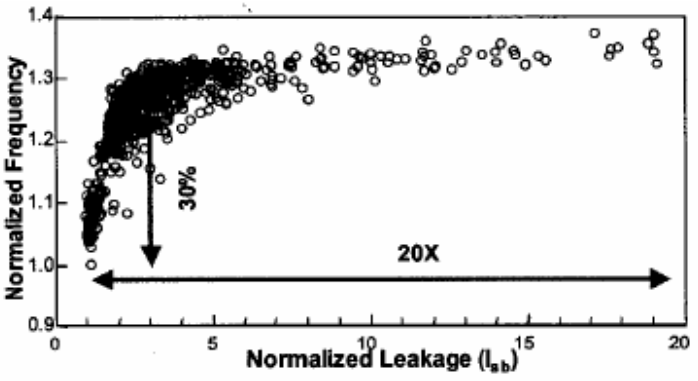


Figure 2.6: Leakage and frequency variation for a microprocessor [13].

This therefore increases the need for variation tolerant techniques to mitigate the effects of the large process uncertainties.

In order to model die-to-die variations the process foundries provide designers with a set of parameters that covers the larger part of the variation spread. The statistical distribution of the process parameter variations can with high accuracy be approximated with a Gaussian distribution [13] [14], as shown in Figure 2.7 for the threshold voltage. The mean process values are usually refereed to as typical values and represent the average parameter value for the given device. Deviation from the mean value which results in increase of performance is refereed to as fast, and vice versa for slow. In order to cover the worst-case spread the fast and slow corners are referred to as a shift of all parameters from

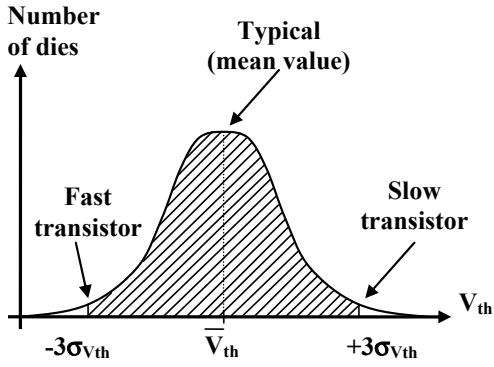


Figure 2.7: Statistical distribution of threshold voltage variation.

the mean values corresponding to ±3 times the standard deviation (σ). This results in more than 99 % coverage of the die-to-die process parameter spread. Combinations of fast NMOS transistors and slow PMOS transistors and vice versa are also provided to analyze circuits for worst-case NMOS-PMOS matching variations [1] [12].

2.4 Clock Distributions and Timing Circuits

Most high-performance digital designs of today utilize a synchronous clock to order events [1]. Although the principle of synchronization is easy in the system design perspective, ordering events on a complete chip in a synchronous fashion comes with a price because the generation and distribution of clock signals are extremely challenging to design. Moreover, latches and flip-flops form the timing elements that synchronize the data flow in a VLSI circuit. Hence, flip-flops and latches are among the most important circuit blocks in a digital synchronous chip design. Ideally timing circuits like flip-flops and latches should add as little latency as possible and have low power dissipation. In practice however, timing elements can actually consume a substantial fraction of the clock-cycle period, and also consume a considerable portion of the energy consumption. Therefore it is of highest interest to design power-efficient flip-flops and latches that are optimized for their desired task.

2.4.1 Timing Issues for Global Clocks

Clock signals have several stringent requirements such as rise and fall times, skew, jitter, and symmetry, which all need to be fulfilled in order to reach desired performance. Figure 2.8 shows the definitions of clock skew and jitter. Clock-skew is variations between clock signals distributed to different parts of a chip, which ideally should be identical. Jitter on the other hand is temporal variations of the clock-signal referred to a reference edge, which changes the phase of the clock signal from cycle to cycle [15] [16]. As can be seen in Figure

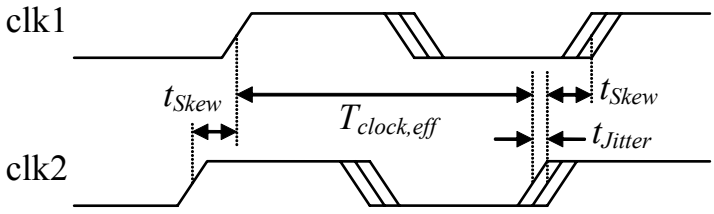


Figure 2.8: Definition of skew and jitter for a clock signal.

2.8 both skew and jitter limits the effective clock cycle period available for logic computation, hence limiting the performance of the entire system.

2.4.2 Clock Distribution Techniques

One conventional way to realize a low skew global clock distribution network is to implement a balanced RC-tree network. The main idea is to distribute the global clock to a central point of the chip and from there branch the clock signal to a number of paths each realized with equal delay. The skew between each leaf node should therefore be minimized. One such tree structure suitable for regular designs, is the H-tree shown in Figure 2.9a [1] [16].

Another common type of clock distribution network is the grid-based structure, shown in Figure 2.9b. This type of network is frequently utilized for the local distribution to the final clock loads. The grid network makes the clock signal easily accessible in the chip, which increases the flexibility in the layout and allows for late floor-plan changes. The principle for the clock-grid network is not to achieve low skew, but rather to minimize the worst-case latency. This sets a maximum allowable grid size in order to not exceed a given clock-skew target. An additional drawback with the grid-based distribution is the excess load that the grid gives. This requires larger drivers, hence leading to additional power dissipation [1] [16].

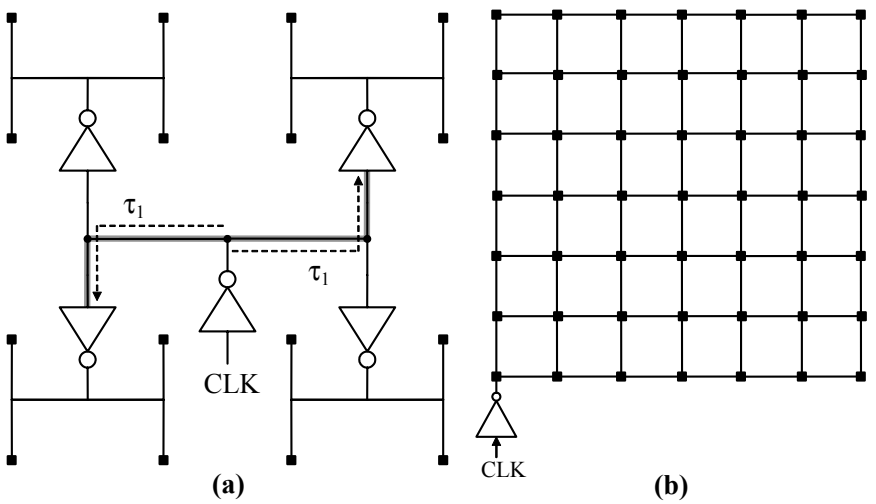


Figure 2.9: Example of (a) a RC-balanced 16-leaf H-tree clock-network and (b) a grid-based clock network.

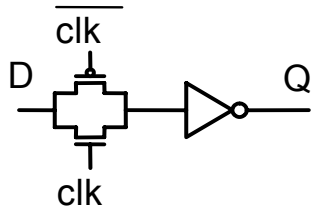


Figure 2.10: Schematic of a level-sensitive latch.

2.4.3 Level-Sensitive Latches

Latches form the simplest kind of synchronizing circuit in a sequential digital system. A latch is a level sensitive device that is either transparent or opaque depending on the signal level of the clock input. A simple schematic of a transmission-gate latch is shown in Figure 2.10. When the clock signal (*clk*) is high the latch lets the input (*D*) pass to the output (*Q*), while if the clock is low the output (*Q*) will hold the previous input data.

A level sensitive latch that is transparent for a high clock signal samples the data on the falling clock-edge [1] [17]. That is, data on the input is sampled and stored at the latch output during the low clock-phase. The timing definitions for a level-sensitive latch are shown in Figure 2.11. Setup time (t_s) is defined as the time that the input (*D*) needs to be stable before the sampling clock-edge in order to capture the correct data. The hold-time (t_h) is defined as the minimum time that the input (*D*) needs to be stable after the sampling clock-edge in order for the latch to have time to capture the correct data [17]. The delay from the data-edge to the output in relation to the sampling clock-edge is defined as data-to-output delay ($t_{d,DQ}$). A change of data during the low clock-phase will not

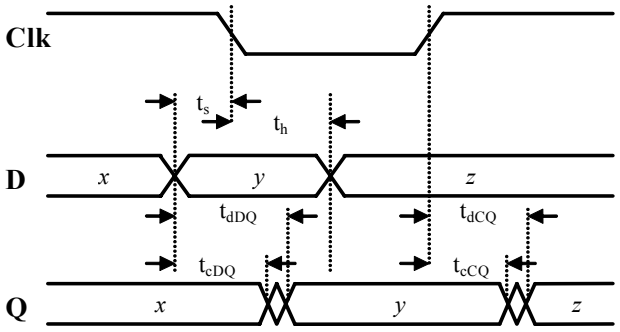


Figure 2.11: Timing definitions for a level-sensitive latch.

show up on the output until a certain delay after the rising clock-edge. This delay is defined as the clock-to-output delay ($t_{d,CQ}$). Hence the level-sensitive latch has two different delays being referenced to two different clock-edges [17].

2.4.4 Edge-Triggered Flip-Flops

A flip-flop is an edge-triggered device that samples an input data on one edge of the clock and then keeps the sampled data on the output during the entire clock period. A simple master-slave flip-flop can be constructed from two cascaded level-sensitive latches as shown in Figure 2.12.

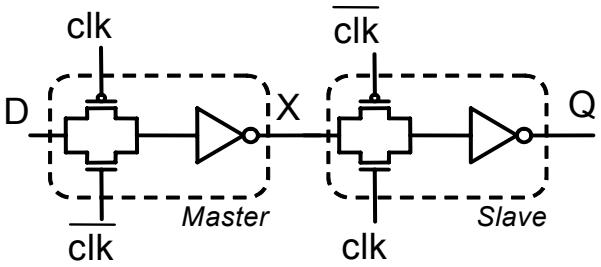


Figure 2.12: Schematic of an edge-triggered flip-flop.

When the clock signal (*clk*) is low the first stage, called master-latch, is transparent and the input is transferred to the intermediate node (*X*). The second transmission gate is opaque so the output (*Q*) is held at its previous state. When the clock signal (*clk*) makes a low-to-high transition the first transmission gate becomes opaque and the second stage, called the slave-latch, becomes transparent and the intermediate data at (*X*) is transferred to the output (*Q*) where it is held for the remainder of the clock period [1] [17].

A timing diagram of a positive edge-triggered flip-flop is shown in Figure 2.13 [17]. All timing relation for the edge-triggered flip-flop is referenced only to the sampling clock-edge (rising edge in Figure 2.13). The timing relations for an edge-triggered flip-flop are defined by essentially five different delays, which are [1]:

- Setup-time (t_s) – the time that the input (*D*) must be stable before the sampling clock-edge in order for the flip-flop to capture the correct data.
- Hold-time (t_h) – the time that the input (*D*) must be stable after the sampling clock-edge in order for the flip-flop to capture the correct data.

- Contamination delay ($t_{c,CQ}$) – the minimum delay from the active clock-edge to the output (Q) of the flip-flop.
- Propagation delay or clock-to-output delay ($t_{d,CQ}$) – the maximum allowable delay from the active clock-edge to the output (Q) of the flip-flop.
- Data-to-output delay or total delay ($t_{d,DQ}$) – The sum of the setup-time and the propagation delay. Represents the total latency of the flip-flop.

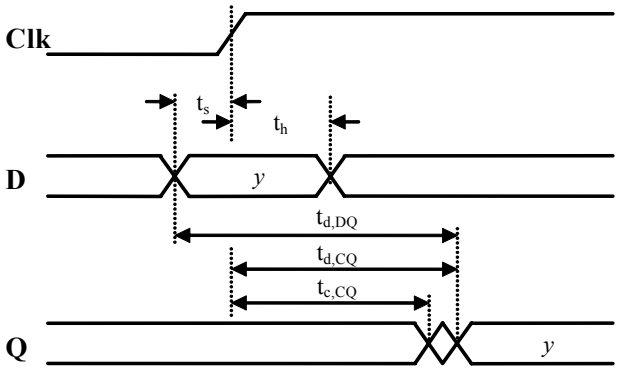


Figure 2.13: Timing definitions for a positively edge-triggered flip-flop.

2.4.5 Obtaining Timing-Metrics for Flip-Flops

The delays for a flip-flop are highly dependent on the arrival of the incoming data. A method to extract the delays for a given flip-flop is shown in Figure 2.14. The figure shows the delay plotted versus the data-to-clock delay ($T_{D\text{-}C}$), which is the time difference between a change of data and the latching clock-edge. When data changes early the clock-to-output delay ($T_{C\text{-}Q}$) will be at the minimum value defined as the contamination delay and denoted by $t_{c,CQ}$. As the data-edge is pushed closer to the latching clock-edge the clock-to-output delay will start to increase monotonically. For a pipeline path the total delay from a data change on the input of a flip-flop the previous cycle to a valid data on the output of the flip-flop the next cycle will be according to equation (2.6). This is the dashed plot in Figure 2.14 ($T_{D\text{-}Q}$). At a certain data-to-clock delay the data-to-output delay ($T_{D\text{-}Q}$) will have an optimum, which is denoted $t_{d,DQ}$. It is obvious from Figure 2.14 that if the data changes later than that optimum point, the total delay will increase dramatically until the flip-flop fails to capture the data. The data-to-clock delay that gives the minimum data-to-output delay is defined as

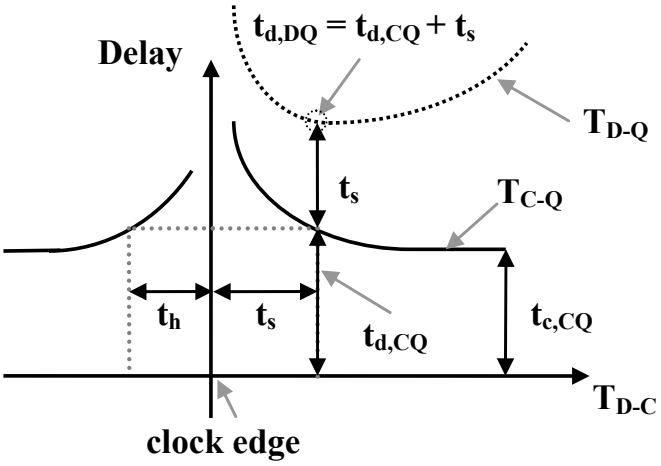


Figure 2.14: Delay metrics for flip-flops.

the setup-time t_s. The clock-to-output delay or propagation delay, $t_{d,CQ}$, is defined for the setup-time according to Figure 2.14. Equation (2.7) defines the optimal data-to-output delay, which is the total minimum latency for the flip-flop from a data change on the input to a corresponding change of the output [18] [19].

$$T_{D-Q} = T_{D-C} + T_{C-Q} \tag{2.6}$$

$$t_{d,DQ} = min\left(T_{D-Q}\right) = t_s + t_{d,CQ} \tag{2.7}$$

The negative side of the x-axis in Figure 2.14 corresponds to the case where data changes after the latching clock-edge. If the data changes long after the latching edge, the output delay would correspond to the contamination delay. However, if data changes close after the latching edge, the output delay will increase monotonically. There is a certain point on the negative T_{D-C} axis where the output delay equals the maximum clock-to-output delay $t_{d,CQ}$. The negative value of the data-to-clock delay at this point is defined as the hold-time t_h as shown in Figure 2.14.

$$t_{Race} = t_{c,CQ} - t_h > t_{skew} \tag{2.8}$$

When cascading two similar flip-flops the output of the first flip-flop is input driver of the second one. The first flip-flop can change output value as early as $t_{c,CQ}$ after the clock-edge, while the second flip-flop needs to have the input

stable as long as t_h in order to capture the correct data. If $t_{c,CQ}$ is shorter than t_h the second flip-flop can fail to capture the data correctly. This is called internal race violation, and to assure that this does not occur, the timing metric in equation (2.8) need to be fulfilled [19]. If there are combinatorial gates in between the two flip-flops the race-margin in (2.8) will include the logic gate delay, which results in that the race margin becomes $t_{c,CQ} - t_h + t_{logic} > t_{skew}$. Hence, for a flip-flop that experience internal race violation some amount of logic in-between the flip-flops can reduce this problem.

2.4.6 Power-Delay Design Space

When optimizing flip-flop circuits, trade-offs between power and delay can be made as for all logic design. A power-efficient flip-flop is one that for a certain delay has the minimal power dissipation and vice versa. This is most easily illustrated in a design-space graph shown in Figure 2.15, which shows the total power for two flip-flops plotted versus the total minimum latency ($t_{d,DQ}$). If a fair and accurate comparisons between different flip-flops topologies are to be made a power-delay plot like Figure 2.15 is needed. As an example comparing flip-flop FF-1 with FF-2 only at one point will yield that one of the topologies is better then the other. However, the truth might be that they are the better choice in different parts of the design space. A low-latency flip-flop that consumes more power (FF-1 at τ_1) could be used in critical parts of a design, while using a slower less power-consuming flip-flop (FF-2 at τ_2) in non-critical parts.

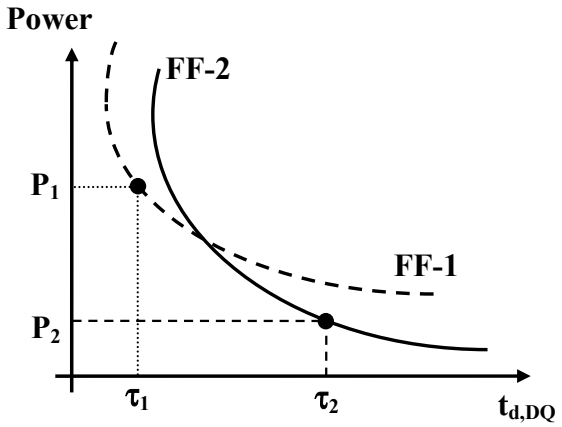


Figure 2.15: Power-delay design space for two different flip-flop topologies.

2.4.7 Robustness Concerns

When latches are transparent the noise robustness is equivalent to that of combinatorial gates in the same circuit topology. However, when a latch is opaque its state should be stored, which sets additional noise constrains on the latch. Noise in a latch or flip-flop can be categorized into five types; input noise, particle and radiation disturbances, crosstalk, power supply noise, and leakage [17] [20].

Input noise arises when the flip-flops are driven from a distant driver, which exposes the latch input connection to noise sources such as crosstalk. This type of noise is usually limited by making sure that the latch input is gate-isolated.

Particles or radiation hitting a storage node in a latch creates electron-hole pairs, which can cause voltage drop on the storage node. For a dynamically held node this drop will reduce the remaining noise margin. A latch with a regenerative feedback (keeper) will also experience a voltage drop, which if the drop is large enough will flip the state of the latch. However, provided that the drop is less than the trip-point of the subsequent gate, latches with regenerative keepers will return to its steady-state value after a certain time. This is not the case for an uncompensated dynamic latch. Increasing immunity against particle generated errors can be accomplished by making sure that enough charge-storage capacitance is used [20].

Capacitive crosstalk from unrelated signals also generates voltage disturbances on the storage nodes. The noise discussion for crosstalk noise can be treated similar to particle disturbances. To limit the effect of crosstalk noise careful layout that exposes the storage nodes with minimal amount of capacitive coupling is required [20].

Power supply noise emanates from the fast-switching of clock signals, which generates current pulses in the power supply network. Dynamically held nodes can not track the power supply variations, which can cause subsequent gates to switch output state even though not intended. Hence power supply noise reduces the noise margin for dynamic latches. In order to mitigate the effect of power supply ripple a feedback keeper with enough strength is needed to make the storage node track the power supply sufficiently [1] [20] [21].

Leakage noise due to subthreshold, gate, and junction leakage exposes the storage node to erroneous charging or discharging. An uncompensated dynamic latch has no way to compensate the storage node of any lost charge. Thus the dynamic storage node has a finite survival time during which it can keep a stored value before the data is lost. An uncompensated latch therefore requires sufficient refreshing to re-supply lost charge on the storage node.

Apart from the noise sources described above also process variation and temperature will impact the robustness of flip-flops and latches as discussed in previous sections.

2.5 Common Flip-Flop Topologies

In the literature there are a large number of flip-flop circuits proposed, which mainly can be classified into three categories. These are master-slave latch pairs, pulsed latches, and sense-amplifier based flip-flops [1].

2.5.1 Master-Slave Latch-Pairs

The most common approach to build an edge-triggered flip-flop is to combine two latches that are clocked on opposite clock phases. An example of a static master-slave flip-flop is shown in Figure 2.16. The advantages with this flip-flop are the simplicity and the excellent race-immunity [18]. However, because the setup time of the flip-flop is determined by the propagation delay of the master-latch and the output latency is determined by the propagation delay through the slave-latch, the total flip-flop latency will be quite large. Moreover, the hard-edge property of a master-slave flip-flop renders any time-borrowing between clock-phases impossible and increases the clock-skew sensitivity [15] [22]. Therefore, this flip-flop is frequently used in non-critical data-paths where the larger latency and clock-skew sensitivity is not impacting the performance of the system.

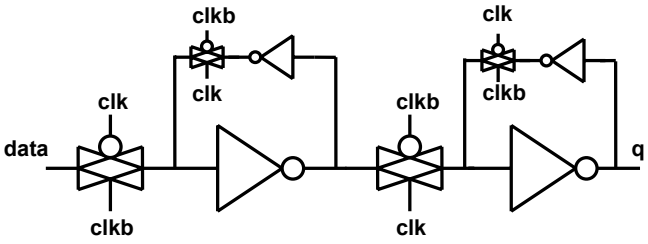


Figure 2.16: Conventional master-slave transmission-gate flip-flop.

An alternative master-slave topology, which only requires a single clock-phase, is the true-single phase clock (TSPC) flip-flop [23]. An implementation example of a dynamic TSPC flip-flop is shown in Figure 2.17. This TSPC flip-flop implementation is triggered on the positive clock-edge. It utilizes a negative TSPC-latch (clocked on PMOS) as the master-latch, which drives a clocked dynamic inverter. Finally the slave-latch comprises a positive TSPC-latch

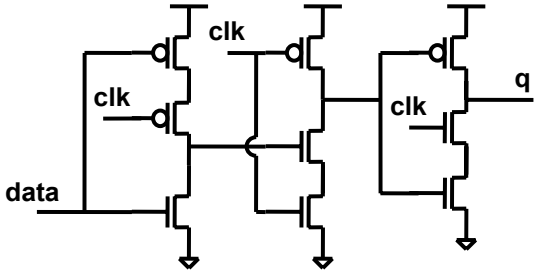


Figure 2.17: True-single phase clock (TSPC) flip-flop [23].

clocked on the NMOS. Due to the single clock the flip-flop is less sensitive to local clock skew and the dynamic implementation leads to fast switching and low clock load. However, apart from the dynamic implementation the TSPC edge-triggered flip-flop is dependent on a sufficiently steep clock signals in order to limit the transparency time for the flip-flop (i.e. hold-time) [23].

2.5.2 Pulsed-Latches

To counteract the hard-edge property of master-slave edge-triggered flip-flops several pulsed-latch approaches have been presented. The principle of a pulsed latch is to create a short pulse on the latching edge of the clock. The pulse is then used to clock a latch, hence obtaining an edge-triggering behavior. The pulse generator could be an external circuit or integrated in the latch design [1]. A simple example of a pulsed-latch using a clocked-CMOS latch is shown in Figure 2.18. The external clock generator could be shared with a number of other latches in order to reduce the total clock load. For a rising edge of the clock (*CLK*) the output of the pulse-generator (*CLKp*) will go high, making the

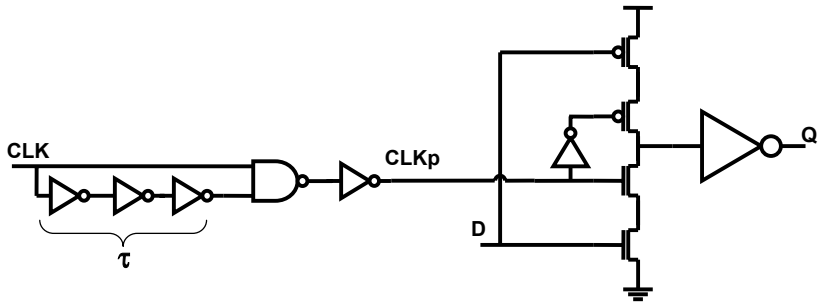


Figure 2.18: Pulsed C^2MOS latch with external pulse-generator.

latch transparent. After a delay (τ) the output of the pulse-generator will go low, thus making the latch opaque. During the high pulse the latch transfers any change of data on the input. This property is referred to as negative setup-time, because data will be correctly latched even though arriving after the rising edge of the main clock signal. This property can be utilized to borrow time from the next clock-cycle. Moreover, the soft-edge can also be used to trade-off time-borrowing for clock skew absorption [22]. The soft-edge property exists at the expense of hold-time, because during the duration of the latching pulse the input can not be allowed to change data erroneously in order not to corrupt the output. Hence, pulsed flip-flops with negative setup time usually have large positive hold-time requirement, which limits the internal race-robustness. However, several pulsed-latches have been described in the literature and some of them are utilized as low-latency flip-flops in critical pipeline stages in high-performance microprocessors where the logic-depth mitigates the reduced internal race-margin. Some of the most popular topologies are the pulsed hybrid-latch flip-flop (HLFF), and the semi-dynamic pulsed-latch flip-flop (SDFF), presented in [24] and [25], respectively.

2.5.3 Sense-Amplifier Based Flip-Flops

A third technique to implement an edge-triggered flip-flop is to utilize a sense-amplifier to sample the data [1] [26]. A typical sense-amplifier based flip-flop is shown in Figure 2.19 [27], where a pre-charged front-end is used to sample the

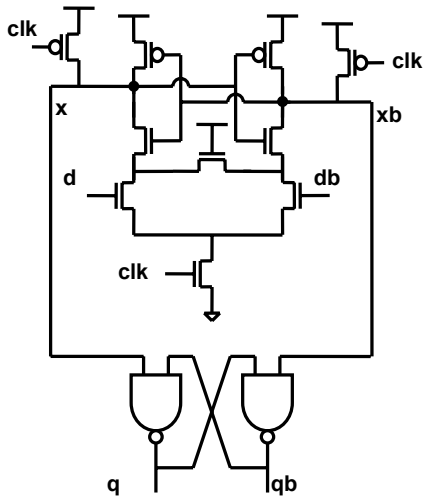


Figure 2.19: Example of a sense-amplifier based flip-flop.

complementary data inputs when the clock makes a rising transition. An SR-latch captures the sampled data and holds it until next rising clock-edge. Due to the amplification provided by the feedback in the cross coupled inverters, the flip-flop can sample input signals with small amplitude difference. Sense-amplifier flip-flops could therefore be utilized as synchronous level-converters between different power-supply regions [28]. Another advantage with the sense-amplifier flip-flop is the low number of clocked transistors, which gives low clock load. Moreover, the flip-flop in Figure 2.19 can at most do one transition per clock-cycle, making it attractive as interface between static and pre-charged dynamic CMOS circuits. One of the largest drawbacks with the sense-amplifier flip-flops is the pre-charged behavior of the sample-stage, which is power-consuming especially when the data activity for the inputs is low.

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Part II

Low-Power Multi-GHz Clocking

Chapter 3

Low-Power Timing Circuits

Timing circuit like flip-flops and latches form the basis in all synchronous digital VLSI designs and the frequent use of sequential circuits for pipelining in high-performance designs tend to increase the number of timing elements implemented per chip. The clock load of each individual flip-flop and latch will add up to form the final clock load connected to the global clock distribution. As the number of flip-flops increases so will the global clock load. Hence, in order to reduce the clock load for the global distribution one way is to minimize contribution of each individual flip-flop.

This chapter treats a number of circuit techniques that can be utilized to reduce the clock load for conventional master-slave flip-flops with the focus on advantages and disadvantages when it comes to power, performance, and robustness. Moreover, a low clock load flip-flop is proposed, which utilizes a leakage compensation technique to increase leakage robustness. Finally a reconfigurable keeper technique is presented, which increases the design flexibility, thus reducing the power-performance spread for static flip-flops and latches due to increasing process parameter variations.

3.1 Low Clock load Master-Slave Flip-Flops

Static master-slave flip-flops like the one discussed in section 2.5.1 utilize interrupted feedback keepers in order to assure static functionality during the opaque phase of the latches. The interruption of the feedback keepers are usually implemented with additional clocked transistors, which results in relatively high clock load. Given the fact that these types of flip-flops are common in digital VLSI designs, it is reasonable to assume that a large portion of the total clock power is due to the excess clocked transistors in the keepers.

3.1.1 Uninterrupted Weak Keepers

One common technique to reduce the clock load for static master-slave flip-flops is to remove the interruption [1] transistors in the feedback keeper as shown in Figure 3.1. This static keeper technique is commonly refereed to as ratioed or weak-keeper. The keeper is directly connected to the storage node of each latch. During a state change the previous value on the output of each latch will drive the keeper to the opposite supply compared to the input, hence the driver of the latch have to fight with the keeper in order to change the state. This contention will, during the switching event, lead to a direct path from power supply to ground, between keeper and input driver as shown in Figure 3.1. This short-circuit current increases the power dissipation and increases the delay of the flip-flop. Hence, it is essential to minimize the size of the keeper in order to reduce the power dissipation and the delay. However, there is a minimum keeper strength that is set by the robustness conditions. Therefore sizing the keepers will be a careful trade-off between power-performance on one hand and static robustness on the other. Nevertheless, for non-critical data-paths where the data activity is low, a weak-keeper flip-flop is a feasible alternative in order to reduce the clock load of the entire chip.

Other weak keeper techniques have been proposed, which limits the

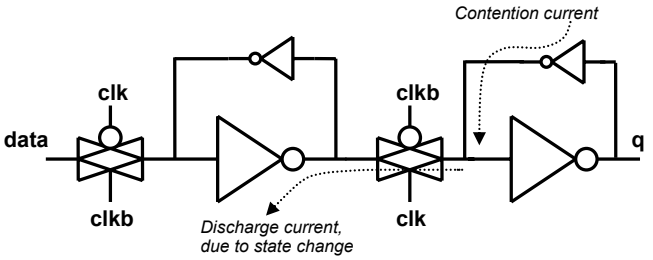

Figure 3.1: Master-slave TGFF with uninterrupted weak keeper.

contention currents of the uninterrupted keepers, such as diode connected transistors used as voltage regulators [2], shown in Figure 3.2a. A diode connected transistors will be off until the voltage difference across the transistors increases above the threshold voltage. Once the storage node has been discharged to $V_{dd} - V_{th}$ by the input driver the contention through the diode connected keeper transistor will increase again. Hence, a voltage regulation diode connected keeper transistor will reduce the strength of the contention, but can not limit it entirely.

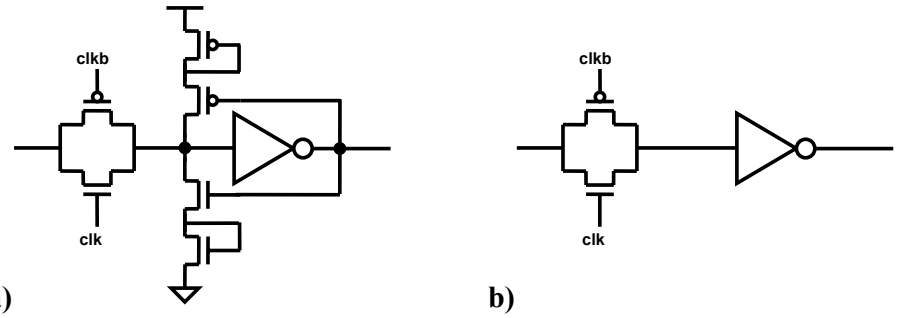

Figure 3.2: a) TG-latch with diode-connected voltage regulating keeper, b) Dynamic uncompensated TG-latch.

3.1.2 Uncompensated Dynamic Latches and Flip-Flops

An intuitive solution in order to reduce the high clock load of interrupted keepers and remove the increased power dissipation for uninterrupted keepers, is to use uncompensated dynamic latches as shown in Figure 3.2a. Apart from lower clock load, dynamic flip-flops and latches have low implementation complexity compared to their static counterparts. Moreover, because no additional load is connected to the storage nodes the state changes will be fast, and there is no risk of contention to occur.

The memory in a dynamic latch relies solely on charge storage on the capacitance in the storage node. This means that the dynamic flip-flops are sensitive to noise of all sorts and the storage time will be limited, which was described in section 2.4.7. An uncompensated dynamic latch must therefore be periodically refreshed, which could limit the usability for completely uncompensated dynamic flip-flops and latches [1]. However, flip-flops and latches are essentially used for temporary memory cells in registers and pipeline paths, which are usually clocked with a continuous clock-signal. This will reduce the storage time requirements considerably. Especially for high-

performance custom-designed data-paths clocked at multi-GHz clock frequencies. Moreover, clock frequencies for high-performance microprocessors have increased by roughly 2x every new microprocessor generation [3], which has increased the refresh rate of the dynamic flip-flops.

3.2 Proposed Leakage Compensating Keeper

With subthreshold currents increasing 5x for every new technology generation [3] obtaining a correct functionality for uncompensated dynamic latched will be hard for sub-90 nm technologies, even at very high clock frequencies. Hence, it will become extremely difficult to take advantage of the great benefits of dynamic flip-flops like low clock load and no contention currents in the future without new keeper techniques. A keeper that compensates for the leakage in a dynamic latch while imposing minimal contention with the input driver is proposed in **Paper 1**. The proposed leakage compensation keeper improves the leakage tolerance, therefore increasing the usability for low-power dynamic latches in sub-90 nm technologies.

3.2.1 Principle of Operation

Figure 3.3 shows a latch implemented with the proposed leakage compensation keeper. The gate terminals of the keeper transistors (M_{n1} and M_{p1}) are connected to the power-supply. The keeper is therefore in off-mode and the storage node is

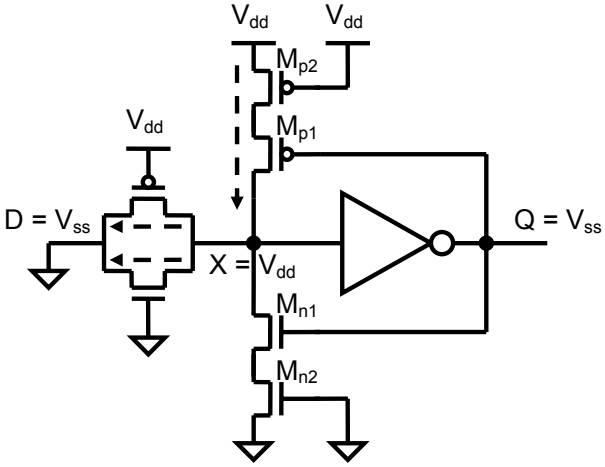

Figure 3.3: Transmission gate latch with leakage compensation keeper at worst-case leakage condition.

thereby exposed with minimal contention current during the switching of states. Furthermore the keeper adds no additional transistors to the clock, hence reducing the total clock load compared to a flip-flop with interrupted keepers.

Assuming that a voltage of V_{dd} is stored at node X, the worst-case leakage condition is when the input is asserted a low voltage (V_{ss}). The subthreshold leakage currents through the transmission gate transistors are then maximized due to DIBL effect according to equation (3.1) [4]. The output of the inverter is also low (V_{ss}), which turns transistor M_{p1} on and transistor M_{n1} off. Both M_{p1} and M_{n1} are realized with minimum size transistors to minimize the load on the storage node. The subthreshold leakage through the transmission-gate and additional leakage such as gate leakage will start to discharge node X. When the

$$I_{subth} \propto W \cdot e^{1/mv_T(V_G+\eta V_D)} \tag{3.1}$$

$$Sizing\ Ratio = \frac{W_{Mp2}}{W_{M,TGn} + W_{M,TGp}} \tag{3.2}$$

voltage on X decreases the drain-source voltage of transistor M_{p2} will increase causing the subthreshold current through M_{p2} to increase. This leakage current will compensate the leakage due to the transmission gates. The subthreshold leakage current is linearly proportional to the transistor width according to equation (3.1). The magnitude of the compensation current can thereby be

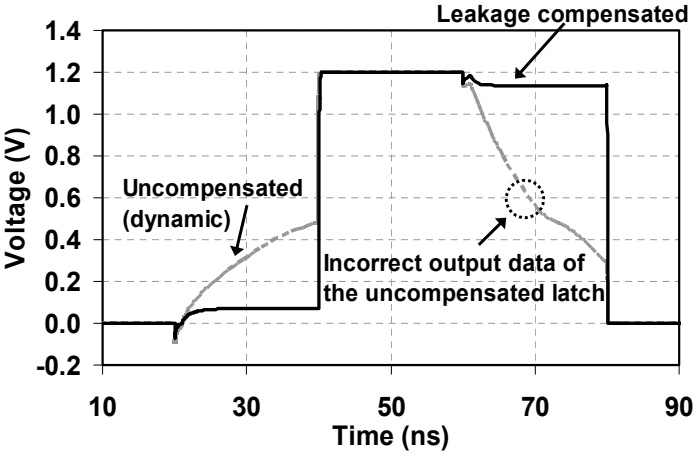

Figure 3.4: Storage node voltage an uncompensated dynamic latch and a leakage compensated latch (f_{clk} = 16 MHz).

adjusted by sizing the transistor M_{p2}, which will have minor impact the contention of the latch. A sizing ratio for the PMOS keeper transistor is defined according to equation (3.2). For a certain sizing ratio the compensation leakage will compensate the leakage currents through the transmission gate (destructive leakage) eventually leading to a steady-state voltage on the storage node. Provided that this steady-state voltage is larger than the trip point of the output inverter the latch will be held stable even though subject to leakage. In Figure 3.4 the steady-state for the storage node X is displayed, compared to an uncompensated transmission-gate based latch. The case where the storage node is holding a low (V_{ss}) voltage can be described analog to the high case.

3.2.2 Improving Low-Frequency Robustness

In order to reduce the clock-power for digital synchronous chips, different clock-gating approaches are extensively utilized. The principle is to turn off the clock for blocks that are idle [5]. Synchronous memory elements should by definition hold their states even when the clock is gated. Moreover, the reliability of digital designs are usually verified and tested under extreme conditions, so called burn-in tests. Elevated temperature and power-supplies are used to accelerate the time to failure due to manufacturing defects. During the test the functionality of the chips are controlled and should be maintained, even at the usually low clock frequencies used [6].

Both described scenarios above of course sets extreme noise robustness constrains on uncompensated dynamic latches and flip-flops in sub-90 nm. A flip-flop or latch implemented with the leakage compensation technique proposed in **Paper 1** is when it comes to conventional DC-noise robustness metrics still dynamic and must be treated as such. Due to this fact a low-frequency operation like during testing or clock gating will eventually lead to that the flip-flop or latch will lose its stored data without sufficient refreshing due to other noise sources apart from leakage. To counteract this, a conditional leakage compensation keeper is proposed. An implementation of a MSFF utilizing the proposed reconfigurable keeper is shown in Figure 3.5. With the control signal asserted to *'low'* the flip-flop is configured in dynamic mode with a leakage compensation keeper as discussed in the previous section. Raising the control signal to *'high'* reconfigures the keeper into static mode, which works with the weak keeper principle described in section 3.1.1. Hence, the keepers can be activated providing a static feedback to the storage nodes during burn-in tests or during any clock-gating.

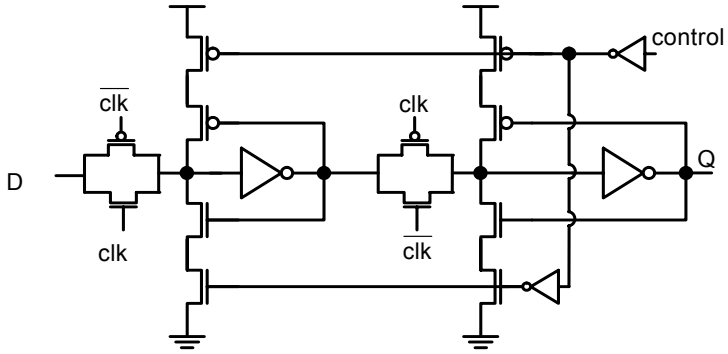

Figure 3.5: Proposed TGFF with conditional leakage compensation keeper.

3.2.3 Summary of Simulation and Measurement Results

To verify the proposed leakage compensation technique a robustness measure is needed. One can define a minimum allowable clock frequency for a dynamic latch as the clock frequency where the output has degraded 10 % from the correct value. Based on this definition a power-delay optimized flip-flop is analyzed for maximum allowable clock-period. A plot showing the leakage compensation technique simulated with 130 nm process data is shown in Figure 3.6. The results indicate that the leakage robustness can be improved considerably. The curve refereed to as *Fast N/P* is the worst-case leakage corner

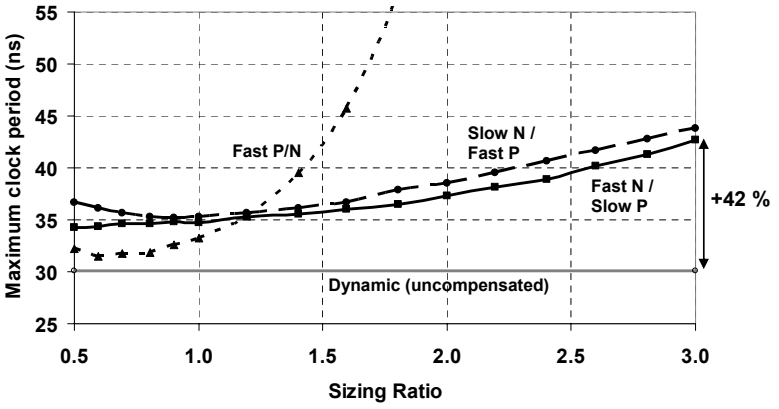

Figure 3.6: Maximal clock period for a leakage compensated flip-flop compared to an uncompensated dynamic flip-flop.

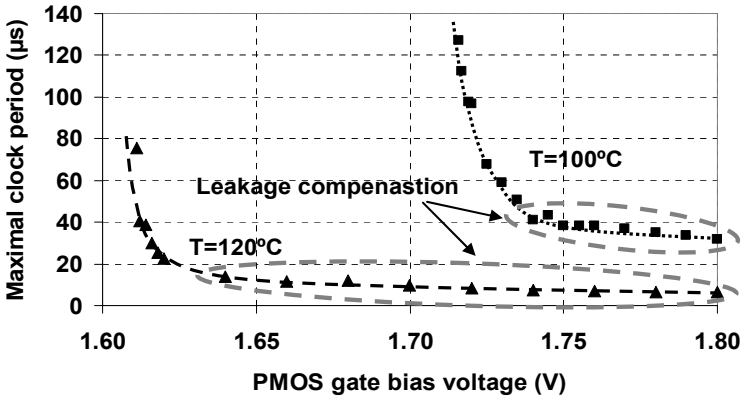

Figure 3.7: Measured impact of leakage compensation in a 180 nm CMOS process.

for both NMOS and PMOS transistors, which shows that a 4x increase in sizing ratio increases the leakage robustness more than 2x. The proposed technique utilizes either a NMOS or a PMOS transistor to compensate for leakage in both NMOS and PMOS transistors, which makes it matching sensitive. The plotted curves in Figure 3.6 refereed to as *Fast N/Slow P* represents the worst-case matching condition. Even at this worst-case condition the proposed leakage compensation technique improves the leakage robustness by 42 % for a sizing-ratio increase of 6x. Power-performance analysis of flip-flops using the proposed keeper technique is presented in **Paper 1**, which shows that even with a constant sizing ratio of 2, delay and power are reduced compared to a static flip-flop using both interrupted and uninterrupted keepers.

To further verify the leakage compensation technique chip measurements on a 180 nm CMOS process [7] were conducted. Identifying the impact of the gate voltage of the subthreshold conduction relation in (3.1), it is clear that changing the gate bias of the keeper transistors will increase the compensating current. This can be utilized to a first order emulate the proposed sizing method. Figure 3.7 shows measurement of maximum allowable clock-period for the case latches should hold a high value on the storage node.

Because an uninterrupted keeper is utilized the clock load compared to a static transmission gate flip-flop with interrupted keeper will be reduced, thus leading to a global clock load reduction. For equal edge-rates of the clock signal a high-performance system using the leakage compensation keeper will require smaller clock drivers, hence will consume less clock power. To verify this global effect

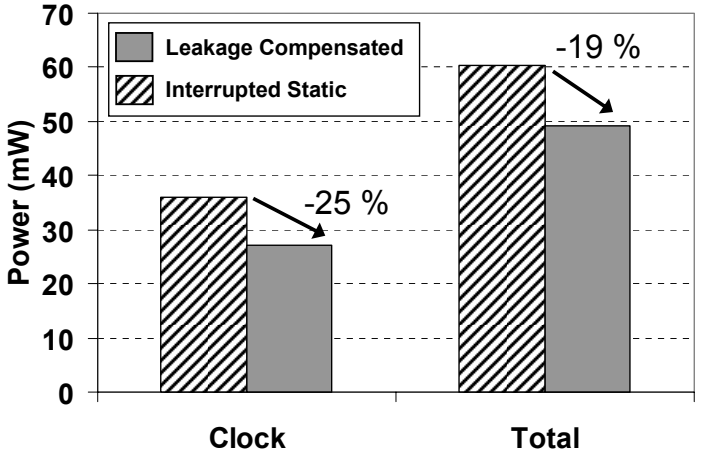

Figure 3.8: Measured chip-power for a pipelined adder structure (180 nm CMOS, F_{clk} = 830 MHz, V_{dd} = 1.86 V).

the test chip includes a pipelined 32-bit ripple-carry adder used as a test vehicle for the proposed keeper technique incorporating over 160 flip-flops. The measurements at a clock frequency of 830 MHz is shown in Figure 3.8, displaying a chip clock power reduction of 25 % and a total power reduction with PRBS data of 19 %, compared to an identical circuit using flip-flops with interrupted keepers.

3.3 Process Variation Tolerant Techniques

3.3.1 Impact on Timing Circuits

The increasing process parameter variation will impact all power and performance metrics as well as the robustness for flip-flops and latches. In order to guarantee robustness constraints for the majority of the fabricated dies, circuits need to be designed for worst case leakage conditions. At fast process corners parameters like threshold voltages are considerably lower than at the typical corner leading to increased subthreshold leakage. Figure 6.1 shows the distribution of NMOS leakage current in a 150 nm CMOS process at 110 ºC [8] [9]. The figure shows a wide range of leakage variations across the process corners. However, the majority of the dies are still located in the relatively lower leakage side of the distribution curve. Hence, a dominating portion of the

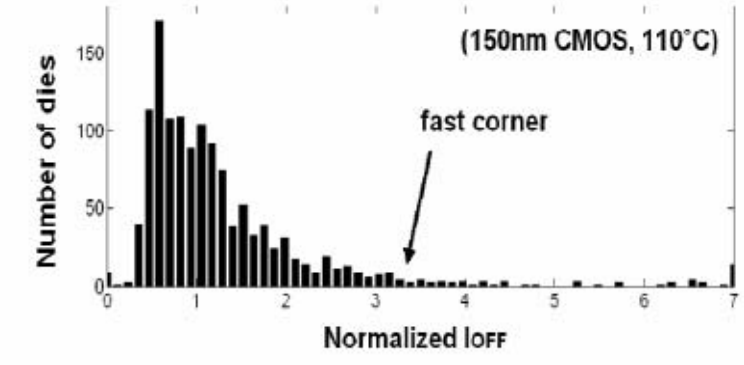

Figure 3.9: Normalized leakage NMOS current distribution [8], [9].

fabricated dies will be over designed as far as robustness is concerned. For a static flip-flop the robustness is determined by the strength of the keepers, which have large impact on the performance and power-dissipation of the flip-flops. As a consequence, sizing circuits for worst-case process corners is an increasingly inefficient methodology resulting in overall degradation of chip performance and power consumption, and/or lower yield.

3.3.2 Proposed Reconfigurable Keeper Technique

To adjust the keeper strength for the actual leakage instead of worst-case would give the lowest performance penalty at a given robustness constrain. The

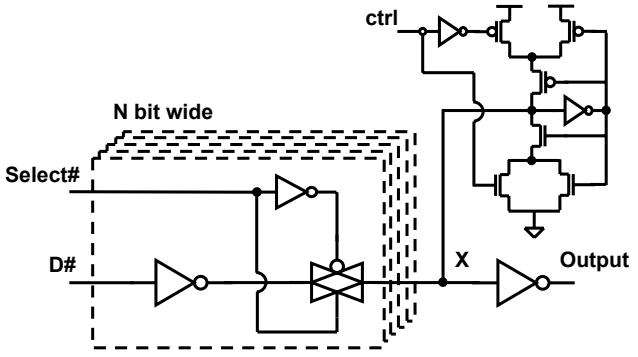

Figure 3.10: N-bit static register-file (MUX-latch) implemented with proposed reconfigurable keeper.

optimal solution would be a variable keeper that holds the internal storage node with an optimal driving strength adjusted for the actual leakage currents. However, a variable keeper with a continual range of driving strength would impose a significant design complexity due to the need for routing of global analog control signals across the chip. Therefore to reduce the complexity, digital control circuitry is a more feasible solution. With a digitally controlled keeper, the driving strength can be adjusted in more than one process corner giving the designer more flexibility to optimize the power and performance of latches and flip-flops.

A technique that reduces the spread in all design metrics of flip-flops and latches is described in **Paper 2**. An implementation example of the proposed keeper is shown in Figure 3.10 for an N-bit MUX-latch commonly used as static register-files. The *N* transmission-gates expose the storage node to extensive leakage currents when all select signals are low. Figure 3.11 shows the normalized DC-robustness for a MUX implemented with conventional keeper and with the proposed variation tolerant keeper. With the control signal (*ctrl*) low the proposed process variation tolerant keeper is configured as a weak keeper, providing sufficient feedback strength to obtain the desired robustness at the typical leakage condition. For high-leakage conditions, like at fast process corners the proposed keeper is reconfigured to the strong mode with *ctrl* high. Moreover, as discussed in section 3.2.2 burn-in testing usually performed during extreme robustness conditions [6] could also be handled with the proposed

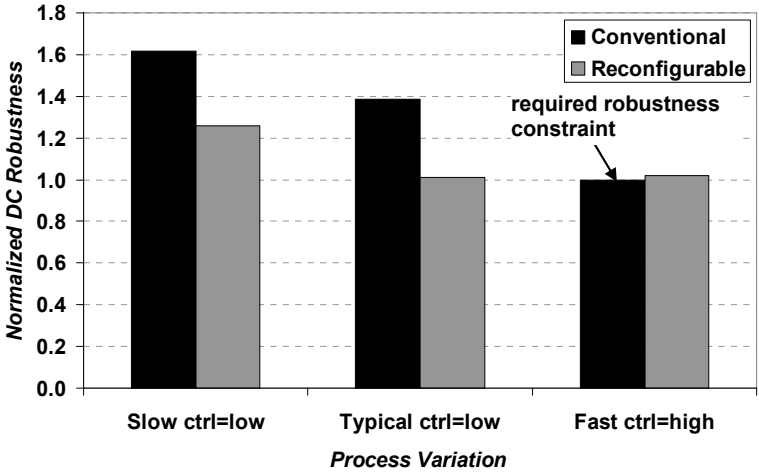

Figure 3.11: Normalized worst-case robustness for 5-to-1 MUX latches.

keeper technique.

The two different modes of operation limit the keeper sizing overhead due to process spread. The more optimized keeper strength will furthermore lead to reduced power and delay, due to less contention.

3.3.3 Variation Tolerant Weak-Keeper for Static Flip-Flops

The weak-keeper concept for conventional master-slave flip-flops was discussed in section 3.1.1 as a technique to reduce the clock load. As stated the technique usually requires careful sizing in order to limit the impact of the keeper on power and performance of the flip-flops or latches. Compared to a flip-flop or latch utilizing an interrupted keeper, the weak keeper approach usually leads to considerable power and performance tradeoffs. The reason is that the interrupted keeper ideally exposes the hold node to minimal contention during the switching regardless of the strength of the keeper. The uninterrupted weak keeper on the other hand will have increasing contention with increasing keeper strength. However, using the reconfigurable keeper technique proposed in **Paper 2** gives further opportunities to reduce the keeper overhead, hence increasing the feasibility of the weak-keeper concept. The approach is to reduce the flip-flop DC-robustness at the typical process corner down to the minimum required DC-robustness. This decreases the contention power and latency overhead. Hence, the majority of the manufactured dies can have reduced contention power and reduced latency, as well as lower clock load due to the uninterrupted keeper. For those manufactured dies that are leaky the keeper can be reconfigured to strong mode providing sufficient keeper strength to obtain the desired DC-robustness at the worst-case leakage corner.

3.3.4 Summary of Simulation Results

The proposed variation tolerant keeper technique in **Paper 2** has been implemented for a 5-to-1 static MUX-latch register-file and a conventional static transmission-gate flip-flop. Both designs have been verified by simulation on an advanced 65 nm multiple-V_{th} CMOS process [10]. For the MUX-latch register-file the delay and power can be reduced by 12 % and 7 %, respectively at typical design corners comparing to a conventional fixed keeper. Worst-case robustness is assured by the optional strong keeper. Furthermore, at typical process corner the proposed reconfigurable keeper lead to a local clock-power reduction of 9 %, without performance and robustness penalties compared to an interrupted keeper for a conventional master-slave flip-flop. This local clock-power reduction can result in significant global clock-power reduction due to the reduced clock load, which was also discussed in section 3.2.

3.4 References

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Chapter 4

Low-Power Resonant Clocking

The evolution of integrated circuits is now entering the nanoscale regime, which leads to increased complexity and need for deeper pipelining for synchronous digital VLSI chips in order to reach the tight performance demands. It has been well recognized that the dominating part of the total power consumption in a high-performance synchronous VLSI design is due to the power dissipation in the clock distribution [1] [2], which emphasize the urgent need for novel and practical solutions for low-power and high-performance clock distribution.

This chapter will provide a brief discussion on some alternative clocking techniques that have been proposed. A background to the power dissipation in conventional clocking techniques is also given followed by a detailed analysis of the power dissipation of energy-recovering clock systems. A novel energy-efficient recovering clocking technique is proposed in **Paper 4** that addressed both total clock-power and power-delay tradeoffs. The power and delay penalties in flip-flops and latches, when using the proposed clocking technique, are discussed in **Paper 3**.

4.1 Background

As a potential clocking solution energy-recovering clocking have gained increasing research interest due to the promising ability for large clock power savings. The main advantage compared to the conventional clocking is that resonant clocking has the ability to recycle the energy needed to charge the clock load when the clock network is discharged.

The ultimate goal for an energy-recovering clock-driver is to recycle all the energy used to charge the clock capacitance. The adiabatic principle of charging capacitance has the potential to reduce the energy consumed well below the conventional $CV^2/2$ relationship. The concept of adiabatic switching can be ideally described by the switch circuit in Figure 4.1. The charge that the capacitance C is charged with is $Q = CV$, and the voltage drop across the resistive switch is IR. The energy dissipated in the resistor is therefore $E = VQ = IR\,CV$. The time it takes to charge the capacitance between 0 and V is denoted T, and the charging current equals CV/T, which gives the energy dissipation $E = RC^2V^2/T$. This relation shows that the energy dissipation related to charging a capacitance with a constant current can get arbitrarily small provided that the charging time is long enough [3]. Although successful implementations of modified adiabatic circuits have been implemented and run above 100 MHz [4], a pure adiabatic technique relies on slow transition times, which makes it less suitable for multi-GHz clocked systems. Instead partly adiabatic techniques based on high-Q resonator circuits have been investigated for implementation of an energy recovering clocking. Low-power clocking based on sinusoidal clocking generated by resonating LC-tanks is treated in [5]. The impact of the timing in flip-flops and latches is discussed. However, the proposed techniques in [5] rely on four-phase clocking leading to large area and latency trade-offs.

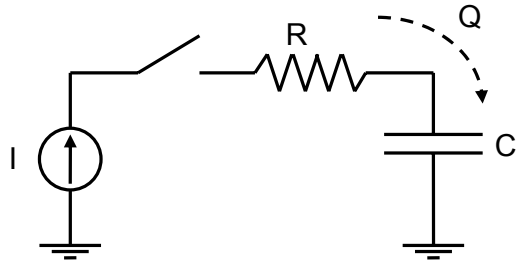

Figure 4.1: Constant current charging with an ideal resistive switch.

Clock distribution based on resonating drivers has also displayed several advantageous properties compared to the conventional clocking when it comes to clock signal integrity. Global clock distribution based on standing-wave oscillators have shown extraordinary good numbers on skew and jitter for the clock signal [6]. However, the technique requires clock signal amplification and buffering due to the limited amplitude of the standing-wave clock signal [6]. Furthermore, the technique has yet to show a power comparison against the conventional buffer-driven clocking. Another solution aimed at reducing the jitter of the global clock signal uses distributed LC-tank oscillators that are injection-locked to an external clock signal [7]. By utilizing distributed resonators in the clock network, low jitter has been displayed together with large reduction of the global clock power dissipation. Both the above techniques although promising, do not consider the impact which the resonant clocking will have on a conventionally designed digital synchronous system.

In order to make the resonant clocking become a feasible alternative to the conventional buffer driven clock distribution approach, a fair comparison between comparable designs using both clocking solutions is required. Recently several working energy-recovering solutions have been shown on fabricated silicon [8] [9]. Although many issues are left unsolved the feasibility of the energy-recovering clock looks very promising.

4.1.1 Power Analysis of a Conventional Clocking

In order to compare the energy-recovering clocking technique with the conventional method a thorough power analysis of the conventional clocking is needed. In Chapter 2 conventional clocking and clock distribution were discussed, and the tree and grid based approaches were presented. The loads on the branches in a balanced RC-tree clock-distribution are effectively driven in

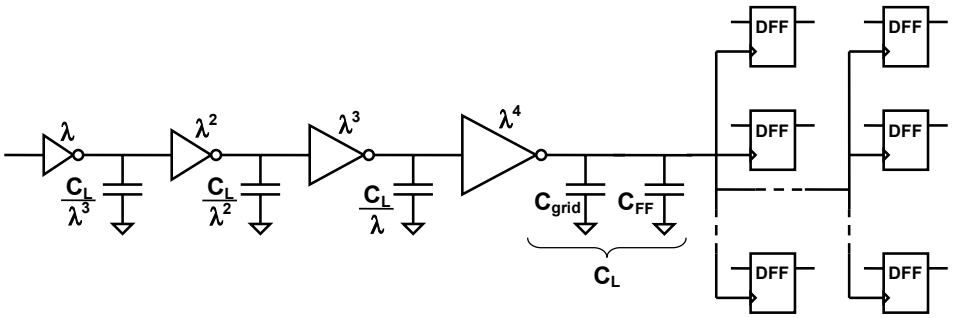

Figure 4.2: Simplified model of a conventional RF-tree clock distribution with local clock grid and clock loads.

parallel, which means that they can be combined to a simplified buffer chain [8]. Furthermore, the grid capacitance can be modeled as a lumped capacitor, assuming that a local clock grid is used for the final distribution to the timing elements (flip-flops and latches). A simplified model of a clock distribution network with a 4-level clock tree and local grid distribution is shown in Figure 4.2. The capacitance C_{grid} is the lumped model of the local distribution grid, while C_{FF} denotes the equivalent capacitance load due to the flip-flops and latches. The final clock load comprises the sum of C_{grid} and C_{FF} and is denoted by C_L. The 4-stage buffer-chain is sized with a tapering factor of λ, which in a well designed buffer gives the intermediate loads in the chain according to Figure 4.2 [8] [10].

$$P_{clock} = C_L V_{dd}^2 f_{clk} + \sum_{n=1}^{N-1} \left(\frac{1}{\lambda^n} \right) C_L V_{dd}^2 f_{clk} \qquad (4.1)$$

The total switching power dissipation can be expressed as the relationship in equation (4.1), where N is the number of stages in the buffer. If the clock buffers are designed with a tapering ratio of 3 ($\lambda = 3$), the relation in (4.1) yields that more than 2/3 of the power is dissipated in the last buffer stage [8] [10]. This is also illustrated by simulation for a 6-stage buffer chain with tapering-factor 3, shown in Figure 4.3. With the objective to reduce the total clock power, primary concern must be to limit the clock power in the last driver stage (local drivers) in

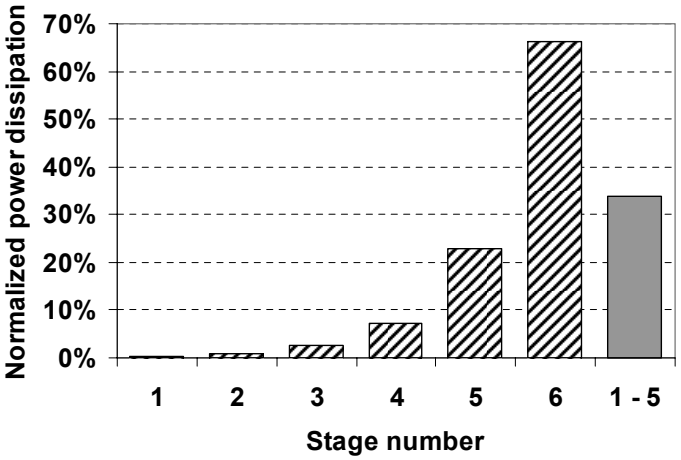

Figure 4.3: Normalized power dissipation for a 6-stage inverter chain with tapering factor of 3.

order to make significant impact. Hence, solutions requiring final clock buffers can only reduce a minor part of the total clock power.

4.1.2 Power Analysis of LC-tank Resonator Clocking

The general idea of a resonator driven clock system is to use a high-Q LC-tank to form an oscillator. Using the same clock load as in Figure 4.2 a simplified schematic model of a resonator driven system will look like Figure 4.4. At resonance the impedance for the parallel L and C_L will be infinite. Hence, power

$$P_{resonant} = \frac{\frac{1}{f_0}\int_0^{1/f_0} V_{Clk}^2 dt}{R} = \frac{3V_0^2}{2R} \tag{4.2}$$

$$P_{resonant} = \frac{3}{4Q}\pi V_{dd}^2 f_0 C_L \tag{4.3}$$

will only be dissipated in the parasitic resistance R, which comprises the total equivalent parallel resistance in the tank including the parasitic resistance in both the inductor and the distributed capacitance from the resonator to the timing circuits. A negative resistance is used to compensate for the lost energy (the current-source in Figure 4.4).

The output voltage of the resonator circuit V_{Clk} will be a sinusoid in the form of $V_0 cos(2\pi f_0 t+\phi)+V_0$. The driving strength of the compensating current source sets the magnitude of V_0 and the average power dissipated for the resonator circuit is determined by the expression in (4.2). The quality factor (Q-value) of the parallel RLC-tank can be expressed as $Q = 2\pi f_0 RC_L$ and if the magnitude of V_0 is $V_{dd}/2$ a full swing clock signal is obtained. Then expression (4.2) can be

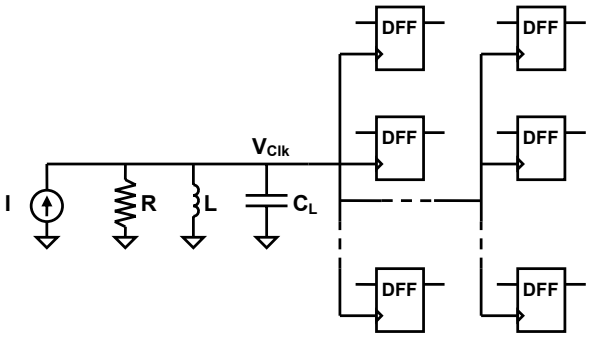

Figure 4.4: Simplified schematic model of a resonator driven clock network.

expressed as equation (4.3). This shows that a better Q-value of the tank reduces the power dissipation of the resonator circuit. Comparing the power dissipated by the resonator circuit and the conventional described by (4.1), yields the expression given in equation (4.4) for a buffer with 4 stages and a tapering factor $\lambda = 3$. This implies that Q needs to be larger than $\pi/2$ in order to obtain a power saving compared to the entire conventional clock buffer [8].

$$\frac{P_{resonator}}{P_{clock}} = \frac{3}{4Q}\pi \Big/ \sum_{n=0}^{N-1}\left(\frac{1}{\lambda^n}\right) = \frac{3}{4Q}\pi \Big/ \frac{40}{27} \approx \frac{\pi}{2Q} \tag{4.4}$$

4.1.3 Issues Concerning Tank Q-value

The efficiency of the LC-tank energy-recovering clock technique relies entirely on what quality factor of the LC-tank that can be obtained. The two contributing components on the Q-value of the LC-tank are the distributed capacitance and the inductor. The definition of the Q-value is given by equation (4.5), where ω_0 is the resonance frequency for the LC-tank given by $1/\sqrt{LC_L}$. The stored energy

$$Q_{tank} = \omega_0 \frac{energy\ stored}{average\ power\ dissipated} = \omega_0 \frac{E_{tot}}{P_{avg}} \tag{4.5}$$

at resonance for the circuit in Figure 4.4 is $E_{tot} = \frac{1}{2}C_L V^2 = \frac{1}{2}C_L (RI)^2$, while the average power dissipation is given by $P_{avg} = \frac{1}{2}I^2 R$. This yields an expression for the total LC-tank Q-value given in equation (4.6) [11]. Let R_L and R_C denote the equivalent parallel parasitic resistance in the inductor and capacitor, respectively. The quality factor for each component can then be expressed as $Q_L = R_L/\omega_0 L$ and $Q_C = \omega_0 C_L R_C$ for the inductance and capacitance respectively. The total LC-tank Q-value can, by applying (4.6), be expressed as a parallel connection of the Q-value of the two lossy reactive components, given in the expression in (4.7) [8] [11]. This means that the total Q-value is limited by the smallest of the Q-values for the reactive components.

$$Q_{tank} = \frac{1}{\sqrt{LC}} \frac{\frac{1}{2}C_L (IR)^2}{\frac{1}{2}I^2 R} = \frac{R}{\sqrt{L/C_L}} = \frac{R}{\omega_0 L} = \omega_0 C_L R \tag{4.6}$$

$$Q_{tank} = \omega_0 C_L (R_L \,//\, R_C) = Q_L \,//\, Q_C \tag{4.7}$$

In RF-design the Q-value of on-chip inductance is usually considered as the limiter of the total Q-value of an LC-tank oscillator. However, obtaining Q-values reaching 10 for inductance values of a few nH has been shown to be possible in modern CMOS processes [12] [13]. Several techniques have been

proposed in order to improve and optimize the Q-values for planar integrated inductors, such as using shunted metal layers [12] and providing good substrate shielding [13]. Using high-resistive substrates underneath the inductor would further improve the Q-value [12]. Other more exotic techniques like wafer-level packaging [14] or micro-machined devices [15] have also been proposed to improve the inductor Q-value considerably. Hence, it is clear that the limiting factor for the total LC-tank Q-value is not the inductance but instead the losses for the distributed capacitance.

In order to achieve a low loss clock network to the flip-flops and latches in the design, all presently used techniques to obtain low-skew clock-grids should be applied. This includes using wide metal wires in the top metal layers in order to reduce the wire resistance. However, for a conventionally driven clock grid a trade-off between power dissipation and grid-capacitance have to be made. This trade-off is not present in the same degree for the case of resonant clocking, because a larger grid capacitance will increase the capacitance Q-value, hence increasing the total tank Q-value and further improving the efficiency of the tank [8]. Although techniques are available to limit the losses in the clock grid it is hard to obtain equivalent parasitic series resistance values less than a few ohms, which is still high enough to make the Q-value of the distributed capacitance the limiting factor for the overall LC-tank Q-value.

4.2 Flip-Flop Power-Performance Tradeoffs

Utilizing a global resonator clock distribution that feeds a clock signal to timing-elements without intermediate buffers has great potential to reduce the clock power dissipation as previously discussed. However, the clock-signal generated by a high-Q LC-tank oscillator is usually a sinusoidal, which has longer rise and fall times compared to a clock signal generated by a rail-to-rail digital clock-buffer in high-performance VLSI systems. This will for conventional flip-flops lead to reduced performance compared to a conventionally clocked flip-flop, due to the reduced edge-rates of the sinusoidal clock. Moreover, because of the sinusoidal clock the short-circuit currents in gates directly feed by the clock increases. As an example for flip-flops that generate a second clock-phase internally the clock is feed to an inverter. A bad-edge signal to this local clock-buffer increases the power dissipation in the inverter considerably. **Paper 3** presents a performance and power study of six conventional flip-flops when used in a resonator clock-system.

Utilizing standard flip-flops even in a resonant clocking system would be advantageous because flip-flops in existing cell libraries could be used just replacing the clock distribution. However, as been shown in **Paper 3** a re-

optimization needs to be done even for conventional flip-flops in order to limit the power-delay trade-offs.

4.2.1 Summary of Simulation Results

The six conventional flip-flops described in **Paper 3** have been simulated and evaluated in a 130 nm multi-V_{th} CMOS process [16] for power and performance. The comparison is done for a clock frequency of 1 GHz, in order to get a relevant difference in edge-rate between the conventional and the resonant clock signals. A single-tone sinusoidal full-swing clock signal at 1 GHz with 1.2 V rail-to-rail swing has a 10-90 % rise/fall time of around 300 ps, which is roughly 10 times larger than a conventional clock-signal generated by a local clock-buffer in the given technology. Power-delay space comparisons show that conventional static master-slave flip-flops will experience a 20-45 % delay penalty at equal power dissipation compared to a conventional clocked flip-flop. Moreover, the requirement of two clock-phases for the master-slave flip-flops results in large excessive power-dissipation in the flip-flops if the second clock-phase is generated internally. A globally distributed second clock-phase will reduce the negative power-tradeoff due to the sinusoidal clock considerably. It however, requires that the second clock-phase is generated and distributed, which possibly leads to larger area-penalty.

Low-latency flip-flops like pulsed hybrid-latch structures (HLFF) do not react well to the sinusoidal clock resulting in between 35-60 % delay penalty, and considerable power-dissipation due to the internal clock-generator. Furthermore, the pulse duration of the flip-flop must be carefully designed due to the bad edge-rate of the incoming clock. A flip-flop type lying somewhere between the MSFF and the pulsed latches in performance is the sense-amplifier based flip-flops. According to the simulation results in **Paper 3** this type of flip-flop has comparable performance and power trade-offs to the MSFF. Moreover, the internal race-margin for the sense-amplifier flip-flops does not seem to degrade as much as for the pulsed latch implementations. Due to the fact that only a single clock-phase is needed the sense-amplifiers have a large advantage compared to the MSFF in a resonant clock design.

4.3 Energy-Efficient Resonant Clock Experiment

A successful experiment of an LC-tank resonant clocking technique is presented in **Paper 4**. The energy-recovering clock experiment is fabricated and measured using a 130 nm multiple-V_{th} CMOS process, with 6 Cu-metal layers [16]. The implemented test chip incorporates comparable designs for proposed resonant LC-tank clocking and conventional clocking. The following section will briefly

describe the implemented parts of the chip including oscillator, clock load, evaluation circuitry, and flip-flops.

4.3.1 Conventional Clock Drivers

The conventional clock driver is implemented with a main driver realized as a four stage inverter-chain with a tapering factor of 3 designed to achieve a fast edge-rate comparable to state-of-the-art high-performance microprocessors. The clock buffer drives one data-path block providing a single-phase clock to the implemented flip-flops.

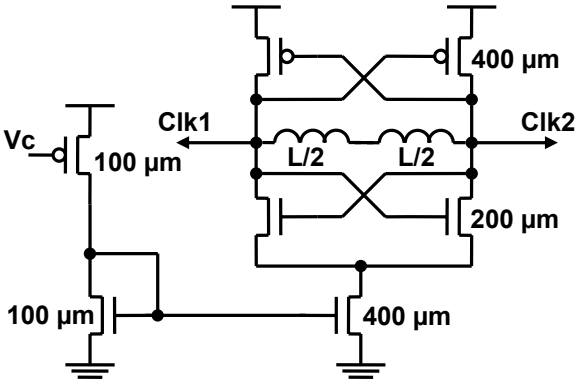

Figure 4.5: Differential complementary negative resistance oscillator used as resonant clock-driver.

4.3.2 Implemented Oscillator Topology

A complementary differential oscillator topology shown in Figure 4.5, is implemented in the test chip. The complementary structure is known to be able to provide larger gain for the same power dissipation compared to a NMOS only solution [17]. Furthermore, the symmetry of the differential design has been shown to limit the up conversion of *1/f* noise, hence improving the phase noise performance of the oscillator [17] [18] [19]. The current source is utilized to control primarily the voltage swing and secondly the oscillation frequency of the oscillator and it is controlled by the external bias voltage V_c via the current mirror circuitry. An essential component in order to form a high-Q resonator circuit is an inductance with sufficiently high Q-value as discussed in section 4.1.3. Based on simulations of the experimental chip a total inductance value of 1.2 nH is required to achieve multi-GHz oscillation frequency.

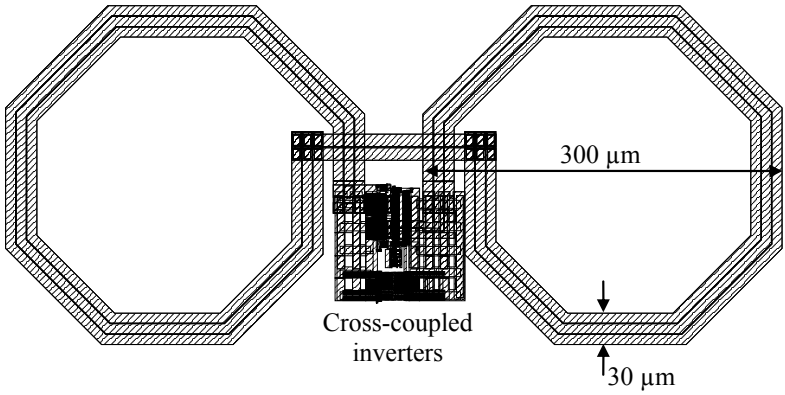

Figure 4.6: On-chip oscillator with two serially connected 600 pH inductors.

Because standard planar spiral inductors essentially are unsymmetrical devices, serially connected spirals each with half the inductance are implemented. Thus the symmetry is maintained. Each inductor is realized as a single-turn spiral in parallel 30 µm wide metal 5 and 6 wires, with an outer diameter of 300 µm. The total inductance value per inductor is estimated to 600 pH and the measurement results indicate an inductance Q-value of about 11, at the oscillation frequency of 1.56 GHz. A layout view of the implemented oscillator is shown in Figure 4.6 and as can be seen the inductors occupy a considerable amount of the total oscillator area. However, the large area consumption is traded-off in this experiment in order to increase the rate of success of the entire clock experiment. Each output phase of the oscillator drives a common data-path block that comprises clock-network and timing elements. This approach is chosen so that only one clock-phase needs to be distributed in the data-path blocks.

4.3.3 Organization of the Data-Path Blocks

A block-level schematic of the implemented test chip is shown in Figure 4.7. The capacitance in the LC-tank is as described in the background aimed to comprise the total clock network including the clock load of all timing circuits. The distributed clock load capacitance in the implemented chip is organized in a data-path block that comprises nearly 900 flip-flops in total. The common grid-based approach is utilized as distribution technique for the clock signals. A wide metal-6 wire (width ~ 30 µm) is used to distribute the output clock from the oscillator to a 14x14 wire clock grid built up from 5 µm wide metal-6 wires,

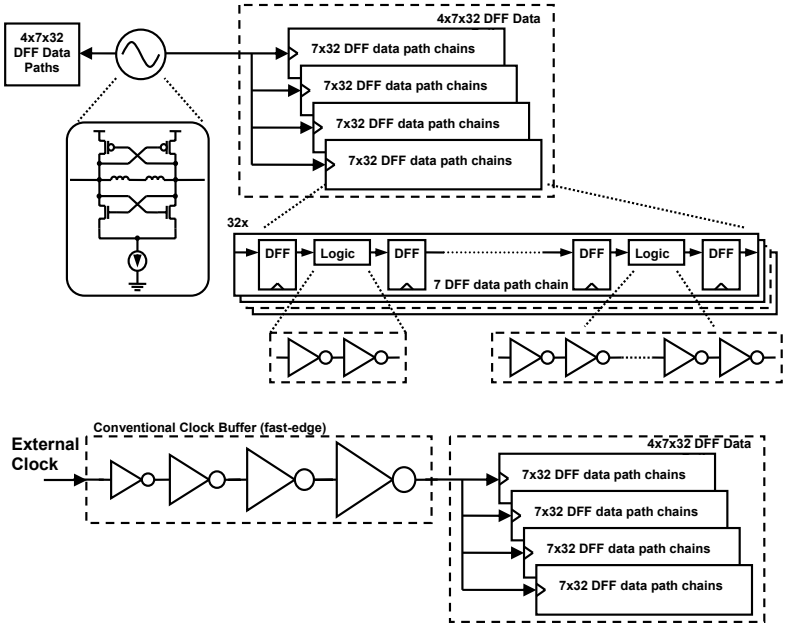

Figure 4.7: Block-level schematic of the implemented chip.

which yields an extracted parasitic resistance of around 1 Ω from corner to corner.

The data-path block is organized in 4 sub-blocks where each sub-block is organized in 32 pipeline paths that include 7 flip-flops per pipeline path, which yields a total of 896 flip-flops per data-path block. 16 of the pipelines in the sub-blocks have a constant logic depth of 2 FO2 inverters between the flip-flops. The remaining 16 pipeline paths are realized with increasing logic depth from 4 FO2 inverters up to as much as 10 FO2 inverters. In order to verify the functionality of the pipeline path a simple evaluation circuitry is added. Pipeline paths with logic depth between 4 and 10 FO2 inverters, are paired together with pipeline paths with logic depth of 2 FO2 inverters. The same input is feed into the two paths, and the outputs are compared using an XOR-gate. The result is finally captured by an SR-latch. If the outputs are not identical the output of the SR-latch will go low, hence indicating an error. Figure 4.8 shows the implemented test circuit. The proposed validation circuitry is able to capture setup-time violations in the more critical pipeline stages provided that no hold-time violations occur. Due to the good internal race-robustness of master-slave flip-flop structures the risk of hold-time violations is minimized in the

implemented test-chip. With the implemented test circuitry we are able to monitor the flip-flop functionality during the entire measurement.

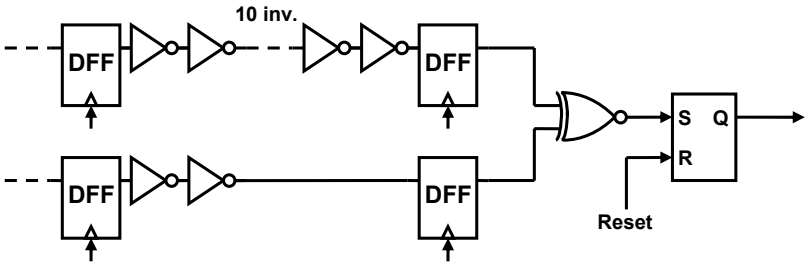

Figure 4.8: Test circuitry functionality evaluation of the pipeline paths.

4.3.4 Implemented Flip-Flops

The experimental chip incorporates conventional master-slave flip-flops as shown in Figure 4.9 and the choice of master-slave flip-flops is done in order to increase the chance of success for the chip. The functionality of this flip-flop has been covered in detail in Chapter 3.

The chosen master-slave flip-flop requires two clock phases and in the implemented chip the second clock-phase is generated locally in each individual flip-flop. This leads to increased power-dissipation in the flip-flops clocked with the oscillator, which is expected and one of the goals with the chip is to determine the impact on conventional flip-flops.

Identical transistor sizing is used in the flip-flops for both conventional clocking and resonant clocking, which could result in that the additional power-performance tradeoff is larger than it needs to be compared to if the flip-flops would have been optimized for the specific clocking strategy. However, the

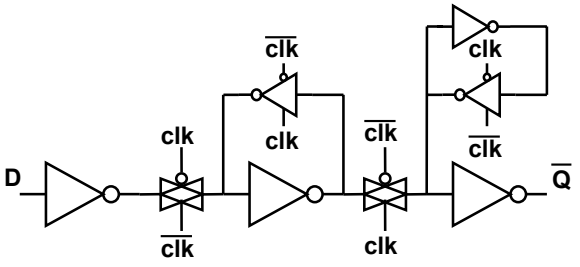

Figure 4.9: Conventional TGMS flip-flop with interrupted keepers.

chosen strategy is used in order to obtain exactly the same clock load for the conventional and the resonant clocking in the experimental chip. Based on simulations the delay tradeoff for the specific flip-flop sizing is 23 %. This corresponds well to the results for master-slave flip-flops presented in **Paper 3**.

4.4 Summary of Results and Discussion

4.4.1 Power Dissipation

In order to make a fair comparison between different clocking solutions the penalty introduced in the flip-flops and latches need to be considered. All together 26 different power supply domains are used in the entire chip in order to make it possible to evaluate the power dissipation of different parts.

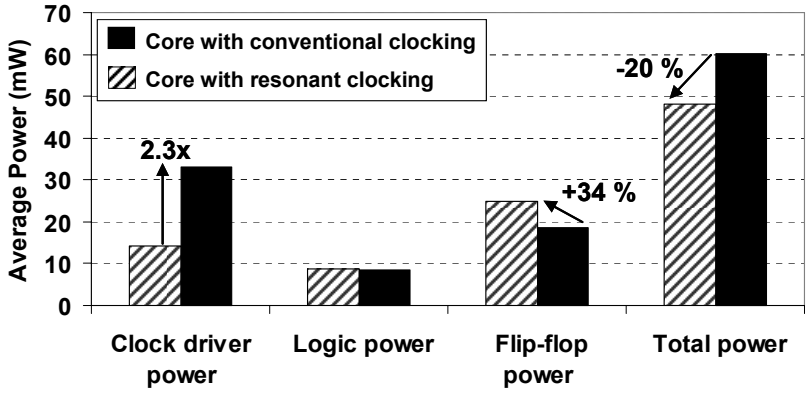

Figure 4.10: Power break-out for experimental chip, at 30 % data activity.

Especially the power dissipation of the clock-driver, flip-flops, and logic are evaluated in the experimental chip. Figure 4.10 shows the power breakout from the experimental chip, measured at a clock frequency of 1.56 GHz and at an input data activity of 30 % (roughly 230 MHz). The dissipated power in the conventional driver designed for fast clock-edge is 2.3x larger compared to the dissipated power in the resonator driver. The total power dissipation in all the implemented flip-flops together is increased by 34 % when clocked with the resonator clock-driver, compared to the flip-flops feed by the conventional clock. Despite this, the resonant clocking core consumes 20 % lower total power dissipation compared to the conventional core.

4.4.2 Clock Signal Integrity

One of the largest obstacles to overcome for the resonant clocking technique is the data dependent load utilized as capacitance of the LC-tank VCO. The state change in the flip-flops causes the total capacitance to vary. The amount of clock load variation is depending on (1) how large portion of the total capacitance that is due to the flip-flops and (2) how much the flip-flops capacitance changes. Any change in clock load capacitance will lead to phase noise on the clock signal causing jitter. This limits the performance of the design and therefore it is of highest concern to characterize and limit the capacitance variation. When the voltage changes on the clock signal the capacitance related to the clock load in the flip-flop will vary due to the different potential at the clock-node. This capacitance variation is the same every cycle and should at steady-state not introduce any cycle-to-cycle jitter. However, the clock load capacitance depends on the voltage levels on the other terminals of the clocked transistors. In case of a transmission gate as in the flip-flop in Figure 4.9, different voltages on the drain and source terminals due to data changes will impact the total gate capacitance. This variation is not cyclostationary and will cause modulation of the clock signal. Figure 4.11 shows the clock load variation of the conventional transmission-gate MSFF in Figure 4.9 when clocked with a

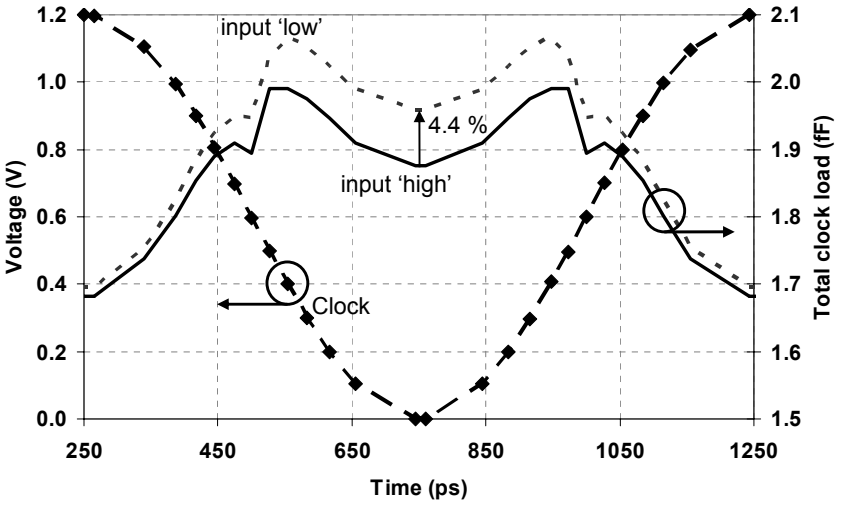

Figure 4.11: Simulated clock load of a sinusoidally clocked TG-MSFF with high and low input data, respectively.

sinusoidal clock with a frequency of 1 GHz. The difference between the cyclostationary variation due to the clock signal voltage and the data dependence is clear. The (4.4 %) variation shown in Figure 4.11 is dependent on the input of the TG-MSFF in Figure 4.9. The measured maximum jitter for the fabricated chip presented in **Paper 4** was 28 ps peak-to-peak for a data activity-ratio of 45 %.

4.5 Future Work

The measurement results from the presented chip in **Paper 4** prove the feasibility of the technique. Certainly there is a long way to go before the conventional clocking techniques can be replaced with an energy-revering clock driver as the one proposed in **Paper 4** and numerous factors need to be considered. One such consideration is how to reduce the resistive losses in the clock-networks and in the integrated inductors in order to increase the efficiency of the LC-tank. Furthermore, for large chips it might be an unfeasible solution to only use one clock driver. This is due to the large capacitance that requires low inductance value in order for the tank to oscillate at multi-GHz frequency. Potentially this could be solved with different types of synchronization between different clock-regions or some sort of phase-locking between two different clock-drivers. A related topic is the frequency tuning of the resonant clocking, which will be crucial to counteract the large uncertainties in the inductor values. Moreover, the commonly used method to reduce clock-power today is to gate the clock to blocks that are idle. With the resonant clock-driver this is not accomplished as easily as for the conventional clocking. In order to accomplish high-performance computing, flip-flops with low latency and low power penalties are required. Last but certainly not least in order to improve the jitter on the clock-signals and reduce the power trade-off more customized flip-flops will furthermore be needed.

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