RF Sampling by Low Pass \(\Sigma\Delta\) Converter for Flexible Receiver Front End

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Sammanfattning
Abstract

In today’s world the multi-standard wireless receivers are gaining more and more popularity. End-users want to access voice, data and streaming media from a single wireless terminal. An ideal approach for multi-standard receiver front-end is to digitize a wide band RF signal available from the antenna. All radio functions such as downconversion, demodulation and channel selection can then be performed in the digital domain. Analog to Digital Converter in such a case should guarantee very high linearity, speed and bandwidth specifications while consuming a lot of power. Unfortunately an ADC with such stringent requirements cannot be realized in today’s CMOS technology.

In a typical receiver a mixer is used to downconvert the RF signal to baseband (or IF) before digitization is performed. A passive mixer is often used in this case to mitigate the effect of the low frequency flicker noise. Especially it can be a sampling mixer which also serves as a S/H circuit usually required for A/D conversion.

In this thesis a lowpass sigma-delta converter with RF sampling is presented. The \(\Sigma\Delta\) modulator is SC passive circuit plus comparator, so an operational amplifier usually needed to realize the integrator is avoided. To reduce the complexity, the sampling mixer in front of the modulator is merged with the passive loop filter. As a result the sampling mixer is closed in the modulator loop, so the overall linearity of the frontend is improved to some extent. Downconversion is combined with digitization that reduces the circuit complexity as well.

The challenges while digitizing high frequency RF signal are discussed in details. Switches required to realize the loop filter are very critical and tend to be nonlinear. Parasitic effects associated with MOS transistors strongly show up at GHz frequencies. Optimized transistor sizes are obtained through simulation while addressing the speed and linearity trade-off. Another major challenge is the \(kT/C\) noise that is the real bottleneck in high frequency SC circuit design. A thermal noise model for \(\Sigma\Delta\)-modulator with second-order loop filter is presented and it is shown that a passive \(\Sigma\Delta\)-modulator is in fact thermal noise limited rather than quantization noise limited. It is because the capacitor values are limited by the very high sampling frequency used in this case.

The downconverting lowpass \(\Sigma\Delta\) modulator with second order SC passive loop filter and 1-bit quantizer is simulated at transistor level in 90nm CMOS process. This modulator can operate at very high sampling frequency up to 4GHz and can sample RF signal with carrier of up to 4GHz as well. The designed \(\Sigma\Delta\) modulator is flexible and supports sub-sampling by 2 to 8 (\(f_s = 500\text{MHz, } ... \text{2GHz}\)).

Besides, the presented design is very power efficient as it does not use OpAmps – which consume most of the power in the typical \(\Sigma\Delta\) modulators.

From schematic simulation on average, signal-to-noise and distortion ratio (SNDR) of 52 dB is obtained (ENOB = 8.3). SNDR results does not vary much for three different cases of baseband digitalization, RF sampling and RF sub-sampling. This SNDR value seems to be a good number for a passive sigma-delta modulator. The detailed simulation results for the three cases discussed in the thesis work shown that, the modulator performs equally well for a wide range of sampling and RF signal frequencies.

Nyckelord
Keyword
RF sampling, Sampling Mixer, Downconversion , Sigma Delta modulator, Low pass Sigma Delta ADC, Passive Sigma Delta ADC, Mixer inside the loop
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To Ammi and Daddy

who loved me and always prayed for my success
Abstract

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The challenges while digitizing high frequency RF signal are discussed in details. Switches required to realize the loop filter are very critical and tend to be
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The downconverting lowpass $\Sigma\Delta$ modulator with second order SC passive loop filter and 1-bit quantizer is simulated at transistor level in 90nm CMOS process. This modulator can operate at very high sampling frequency upto 4GHz and can sample RF signal with carrier of upto 4GHz as well. The designed $\Sigma\Delta$ modulator is flexible and supports sub-sampling by 2 to 8 ($f_s = 500MHz, \ldots 2GHz$).

Besides, the presented design is very power efficient as it does not use OpAmps – which consume most of the power in the typical $\Sigma\Delta$ modulators.

From schematic simulation on average, signal-to-noise and distortion ratio (SNDR) of $52\ dB$ is obtained (ENOB = 8.3). SNDR results does not vary much for three different cases of baseband digitalization, RF sampling and RF sub-sampling. This SNDR value seems to be a good number for a passive sigma-delta modulator. The detailed simulation results for the three cases discussed in the thesis work shown that, the modulator performs equally well for a wide range of sampling and RF signal frequencies.
Abbreviations

ΣΔ  Sigma Delta
ADC  Analog to Digital Converter
DAC  Digital to Analog Converter
IF   Intermediate Frequency
RF   Radio Frequency
OSR  Oversampling Ratio
CMOS Complementary Metal Oxide Semiconductor
DSP  Digital Signal Processor/Processing
IR   Image Reject
LNA  Low Noise Amplifier
VGA  Variable Gain Amplifier
AGC  Automatic Gain Control
SNR  Signal-to-Noise Ratio
BW   Bandwidth
LSB  Least Significant Bit
MSB  Most Significant Bit
SFDR Spurious Free Dynamic Range
CM   Cross Modulation
SNDR Signal-to-Noise-and-Distortion Ratio
SINAD Signal-to-Noise-and-Distortion Ratio
THD  Total Harmonic Distortion
IM   Intermodulation Distortion
HD   Harmonic Distortion
PDF  Probability Density Function
INL  Integral Non-Linearity
DNL   Differential Non-Linearity
LO    Local Oscillator
SC    Switched Capacitor
ENOB  Effective Number of Bits
SDM   Sigma Delta Modulator
FFT   Fast Fourier Transform
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Chapter 1

A/D Conversion in Radio Receivers

1.1 Introduction

Most of the material in this chapter is taken from [1, chap2].

Main function of a radio receiver is the reception of a weak, desired channel from a wide spectrum. In the presence of strong interferers, signal should be detected by the receiver with minimum specified signal-to-noise-and-distortion ratio. To accomplish the task of selectivity and sensitivity, filters and amplifiers are needed to suppress the interference signals and to provide power gain to the desired channel respectively. Generally amplifier blocks determine the sensitivity and filters determine the selectivity of the receiver. A desired channel may be modulated at a higher frequency so a mixer is also required to down convert the channel to some appropriate lower frequencies. Analog-to-digital converters are becoming a more and more important part of the contemporary receiver architecture. Technology scaling (size and supply voltage and hence power consumption reduction) allows analog functionality such as filtering and mixing, to be migrated to digital signal processors with a higher degree of performance. Hence ADCs are seeking its place closer to the antenna. Shifting part of the selectivity to DSP require an ADC with large dynamic range and high linearity. The place of ADC in a receiver front end and performance matrices of ADCs are discussed in the following sections.
1.2 Image Problem

Before discussing some receiver architectures and ADC performance requirements in these architectures, the image problem is worth mentioning.

Figure 1-1[2, chap1] shows two cases of down-conversion in a receiver: down-conversion of passband RF signal to IF and to baseband. In non-zero IF conversion case, the undesired image band will be superimposed on the desired band after mixing. It is necessary to suppress any signal in the image band prior to mixing. Image suppression is achieved with an image reject filter (IR) in super-heterodyne architecture as shown in Figure 1-3.

In the zero-IF architectures $f_{LO}$ is equal to $f_{RF}$, so image band is the same as desired signal band and hence no image rejection is needed. However, this is not entirely true for phase and frequency modulated signal where upper and lower side-bands do not contain same information. In this case the image reject filter cannot be used. To achieve sufficient suppression of the image band, quadrature mixing is usually used.

1.3 From baseband to RF Digitization

The position of ADC in a receiver front-end is of great importance as it affects overall performance, complexity, power consumption and cost. Figure 1-2 shows the partitioning of a conventional receiver front-end.

Shifting analog components such as filters, mixers and amplifiers to the digital domain or, in other words, moving the ADC towards the antenna, reduces
the complexity of the receiver. However, as the ADC moves closer to the antenna, the required performance specifications for the ADC become very stringent.

1.3.1 Heterodyne receiver with baseband Digitization

The traditional superheterodyne receiver architecture is shown in Figure 1-3. RF signal received by the antenna is filtered by a wideband bandpass filter, and amplified by LNA. A desired channel is down-converted to intermediate frequency by tuning \( f_{LO1} \). Before mixing to IF, IR filter must suppress the image signal. The channel select filter suppresses the adjacent channels and passes the desired channel to the variable gain amplifier (VGA). VGA with automatic gain control (AGC) finally fits the signal power into the dynamic input range of the subsequent blocks. \( f_{LO2} \) down-converts the IF signal to baseband. As mentioned earlier, quadrature down-conversion is employed for sufficient image suppression. At this stage after passing through the anti-aliasing filter, the baseband signal is digitized.

Requirements for the ADC regarding dynamic range, linearity, and bandwidth in the superheterodyne receiver are relaxed because of all the filters, in particular the channel filter, preceding the A/D converters. In addition, the baseband channel can be digitized at a relatively low sample rate. Hence power efficiency of the ADC can be high. Image rejection requirements strongly depend on the choice of the second IF frequency (which can be zero in this case).
Shortly, if low-IF is chosen then offset as well as flicker noise does not interfere with the desired signal. On contrary as the desired channel is translated down to baseband in zero-IF, DC offset and flicker noise are present in the middle of the signal band and interfere with the signal. However power consumption and linearity of the receiver is improved as IF stages are not present in this case. This type of receiver is known as zero-IF or homodyne receiver and is shown in Figure 1-4.

1.3.2 Heterodyne receiver with IF digitization

In the configuration shown in Figure 1-5, A/D conversion is performed after the signal is downconverted to IF, further downconversion to baseband is then performed in the digital domain. Because IF signal is digitized, $\frac{1}{f}$ noise and DC offset problem is largely reduced. Comparing to baseband digitization, only one ADC is required as I/Q mixing can be performed digitally with high linearity and perfect matching.
The drawback of IF digitization is that high sampling rate is required to simply satisfy the Nyquist criteria ($f_s \geq 2f_{IF}$), specially when IF is high. The high sampling rate translates to high power consumption and also linearity and dynamic range requirements are difficult to achieve for ADC in this case. Finally, because channel filtering and VGA are missing now, it puts further requirements onto the ADC in terms of linearity and dynamic range.

**1.3.3 RF digitization**

Receiver architecture with RF digitization is shown in Figure 1-6. This architecture only contains LNA, ADC and DSP processor. All radio functions such as downconversion, demodulation and channel selection are performed in the digital domain. The concept of such an architecture is to digitize the whole frequency band for a particular standard and then multiple frequency channels can be selected with parallel digital filter banks. To handle such a wideband RF signal coming directly from antenna, ADC should now guarantee very high linearity and bandwidth requirements. The power consumption will also be largest as compared to IF and baseband digitization.

Because of such stringent requirements on ADC, it is impossible to realize it in today’s CMOS technology.

**1.4 Digitization with bandpass $\Sigma \Delta$ modulator**

Speed, power and linearity constraints on ADCs are re-emphasized in this section in a context of $\Sigma \Delta$ modulator. In the superheterodyne receiver architecture of Figure 1-3, A/D conversion is performed at baseband. Although requirements on ADC are relaxed due to low frequency and pre-filtering stage, the overall receiver performance may not be satisfactory, for most of the applications.
IF stages introduce extra noise and distortion to the signal. Furthermore these IF stages require external filters and overall power consumption of the receiver can be very high as compared to zero IF digitization case. To overcome some of these problems bandpass $\Sigma\Delta$ modulators can be used, where downconversion is also achieved along with IF digitization. Center frequency of $\Sigma\Delta$ modulator is highly dependent on gains of the op-amps used to implement the resonator (loop filter). This dependency on gain limits the achievable SNR as IF increases. In addition distortion produced in bandpass $\Sigma\Delta$ modulator increases as IF increases. As shown in Figure 1-7, if bandpass $\Sigma\Delta$ modulator is used in zero IF receiver then no mixer is required for RF to baseband downconversion, because mixing is also performed by bandpass $\Sigma\Delta$. For such an architecture, sampling frequency ($f_s$) should be higher than radio frequency ($f_{RF}$). Typically it follows $f_s = 4f_{RF}$.

For, say, 1 GHz RF signal $f_s$ of 4 GHz is very high, which will put very tough requirements on ADC, even higher than for direct RF down conversion case. Furthermore, also the centre frequency shift dependency on gain of the op-amp can be enormous at RF frequency. Parasitic effects at such a high rate can be a major cause of distortions, which is undesirable. Finally bandpass $\Sigma\Delta$ modulator is not a wideband digitizer.
1.5 RF sampling/Digitization with lowpass $\Sigma\Delta$ modulator

Another approach for IF digitization [3], adopted here for RF digitization, which is the topic of this thesis, is described in this section. The dashed box portion in Figure 1-4 (Homodyne receiver architecture) is redrawn in Figure 1-8(a). Here RF signal is first mixed down to DC (where $f_{LO} = f_{RF}$) and then digitized with a lowpass $\Sigma\Delta$ modulator, while the lowpass filter serves as anti-aliasing filter. As shown in Figure 1-8 (b) passive sampling mixer can be used instead of the active mixer and low pass filter can be removed from the structure, when the oversampling ratio is very high.

By examining the circuit it can be seen that the switch and the loading capacitor $C_s$ form a S/H circuit which is essential for a typical A/D conversion process.

A block diagram of discrete time lowpass $\Sigma\Delta$ ADC with S/H is shown in Figure 1-9, where $H(z)$ is a lowpass passive switch capacitor filter. Mixing function achieved by S/H can be then merged with the sampling process in the ADC. Because the S/H will be now acting as a mixer, $f_s$ should not necessarily be greater than or equal to $f_{RF}$, but subsampling can be used where $f_s$ can be X times smaller than $f_{RF}$, (where X is an integer). However, the bandpass sampling criteria, which states that “A bandpass signal can be digitized without aliasing if the relation, $f_s \geq 2BW$ holds”. should not be violated.
Figure 1-9: Block diagram of discrete time lowpass $\Sigma\Delta$ ADC with 1 bit quantizer

(Where $BW$ is the bandwidth of the bandpass signal and $f_S$ is the sampling frequency).

A detailed discussion on the design and implementation of downconverting lowpass passive switch capacitor $\Sigma\Delta$ ADC is given in Chapter 4.

### 1.6 Performance metrics

Important specifications for ADC, embedded in a radio receiver are the dynamic range and non-linearity.

#### 1.6.1 Dynamic range

Different terms are used in literature to indicate dynamic range. Most commonly occurring are dynamic range, signal-to-noise-ratio and resolution.

**Dynamic range (DR)** – ratio between maximum signal power ($P_{\text{max}}$) and minimum detectable signal power ($P_{\text{min}}$) within a frequency band of interest. Or more specifically [4, chap 6] for an ADC, it is the ratio of input signal power for a full-scale sinusoidal input to the input signal power when the corresponding SNR is 1 (0dB). Mathematically

$$DR = 10 \log_{10} \left( \frac{P_{\text{max}}}{P_{\text{min}}} \right)$$

**Signal-to-noise ratio** – ratio of the signal power $P_s$, and noise power $P_n$, within a certain band of interest.

$$SNR = 10 \log_{10} \left( \frac{P_s}{P_n} \right)$$

**Resolution** – smallest output step, or least significant bit (LSB), which indicates a change of the input signal. $LSB = \frac{V_{\text{REF}}}{2^N}$, where $N$ is the number of ADC bits
and $V_{REF}$ is the ADC reference voltage. For example: for $V_{REF} = 2\,V$ and $N = 8$, $LSB = 7.8125\,mV$. Resolution is also specified in bits, as in this case resolution is 8 bits.

## 1.6.2 Non-linearity

Mathematically, memoryless nonlinearities are specified by a power series

$$s_o(t) = \alpha_1 s_i(t) + \alpha_2 s_i^2(t) + \alpha_3 s_i^3(t) + \cdots$$  \hspace{1cm} (1.3)

Where $s_i(t)$ and $s_o(t)$ are the input and output signals respectively and $\alpha_1$ is the small signal gain. Only second and third-order nonlinearities are usually considered for a receiver, because either higher order nonlinearities get very small, or they are not important.

**Harmonic distortion** – if we drive a nonlinear system with a single tone $s_i(t) = S_1 \cos \omega_1 t$ then using (1.3), the output of the nonlinear system can be written as

$$s_o(t) = \alpha_1 S_1 \cos \omega_1 t + \alpha_2 S_1^2 \cos^2 \omega_1 t + \alpha_3 S_1^3 \cos^3 \omega_1 t.$$  \hspace{1cm} (1.4)

After simple manipulation:

$$s_o(t) = \frac{\alpha_2 S_1^2}{2} + \left( \alpha_1 S_1 + \frac{3\alpha_3 S_1^3}{4} \right) \cos \omega_1 t + \frac{\alpha_2 S_1^2}{2} \cos 2\omega_1 t + \frac{\alpha_3 S_1^3}{4} \cos 3\omega_1 t.$$  \hspace{1cm} (1.5)

The harmonic distortion is defined as the ratio of the amplitude of a particular harmonic to the amplitude of the fundamental. If we assume $\alpha_1 S_1 \gg \frac{3\alpha_3 S_1^3}{4}$ then second and third order harmonic distortion, represented with $HD_2$ and $HD_3$ respectively are given as.

$$HD_2 = \frac{ampl. \text{ of second harmonic}}{ampl. \text{ of fundamental}} \approx \frac{\alpha_2 S_1}{2\alpha_1}$$  \hspace{1cm} (1.6)
Examples of $HD_2$ and $HD_3$ are shown in Figure 1-10 (a).

**Spurious-free dynamic range (SFDR)** – is a ratio between the desired output signal power $P_s$, to the in-band distortion component with maximum power $P_{d,max}$. In-band distortion can be due to harmonic distortion or intermodulation distortion. An example SFDR is shown in Figure 1-10(b). Mathematically

$$SFDR = 10 \log_{10} \left( \frac{P_s}{P_{d,max}} \right)$$  \hspace{1cm} (1.8)

**Cross modulation (CM)** – when a desired weak signal and strong interferer pass through a nonlinear system described by equation (1.3) then the modulation (noise) on the amplitude of the interferer is transferred to the amplitude of the weak desired signal. As shown in the Figure 1-10 (d) cross modulation is described as the ratio of desired signal power to the cross modulation distortion components.

**Signal-to-noise and distortion ratio (SNDR)** – ratio between signal power, and noise plus total harmonic distortion (THD). where THD is defined by the following expression

$$THD = \sqrt{HD_2^2 + HD_3^2 + \cdots}$$  \hspace{1cm} (1.9)

**Intermodulation distortion (IM)** – intermodulation distortion occurs when more than one tone is present at the input of nonlinear system. The intermodulation distortion is commonly analyzed using “two tone test”. Assume two strong interferers at the input of the nonlinear system, specified by $s_i(t) = S_1 \cos \omega_1 t + S_2 \cos \omega_2 t$. Using equation (1.3)

$$s_o(t) = \alpha_1(S_1 \cos \omega_1 t + S_2 \cos \omega_2 t) + \alpha_2(S_1 \cos \omega_1 t + S_2 \cos \omega_2 t)^2$$
$$+ \alpha_3(S_1 \cos \omega_1 t + S_2 \cos \omega_2 t)^3.$$  \hspace{1cm} (1.10)
After simple trigonometric manipulations, the second and third order intermodulation products can be written as:

\[ \omega_1 \pm \omega_2: \alpha_2 S_1 S_2 \cos(\omega_1 + \omega_2)t + \alpha_2 S_1 S_2 \cos(\omega_1 - \omega_2)t; \]

\[ 2\omega_1 \pm \omega_2: \frac{3\alpha_3 S_1^2 S_2}{4} \cos(2\omega_1 + \omega_2)t + \frac{3\alpha_3 S_1^2 S_2}{4} \cos(2\omega_1 - \omega_2)t; \]

\[ 2\omega_2 \pm \omega_1: \frac{3\alpha_3 S_2^2 S_1}{4} \cos(2\omega_2 + \omega_1)t + \frac{3\alpha_3 S_2^2 S_1}{4} \cos(2\omega_2 - \omega_1)t; \quad (1.11) \]

When strong interferers applied to the nonlinear system, are very close to each other and to the signal of interest with frequency \( \omega_0 \), then as can be seen from the Figure 1-11 (a) the third order intermodulation products \( (I_{D3}) \) with frequency \( 2\omega_2 - \omega_1 \) will fall directly into the band of interest and will corrupt the desired...
signal at $\omega_0$. Furthermore, interferers at $\omega_1$ and $\omega_2$ are close to $\omega_0$, and therefore a very sharp filter is needed to filter them out.

Assuming $S = S_1 = S_2$ in equation (1.11), which is generally the case of two tone test, the third-order-intermodulation distortion (IM3) is given by

$$IM_3 = \frac{ampl. \ of \ third \ order \ intermod. \ product}{ampl. \ of \ fundamental}$$  \hspace{1cm} (1.12)

$$IM_3 = \frac{I_{D3}}{I_{D1}} = \frac{3\alpha_3}{4\alpha_1}S^2$$  \hspace{1cm} (1.13)

By comparing (1.7) and (1.13) it can be seen that $IM_3 = 3HD_3$. $IM_3$ is graphically shown both in Figure 1-10 (c) and Figure 1-11 (a).

Unlike the case of a heterodyne receiver, in zero-IF receiver the second-order intermodulation products ($I_{D2}$) are very harmful and may fall directly into the desired downconverted band as shown in Figure 1-11 (a). This problem must be resolved for the successful implementation of a direct conversion receiver. $IM_2$ is given as:

$$IM_2 = \frac{ampl. \ of \ second \ order \ intermod. \ product}{ampl. \ of \ fundamental}$$  \hspace{1cm} (1.14)
Again by comparing (1.6) and (1.15) it can be seen that $IM_2 = 2HD_2$. $IM_2$ is also shown graphically both in Figure 1-10 (c) and Figure 1-11(a).

**Intermodulation intercept point (IP)** - Intermodulation intercept point 3 (IP3) is the most important specification of intermodulation distortion. IP3 is measured by the two tone test. From (1.5) it can be seen that when $S$ increases, the fundamental at $\omega_1$ increases linearly. On the other hand from (1.11) we can see that $I_{D3}$ increases in proportion to $S^3$. Plotted on the logarithmic scale in Figure 1-11(b), the magnitude of $I_{D3}$ grows at thrice the rate of $I_{D1}$. IP3 is the intersection of the extrapolated $I_{D3}$ and $I_{D1}$.

Mathematically, for the input level $S_{IP3}$, $I_{D1}$ and $I_{D3}$ will be having same amplitude as shown in Figure 1-11(b), then using (1.5) and (1.11)

\[
I_{D1} = I_{D3} \\
\left| \alpha_1 \right| S_{IP3} = \frac{3}{4} \left| \alpha_3 \right| S_{IP3}^3
\]  

(1.16)

Thus the input $IP_3$ is

\[
S_{IP3} = \sqrt[3]{\frac{4 \left| \alpha_1 \right|}{3 \left| \alpha_3 \right|}}
\]  

(1.17)

With the aid of Figure 1-11(a) a useful equation that relates the IP3 to IM3, expressed in decibels is as follows

\[
IIIP_3 \mid dBm = P_{in} \mid dBm - \frac{IM_3 \mid dB}{2}
\]  

(1.18)
1.7 Bibliography


Chapter 2

Basics of Data Converters

In this chapter we will very briefly discuss Nyquist-rate digital-to-analog (DAC) and analog-to-digital (ADC) converters. Understanding the operation of basic ADC and DAC is essential for building more complex data converters. Data converters can be roughly divided into two categories [1, chap1].

Nyquist-rate data converters: In the Nyquist-rate data converters, there is one-to-one correspondence between the input and output. Output of the converter at any time only depends on the present input and not on the previous inputs; converters are memory-less. As the name suggest, sampling rate $f_s$ of such a converter can be as small as Nyquist-criteria suggests (twice the bandwidth $f_B$ of the input signal). However due to difficulties in realizing anti-aliasing and reconstruction filter, $f_s > 2f_B$ is used ($f_s = (3 \text{ to } 20)f_B$ is typical).

Oversampled converters: By choosing the sampling rate higher than the Nyquist-rate data converters, quantization noise within the band of interest can be reduced by filtering out the noise outside the band. This filtering is performed in digital domain in case of ADC and in analog domain in case of DAC. Data converters that just use oversampling are seldom used; rather oversampled converters with noise shaping are used. Such converters use feedback system. In this case output of a converter at any instance in time is dependent on all the
previous outputs. Oversampling with noise shaping is achieved with structure called sigma delta modulator. Sigma-delta or delta-sigma modulators are discussed in detail in chapters 3.

2.1 Digital-to-analog converter

Block diagram of DAC is shown in (dashed box) Figure 2-1. $v_{OUT}$ is the voltage output. $D_{in}$ is the digital input word consists of $N$-bits ($b_0, b_1, \ldots b_N$) and $V_{REF}$ is the constant DC voltage. $b_0$ is the least-significant bit (LSB) and $b_N$ is the most-significant bit (MSB). Voltage output can be expressed as.

$$v_{OUT} = V_{REF}D_{in} = V_{REF}(b_0 2^{-1} + b_1 2^{-2} + \ldots + b_N 2^{-N}) \quad (2.1)$$

Resolution of the DAC is equal to number of bits in the applied digital word. Ideal transfer characteristics for 3-bit DAC is shown in Figure 2-2. Output voltages of the DAC are well defined values and are separated by

$$V_{LSB} = \frac{V_{REF}}{2^N} \quad (2.2)$$

$V_{LSB}$ is a voltage change at the output of the DAC when LSB of the input word is changed. Note that, maximum output voltage of the DAC, which is called full-scale voltage ($V_{FS}$) is not equal to $V_{RF}$ but,

$$V_{FS} = V_{RF} - V_{LSB} = V_{RF}(1 - 2^{-N}) \quad (2.3)$$

![Figure 2-1: N-bit DAC (dashed box) in signal processing applications](image-url)
There are variety of ways to realize integrated Nyquist-rate DACs. They are categorized into four main types [2, chap12]: decoder, binary-weighted, thermometer-code and hybrid. Resistor string, 3-bit, decoder based DAC which is the most straightforward approach, is shown as an example in Figure 2-3.
2.2 Analog-to-Digital converter

ADC is the inverse of DAC. However it is not possible to continuously convert the incoming analog signal to digital output code, input to ADC must be sampled. Hence A/D conversion process is done in two steps, sampling and quantizing. Figure 2-4 shows the A/D conversion process. Anti-aliasing filter is needed to limit the input signal below $f_s/2$, such that after A/D conversion spectrum of discrete time signal does not overlap.

Sample-and-hold circuit maintains the input analog signal constant to the ADC during conversion time. The shaded box of Figure 2-4 is redrawn as a single equivalent block in case of voltage ADC in Figure 2-5.

Figure 2-4: General block diagram of ADC

$D_{out}$ is the digital output word consist of N-bits ($b_0, b_1, \ldots, b_N$) and $v_{in}$ and $V_{REF}$ is the analog input and reference voltage respectively. $V_{LSB}$ for ADC is the same as for DAC and is defined in (2.2). Following relation relates these signals.

$$V_{REF}(b_0 2^{-1} + b_1 2^{-2} + \cdots + b_N 2^{-N}) = v_{in} \pm V_x$$  \hspace{1cm} (2.4)

where

$$-\frac{1}{2} V_{LSB} \leq V_x < \frac{1}{2} V_{LSB}$$  \hspace{1cm} (2.5)

Figure 2-5: Block diagram of ADC
Figure 2-6: Input ouput characteristics of 3-bit ideal ADC

Input-output characteristic of 3-bit ideal ADC is plotted in Figure 2-6. Original transfer characteristics are shown as shaded-dashed staircase curve, while solid staircase curve is the $1/2 V_{LSB}$ shifted version of the original. Note that there is now a range of input values, which produce a certain digital code. For example: for the original case, input values in the range $\{V_{REF}/8 \leq v_{in} < 2V_{REF}/8\}$ produce a single code 001. This signal ambiguity produces quantization error at the output of the ADC. Quantization error is also plotted for both cases, which can be recognized as the difference of the output of infinite resolution ADC and $N$-bit ADC (3-bit ADC in this case). See how the range of full scale voltage ($V_F$) and quantization error ($v_q$) of ADC differ for both cases. Quantization error for shifted case is $\{-1/2 V_{LSB} \leq v_q < 1/2 V_{LSB}\}$, which is more desirable than $\{0 \leq v_q < V_{LSB}\}$ (original case).
Finally, input to the ADC should remain within the $V_{FS}$ range. Otherwise quantization error will be larger than $1/2 V_{LSB}$ (bold characteristics). This fact is emphasized in Figure 2-6.

### 2.3 Quantization noise

We can model quantization error as being equivalent to additive noise source. Block diagram in the Figure 2-7 is considered for investigating quantization noise behavior. After rearranging the equation at the output, $v_1$ is

$$v_1 = v_{in} + v_q$$  \hspace{1cm} (2.6)

If $v_{in}$ is a ramp function then output $v_q$ can be seen from Figure 2-6 with x-axis changed from voltage to time. Equation (2.6) reveals that quantized signal $v_1$ can be modeled as the input signal, $v_{in}$ plus some additive noise signal, $v_q$.

![Figure 2-7: Circuit to investigate the quantization noise behavior](image)

Using stochastic approach [3, chap11], if we assume that input signal is varying rapidly such that quantization error $v_q$ is random variable uniformly distributed between $\pm V_{LSB}/2$. Where $V_{LSB}$ is defined by (2.2). Probability density function of such a signal is, $F_q(x)$ shown in Figure 2-8 will be a constant value. Average value of quantization error, $v_{q(avg)}$ is zero.

$$v_{q(avg)} = \int_{-V_{LSB}/2}^{V_{LSB}/2} xF_q(x) \, dx = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} x \, dx = 0$$  \hspace{1cm} (2.7)

![Figure 2-8: Assumed PDF for quantization error, $v_q$](image)
And the rms value of the quantization error power

\[
\frac{v_q^2}{V_{LSB}} = \int_{-V_{LSB}}^{V_{LSB}/2} x^2 F_q(x) \, dx = \frac{1}{V_{LSB}} \int_{-V_{LSB}}^{V_{LSB}/2} x^2 \, dx = \frac{V_{LSB}}{\sqrt{12}}
\]

(2.8)

(2.9) gives best possible SNR for N-bit ADC, SNR decreases for reduced input signal.

There are variety of ways to realize integrated Nyquist-rate ADC. Number of architecture suitable for particular applications can be found in great detail in [2, chap13], [3,chap13 ], [4,chap34]. Most straight forward and simplest is the flash ADC. 2-bit flash ADC is shown in Figure 2-9 as an example.
Dynamic characteristics of data-converters are discussed in Section 1.6. Static characteristics for data-converters are also very important in understanding their design. Static characteristics for data-converters are listed below. We will not discuss them here. Detailed discussion on these characteristics can be found in [2], [3] and [4].

- Gain error
- Integral non-linearity (INL)
- Differential non-linearity (DNL)
- Monotonicity
- Missing Codes
2.4 Bibliography


Chapter 3

Principle of ΣΔ ADC

In the previous chapter we have discussed the concept of Nyquist-rate ADCs. Although Nyquist-rate ADCs can be very fast, their resolution is limited to a 10-12bit range. In this chapter we will discuss a different class of ADCs called sigma-delta (ΣΔ) modulator, which are very popular in wireless communication. Achievable resolution of ΣΔ ADCs can be much higher than Nyquist-rate ADCs (typically in the range 13-20bits). With today’s process technologies they can achieve the speed comparable to Nyquist-rate ADCs. Oversampling and noise shaping are two key techniques employed in these ADCs.

3.1 Oversampling

For a band-limited signal $f_B$, the Nyquist-rate is $2f_B$, which is the minimum sample rate to avoid aliasing. If the sampling rate is higher than the Nyquist-rate of ADC, then it is called oversampling. Oversampling ratio is defined as:

$$OSR = \frac{f_s}{2f_B}$$

(3.1)

Oversampling ADC relaxes the requirements placed on the analog circuitry at the expense of more complicated digital circuitry. This trade-off becomes more
Chapter 3: Principle of ΣΔ ADC

Desirable for contemporary CMOS process technologies with 1V power supplies, where complicated high-speed digital circuitry is more easily realized in less area. Realization of high-resolution analog circuitry is complicated by low power-supply voltages. With oversampling converters the analog components have reduced requirements on matching tolerances and amplifier gains. Another advantage of oversampling ADC is that it relaxes the specification of anti-aliasing filter. Figure 3-1 shows the comparison of anti-aliasing filter in case of Nyquist-rate and oversampling ADC. For the oversampling case, it can be seen that, analog filter with such a relax requirements can be realized as a simple first order RC filter. Furthermore, extra dynamic range can be obtained at the output of the ADC, because for high OSR, quantization noise power is spread over large frequency range and out of band-noise can be filtered out using digital filter.

It is assumed that the quantization noise is independent from the input signal. Moreover, the quantization noise power spectral density is uniformly distributed in the sampling frequency band $\pm f_s$, i.e. the quantization noise is so-called white noise (constant over frequency). Power spectral density $S_e(f)$ of quantization noise, is shown in Figure 3-2.

$$S_e(f) = \frac{(\Delta^2/12)}{f_s}$$
Amplitude of power spectral density \( (h_e) \) is calculated by noting that total noise power is \( \Delta^2/12 \) (\( \Delta = V_L, V_B \) = quantization step) and, with two-sided definition of power

\[
P_{e,\text{total}} = \int_{-f_s/2}^{f_s/2} S_e(f)df = \int_{-f_s/2}^{f_s/2} h_e df = h_e f_s
\]

\[
h_e = \frac{P_{e,\text{total}}}{f_s} = \frac{\Delta^2}{12 f_s}
\] (3.2)

So, as the sampling frequency increases, amplitude of spectral density decreases, but total quantization noise power \( \Delta^2/12 \) remains the same. Shown in the Figure 3-3(a) is an oversampled ADC system. Assuming the signal frequency is below \( f_B \), the quantized signal \( y(n) \) is then filtered by a low-pass digital filter \( H_d(f) \) whose frequency response is shown in Figure 3-3 (b). Power of the input signal remains the same as input signal is band-limited to \( \pm f_B \), but quantization noise power is shaped by \( H_d(f) \) as follows [1].

\[
P_e = \int_{-f_s/2}^{f_s/2} S_e(f)H_d^2(f)df
\]

\[
= \int_{-f_s/2}^{f_s/2} S_e(f)H_d^2(f)df
\]

\[
= \int_{-f_0}^{f_B} \frac{\Delta^2}{12 f_s} \cdot 1 df
\]

\[
= \frac{\Delta^2}{12 f_s} \cdot 2f_B
\] (3.3)
By comparing (2.8) and (3.4) it can be seen that quantization noise power of the oversampled ADC is $1/OSR$ times the Nyquist-rate ADC. Equation (3.4) also reveals that by doubling $OSR$, quantization noise power is halved or reduced by 3 dB.

Assuming a full-scale sinusoidal input with peak-to-peak amplitude equal to $V_{REF}$. Maximum signal power is then:

$$P_S = \left(\frac{V_{REF}}{2\sqrt{2}}\right)^2 = \left(\frac{\Delta 2^N}{2\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$$

Where (2.2) ($\Delta = \frac{V_{REF}}{2^N}$) is used in (3.5). Peak signal-to-noise ratio can now be calculated as

$$SNR_p = 10 \log \left(\frac{P_S}{P_e}\right)$$

From (3.4) and (3.5)

$$SNR_p = 10 \log \left[\frac{\Delta^2 2^{2N}}{8}\right] = 10 \log \left[\frac{12 \cdot 2^{2N} \cdot OSR}{8}\right]$$
We can see the improvement of the peak signal-to-noise ratio in (3.7) as compared to (2.9). 10 log(OSR) term is the SNR enhancement obtained from oversampling. Oversampling gives us SNR improvement of 3dB/octave or 0.5bits/octave, where 1 octave implies doubling of the sampling rate.

Note that (3.7) is only valid for full-scale input. For smaller inputs adjustment should be made to get the valid estimate.

3.2 Oversampling with noise shaping

In the straightforward approach of oversampling SNR gain is quite limited. For example, given a 4-bit bit A/D converter, using (2.9) \( SNR = 25.84 \text{dB} \). Now what sample rate is required to obtain 80 dB SNR, if \( f_B = 25k\text{Hz} \).

Increase needed in SNR is \((80 - 25.84) \approx 54\text{dB}\). From (3.7) oversampling gives 3dB/octave. So we require 54 dB divided by 3dB/octave, or 18 octaves. Thus, the required sampling rate, \( f_S \) is

\[
f_S = 2^{18} \times 2 f_B \approx 13GHz
\]

As evident from this example, a major disadvantage of straight oversampling is that the accuracy-speed trade-off is not efficient. Hence noise shaping is needed to improve the SNR faster than 3dB/octave.

3.3 ΣΔ Modulator

System architecture of ΣΔ ADC is given in the Figure 3-4. When the OSR ratio is large, anti-aliasing filter can be a simple RC lowpass filter. After passing through S/H block, ΣΔ modulator converts the analog signal into low resolution digital signal. Decimator, then filter out the out of band quantization noise and provide the high resolution signal at lower sampling rate, where \( M \leq OSR \). S/H block shown is not needed when ΣΔ ADC is realized using switched capacitor circuits, because analog signal is inherently sampled by switches and input capacitors.
The basic ΣΔ modulator in shown in Figure 3-5. Sampled input is assumed to the ΣΔ modulator. Digital to analog converter is needed as output of the modulator is a digital signal. Equivalent linear model of Figure 3-5 is shown in Figure 3-6. Using the linear model signal transfer function $H_S(z)$ from $x(n) \rightarrow y(n)$ can be written around the loop, while considering $e(n) = 0$. $k = 1$ is considered.

$$H_S(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)}$$  \hspace{1cm} (3.8)

In the same way considering $x(n) = 0$, noise transfer function $H_N(z)$ is
By superposition total output $Y(z)$ can be written such as noise and input signal being independent are modified with the respective transfer functions.

$$Y(z) = H_S(z)X(z) + H_N(z)E(z)$$  \hspace{1cm} (3.10)

### 3.3.1 First-order lowpass $\Sigma\Delta$ modulator

From (3.8) and (3.9) it is obvious that $H(z)$ should be chosen such that it has a large gain within a band of interest, so that $H_S(z)$ approaches to unity and $H_N(z)$ approaches to zero within the band of interest. Hence to realize lowpass first order noise shaping, $H_N(z)$ should have a zero at $\omega T = 0$ (i.e., $z = 1$), so that it is a high pass filter. For this $H(z)$ should have a pole at $\omega T = 0$ (or $z = 1$). For this reason loop-filter, $H(z)$ should be a discrete time integrator.

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$  \hspace{1cm} (3.11)

Block diagram of first-order $\Sigma\Delta$ modulator with discrete time integrator as a loop filter is shown in Figure 3-8. ADC as a quantizer equivalent is used in the Figure.

Using (3.11) in (3.8), signal transfer function is given by

$$H_S(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} = \frac{z^{-1}}{1 + \frac{z^{-1}}{1 - z^{-1}}} = z^{-1}$$  \hspace{1cm} (3.12)

Similarly from (3.11) and (3.9), noise transfer function is given as

$$H_N(z) = \frac{E(z)}{X(z)} = \frac{1}{1 + H(z)} = \frac{1}{1 + \frac{z^{-1}}{1 - z^{-1}}} = 1 - z^{-1}$$  \hspace{1cm} (3.13)
Figure 3-7: Loop filter, signal and noise transfer function of first-order lowpass ΣΔ modulator

\[ H(z), H_S(z) \] and \[ H_N(z) \] are plotted in Figure 3-7, where \( \pi \) represents half of the sampling frequency. It can be seen that noise passes through a first order high pass filter and signal is passed to the output of the modulator unmodified with a clock-cycle delay. This is how noise is shaped: suppressed at low frequencies, and pushed to high frequencies i.e., out of band of interest. In this way lowpass ΣΔ modulator gives high dynamic range within the band of interest, as out of the band noise at high frequencies can then be removed by digital lowpass filter.

In the time domain, the integrator integrates the difference of input and the feedback signal of the modulator. Result of the integrator is then fed to the quantizer. Negative feedback tries to minimize the difference between the input signal and the output signal of the modulator. As a result, the average of the output signal of the ΣΔ modulator is tracking the input signal.

For first-order modulator of Figure 3-8, while using one-bit ADC (2-levels), input, output signals of the ΣΔ modulator and output signal of the integrator are show in Figure 3-9. It can be seen that output of the ΣΔ modulator tracks the input signal. The benefit of 1-bit ADC is that the linearity of 1-bit ADC is assured. Since there are only two output levels, and two points define a straight line, so 1-bit ADC is inherently linear. Similar arguments applied to 1-bit DAC. Furthermore since DAC is placed outside the loop, any nonlinearity introduced by the DAC will not be corrected. Therefore the single-bit quantizer (combination of 1-bit ADC and 1bit DAC) is widely used.
Three-bit quantizer generates less quantization noise power compared to the single-bit quantizer, as shown in the Figure 3-10. As a result, the average value of the output tracks the input signal much closer than the single-bit one.
Signal-to-noise ratio of first-order $\Sigma\Delta$ modulator:

Quantization noise power over a frequency band of interest, $0 \rightarrow f_B$, can be calculated.

$$P_e = \int_{-f_B}^{f_B} S_e(f) |H_N(f)|^2$$  \hspace{1cm} (3.14)

Where $H_N(f) = H(z = e^{j\omega T}) = H(z = e^{j2\pi f/f_s})$. Using (3.13) magnitude of noise transfer function $|H_N(f)|$ is then given as:

$$H_N(f) = 1 - e^{-j2\pi f/f_s}$$
$$= e^{-j\pi f/f_s}[e^{j\pi f/f_s} - e^{-j\pi f/f_s}]$$
$$= e^{-j\pi f/f_s} \cdot 2j \cdot \sin \left( \frac{\pi f}{f_s} \right)$$

$$|H_N(f)| = 2 \sin \left( \frac{\pi f}{f_s} \right)$$  \hspace{1cm} (3.15)

Using (3.14) and (3.15)

$$P_e = \int_{-f_B}^{f_B} \left( \frac{\Delta^2}{12f_s} \right) \left[ 2 \sin \left( \frac{\pi f}{f_s} \right) \right]^2 df$$  \hspace{1cm} (3.16)

If $OSR \gg 1$ which means $f_s \gg f_B$, then $\sin(\pi f/f_s) \approx \pi f/f_s$, we get

$$P_e = \int_{-f_B}^{f_B} \left( \frac{\Delta^2}{12f_s} \right) \left( \frac{\pi f}{f_s} \right)^2 df$$

$$= \left( \frac{\Delta^2}{12f_s} \right) \left( \frac{\pi}{f_s} \right)^2 \int_{-f_B}^{f_B} f^2 df$$
Assuming maximum signal power as before, then from (3.5), (3.6) and (3.17), peak signal-to-noise ratio is given as:

\[
P_e = \frac{\Delta^2 \pi^2}{36} \left( \frac{1}{OSR} \right)^3
\]  

(3.17)

By comparing with (3.7) gain in SNR is 9 dB/octave or 1.5 bits/octave. Where, octave implies doubling of OSR.

### 3.3.2 Second-order lowpass \(\Sigma\Delta\) modulator

Second-order noise shaping can be achieved by using two integrators inside the loop such that noise transfer function is a second order high-pass function. Block diagram of second-order modulator is shown in the Figure 3-9. Simulations have shown that \(\Sigma\Delta\) modulator can be unstable when order is greater than one. Coefficient \(a_1\) and \(a_2\) are introduced to insure the stability of the modulator. Note that different types of integrators are used here. \(H_1(z)\) is the non-delayed integrator while \(H_2(z)\) has a delay element in its forward path. \(H_2(z)\) is the same as used in first-order \(\Sigma\Delta\) modulator. As we will see soon that this choice simplifies the SNR calculation quite a bit. Transfer function \(H_1(z)\) is given as
From Figure 3-11 and using (3.11) and (3.19), it can be easily shown now that signal and noise transfer functions are:

\[
H_{S}(z) = \frac{H_1(z)H_2(z)}{1 + H_1(z)H_2(z) + H_2(z)} = z^{-1} \quad (3.20)
\]

\[
H_{N}(z) = \frac{1}{1 + H_1(z)H_2(z) + H_2(z)} = (1 - z^{-1})^2 \quad (3.21)
\]

It should be noticed that for same type of integrators signal and noise transfer functions will be different than (3.20) and (3.21). However both delayed or both non-delayed integrator or any combination of them can be used in second or higher order modulators. From circuit-implementation point of view delayed integrator \((H_2(z) = H(z))\) is preferred.

**Stability of higher-order ΣΔ modulator**

Simulation results with ideal blocks for \(a_1 = a_2 = 1\) is shown in Figure 3-12. As shown that integrator outputs \(u(n)\) and \(v(n)\) grows out of bound which leads to the instability of ΣΔ modulator. Notice that the output of second integrator, \(v(n)\) is in kV. Thus to stabilize the loop, coefficient values less than one should be chosen. Simulations have shown that optimum value for coefficients is \(a_1 = a_2 = 0.5\), which is consistent with [2]. Simulation results for such choice of coefficients are shown in Figure 3.13. In this case ΣΔ modulator is indeed stable. Along with providing higher SNR, ΣΔ modulators with multi-bit quantizer are more stable than their single-bit counterpart. However ΣΔ modulator with more than one bit quantizer tends to be non-linear.
Figure 3-12: Simulation results for $\alpha_1 = \alpha_2 = 1$ of Figure 3-11

Figure 3-13: Simulation results for $\alpha_1 = \alpha_2 = 0.5$ of Figure 3-11
Signal-to-noise ratio of second-order $\Sigma\Delta$ modulator:

From (3.21), it can be shown that magnitude of noise transfer function is

$$|H_N(z)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \tag{3.22}$$

Resulting quantization noise over the band of interest is then given by

$$P_e = \frac{\Delta^2 \pi^4}{60} \frac{1}{OSR^5} \tag{3.23}$$

As in (3.5), assuming maximum signal power, peak signal-to-noise ratio is

$$SNR_p = 10 \log \left(\frac{P_s}{P_e}\right)$$

$$= 10 \log \left[\frac{\Delta^2 2^{2N}}{8 \frac{\Delta^2 \pi^4}{60}} \frac{1}{OSR^5}\right]$$

$$= 10 \log \left(\frac{3}{2} 2^{2N}\right) + 10 \log \left(\frac{5}{\pi^4}\right) + 10 \log(OSR)^5$$

$$SNR_p = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \tag{3.24}$$

SNR gain is 15 $dB$/octave or 2.5 bits/octave.

3.3.3 $n$th-order lowpass $\Sigma\Delta$ modulator

Block diagram of $n$th-order $\Sigma\Delta$ modulator is shown in the Figure 3-14. $n$th-order $\Sigma\Delta$ modulator realize $n$th-order noise-shaping by using $n$-integrators. As discussed before coefficients $a_1, a_2 ... a_n$ are introduced to insure the stability of modulator.
Figure 3-14: Block diagram of $n$th-order $\Sigma\Delta$ modulator

**Signal-to-noise ratio of $n$th-order $\Sigma\Delta$ modulator:**

Here we will obtain the generalized peak signal-to-noise ratio for $n$th-order $\Sigma\Delta$ modulator.

Using the linear model of Figure 3-14 Signal and noise-transfer function are given as

$$H_S(z) = \frac{Y(z)}{X(z)} = z^{-1}$$  \hspace{1cm} (3. 25)

$$H_N(z) = \frac{Y(z)}{E(z)} = (1 - z^{-1})^n$$  \hspace{1cm} (3. 26)

Magnitude of the noise transfer function can be calculated and is given by:

$$|H_N(z)| = \left[ 2 \sin \left( \frac{\pi f}{f_s} \right) \right]^n$$  \hspace{1cm} (3.27)

Quantization noise for $n$th order modulator over the band from 0 to $f_B$ is

$$P_e = \frac{\Delta^2 \pi^{2n}}{12(2n + 1)} \left( \frac{1}{OSR} \right)^{2n+1}$$  \hspace{1cm} (3.28)

Same as before, assuming maximum signal power, then using (3.5) and (3.28), peak signal-to-noise ratio is given as

$$SNR_P = 10 \log \left( \frac{P_s}{P_e} \right)$$
\[ \begin{align*}
\text{SNR}_p &= 6.02N + 1.76 + 10 \log \left( \frac{2n + 1}{\pi^{2n}} \right) + (2n + 1) 10 \log(\text{OSR})^{2n+1} \\
\end{align*} \]

For each doubling of \( \text{OSR} \), last term of (3.29) will be

\[ (2n + 1) 10 \log(\text{OSR}) = (2n + 1) 3 dB = (6n + 3) dB \]  (3.30)

Which means that gain in \( \text{SNR} \) is \((6n + 3) \text{dB/octave}\) or equivalently \( n + 0.5 \text{bits/octave} \).

Magnitude plots of first to forth-order noise transfer functions are plotted in Figure 3-15. As the order of the noise transfer function increases, noise at lower frequencies decreases and more noise is pushed towards higher frequencies.

Figure 3-15: Magnitude plots of first to forth-order noise transfer function
3.4 Output frequency spectrum of ΣΔ modulators

For single tone sinusoidal inputs, output frequency spectrums of first and second-order ΣΔ modulators with ideal components are plotted in Figure 3-16 and Figure 3-17 respectively. By comparing the two figures the higher slope of quantization noise can be noticed in second-order case.

Another important point that can be illustrated from the same figures is that the first-order ΣΔ modulator has much more noticeable distortion components at its output as compared to the second-order ΣΔ modulator.

Let us investigate the cause of distortions at the output of first-order ΣΔ modulator. It is interesting to note that 1-bit quantizer is inherently linear and also the components used are ideal, hence these distortions are not the harmonics of the input signal, so what is the cause of distortion? Idle tones: This phenomenon is characteristic to first order ΣΔ modulator and distortions appear at the output of the modulator are sub-multiple harmonics of the sampling frequency and are highly dependent on input signal amplitude. Due to this problem, first order lowpass ΣΔ modulator is seldom used in radio-frequency applications. Idle tone problem can be quantified by providing dc input to the modulator. Detailed discussion on this phenomenon can be found in [3, chap2].
Figure 3-17: Output-spectrum of second-order $\Sigma\Delta$ modulator with 1-bit quantizer

Figure 3-18: Dependency of idle tones in first and second-order $\Sigma\Delta$ modulator on OSR

Figure 3-18 shows the dependency of idle tone (also called limit-cycle tones) in first-order and second-order $\Sigma\Delta$ modulator on OSR [4]. As the OSR increases
magnitude of tones decreases. Doubling of OSR decreases the idle tones by 6dB for first-order modulator and 12dB for second-order modulator.
Chapter 3: Principle of ΣΔ ADC

3.5 Bibliography


[3]. R. Schreier and Gabor C. Temes, Understanding Delta-Sigma Data Converters, IEE Press.

Chapter 4

Design of Passive $\Sigma \Delta$ ADC with Sampling Mixer inside the loop

In section 1.5 we have motivated the need for passive lowpass $\Sigma \Delta$ ADC. As the input and sampling frequency of $\Sigma \Delta$ ADC increases, requirement specification on blocks used to realize $\Sigma \Delta$ ADC become harder to meet. In the switch capacitor realization of $\Sigma \Delta$ ADC, op-amp gain, bandwidth/settling time and unity gain frequency are very important specifications. Bandwidth of the op-amp should be at least five times greater than the highest frequency component of the input signal [1]. Settling time of the op-amp should be small enough so that it can sample the correct value within $T_S/2$, where $T_S$ is the sampling period. Settling time within the range $1.5(T_S/2) < \tau \leq 4(T_S/2)$ will introduce gain error which can be tolerated in many applications. However for $\tau > 4(T_S/2)$, either gain error introduced is not tolerable or op-amp simply is not able to sample the settled value. With enormous need for higher and higher frequencies there is indeed a demand for alternate switched $\Sigma \Delta$ ADC topology.

Op-amp used in switch capacitor integrator is the major cause of power consumption in the $\Sigma \Delta$ ADC. One approach to reduce the power consumption is to realize the passive loop-filter for discrete time $\Sigma \Delta$ ADC. In this approach op-
amp is removed and integrator is realized as RC equivalent filter. This approach is used in [1] and low to moderate SNR is achieved with major reduction in power consumption. As this approach removes op-amp from the structure, it is very attractive for high frequency switch capacitor ΣΔ ADCs. In this chapter we will explain the design procedure for RF sampling lowpass passive ΣΔ ADC based on this approach. We have used the $f_{RF}$ up to 4GHz with the desired band of 20MHz, and using sub-sampling, sampling frequency $f_S \leq 4GHz$ is used. The oversampling ratio in this case is $OSR = f_S/2f_B = (4 GHz)/(40 MHz) = 100$. We have then simulated our designed ΣΔ ADC at circuit level in 90nm CMOS process.

4.1 Passive ΣΔ ADC with first-order loop-filter

Block diagram of 1-bit passive ΣΔ ADC with S/H is shown in Figure 4-1 (a). Operation of this ΣΔ ADC is the same as the active counterpart, except loop-filter does not have any gain now. Large loop gain is provided by the 1-bit ADC (comparator), which is required to suppress the quantization noise. Linear model of this modulator is given in Figure 4-1 (b). $e(n)$ is the quantization noise and $G$ is the equivalent gain factor of the 1-bit ADC.

![Figure 4-1](image_url)

Figure 4-1: (a) Block diagram of a passive ΣΔ ADC with 1-bit quantizer (b) equivalent linear model
Note that in Chapter 3 we have assumed $G = 1$. For passive $\Sigma\Delta$ ADC $G$ becomes very important. Since $\Sigma\Delta$ modulator is a non-linear system and furthermore, because gain is not defined for 1-bit quantizer, $G$ can only be determined from simulation. We will extract the equivalent comparator gain from simulation in later part of this Chapter. $G$ here is assumed to be constant and is usually on the order of thousands.

From the linear model we can write the signal and quantization noise transfer function $H_S(z)$ and $H_N(z)$ respectively as

$$H_S(z) = \frac{Y(z)}{X(z)} = \frac{G H(z)}{1 + G H(z)} \approx 1$$  \hspace{1cm} (4.1)

$$H_N(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + G H(z)} \approx \frac{1}{G H(z)}$$  \hspace{1cm} (4.2)

Where we have assumed $G \gg 1$.

### 4.1.1 First-order loop filter design

Schematic diagram of first-order continuous time passive RC filter is shown in Figure 4-2. Transfer function in frequency domain and -3dB frequency of this filter is

$$H(j\omega) = \frac{1}{1 + j\omega R_1 C_1} = \frac{1}{1 + j \left( \frac{\omega}{\omega_{-3dB}} \right)}$$  \hspace{1cm} (4.3)

$$f_{-3dB} = \frac{1}{2\pi R_1 C_1}$$  \hspace{1cm} (4.4)

There are five methods to realize a resistor in switched capacitor circuits [2, chap9].

![Figure 4-2: Schematic of first-order RC filter.](image)
Three different realizations of switched capacitor resistors are shown in Figure 4-3. \( \phi_1 \) and \( \phi_2 \) are two non-overlapping clocks with frequency equal to \( f_S \). Equivalent resistance for (a) and (b) can be shown to be equal to \( 1/f_S C_R \), and for (c) \( R = -1/f_S C_R \). We will use the negative switched capacitor transresistor in realizing switched capacitor loop filter. As we will see later that the use of negative switched capacitor transresistor simplifies the feedback addition in \( \Sigma\Delta \) ADC and most importantly it easily allows the merging of S/H circuit with the loop filter.

Using the circuit in Figure 4-3 (c) switched capacitor equivalent of the continuous-time passive RC filter along with non-overlapping clocks is shown in Figure 4-4. We can find the transfer function of this filter by analyzing the circuit in time domain during each phase period (\( \phi_1 \) and \( \phi_2 \)). Starting with \( \phi_1 \) phase during the time interval from \( t - \tau \) to \( t \). Figure 4-5 (a) is the equivalent of Figure 4-4 (a) during this time interval. At the end of this time interval i-e at time \( t \) \( C_{R_1} \) is charged to \( v_{\text{in}}(t) \). However \( C_1 \) remains at the voltage, it was charged at the end of previous interval, which is \( v_{\text{out}}(t - \tau) \). Figure 4-5 (b) shows the equivalent of the Figure 4-5 (a), where voltage across \( C_1 \) is represented by a \( v_{\text{out}}(t - \tau) \) source and \( C_1 \) is shown as uncharged capacitor.
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Figure 4-5: (a) Equivalent circuit of Figure 4-4 (a) during time interval from $t - \tau$ to $t$
(b) simplified equivalent of (a)

Because $C_1$ is uncharged, then

$$v_{out}(t) = v_{out}(t - \tau) \quad (4.5)$$

Now consider the next clock phase, $\phi_2$ during the time interval from $t$ to $t + \tau$. Equivalent circuit of Figure 4-4 (a) during this period is shown in Figure 4-6. $C_{R1}$ with its previous voltage $v_{in}(t)$ is connected in parallel with $C_1$ which has the voltage given by (4.5). Then the output of Figure 4-6 can be expressed as the superposition of two voltage sources $v_{in}(t)$ and $v_{out}(t)$.

$$v_{out}(t + \tau) = -\left(\frac{C_{R1}}{C_{R1} + C_1}\right)v_{in}(t) + \left(\frac{C_1}{C_{R1} + C_1}\right)v_{out}(t) \quad (4.6)$$

Advancing (4.5) by one full period gives

$$v_{out}(t + 2\tau) = v_{out}(t + \tau) \quad (4.7)$$

Using (4.7) into (4.6) yields the result as

$$v_{out}(t + 2\tau) = -\left(\frac{C_{R1}}{C_{R1} + C_1}\right)v_{in}(t) + \left(\frac{C_1}{C_{R1} + C_1}\right)v_{out}(t) \quad (4.8)$$

Applying z-transform on both sides of (4.8), we get

Figure 4-6: Equivalent circuit of Figure 4-4 (a) during the time interval from $t$ to $t + \tau$
Writing (4.9) in a transfer function form gives

\[
H(z) = \frac{v_{out}(z)}{v_{in}(z)} = -\frac{\left(\frac{C_{R1}}{C_{R1} + C_1}\right)}{z - \left(\frac{C_1}{C_{R1} + C_1}\right)}
\]

\[
= -z^{-1}\left(\frac{C_{R1}}{C_{R1} + C_1}\right)
\]

\[
= -\frac{z^{-1}}{1 - z^{-1}\left(\frac{C_1}{C_{R1} + C_1}\right)}
\]

\[
= -\frac{z^{-1}}{1 + \frac{C_1}{C_{R1}} - \frac{C_1}{C_{R1}}z^{-1}}
\]

\[
H(z) = -\frac{1}{1 + \alpha - \alpha z^{-1}}
\]  \( (4.10) \)

Where \( \alpha = \frac{C_1}{C_{R1}} \).

Frequency response of (4.10) is required and can be found by substituting \( z = e^{j\omega T} \)

\[
H(e^{j\omega T}) = -\frac{e^{-j\omega T}}{1 + \alpha - \alpha e^{-j\omega T}}
\]

\[
= -\frac{1}{(1 + \alpha)e^{j\omega T} - \alpha}
\]

\[
H(e^{j\omega T}) = -\frac{1}{(1 + \alpha)\cos(\omega T) - \alpha + j(1 + \alpha)\sin(\omega T)}
\]  \( (4.11) \)

By simple manipulation we can find the magnitude response from (4.11). The final result is given as

\[
|H(e^{j\omega T})| = \frac{1}{\sqrt{1 + 2\alpha(1 + \alpha)(1 - \cos(\omega T))}}
\]  \( (4.12) \)
If we assume that $\omega T = 2\pi f_s / f_s \ll 1$, then $\cos(\omega T)$ approaches 1 and $\sin(\omega T)$ approaches $\omega T$. Substituting these approximations into frequency response of (4.11) results in

$$H(e^{j\omega T}) \approx -\frac{1}{(1 + \alpha) - \alpha + j(1 + \alpha)\omega T} = -\frac{1}{1 + j(1 + \alpha)\omega T} \quad (4.13)$$

Ignoring the minus sign and comparing (4.13) with (4.3), we can find the design parameter $\alpha$ as follows

$$\frac{\omega}{\omega_{-3dB}} = (1 + \alpha)\omega T \quad (4.14)$$

Solving for $\alpha$ gives

$$\alpha = \frac{1}{\omega_{-3dB}T} - 1 = \frac{f_s}{2\pi f_{-3dB}} - 1 \quad (4.15)$$

Similar result is obtained if equivalent resistance, $R_1 = 1/f_s C_R$ of switched capacitor circuit of Figure 4-3 (c) is used in (4.4). So $f_{-3dB}$ bandwidth of switched capacitor low pass filter of Figure 4-4 (a) is then given by

$$f_{-3dB} = \frac{f_s C_{R1}}{2\pi C_1} = \frac{f_s}{2\pi \alpha} \quad (4.16)$$

Where $\alpha = C_1/C_{R1}$ is used in (4.16). Solving for $\alpha$, we get

$$\alpha = \frac{f_s}{2\pi f_{-3dB}} \quad (4.17)$$

Note that for $f_s \gg f_{-3dB}$ (4.17) $\approx$ (4.15).

### 4.1.2 ΣΔ ADC with built-in mixer/Merging the S/H with the loop-filter

Figure 4-1 (a) is redrawn in Figure 4-7. Here switched capacitor lowpass filter of Figure 4-4 (a) is used as a loop filter.
As discussed in section 1.5, mixing function achieved by Sample and Hold (S/H) circuit can be merged with the loop filter. For RF sampling, $f_{LO} = f_S$ is used here.

Figure 4-8 (a) shows a circuit diagram of single-ended passive $\Sigma\Delta$ ADC with built in sampling mixer. We can see that mixer is now inside the loop and is merged with the loop filter. During clock phase $\phi_2$, RF signal is mixed down to baseband by the sampling mixer which is composed of two switches $S_1$ and $S_2$, and is sampled and held on capacitor $C_{R1}$. Clocking scheme for Figure 4-8 (a) is shown in Figure 4-8 (b). To achieve the bottom plate sampling $S_2$ is turned off first.

Figure 4-8: (a) Switched capacitor $\Sigma\Delta$ ADC with builtin sampling mixer (b) clocking scheme for (a)
Subtraction of the input signal and DAC output is achieved by sampling the input signal onto capacitor $C_{R1}$ in phase $\phi_2$ and then the sampling the complement of the output i.e $\tilde{y}(n)$ on $C_{R1}$ in the other clock phase, $\phi_1$.

**Noise transfer function**

Using (4.2) and (4.10), expression for noise-transfer function is given as

$$H_N(z) = \frac{1}{GH(z)} = \frac{1 + \alpha - az^{-1}}{Gz^{-1}}$$  \hspace{1cm} (4.18)

Magnitude transfer function of (4.18) can be obtained by using $z = e^{j\omega T}$ and then taking absolute on both sides. Final result is given below.

$$|H_N(e^{j\omega T})| = \sqrt{1 + 2\alpha(1 + \alpha)(1 - \cos(\omega T))} \frac{1}{G}$$  \hspace{1cm} (4.19)

For the bandwidth, $f_{-3dB} = 10 \text{MHz}$ and the sampling frequency, $f_s = 2 \text{GHz}$, using (4.15) design parameter $\alpha$ is obtained as

$$\alpha = \frac{C_1}{C_{R1}} = \frac{2 \times 10^9}{2\pi \times 10 \times 10^6} - 1 = 30.83 \approx 30$$  \hspace{1cm} (4.20)

For $\alpha = 30$, $f_{-3dB} = 10.61 \text{MHz}$. For $\alpha = 30$ magnitude plots of lowpass filter and noise transfer function using (4.12) and (4.19) respectively are plotted in the Figure 4-9. Equivalent gain $G = 100$ is assumed here for 1-bit ADC. We will see in simulation results that G is even larger than 100. X-axis in this plot is normalized frequency axis. Here 0.0053 corresponds to $f_{-3dB} = 10.61 \text{MHz}$. At DC magnitude of $H(z)$ is 1 while magnitude of $H_N(z)$ is $1/G = 0.01$. Comparing with ideal integrator case $H_N(z = 1) \neq 0$, which degrades the noise shaping at lower frequencies.

**4.1.3 The switch**

All the switches used in the circuit of the Figure 4-8 (a) are CMOS transmission gates. Dummy transistors are used for charge injection cancellation and clock feedthrough suppression [3, chap12].
Figure 4-9: Magnitude plot of low pass filter and noise transfer function using (4.12) and (4.19)

This switch is shown in Figure 4-10.

Figure 4-10: CMOS transmission gate with dummy transistors
4.1.4 Distortion in the sampling mixer

There are three main types of distortion in sampling mixer [4]. Top plate sampling mixer is shown in Figure 4-11.

1. Time invariant distortion

Time invariant distortion is mainly determined by non-linear on-resistance \((R_{ON})\) of the MOS transistor. For this type of distortion expressions for HD2, HD3 and IM2 and IM3 are given below.

\[
HD_2 = \frac{V_{RF}}{2} \frac{j\omega_{RF}C}{k(V_G - V_t)^2}, \quad HD_3 = \frac{V_{RF}^2}{4} \frac{j\omega_{RF}C}{k(V_G - V_t)^3}
\]

\[
IM_2 = 0, \quad IM_3 = \frac{V_{interf}^2}{4} \frac{j\omega_{RF}C}{k(V_G - V_t)^3}
\]

Where \(k = \mu_0 C_{ox} W/L\).

2. Non-uniform sampling distortion

The instance of sampling in the sampling mixer occurs when \((V_{GS} - V_t) = 0\), so the time at which sampling occurs does not only depends on gate voltage but also on the input voltage. This introduces distortion. Expressions for this type of distortion given in [4] are

\[
HD_2 = \frac{V_{RF}}{4} \frac{j\omega_{RF}T_f}{V_G}, \quad HD_3 = \frac{3V_{RF}^2}{32} \left(\frac{\omega_{RF}T_f}{V_G}\right)^2
\]

\[
IM_2 = 0, \quad IM_3 = \frac{V_{interf}^2}{32} \left(\frac{\omega_{RF}T_f}{V_G}\right)^2
\]
Where $T_f$ is the finite, local oscillator (LO) waveform fall time. LO waveform with $T_f$ is also shown in Figure 4-11.

3. Time varying distortion

Time varying distortion is studied with arbitrary LO waveform. This type of distortion is not relevant in our case. We will refer the interested reader to [4] for the discussion of this type of distortion.

Non-uniform sampling distortions are mainly due to finite $T_f$. We assume here that clock with small enough $T_f$ can be used such that non-uniform sampling distortions are ignorable.

We are mostly interested in time invariant distortions. $HD_2$ can be suppressed by using differential structures, $IM_2 = 0$, so we will only concentrate on $HD_3$ and $IM_3$. (4.21) and (4.23) shows that these two types of distortions are directly proportional to the sampling capacitor ($C$) and the input frequency ($\omega_{RF}$), and inversely proportional to the size of the transistor ($W$) used to realize the switch. Sampling capacitor can be chosen from the thermal noise requirements and then the size of the switch can be determined from one of the expression. However for the input frequency of 2 GHz, expressions (4.21) and (4.23) results in very huge transistor sizes which are impractical to use. Furthermore simulation shows that with such huge sizes of the transistors, mixer distortion performance is degraded rather than improved. This is because for switch sizes larger than certain value gives rises to the non-linear effects of parasitic capacitances which then dominates the distortions which were initially due to the non-linear on-resistance ($R_{ON}$) of the transistor.

4.1.5 Fully differential passive $\Sigma\Delta$ ADC with first-order loop filter

In this section we will complete the design of our fully differential passive $\Sigma\Delta$ ADC with mixer inside the $\Sigma\Delta$ modulator loop using first-order loop filter. This design is simulated in 90nm CMOS technology.

Noting the dependency on RF frequency and sampling capacitor from (4.21) and (4.22), using simulation with ideal switches, size of the sampling capacitor $C_{R1}$ in the Figure 4-8 (a), is chosen as 100fF. Design parameter $\alpha = 30$ is already obtained in (4.20). Using the relation $\alpha = C_1/C_{R1}$, $C_1 = 3pF$. Again using simulation, suitable switch sizes are obtained. Differential implementation of our passive $\Sigma\Delta$ ADC is shown in the Figure 4-12.
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Figure 4-12: Fully differential switched capacitor ΣΔ ADC with built-in sampling mixer using first-order loop filter.

Design parameters $C_1$, $C_{R1}$ and $S_1, S_2, S_3, S_4$ and $S_5$ (transistor widths) for the circuit of Figure 4-12 are tabulated in Figure 4-13 (a) and (b) respectively. Here $S_{i,N}$ and $S_{i,P}$ are the sizes of NMOS and PMOS transistors in the transmission gate. Sizes of the switches which sample the input RF signal are very crucial. Distortion created by these switches will be propagated throughout the loop. For this reason $S_1$ is chosen larger than the other switches. On the other hand $S_1$ should be kept small enough such that parasitic capacitances of the MOS transistor should not dominate the overall distortion.

<table>
<thead>
<tr>
<th>$f_s = 2 \text{ GHz, OSR} = 100$</th>
<th>Switch Sizes</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC Version</td>
<td>SC Version</td>
</tr>
<tr>
<td>$f_{-3dB} = 10.61 \text{ MHz}$</td>
<td>$f_{-3dB} = 10.61 \text{ MHz}$</td>
</tr>
<tr>
<td>$R_1 = 5 \text{ k}\Omega$</td>
<td>$C_{R1} = 100fF$</td>
</tr>
<tr>
<td>$C_1 = 3pF$</td>
<td>$C_1 = 3pF$</td>
</tr>
</tbody>
</table>

Figure 4-13: Design parameters for the circuit of the Figure 4-12
For multi-bit DAC, linearity of switches $S_4$ and $S_5$ are also very important. Distortion performance of $\Sigma\Delta$ ADC of Figure 4-12 can be improved if $S_1$ is realized as a boot-strapped switch.

$V_{REF+} = V_{dd}$ and $V_{REF-} = 0\,V$ are the high and low reference voltages respectively for the DAC. This gives full-scale voltage for the DAC, $V_{FS} = V_{dd}$. Common mode voltage, $V_{CM} = V_{dd}/2$ is added to the circuit so that input to the comparator should stay at the DC level of $V_{dd}/2$.

1-bit ADC block shown in the Figure 4-12 is an ideal comparator. Ideal Verilog-A model is used for this block. Full-scale voltage for the ADC ($V_{FS}$) is also equal to $V_{dd}$. Trip point for this comparator is $V_{dd}/2$. Output of the comparator is a digital signal which has logic-high voltage = $V_{dd}$ and logic-low voltage = $0\,V$. $V_{dd}$ in 90nm CMOS process is 1.2 V. Programming model of the comparator is given in the Appendix B.

### 4.1.6 Equivalent gain (G) of the 1-bit ADC

The equivalent comparator gain can be identified by the comparison of the SDM linear model and the frequency response obtained by simulation of the model with a switching comparator. Output frequency spectrum from DC upto approximately $f_s/2$ is shown in Figure 4-14. This plot is obtained by using ideal switches and the parameter values ($f_s = 2GHz$, $f_{RF} = 2.0011GHz$, $C_{R1} = 10fF$ and $C_1 = 2pF$) in the circuit of the Figure 4-12.

From (4.2) the transfer function for the quantization noise is given as

$$H_N(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + GH(z)}$$

We can compare the $H_N(z)$ with the simulated noise response of the Figure 4-14, while assuming the unshaped quantization noise is white.

From simulation the difference between noise levels at high and low frequency is $\Delta P \approx 44dB$, we find:

$$20 \log(1 + GH(f_{low})) - 20 \log(1 + GH(f_{high})) = \Delta P = 44dB \quad (4.25)$$

For a passive loop filter, ideally we can assume $H(f_{low}) = 1$ and $H(f_{high}) = 0$. Hence, the approximate estimate of $G$ follows:
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Figure 4-14: Output frequency spectrum of Figure 4-12, plotted for finding the equivalent gain $G$ of the 1-bit ADC.

\[ 20 \log G = \Delta P = 44 \]  \hspace{2cm} (4.26)

Solving for $G$, result in

\[ G = 10^{2.2} = 160 \]  \hspace{2cm} (4.27)

Equivalent gain $G$ of the comparator is smaller than expected. $G$ is also dependent on the bandwidth of the loop filter [1].

4.1.7 Simulation Results

$\Sigma\Delta$ ADC in Figure 4-12 is simulated in 90nm CMOS process. Parameters tabulated in Figure 4-13 are used for these simulations. Figure 4-15 shows the output spectrum of our $\Sigma\Delta$ ADC over the desired bandwidth of 10 MHz.
Figure 4-15: Simulation results for the ΣΔ ADC of Figure 4-12.

Input RF signal amplitude, \( V_{RF} \) is 300 mV and the RF frequency, \( f_{RF} \) is 2.0011 GHz \( (2 \text{ GHz} + 1.1 \text{MHz}) \). Clock frequency \( f_S = 2 \text{ GHz} \) is used.

For our downconverting ΣΔ ADC we should expect the mixed-down signal at \( f_{RF} - f_S = 1.1 \text{ MHz} \). This is shown in the Figure 4-15. Note that second-order distortion components \( I_{D2} \) are suppressed due to differential structure. On the other hand we have noticeable third-order distortion \( HD_3 \) which degrades the SINAD of the ΣΔ ADC and hence achievable ENOB. These distortion components are mainly due to the mixer, sampling the RF signal.

From (4.21) we see that for a given frequency, distortions \( HD_3 \) can be reduced by increasing the sampling switch size \( S_1 \). Switch sizes tabulated in the Figure 4-13 are optimized sizes obtained by simulation. We observed that switch sizes larger than given in Figure 4-13 give rise to non-linear effects of the MOS parasitic capacitances which dominates the overall distortion.
From (4.21), distortions created in the sampling mixer are also proportional to the sampling capacitor $C_R$. So using simulation it is seen that for $C_{R1} = 10 fF$ and $C_1 = 3 pF$ (same as before) resulted in minimum $HD_3$ in this case. Simulation results with $V_{RF} = 200 mV$ are shown in Figure 4-16. We can see that distortions are now suppressed to much extent.

However there are two potential problems with using such a small capacitor value for $C_R$. First; the smaller capacitor value like one we have used can very easily expose to large process variations which does not guarantee the expected result from the fabricated chip in most of the cases. Second; $kT/C$ noise generated with this capacitor value will dominate the quantization noise. Which means that, contrary to our assumption, the quantization noise will not be the only dominant source of noise in our $\Sigma\Delta$ ADC. This issue is discussed later in this Chapter.

This should be noted that $SNR_p$ expressions derived in Chapter 3 are not the valid $SNR_p$ approximations for the passive $\Sigma\Delta$ ADC. Estimate for $SNR_p$ should
be re-evaluated in this case. Due to the unavailability of suitable model for SNR, we mostly relied on simulation.

4.2 Passive $\Sigma\Delta$ ADC with second-order loop-filter

In this section we will design the passive $\Sigma\Delta$ ADC with second-order loop-filter. Note that this is not the second-order $\Sigma\Delta$ ADC but the loop filter used is a second-order filter. However, as we will see in the simulation results that, though gain in SNR is not quite enough, but distortion performance is substantially improved.

The reason for distortion performance improvement can be supported from Figure 3-18 where we have seen that for the given OSR, limit cycle tones are 12 dB less in second-order $\Sigma\Delta$ modulator than first-order $\Sigma\Delta$ modulator. Simulation showed that this is also true to some extent for passive $\Sigma\Delta$ ADC with second-order loop filter.

4.2.1 Second-order loop filter design

Second-order continuous-time passive RC filter is shown in Figure 4-17. In [5] it is assumed that the two sections of this filter do not have any loading effect on one another. Using the assumption, only second RC section of the filter need to be designed. For $R_2$ we have used the switched capacitor equivalent of the Figure 4-3 (a) (shunt switched capacitor resistor). Using the first section same as in Figure 4-4, final second-order switched capacitor equivalent of Figure 4-17 is shown in Figure 4-18.

Using the approach given in section 4.1.1 transfer function for the second RC section of the Figure 4-18 can be obtained as

$$H(z) = \frac{z^{-1} \left( \frac{C_{R2}}{C_{R2} + C_2} \right)}{1 - z^{-1} \left( \frac{C_2}{C_{R2} + C_2} \right)} = \frac{z^{-1}}{1 + \beta - \beta z^{-1}}$$ (4.28)

![Figure 4-17: Second-order RC lowpass filter](image_url)
Where, we have used $\beta = C_2 / C_{R2}$ in (4.28). Similar to (4.17) design parameter $\beta$ can be obtained using the relation

$$\beta = f_s / 2\pi f_{-3dB}$$  \hspace{1cm} (4.29)

Note that transfer function for the second RC section and transfer function for the first RC section are the same except that (4.28) is non-inverting. It can be seen that two sections in the circuit of Figure 4-18 are not completely interacting.

For -3dB bandwidth of 15 MHz $\beta = 2$ is obtained from (4.29). Choosing $C_{R2} = C_{R1} = 100 fF$, results in $C_2 = \beta \times C_{R2} = 2.1 fF$.

### 4.2.2 Fully differential passive $\Sigma\Delta$ ADC with second-order loop filter.

Circuit diagram of fully differential passive $\Sigma\Delta$ ADC with second-order loop filter is shown in Figure 4-19. This is our final design of passive switched capacitor $\Sigma\Delta$ ADC with mixer inside the modulator loop. Loop-filter has two poles at $p_1 = 10.6 MHz$ and at $p_2 = 15 MHz$. Design parameters for the circuit of Figure 4-19 are tabulated in Figure 4-20.

### 4.2.3 Simulation results

Simulation results for $f_{RF} = (2.0011, 3.0011, 4.0033) GHz, V_{RF} = 200 mV$ and $f_s = (2, 3, 4) GHz$ are shown in Figure 4-21 to Figure 4-23. By comparing these results with the Figure 4-15, we see that higher SNR is achieved with second-order loop filter. Furthermore using the same capacitor values of $C_{R1} = 100 fF$ and $C_1 = 3 pF$ in the first section of the second-order loop filter, distortion performance in Figure 4-21 is better than the Figure 4-15. As we discussed before that larger capacitor values are desired to reduce the $kT/C$ noise.
Figure 4-19: Fully differential switched capacitor ΣΔ ADC with built-in sampling mixer using second-order loop filter.

\[
\begin{align*}
V_{\text{ref}^-} & \quad V_{\text{ref}^+} \\
\bar{y}(n) \omega_1 & \quad s_1 \quad s_3 \quad y(n) \omega_1 \\
v_{\text{in}^+}(t) & \quad s_1 \quad \phi_2 \\
\phi_1 & \quad C_{R1} \\
\phi_2 & \quad s_2 \quad \phi_2 \omega_1 \\
C_{CM} & \quad s_2 \quad \phi_2 \omega_1 \\
v_{\text{in}^-}(t) & \quad s_1 \quad \phi_2 \\
\phi_1 & \quad C_{R1} \\
\phi_2 & \quad s_2 \quad \phi_2 \omega_1 \\
C_{CM} & \quad s_2 \quad \phi_2 \omega_1 \\
\bar{y}(n) \omega_1 & \quad s_1 \quad y(n) \omega_1 \\
V_{\text{ref}^+} & \quad V_{\text{ref}^-} \\
V_{\text{ref}^+} = V_{dd}, & \quad V_{\text{ref}^-} = 0 \text{ V} \\
V_{CM} = V_{dd}/2, & \quad V_{dd} = 1.2 \text{ V}
\end{align*}
\]

Figure 4-20: Design parameters for the circuit of Figure 4-19.

<table>
<thead>
<tr>
<th>Switch Sizes</th>
<th>RC Version</th>
<th>SC Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>(S_{1,N})</td>
<td>(S_{1,P})</td>
<td>10 (\mu)m</td>
</tr>
<tr>
<td>(S_{2,N})</td>
<td>(S_{3,N})</td>
<td>35 (\mu)m</td>
</tr>
<tr>
<td>(S_{5,N})</td>
<td>(S_{6,N})</td>
<td>7 (\mu)m</td>
</tr>
<tr>
<td>(S_{7,N})</td>
<td>(S_{2,P})</td>
<td>25 (\mu)m</td>
</tr>
<tr>
<td>(S_{3,P})</td>
<td>(S_{4,P})</td>
<td></td>
</tr>
<tr>
<td>(S_{5,P})</td>
<td>(S_{6,P})</td>
<td></td>
</tr>
<tr>
<td>(S_{7,P})</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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Figure 4-21: Simulation results for the circuit of Figure 4-19, $f_S = 2$ GHz

- $f_{RF} = 2.0011$ GHz.
- $V_{RF} = 200$ mV.
- $f_S = 2$ GHz.
- $C_{R1} = 100 \, \text{fF}$, $C_1 = 3 \, \text{pF}$.
- $C_{R1} = 100 \, \text{fF}$, $C_2 = 2.1 \, \text{pF}$.

Figure 4-22: Simulation results for the circuit of Figure 4-19, $f_S = 3$ GHz

- $f_{RF} = 3.0011$ GHz.
- $V_{RF} = 200$ mV.
- $f_S = 3$ GHz.
- $C_{R1} = 100 \, \text{fF}$, $C_1 = 3 \, \text{pF}$.
- $C_{R1} = 100 \, \text{fF}$, $C_2 = 2.1 \, \text{pF}$.
Figure 4-23: Simulation results for the circuit of Figure 4-19, $f_s = 4 \text{ GHz}$

Figure 4-24: Simulation results for the circuit of Figure 4-19, subsampling, $f_s = 1 \text{ GHz}$
Figure 4-25: Simulation results for the circuit of Figure 4-19, subsampling, $f_S = 1.5$ GHz

Figure 4-26: Simulation results for the circuit of Figure 4-19, subsampling, $f_S = 2$ GHz
Simulation results for the sub-sampling case are shown in Figure 4-24 to Figure 4-26. RF signal amplitude $V_{RF} = 200 \, mV$ is used in all cases. Bandwidth to analyze is adjusted for different cases to keep the OSR = 100. Summary of simulation results for ΔΣ modulator with second-order loop filter is tabulated in Figure 4-27. We see that this architecture is capable to operate for a range of clock frequency values (upto 4 GHz).

<table>
<thead>
<tr>
<th>Sampling Cases</th>
<th>S/N</th>
<th>$f_{RF}$ (GHz)</th>
<th>$f_s$ (GHz)</th>
<th>BW (MHz)</th>
<th>OSR</th>
<th>SINAD (dB)</th>
<th>SNR (dB)</th>
<th>ENOB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseband sampling</td>
<td>1</td>
<td>0.0099</td>
<td>2</td>
<td>10</td>
<td>100</td>
<td>51.0</td>
<td>51</td>
<td>8.2</td>
</tr>
<tr>
<td>RF sampling</td>
<td>2</td>
<td>4.0033</td>
<td>4</td>
<td>20</td>
<td>100</td>
<td>51.8</td>
<td>52.5</td>
<td>8.3</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>3.0011</td>
<td>3</td>
<td>15</td>
<td>100</td>
<td>51.5</td>
<td>52.2</td>
<td>8.3</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>2.0011</td>
<td>2</td>
<td>10</td>
<td>100</td>
<td>53.2</td>
<td>53.2</td>
<td>8.5</td>
</tr>
<tr>
<td>RF sub-sampling</td>
<td>5</td>
<td>2.00055</td>
<td>1</td>
<td>5</td>
<td>100</td>
<td>50.3</td>
<td>50.3</td>
<td>8.1</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>3.0011</td>
<td>1.5</td>
<td>7.5</td>
<td>100</td>
<td>51.4</td>
<td>51.4</td>
<td>8.3</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>4.0033</td>
<td>2</td>
<td>10</td>
<td>100</td>
<td>51.4</td>
<td>51.9</td>
<td>8.3</td>
</tr>
</tbody>
</table>

Figure 4-27: Summary of simulation results for the circuit of Figure 4-19.

4.3 Circuit Noise Estimation for Passive ΣΔ ADC

Thermal noise is not taken into account for the simulations performed. However with simple model it can be shown that Passive ΣΔ ADC of the Figure 4-19 is thermal noise limited instead of quantization noise limited [5]. Figure 4-28 shows the noise analysis for the circuit given in Figure 4-19. Here switched capacitors are replaced with their equivalent resistors and their control phases ($\phi_1$ and $\phi_2$) are shown on top of the associated resistors. There are two thermal noise sources in the model, $V_{n,H1}$ from the first section of the second-order loop filter and $V_{n,H2}$ from the second section of the second-order loop filter.

Two sections of the loop filter are separated with the dashed vertical line in the figure. Expressions for the $V_{n,H1}$ and $V_{n,H2}$ can be obtained by analyzing the circuit in Figure 4-28 in two clock phases ($\phi_1$ and $\phi_2$). $V_{n,H1}$ has the following transfer function:

$$V_{n,H1}^2 = V_{n1}^2 + V_{n2}^2 = \frac{kT}{C_{R1}} + \frac{kT}{C_{R1}(C_{R1} + C_1)/C_1}$$ (4.30)
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Figure 4-28: Thermal noise model of passive ΣΔ ADC of the Figure 4-19

Noise terms \( V_{n1} \) and \( V_{n2} \) represent noises generated during \( \phi_1 \) and \( \phi_2 \) respectively. Similarly for the second section of the second loop filter, \( V_{n,H2} \) can be obtained as

\[
V_{n,H2}^2 = V_{n3}^2 + V_{n4}^2 = \frac{kT}{C_{R2}(C_{R2} + C_1)/C_1} + \frac{kT}{C_{R2}(C_{R2} + C_2)/C_2} \quad (4.31)
\]

Estimate of thermal noise can be obtained by calculating \( V_{n1}^2 \) only. Using \( C_{R1} = 100 fF \) from the Figure 4-19 \( V_{n1}^2 \) is

\[
V_{n1}^2 = \frac{kT}{C_{R1}} = \frac{1.381 \times 10^{-23} \times 273}{100 \times 10^{-15}} = 3.77 \times 10^{-8} \Rightarrow -74.23 \text{ dB} \quad (4.32)
\]

If we assume 50 Ω matching then signal power for peak RF signal of \( V_{RF,p} = 200 \text{ mV} \) is given as

\[
P_s = \frac{(V_{RF,p})^2}{\sqrt{2} R} = \frac{(0.2)^2}{\sqrt{2} \times 50} = 400 \mu W \Rightarrow -33.98 \text{ dB} \quad (4.33)
\]

From (4.32) and (4.33) SNR is 40.25 dB. This SNR is calculated with only input sampling capacitor \( C_{R1} \). All the further stages will degrade the SNR even more.

Hence for better thermal noise performance large capacitor values should be chosen. Specially capacitors \( C_{R1} \) and \( C_{R2} \) should be made large.
4.4 Bibliography


Chapter 5

Conclusions and Future Prospects

5.1 Conclusions

This thesis demonstrates that IF sampling by lowpass ΣΔ ADC, proposed in [1] can be extended to radio frequencies (upto 4 GHz). In this report we have shown that it is possible to sample a RF signal by using passive lowpass ΣΔ ADC. Passive switched capacitor ΣΔ ADC with mixer inside the modulator loop is successfully implemented in 90nm CMOS process at the circuit level. Firstly, for a 2 GHz RF signal with the bandwidth of 10 MHz while using the sampling frequency of 2 GHz (OSR = 100) a passive lowpass ΣΔ ADC with the first-order loop filter is designed. We have seen that the downconverted signal at the output of the lowpass ΣΔ ADC with the first-order loop filter is not free from distortion. By taking motivation from [2], to improve the noise and distortion performance a lowpass ΣΔ ADC with second-order loop filter is then designed. It is observed that by using the second-order loop filter, downconverted signal at the output of the lowpass ΣΔ ADC has much improved signal-to-noise-and-distortion ratio (SINAD). With 4 GHz clock and using 1bit quantizer, SINAD of 51.8 dB and SNR of 52.5 dB are achieved. This SNR value is a good number for a passive ΣΔ ADC. Comparing SINAD and SNR shows a high linearity of this ADC. This ΣΔ ADC is flexible and can handle sub-sampling. For a RF signal of 4GHz and clock frequency of 2 GHz the system yields in a SINAD of 51.4 dB and SNR of 51.9 dB.
Finally we will conclude that first-order downconverting lowpass $\Sigma\Delta$ ADC is very attractive for sampling high frequency RF signals and is capable of achieving a reasonable signal-to-noise ratio for a moderate OSR. A better performance can be expected when this circuit is upgraded to make a second-order $\Sigma\Delta$ architecture.

5.2 Future Prospects

Passive $\Sigma\Delta$ ADC developed in this thesis may be capable to achieve a much larger SINAD, if some modifications are done in the architecture of the circuit in Figure 4-19. $\Sigma\Delta$ ADC shown in this figure is not a second-order $\Sigma\Delta$ ADC but only the loop filter is a second-order filter. One possible point to inject the second feedback signal is the point ‘b’ shown in the same figure. However, doing so one will introduce an interaction of the feedback signal with the sampling capacitor $C_1$ of the first section of the loop filter. A buffer can be introduced at point ‘a’ to separate the first and second section of the loop filter. For all these changes to be effective the clocking schemes shown in Figure 4-19 perhaps need to be altered. Furthermore different switched capacitor resistors (shunt, parallel, series-shunt, bilinear) can be tried, especially for the second section of the loop filter.

Since, switch $S_1$ (Figure 4-19) samples the high frequency RF signal, linearity of this switch is very important. The overall linearity will be improved, if switch $S_1$ can be linearized. A bootstrapped switch can be used in this case.

To improve the output dynamic range of $\Sigma\Delta$ ADC, multi-bit quantizer can be used. The difficulty here is that, especially at GHz frequency, multi-bit DAC in the feedback path tends to be non-linear. An approach for a highly linear DAC design should be considered in this case.

Once capacitor values are optimized, passive $\Sigma\Delta$ ADC will not give equally good performance for a large range of different clock frequencies (from the perspective of sub-sampling). -3dB bandwidth of the loop filter is directly dependent on the clock frequency. To improve the flexibility of the modulator a variable capacitor technique should be developed, such that when clock frequency is changed, bandwidth of the switched capacitor filter should not change too much. One approach can be, to use different sets of capacitors which can be connected and disconnected from the structure. This can be achieved with switches.
5.3 Bibliography


Appendix A

Matlab Codes

A.1 Matlab Codes for ADC Evaluation

A.1.1 Matlab Code for ADC Evaluation

%%%%%%%%%%%%%%%%%%%%%%
% Matlab code to evaluate an ADC, the program uses the m-files sinefit.m,
% measure_sinad.m and lowpass.m.
% The data to be evaluated has to be at least 16,000 samples long and be
% loaded from a file into the variable InData.
% 
%%%%%%%%%%%%%%%%%%%%%%

titel = ['\Sigma\Delta'];
InData = load('D:\Fahad Qazi\SDM.txt'); % Load the sequence to analyze
fsample = 2500; % Sampling frequency in MHz
fmaxband = 10; % Bandwidth to be analyzed in MHz
fIn = [1.1]; % Input frequencies, row vector in MHz
lp = lowpass(fsample, fmaxband); % Create the low-pass filter
InPow = 3;
% Section to find possible in-band harmonics and intermodulation. What is % considered in-band in this section is actually 1.1 times the maximum % frequency of the band in order to remove any spirouses with low % attenuation in the low-pass filter

% Find in-band harmonics
Dist = []; for n=1:1:5, for m=1:size(fIn,1), if fIn(m)*(2*n+1)<fmaxband*1.1, Dist = [Dist, fIn(m)*(2*n+1)]; end; end; end;

% Set maximum harmonic to be evaluate for intermodulation products
IMMax = 3;

% Find in-band intermodulation products
for n=1:1:length(fIn), for m=n+1:1:length(fIn), for k1=1:1:IMMax, for k2=1:1:IMMax, if ((k1*fIn(n)-k2*fIn(m))<fmaxband*1.1) && ((k1*fIn(n)-k2*fIn(m))>0), Dist = [Dist, k1*fIn(n)-k2*fIn(m)]; end; if ((k1*fIn(m)-k2*fIn(n))<fmaxband*1.1) && ((k1*fIn(m)-k2*fIn(n))>0), Dist = [Dist, k1*fIn(m)-k2*fIn(n)]; end; end; end; end;

% Low-pass filtering the input signal
InData = filter(lp,InData);

% Determine the number of fft points possible after at least 16,000 samples % have been discarded
FFT_Points = 2^(floor(log2(length(InData)-1)));

% Determine how many initial samples to discard
wait = length(InData)-FFT_Points;

% Determine SINAD and signal power
[SINAD,ND,rmsfIn,rmsND] = ... measure_sinad(InData(wait:length(InData)),(2*pi/fsample) *fIn);

% Fouriertransform the input including the signal to determine the signal % power
fftTot = fft(InData(wait:length(InData)),FFT_Points);
fftTot = fftTot(1:round(fmaxband*FFT_Points*1.1/fsample));
fftTot = 10*log10((fftTot.*conj(fftTot)));

% Fouriertransform the remaining signal after the input signals have been
% removed to be able to visualize the inband noise spectrum
fftND = fft(ND,FFT_Points);
fftND = fftND(1:round(fmaxband*FFT_Points*1.1/fsample));
fftND = 10*log10((fftND.*conj(fftND)))-max(fftTot);

% Create a variable for the x-data of the plot
f = fsample*(0:round(fmaxband*FFT_Points*1.1/fsample)-1)/(FFT_Points);

% If there are no spiruouses, set rmsD to 0 and rmsND to rmsN, otherwise
% determine their rms values. After this rmsIn, rmsN, rmsD and rmsND
% contains the rms values for the insignal, in-band noise, in-band
% distorsions and in-band noise + distorsions respectively
if isempty(Dist),
    rmsD = 0;
    rmsN = rmsND;
else
    % Remove the spirouses to determine SNR
    [SNR,Noise,rmsD,rmsN] = measure_sinad(ND,(2*pi/fsample)*Dist);
end;

% Set SNR to rms of the signal compared to the rms of the noise without
% spirouses
SNR = 20*log10(sqrt(sum(rmsfIn.^2))/rmsN);

% Effective number of bits is derived from SINAD
ENOB = (SINAD-1.76)/6.02;

% SFDR is the rms of the input signal compared to the rms of the in-band
% domenating frequency
SFDR = -max(fftND);

% Reset the rms value of the signal in the fouriertransformed noise
for n=1:1:length(fIn),
    fftND(round(fIn(n)*FFT_Points/fsample)+1) = ...
        fftTot(round(fIn(n)*FFT_Points/fsample)+1)-max(fftTot);
end;

% Print the calculated values on the screen
fprintf('SINAD = %1.3f dB\n', SINAD);
fprintf('SNR   = %1.3f dB\n', SNR);
fprintf('SFDR  = %1.3f dB\n', SFDR);
fprintf('ENOB  = %1.2f\n', ENOB);

% Print what harmonics have been removed to determine SNR on the screen
fprintf('Harmonics removed at: ');
fprintf('%1.1f, ',Dist);
fprintf('\n\n');

% Section to create the title of the plot with relevant information
if length(fIn)==1, titel = [titel ', f_{in}= ', num2str(fIn), ' MHz'];
else
Appendix A: Matlab Codes

```matlab
% Plot the spectrum of the input signal
fftND = fftND + InPow;
hold on
plot(f, fftND, 'k');
title(titel);
set(get(gca,'XLabel'),'String','Frequency (MHz)');
set(get(gca,'YLabel'),'String','Signal Power (dBfs)');
xlim([0 fmaxband+0.5]);
ylim([-130 0]);
grid on

A.1.2 Matlab Code for Low-pass Filter

function Hd = lowpass(Fs,Fpass)

%LOWPASS Returns a discrete-time filter object.
%Fs is the Sampling Frequency and Fpass the Passband Frequency.
% Chebyshev Type I Lowpass filter designed using the CHEBY1 function.

Apass = 0.01;          % Passband Ripple (dB)
N     = 15;            % Filter order

% Calculate the zpk values using the CHEBY1 function.
[z,p,k] = cheby1(N, Apass, Fpass/(Fs/2));

% To avoid round-off errors, do not use the transfer function. Instead
% get the zpk representation and convert it to second-order sections.
[sos_var,g] = zp2sos(z, p, k);
Hd          = dfilt.df2sos(sos_var, g);

A.1.3 Matlab Code for Measure_sinad

function [sinad,noise,rmswk,rmsn] = measure_sinad(y, wk)
%[sinad,noise,rmswk,rmsn] = measure_sinad(y, wk)
%Computes SINAD (signal to noise and distortion ratio) according to
%IEEE1241 using a three-parameter fit on the angular frequencies
%specified in wk.

N = length(y);
```
n = 1:N;
K = length(wk);

%M juris posi di 8   sio 8 0
[ m, p, o ] = sinefit(y, n, wk);

%M juris posi di 8   sio 8 0
xr = zeros(K, N);
for k = 1:K
    xr(k, :) = m(k) * cos(wk(k) * n + p(k));
end

noise = y - sum(xr, 1) - o;

%M juris posi di 8   sio 8 0
rmss = sqrt(sum(m.^2 / 2));

%M juris posi di 8   sio 8 0
rmswk = m./sqrt(2);

%M juris posi di 8   sio 8 0
rmsn = sqrt(1/N*sum(noise.^2));

%M juris posi di 8   sio 8 0
sinad = 20*log10(rmss/rmsn);

A.1.4 Matlab Code for Sinefit

function [magnitudes, phases, offset] = sinefit(y, n, wk)
% Uses a least squares fit to find the amplitudes and phases
% of the sinusoidal components of angular frequencies given
% by wk. A three-parameter fit according to IEEE STD1241 Sec.
% 4.1.4.1 is performed.
% y is a row vector containing data samples
% n is a row vector containing the sample indeces
% wk is the set of angular frequencies of the sinusoids
% The component k is given by
% xk = magnitudes(k) * cos(wk(k) * n + phases(k))
% The residual of the fit is given by
% x = y - sum of xk - offset
% [magnitudes, phases, wk, offset] = sinefit(y, n)
% Performs a four-parameter fit according to IEEE STD1241 Sec.
% 4.1.4.3. Not implemented.

N = length(n);
K = length(wk);

% Build D0
D0 = zeros(N, 2*K+1);
for k = 1:K
    D0(:, 2*k-1) = cos(wk(k)*n)';
    D0(:, 2*k) = sin(wk(k)*n)';
end
D0(:, 2*K+1) = ones(N, 1);

% Compute the least squares fit x0
x0 = (D0'*D0)\(D0'*y');

% Extract the magnitudes
for k = 1:K
    magnitudes(k) = sqrt(x0(2*k-1)^2 + x0(2*k)^2);
end

% Extract the phases
for k = 1:K
    if x0(2*k-1) < 0
        phases(k) = atan(-x0(2*k)/x0(2*k-1)) + pi;
    else
        phases(k) = atan(-x0(2*k)/x0(2*k-1));
    end
end

% Extract the offset
offset = x0(2*K+1);

A.2 Matlab Code for the Plots of Figure 3-15

Fs = 1;
f = 0:0.01:Fs/2;
y = 2* sin((pi*f)/Fs);

% First Order Noise Shaping
y1 = y;
plot(f,y1)
hold on

% Second Order Noise Shaping
y2 = y.^2;
plot(f,y2,'r')
hold on

% Third Order Noise Shaping
y3 = y.^3;
plot(f,y3,'m')
hold on

% Forth Order Noise Shaping
y4 = y.^4;
plot(f,y4,'b+:')
grid on
hold on
A.3 Matlab Code for the Plots of Figure 4-9

```matlab
clc
close all

Fs = 1;
alpha = 30;
f = 0:1/1e6:Fs/2;

D = 1 + 2*alpha*(1+alpha)*(1-cos(2*pi*f/Fs));

% Plot for Noise Transfer Function
H = sqrt(D)/1e3;
HdB = 20*log10(H);
plot(f,H)
hold on

% Plot for Signal Transfer Function
H = 1./sqrt(D);
HdB = 20*log10(H);
plot(f,H,'r')
grid on

ylim([0 0.16]);

xlabel('Normalize Frequency (f/f_{s})');
ylabel('Magnitude');
```
Appendix B

Verilog-A Codes

B.1 Verilog-A Code for 1-bit ADC (Comparator)

// VerilogA for PROJECT, comparator, veriloga

`include "constants.vams"
`include "disciplines.vams"

module comparator(clk,vpos,vneg,vout);
output  vout;
input clk, vpos,vneg;
electrical vout,clk,vpos,vneg;

parameter real trise = 5p from [0:inf);
parameter real tfall = 5p from [0:inf);
parameter real tdel  = 0p  from [0:inf);
parameter real vlogic_high = 1.2;   // 0.6/2 + 0.25/2
parameter real vlogic_low  = 0;     // 0.6/2 - 0.25/2
parameter real vtrans_clk  = 0.6;
parameter real vref        = 1.2;

real halfref;
real diff;
real vx;

analog begin
    @ ( initial_step ) begin
        halfref=vref/2;

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end

@ (cross(V(clk) - vtrans_clk,1))
begin
    vx = 0;
    diff = V(vpos)-V(vneg);

    if ((diff)+0.6> halfref)
        begin
            vx = vlogic_high;
        end
    else
        begin
            vx = vlogic_low;
        end
end

V(vout) <+ transition (vx,tdel,trise, tfall);
end
endmodule

B.2 Verilog-A Code for file writer

// This piece of code is used to collect data samples from cadence software
// VerilogA for PROJECT, sample_gen, veriloga

`include "constants.h"
`include "disciplines.h"

module sample_gen( in, clk );
input in,clk;
electrical in,clk;

parameter real vtrans = 0.6;
parameter fileName = "~/edu/fahqa640/MS_Thesis/SDM.txt";

integer fileHandle;

analog
    begin
        @ (initial_step)
            fileHandle = $fopen(fileName);
        @ (final_step)
            $fclose(fileHandle);
        @ (cross (V(clk) - vtrans,+1))
begin
    $fstrobe(fileHandle,"%d",(V(in) > 0.6));
end
end
dendmodule