Institutionen för systemteknik
Department of Electrical Engineering

Examensarbete

A 65nm, Low Voltage, Fully Differential, SC Programmable Gain Amplifier for Video AFE

Examensarbete utfört i Electronic Systems
vid Tekniska högskolan i Linköping
av

Syed Ahmed Aamir

LiTH-ISY-EX--10/4325--SE

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En 65 nm, fullt differentiell, programmerbar SC-förstärkare för video-AFE med låg matningspänning.

A 65nm, Low Voltage, Fully Differential, SC Programmable Gain Amplifier for Video AFE

Författare
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Sammanfattning
Abstract

Due to rapid growth of home entertainment consumer market, video technology has been continuously pushed to deliver sharper pictures with higher resolution. This has brought about stringent requirements on the video analog front end, which often coupled with the low power and low voltage regulations had to deal with short channel effects of the deep submicron CMOS processes.

This thesis presents the design of a fully differential programmable gain amplifier, as a subcircuit of a larger video digitizing IC designed at division of Electronic Systems. The switched capacitor architecture of the PGA does not only buffer the signal, but performs compensation for the sync-tip of analog video signal.

The pseudo differential OTA eliminates tail current source and maintains high signal swing and has efficient common mode feedforward mechanism. When coupled with a similar stage provides inherent common moode feedback without using an additional SC-CMFB block.

The PGA has been implemented using a 65 nm digital CMOS process. Expected difficulties in a 1.2 V OTA design make themselves evident in 65 nm, which is why cascaded OTA structures were inevitable for attaining gain specification of 60 dB. Nested Miller compensation with a pole shifting source follower, stabilizes the multipole system. The final circuit attains up to 200 MHz bandwidth and maintains high output swing of $\pm$ 0.85 V. High slew rate and good common mode and power supply rejection are observed. Noise requirements require careful design of input differential stage. Although output source follower stabilized the system, it reduces significant bandwidth and adds to second order non-linearity.

Nyckelord
Keywords

video, analog, low voltage, SC, CMFB, OTA, PGA

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List of Acronyms & Abbreviations

ADC Analog to Digital Converter

AFE Analog Front End (The analog, signal processing circuitry that precedes the ADC, usually found in mixed signal and RF transceiver chains)

CVI Component Video Interface (Video interfaces where signal is split into two or more separate components.)

CMFB Common Mode Feedback (A feedback control subcircuit in fully differential amplifiers, which helps fix the optimum output common mode voltage.)

CMFF Common Mode Feedforward (A circuit that senses the input common mode, and subtracts it at outputs of a fully differential OTA.)

CRT Cathode Ray Tube (A vacuum tube containing electronic gun that fires beam of charged electrons, which illuminate themselves as pixels to display the video frame.)

CMOS Complementary Metal Oxide Semiconductor (The most popular fabrication technology for designing digital, mixed signal and RF integrated circuits.)

CVBS Composite Video Baseband Signal (Video signal containing composite video, blanking and sync on a single wire interface.)

DM Differential Mode

DLL Delay Locked Loop (A digital circuit used to modify the phase of the input clock reference)

DVI Digital Visual Interface (An interface for digital, high visual quality displays.)

DTV Digital Television

DAC Digital to Analog Converter

ED Enhanced Definition (A component video format)

EMI Electromagnetic Interference (Electromagnetic or RF radiation from an external device that affects the performance of an electronic circuit.)

HDTV High Definition Television

HDMI High-Definition Multimedia Interface (A high quality all digital interface for uncompressed audio/video data.)

HD Harmonic Distortion (The undesired harmonic components produced at the output of an amplifier, along with the fundamental tone.)

HD High Definition (The family of highest end color TV standards, presenting a higher resolution, clear, crisp and more detailed picture.)

IRE Institute of Radio Engineers (A unit of measurement for video signals.)

LSB Least Significant Bit (The smallest voltage level that an ADC can convert, or DAC can output.)

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NTSC National Television System Committee (An analog color TV standard widely used in Americas and far eastern countries.)

OTA Operational Transconductance Amplifier (A differential amplifier that produces high impedance current output, for an input differential voltage signal.)

PAL Phase Alternate Line (Color TV system mainly used in Europe and Asia.)

PGA Programmable Gain Amplifier (An amplifier with programmable gain settings)

PLL Phase Locked Loop (A feedback controlled oscillator circuit that locks on to the phase and frequency of an input reference signal.)

RGB Red Green Blue

S-Video Separated Video (A two wire video signal interface that keeps chroma and luma separate.)

SD Standard Definition (A component video color TV standard)

SECAM Séquentiel couleur avec mémoire aka. Sequential Color with Memory (Color TV system used in France and Russia.)

SC Switched Capacitor

SPICE Simulation Program with Integrated Circuit Emphasis (A computer aided program for simulations of electronic circuits.)

SC-CMFB Switched Capacitor Common Mode Feedback (SC implementation of CMFB circuit block)

SOG Sync On Green (A Sony® standard, which presents sync on green channel only.)

SOY Sync On Luma

TI-PSAR Time Interleaved, Parallel, Successive Approximation Register (An interleaved SAR ADC architecture with much higher throughput.)

VESA Video Electronics Standards Association (An international organization for defining computer graphics standards.)

Chapter 1

Introduction

1.1 Evolution of Video Technology

Although the world's first working television system is credited to the Scottish engineer John Logie Baird [1], who was the first person to produce a live moving television image by reflected light in 1925, it was Philo Farnsworth, who was able to demonstrate the first working television system with electronic scanning of both the pickup and display devices two years later [3]. The Russian born Vladimir Zworykin [4] and Hungarian scientist Kalman Tihanyi [2] also made significant contributions demonstrating most of the features of the modern picture tubes. In brief, Farnsworth's Image Dissector [3], an early all electronic television tube, and an improved version by Zworykin called Iconoscope [4], in which a beam of high velocity electrons scanned a photo emissive mosaic, were essentially the basis of modern electronic television sets, the world saw later on.

1.1.1 The Continuous Video Picture

The continuous motion of video is of course a series of still images, changing fast enough to look like a video scene. The raster image painted on our screens is refreshed at a rate of 50 to 90 Hz, depending upon video standards. The image is painted on the screen on a line-by-line basis. Traditionally, two kinds of scanning systems have been in use; most television systems use the interlaced scanning. Every picture painted on screen is referred to as a frame. Each frame is divided into two separate sub-frames called fields. The two fields are referred to as odd numbered horizontal lines and the corresponding even fields, and are painted one at a time. The frame refresh rate is typically in the range from 25 Hz to 72 Hz.

As opposed to interlaced displays, progressive video scans the entire picture line by line, without splitting into fields as in interlacing, avoiding the flickering effect. Hence they are also called non interlaced scans; as common in most computer monitors. The resulting picture is of higher quality, smoothed edges and finer detail. Almost all HDTVs these days are progressively scanned, and the sharper picture in a $720p$ display is superior than that of a $1080i$. The latest progressive

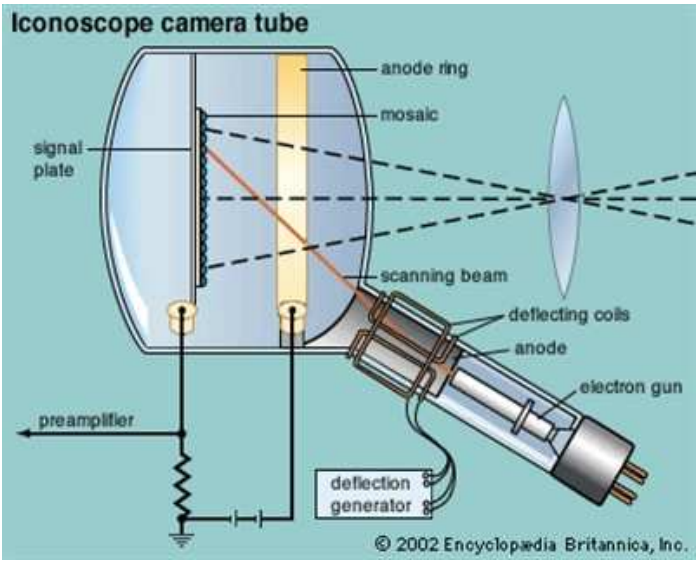


Figure 1.1: Zworkyin's Iconoscope, an early electronic TV © Encyclopedia Britannica [4].

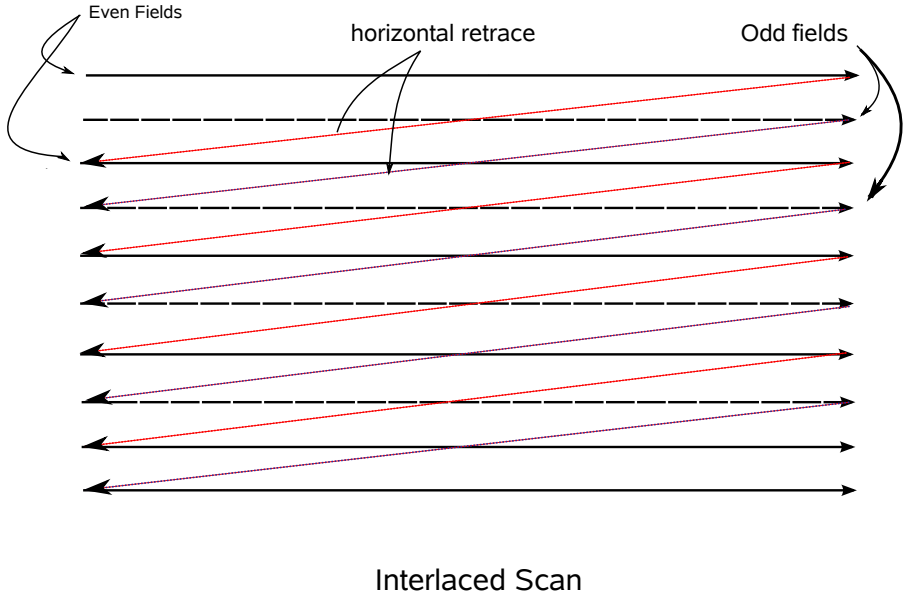


Figure 1.2: Interlacing in video [10].

scan video standards support resolutions up to 1920 × 1080 which is also referred to as full HD in the video consumer industry. It is being supported by BlueRay Disc Player ™, Sony PS3 ™ among others and is regarded as the best available source of high definition media currently [5].

1.2 Analog and Digital Video Data

When the video system jumped from grayscale to their colored counterparts, bandwidth requirements increased threefolds to accommodate red, blue and green signals. Hence alternate methods to transmit the color picture while utilizing the same bandwidth were tried. This gave rise to the composite video signal, which is still used in NTSC, PAL and SECAM video standards. Many similar ways of representing video data has evolved over the years, all of them are mathematically related to the RGB.

Other standards used in video consumer industry include S-Video, YP_bP_r in the analog domain and YC_bC_r and RGB as digitized versions of YP_bP_r and RGB.

Various analog and digital audio/video interfaces exits. The table below lists a few popular digital and analog interfaces in the decreasing order of their video quality [6]:

- HDMI (digital YC_bC_r)
- DVI (digital RGB)
- Analog YP_bP_r
- Analog RGB
- Analog S-Video
- Analog Composite

1.2.1 Color Spaces

A color space is a mathematical representation of a number of colors in terms of three or more coordinates. The three primary colors are the old red, green, blue (RGB) that are mixed to form any desired color. R'G'B' are mathematically manipulated non-linear form of RGB colors, popularly known as gamma corrected colors, adopted instead of the true linear RGB colors. To save bandwidth, cost and the processing power, R'G'B' are mathematically manipulated yet further, to derive several other forms of video signals, some of them will be mentioned below.

The color systems have access to the image pixel, directly stored in color intensity and format, to expedite the pixel refreshing process. This is the reason why most video standards use the luma and the two color difference signals.

Brightness or luminance (Y) derived from linear RGB of a pixel, has a nonlinear gamma corrected variant called luma while chroma (C') consist of color, hue and saturation information ,and is utilized instead of the chrominance signal (C). Fig. 1.3 indicates a very simplified RGB signal flow showing how different video interfaces are obtained from initial RGB signals.

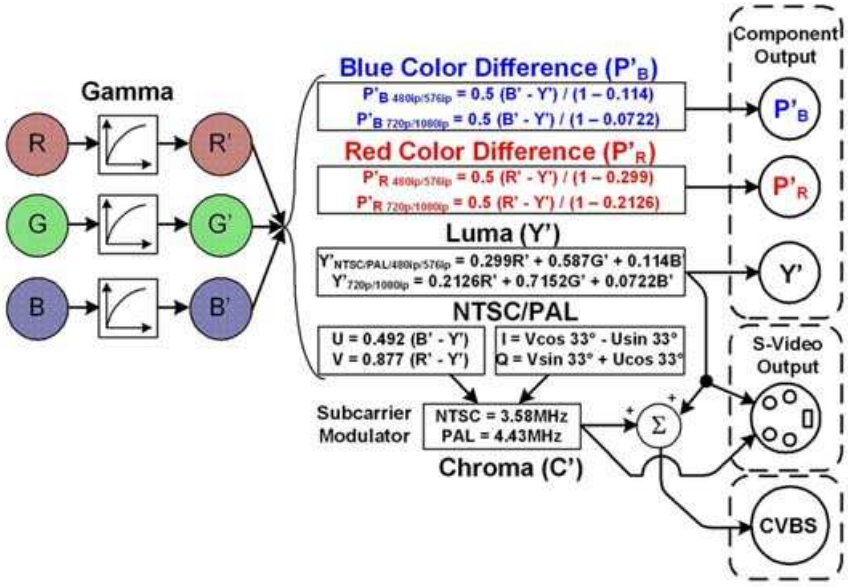


Figure 1.3: Process flow of RGB to component video conversion © Texas Instruments, Inc. [8].

1.2.2 Analog Video Transmission

The original NTSC and PAL systems were singled wired transmission systems, commonly called composite video baseband signal (CVBS). They had a bandwidth limited to less than 6 MHz with voltage amplitudes between −40 IRE (−286 mV NTSC/−300 mV PAL) to +100 IRE (714 mV NTSC/ 700 mV PAL) with slight variation between standards.

IRE, comes from Institute of Radio Engineers, and is a unit of measurement for composite analog video waveforms. Since amplitude of active video signal at any instance measures the pixel's brightness, IRE are quantified in percentage, starting from blanking level to the highest voltage of reference white level. In NTSC systems reference white level is 100 IRE which equals 714 mV.

The **CVBS** signal combines luma with the chroma signal, both occupying the same frequency spectra, essentially making it difficult to separate them without some picture distortion. Thats why the **S-Video** kept them as separate signals, while maintaining similar bandwidth as CVBS. As a consequence two wires had to be used.

Component video as an improvement upon S-Video, eliminated the need for modulation of chroma signal, reduced errors and introduced the color difference signal instead. The resulting component video signal utilized the luma (Y), the blue color difference P'_b, and the red color difference P'_r. The two color difference signals were kept on separate wires, giving rise to a three wire interface. The digital domain counterpart is referred to $YC'_bC'_r$.

Component analog video further comes in different formats. They include the standard definition (SD), enhanced definition (ED) and high definition (HD).

HD video
The high definition video typically includes $720p$, $1080i$ and $1080p$. The luma signal in $720p$ and $1080i$ has a bandwidth limited to 30 MHz while the color difference up to 15 MHz. The luma on $1080p$ has a bandwidth limit of 60 MHz and 30 MHz for the color difference. The bandwidth and sync widths of course do vary for the different frame rates and sampling rates for the above mentioned standards. The luma channel in HD video requires 1 V_{pp}, while the color difference requires 700 mV_{pp}. Due to the tri-sync levels in HD signals, and due to faster rates, the sync width could be as short as 0.15 μs in $1080p$. Please refer to Table. 1.2 for a comparison of specifications on various video formats.

Sync information
Video formats present the sync information in varying forms, sometimes as separate signal; at times on only one stream others (e.g. SONY® keeps it on green, hence named Sync-On-Green (SOG)™. Some interfaces such as the component video interface embed it in the luma signal, thus referred to as Sync-On-Luma (SOY).

1.2.3 $\mathrm{Y'C'_bC'_r}$ Color Space

$\mathrm{Y'C'_bC'_r}$ is a scaled and offset adjusted version of the YUV color space. Y is defined to have a nominal 8-bit range of $16-235$; C_b and C_r are defined to have a nominal range of $16-240$. The are several $\mathrm{YC}_b\mathrm{C}_r$ sampling formats, such as $4:4:4$, $4:2:2$, $4:1:1$ and $4:2:0$.

The basic equations for an HDTV format to convert between 8-bit digital R'G'B' data with a $16-235$ nominal range and $\mathrm{YC}_b\mathrm{C}_r$ are:

$$\begin{pmatrix} Y_{709} \\ C_b \\ C_r \end{pmatrix} = \begin{pmatrix} 0.213 & 0.715 & 0.072 & 0 \\ -0.117 & -0.394 & 0.511 & 128 \\ 0.511 & -0.464 & -0.047 & 128 \end{pmatrix} \begin{pmatrix} R' \\ G' \\ B' \end{pmatrix}$$

$$\begin{pmatrix} R' \\ G' \\ B' \end{pmatrix} = \begin{pmatrix} 1 & 1.540 & 0 \\ 1 & -0.459 & -0.183 \\ 1 & 1.816 & 0 \end{pmatrix} \begin{pmatrix} 1 \\ C_r - 128 \\ C_b - 128 \end{pmatrix}$$

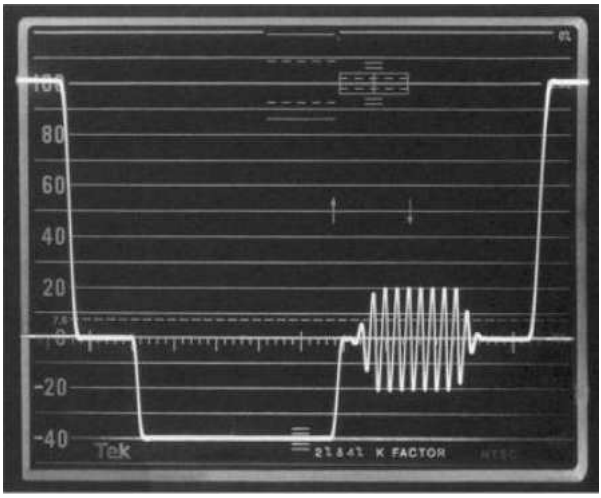


Figure 1.4: A video waveform as measured on IRE scale © Tektronix Inc. [7].

1.3 The Video Signal Composition

The analog video signal is a sub-volt signal containing the timing and intensity information for each horizontal line drawn. The timing pulse ensures the display device remains synchronized with the video signal. The two fields are synchronized using the horizontal and vertical synchronization signals. The resulting signal is a composite video signal. Each horizontal video line consists of horizontal sync, back porch, front porch, active pixel region [9, 10]. Although this video signal waveform has this generalized form since the early days of broadcast TV, many formats come with differing schemes, and any particular video format may lack an interval, sync pulse etc, among others. Video designers generally take measures to deal with all kinds of various standards, as a way to design all encompassing video AFEs.

1.3.1 Synchronization Pulses

The horizontal sync is the synchronization pulse that indicates the start of new video horizontal line. It is preceded by the the front porch and is followed by the back porch interval. Sometimes this hsync duration is used by clamp circuits to restore the DC.

The vertical sync is the vertical synchronization series of pulses that marks the end of one field and signals the screen to perform a vertical retrace.

1.3.2 Sync-Tip

The width of the sync pulse is also mentioned as sync-tip, especially in clamped systems where the sync-tip level of -300 mV is often important enough to deal

with.

1.3.3 Front and Back Porch

The interval of the video signal between the end of color burst and the start of active video signal is the back porch. Alternately, the total interval between the sync-tip and the start of active video signal is also referred to as back porch. After the end of active video signal line, the sync-tip is separated by the front porch interval.

1.3.4 Color Burst

A high frequency signal in NTSC, which provides a phase and amplitude reference for a particular color, and is mostly located at back porch is the color burst. Typically 8 to 10 cycles, and has an amplitude of $\pm$ 20 IRE of the color reference frequency.

1.3.5 Breezeway

Since color burst is often located on back porch, the interval between color burst and sync-tip is referred to as breezeway.

1.3.6 Blanking Interval

The whole duration which consists of sync-tip and the front and back porch intervals constitutes the vertical or horizontal blanking intervals. The duration allocated for retrace of the signal from the rightmost edge of the screen back to the first left edge, to start another scan line is referred to as horizontal blanking. Similarly vertical blanking interval is the period allocated for retrace of the signal from the bottom right, back to the top left edge, to start another field or frame. This retrace was highlighted in Fig. 1.2.

1.3.7 Blanking and Black Level

These are the specific voltage levels of the analog waveform during blanking time or the on screen black voltage level during the active video signal. In most systems, the sync-tip level (≈ -300 mV, 7.5 IRE) is the only duration, where voltage goes to a slightly more negative value than blanking level, while some have black level at same level as that of blanking level.

1.3.8 Clamp

The circuit that forces a portion of the video signal to a specific DC voltage, to restore the DC level is referred to as clamp circuit. Usually clamping is done either on the back porch, or the sync-tip of the video waveform. Also called DC restore, a black level clamp to ground circuit, forces the back porch voltage to be equal to

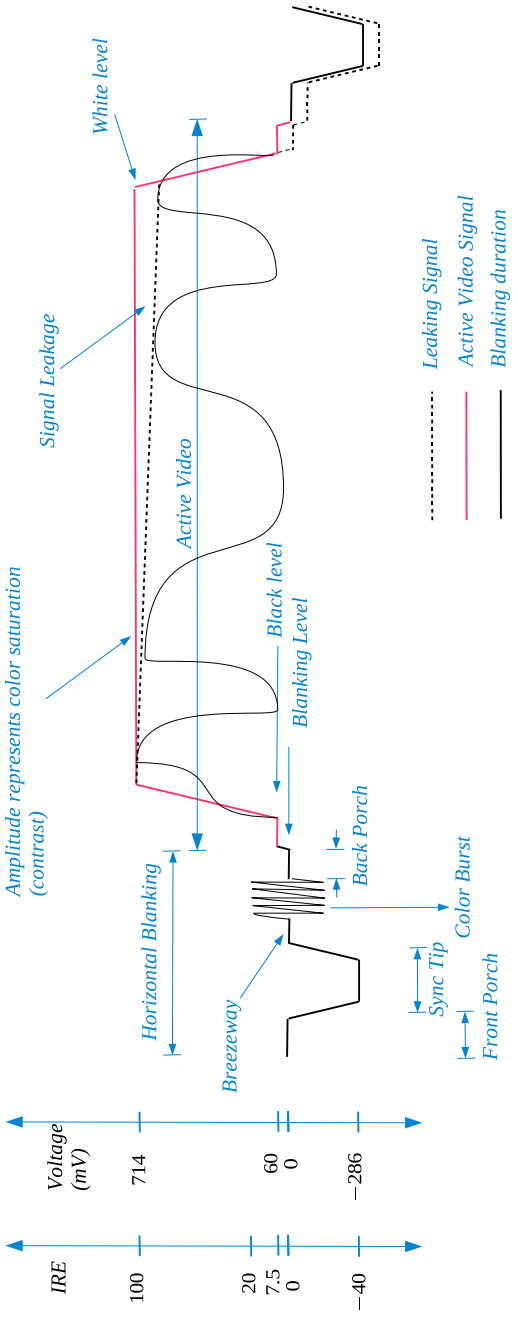


Figure 1.5: A general video signal waveform [10].

zero volts. On the other hand, a peak level clamp forces the sync-tip voltage to be equal to a specified voltage.

1.3.9 Chroma Signal

This is the actual color information of the video signal. This signal consists of two quadrature components modulated on a carrier at the color burst frequency. The phase and amplitude of these analog waveform determine the color content of each pixel. Sometimes referred to incorrectly as chrominance, which in fact is the displayed color information.

1.3.10 Luma Signal

The monochrome or black-and-white portion of the analog video signal. This term is sometimes incorrectly called luminance, which refers to the actual displayed brightness.

1.3.11 Color Saturation

This is the amplitude of the color modulation on a standard video signal. The larger the amplitude of this modulation, the more saturated (intense) the color would get. This amplitude control is commonly a contrast control in television sets.

1.4 Requirements on Popular Video Standards

Tables 1.1 & 1.2 highlight some of the analog requirements that some video consumer industry standards impose on the video analog front ends, along with their signal specifications. Requirements for both TV as well as VGA standards are enlisted, although this thesis would primarily address the high definition television standards.

Format	Standard	Bandwidth	Min.SR	Sync Width	Amplitude
VGA	640×480	12.6	112	3.8	1/0.7
SVGA	800×600	20	178	3.2	1/0.7
XVGA	1024×768	32.5	289	2.092	1/0.7
SXGA	1280×1024	54	480	1.037	1/0.7
UXGA	1600×1200	81	719	1.185	1/0.7
UWXGA	1920×1200	96.6	858	1.035	1/0.7

Table 1.1: A list of VESA standards and their analog requirements.

Format	Standard	Bandwidth	Min.SR	Sync Width	Amplitude(Vpp)
NTSC	CVBS	<6	53	4.7	1.221
	S-Video	<6	53	4.7	1
		2.2 to 4.2	37	None	0.836
	(SD)	<6.75	60	4.7	1
		<3.375	30	9.4	0.7
	(ED)	12	106	2.33	1
		6	53	4.67	0.7
PAL	CVBS	<6	53	4.7	1.2335
	S-Video	<6	53	4.7	1
		3.2 to 5	44	None	0.885
	(SD)	<6.75	60	4.7	1
		< 3.375	30	9.4	0.7
	(ED)	12	106	2.33	1
		6	53	4.67	0.7
HDTV	720p	30	266	0.54/0.59	1
		15	133	1.08/1.18	0.7
	1080p	60	532	0.296	1
		30	266	0.592	0.7

Table 1.2: Popular consumer TV standards with their analog requirements and signal characteristics.

Chapter 2

Video Analog Front Ends

This thesis is related to the analog front end of a high speed video digitizer IC, designed at the division of Electronic Systems, Department of Electrical Engineering. The project has been carried out as a combined teamwork among graduate students and researchers at the division under the technical leadership of Dr. J Jacob Wikner. The video IC design task was divided into various mixed signal and all-digital blocks of the video digitizing and time-reference channel streams.

The video IC to be implemented, was a state-of-the-art design targeting video resolutions defined by the high definition video standards, featuring:

- a high performance 12-bit digitizer AFE
- up to 300 MS/s maximum conversion rate
- low jitter all digital PLL and DLL
- 65 nm CMOS process

2.1 The High Speed Video IC Architecture

The architecture of the video IC, containing various building blocks has been outlined in Fig. 2.1. The dashed line marks the boundaries of the two separate channels in the IC, the digitizing channel and the time-reference channels.

2.1.1 Time-Reference Channel

The time-reference channel stream as shown in Fig. 2.1 consists of clock generation and currents and voltages reference blocks. Essentially, there exists an all-digital phase-locked loop (PLL), a delay-locked loop (DLL), an RC wakeup oscillator, bandgap reference, slicer and voltage regulator blocks.

The signal chain starts from the multiplexer selecting proper reference either from the slicer detecting timing information from input video signal, or generated

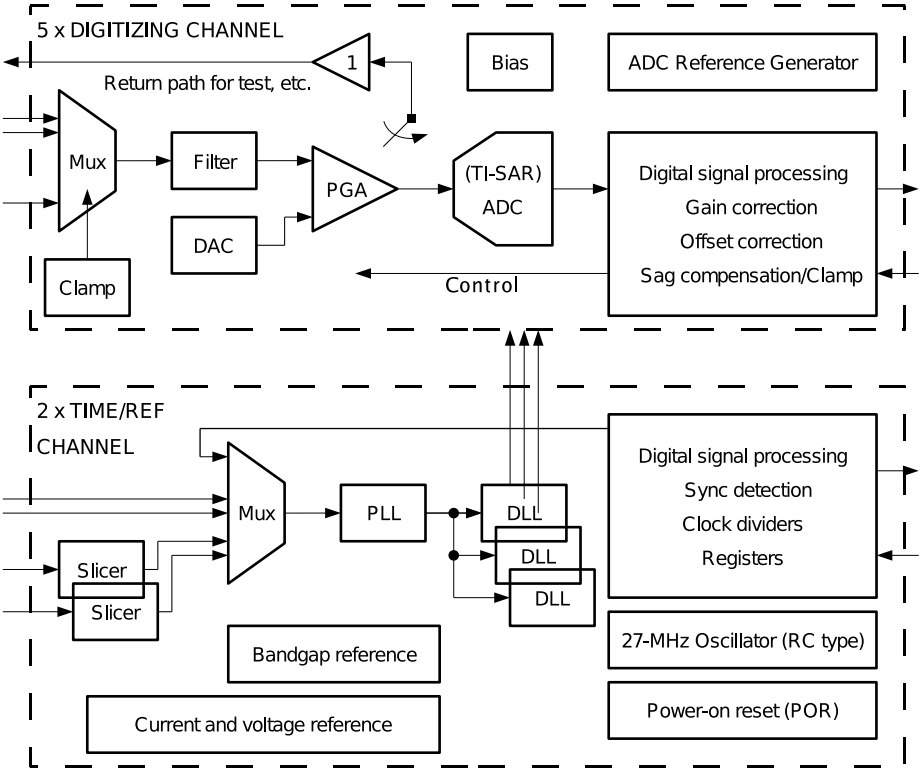


Figure 2.1: The high speed video digitizer IC designed at division of Electronic Systems, with digitizing and time-reference channel streams.

digitally, or as an external trigger. The PLL takes this signal and generates a higher frequency signal aligned to its input reference (hsync of video signal). The delay-locked loop (DLL) will shift this high frequency clock in phase, producing a total of 32 equally spaced phases. The reason for generating 32 phases is to maintain the parametric design for yield on minimum of three sigma quality standards ($3\% \approx 1/32$).

All-digital DLL & PLL

The PLL is responsible for generating higher frequency with an output range of 10−300 MHz, whereas the DLL having similar input range up to 300 MHz generates 32 phases maintaining fix duty cycle of 50% and a long term jitter of ± 2%. Each input in the multiplexer stream would have a DLL and a PLL. The PLL is also an all-digital version, replacing the VCO with digital DCO block and maintaining strict 50% duty cycle. The reason for measuring long term jitter over 2000 clocks, is to capture the effect of parameters such as $1/f$ noise, etc., on overall clocks.

Oscillator

Oscillator is an ultra low power 10 μW RC type wakeup oscillator which maintains a standby mode, unless digitally triggered upon detection of on-screen activity.

Voltage regulator and bandgap reference

A voltage regulator provides reference voltages required by on chip components, and is derived from the externally available supply. A bandgap reference ensures fix supply voltage for on chip components, safe from process, voltage and temperature variations.

2.1.2 Digitizing Channel

The digitizing channel consists of an input multiplexer, low pass filter, the PGA, a 12-bit ADC, bias, clamp circuit and auxiliaries. A substantial part is also the digital error and gain correction block in the channel. Modern video AFEs consist of five of such digitizing blocks to cover most of the different video standards. Some auxiliary blocks generate reference voltages for the ADC and all other on chip components.

2.1.3 Signal Chain of the Video Digitizing Channel

The AC coupled analog video signal (YP_bP_r, RGB) is multiplexed among a range of input devices (VGA, DTV tuner, S-Video, set-top box, DVI, HDMI etc.), whose DC point is restored with the help of the clamp circuit. The video signal gets band limited with the help of an active antialiasing filter. It is then fed to the programmable gain amplifier which generates a differential signal, buffers the signal

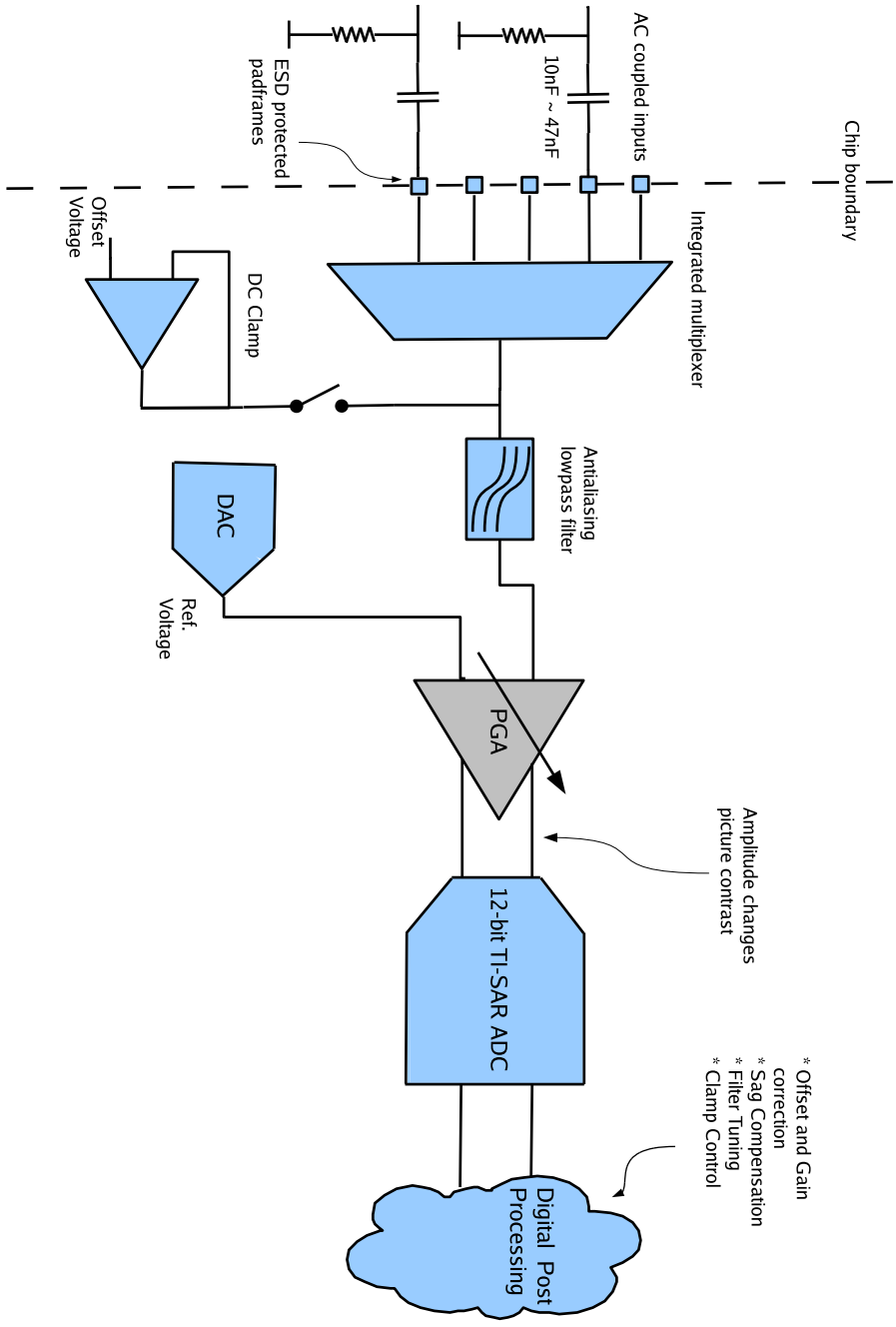


Figure 2.2: The video AFE signal chain.

and scales it in amplitude, as required by the system. Finally, this signal is digitized by the 12-bit TI-PSAR ADC.

2.1.4 AC Coupling

AC coupling allows the video designer to set optimal DC level, independent of the driving signal's DC bias level.e.g, an ADC driver circuit sets the clamping or blanking levels of the video signal, equivalent to internal ADC code-zero voltage, regardless of the driving signal's absolute DC level.

2.1.5 Clamping and DC Restoration

To digitize an AC coupled video waveform, DC restoration is necessary; to put the DC component back into the signal. With AC coupled signal, the bias voltage will vary with video content and the brightness information would be removed. This circuit adjusts the clamp level to the correct brightness of the picture during the back porch or the sync-tip section of the video signal.

2.1.6 Anti Aliasing Filter

The images dictated by the DAC/ADC's sampling frequency would possibly fold down in the baseband, degrading the picture quality. Hence antialiasing filter would necessitate. Even if ADC/DAC has digital filtering, analog pre-filtering would still be required. Such a filter would also reduce EMI interference, as well as the signal noise floor by reducing bandwidth.

2.1.7 Type of Filter

While designing a video filter one must consider the specification on the filter's group delay, passband flatness, corner frequency and perhaps roll-off rate. Once a corner frequency is selected, we would probably desire the flattest passband possible with most attenuation near the ADC/DAC sampling frequency. From this perspective a Chebychev or Cauer filter seems a good option. On the other hand, group delay must prevent excessive ringing and overshooting, when the picture changes abrupt frequencies (a black-to-white and back on every pixel). If let go, it can appear as fuzzy edges on the display screen, although the attenuation would be good! Chebychev or Cauer filter will maintain this ringing due to variations in group delay. A Bessel filter offers best group delay but has the disadvantage of transmission zeroes in both pass and stop bands. A good balance hence, is offered by a Butterworth filter due to its maximally flat amplitude response, a reasonable rate of attenuation and respective group delay [8].

2.1.8 Split Filter Architecture and Digital Tuning

The video signal specifications preferably require a fifth-order Butterworth filter, but the design complexity increases considerably upon moving to higher order active analog filters. Hence, one may opt for a 'split architecture' comprised of

a passive filter and an active Gm-C or OTA-C filter, instead. The passive filter would cater for the dominant poles whereas higher-frequency poles would be dealt by the active implementation. Tuning can be done digitally, implemented as a feedback control loop.

2.2 ADC

The ADC which takes the differential signal from the PGA in the video AFE chain, is a 12-bit, 300 MS/s time-interleaved, parallel, successive approximation register architecture. The 12 bits provides higher resolution and has been time-interleaved by a factor of 16, multiplying significantly the sample rate of ADC, up to 300 MS/s. The selection of SAR ADC is motivated by the faster, short-channel 65 nm process which encourages all-digital components, and SAR architecture remains least on analog content. The time interleaved architecture further helps in achieving higher throughput. Sigma-delta would be suitable for low bandwidth and has more analog components, like does the pipelined architectures which may also increase power consumption. The offset and gain errors are maintained at 1% maximum (translates to $\pm$ 32 LSB).

2.3 Programmable Gain Amplifier

As mentioned previously, the objective of this thesis is to design the programmable gain amplifier, and has been implemented as a low voltage, fully differential, switch capacitor architecture. The choice for a fully differential architecture is obviously due to the high output signal swing, improved linearity and noise suppression, but at the cost of additional CMFB circuit.

PGA takes multiplexed and filtered video signal from the 'mux-clamp' block and is referenced from a DAC. The operational transconductance amplifier designed for the PGA is a novel cascaded fully balanced, pseudo differential OTA, with common mode feedforward and inherent common mode feedback detector [13].

2.3.1 Revisited PGA Architecture due to CMOS Process Limitations

The selection of the CMOS process was initially decided to be a 180 nm, which could be more helpful for analog blocks such as PGA, oscillator, etc., as compared to another 65 nm CMOS process, which was later adopted due to practical reasons.

The fully differential PGA design initially anticipated, was to be a single OTA structure where cascaded OTAs were used to make available CMFB, in selected architecture. However, due to the lower gain in devices from the process library, the architecture had to be revisited and finally both the cascaded structures of fully differential OTA were utilized to provide required gain. Initially, the second OTA structure was meant to integrate the active filter implementation of the suggested

split filter architecture, described in section 2.1.8. CMOS process issues have been further highlighted in section 5.2.

2.3.2 PGA Specifications

The video PGA in conjunction with the full AFE chain preceding clamp and filter needed to satisfy a group of important properties. They are mostly specified in Table. 2.1.

Supply voltage	1.2 V
Power consumption	50 mW
3db Bandwidth	500 MHz
Gain settings	0.5, 1, 2
Linearity (at 30 MHz)	60 dB
Signaling mode	differential in/differential out
Leakage	0 A
Area	0.1 mm^2
CMRR	50 dB
Temperature range	0 to 115
Supply tolerances	$\pm$ 10%
Slew rate	5 mA/0.5 pF, 250 V/μs
Noise level	$< Q_N$ of 12-bit ADC

Table 2.1: The PGA specifications.

2.3.3 Linearity and Noise

The video front end had to be linear enough to pass the whole band of input video signal with full linearity. This dictates the requirement on OTA's DC gain and set to be minimum of 60 dB. The PGA noise, in general, should be less than the quantization noise of a 12-bit ADC.

2.3.4 Slew Rate

The PGA would preferably charge the output node during the shortest sync-tip duration, from among the video standards. This time duration could be as short as 0.15 μs.

2.3.5 Bandwidth

A higher video bandwidth is required to present a sharper picture. Notice that this is specially true to accommodate the higher definition standards than the conventional NTSC and PAL standards. This video AFE targets up to 500 MHz bandwidth throughout the chain, to cover, all currently available TV standards. The PGA should preferably target higher than 500 MHz to compensate for preceding band limitations caused by clamping or filter circuits.

The bottleneck on bandwidth in the AFE is the low voltage PGA where achieving as high as 600 MHz becomes challenging especially with 3 or 4 gain stages.

2.3.6 Leakage

The video front end (clamp to PGA) needs to set the DC conditions without having to break the signal path. The video picture would suffer, as indicated in Fig. 1.5, if there is any signal leakage to ground. The video clamps strive to ensure that no DC signal leakage occurs.

2.4 On Screen Artifacts due to Errors in Video AFE

A significant variation from the standard video AFE specifications can probably lead to undesirable distortive effects, which may be visible to the eye beyond a certain limit. Some of them are described below.

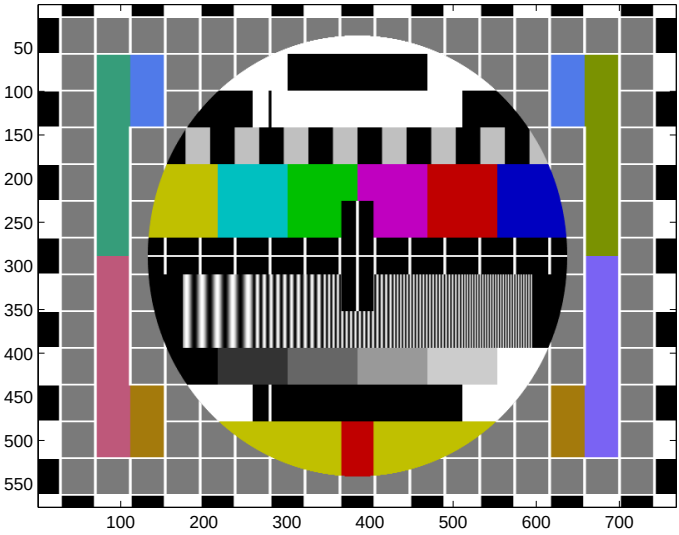


Figure 2.3: The popular Philips PM5544 test card.

2.4.1 Effect of Flicker Noise

The transistor's flicker noise becomes apparent in video applications as a slight shift from pixel line-to-line. This is primarily due to sampling variations, which

can occur with the creation of a small pedestal on sampling capacitor. The sync-tip frequency is within the 1/f range for MOS devices, thus making itself visible.

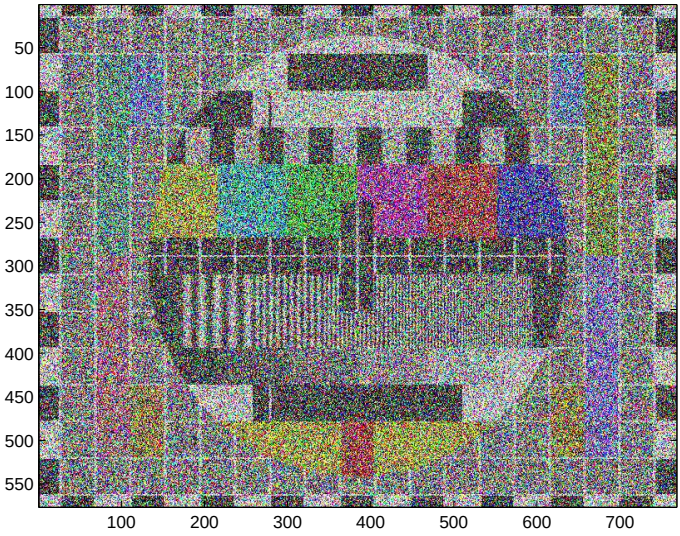


Figure 2.4: Effect of noise on test pattern.

2.4.2 ADC Errors

If there are large gain and offset errors in the TI-PSAR ADC architecture, having an interleaving factor M, and no. of pixels per line being a multiple of this factor M, it would appear as a distinct raster on the screen.
Variations in gain, phase and offset in general, among adjacent color streams can result in a slight skew in color space. In digitizing channel these errors are compensated for in the digital domain, once the signal has been digitized.

2.4.3 Timing Errors

The cycle to cycle jitter of PLL and DLL again have a maximum limitation which, if violated, can appear quite distinctly. The jitter causes a variation of pixel sampling time due to skewed sync-tip, distorting a vertical pixel raster on screen as shown in Fig. 2.6.

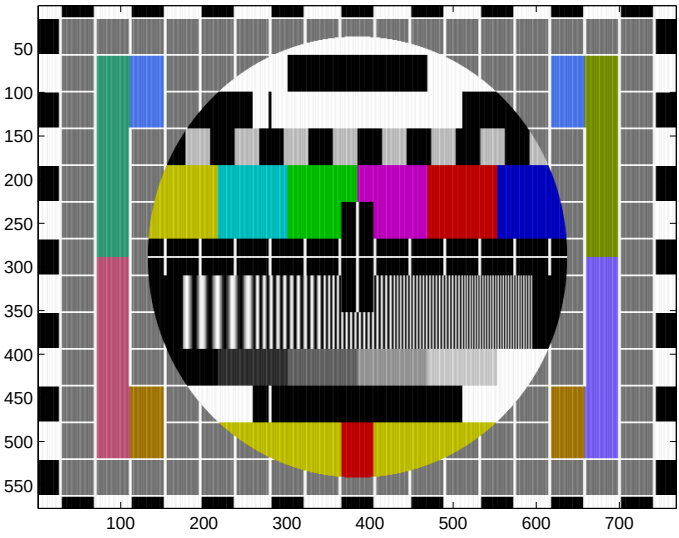


Figure 2.5: Vertical stripes due to large offset and gain errors in ADC.

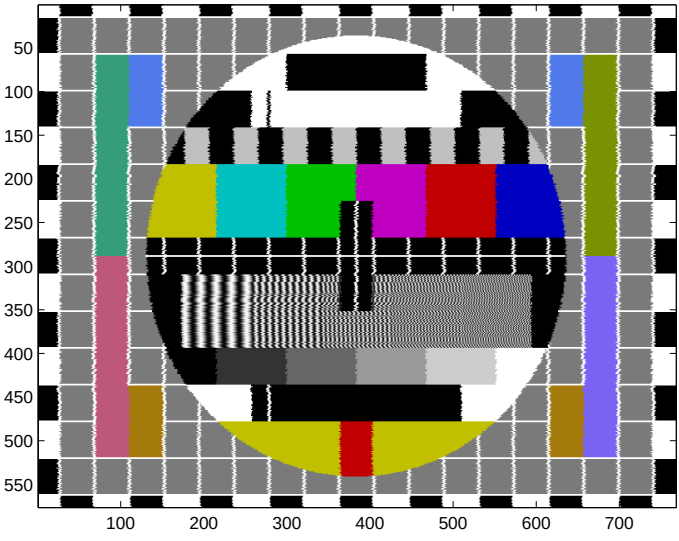


Figure 2.6: Image distortion caused by hsync jitter.

2.4.4 Leakage

Any leakage in the active video signal path would cause loss in DC signal, evident on screen as loosing picture brightness over time. Fig. 2.7 demonstrates this effect.

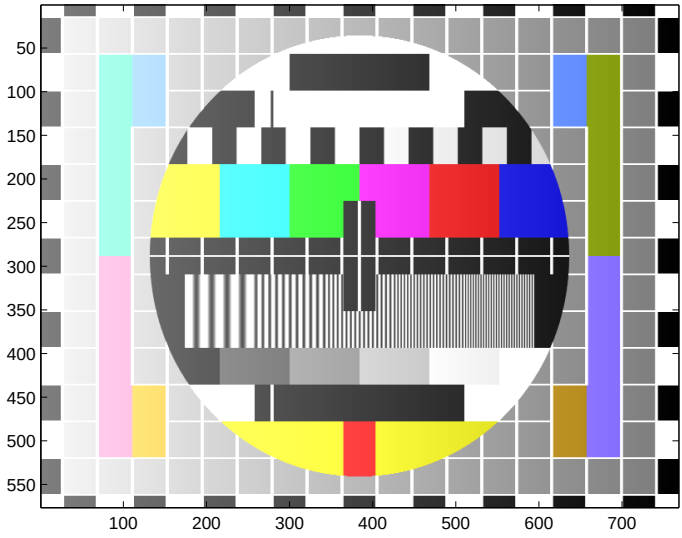


Figure 2.7: Varying brightness levels in a leaking video signal.

Chapter 3

OTA Architecture

A.N. Mohieldin, E. Sanchez-Sinencio and J. Silva-Martinez [13] presented a relatively novel low voltage, fully balanced, fully differential OTA architecture with common mode feedforward and inherent common mode feedback detector. The architecture strives to cut the number of stacked transistors to two, making it an attractive option for low voltage applications. A similar OTA in cascade, helps stabilize the output common mode point acting as a CMFB circuit.

3.1 A Pseudo Differential OTA and Common Mode Feedforward Technique

OTA architectures can be loosely classified into two main groups, the 'fully differential' and 'pseudo differential' architectures. The difference emanates from the presence of the tail current source in fully differential OTA, while the pseudo differential version end ups with two independent inverters only.

The need for a tail current source

In case of a common mode disturbance on the input differential lines, the transconductance, as well as maximum output range can vary, pertaining to an input common mode change of MOS input differential pair. In order to minimize this dependence of bias currents on input common mode level, a tail current source I_{ss}, which makes I_{d1}, I_{d2} independent of V_{inCM}. Hence when $V_{in1} = V_{in2}$, the bias current in each branch is $I_{ss}/2$ and V_{outCM} equals $V_{dd} - R_d/I_{ss}/2$, a well defined output voltage. Removing this current source results in poor rejection to common mode noise, and requires a stronger CMFB circuit to stabilize the output DC point.

The proposed architecture uses the common mode feedforward technique to reduce A_{CM} at low frequency to the order of unity:

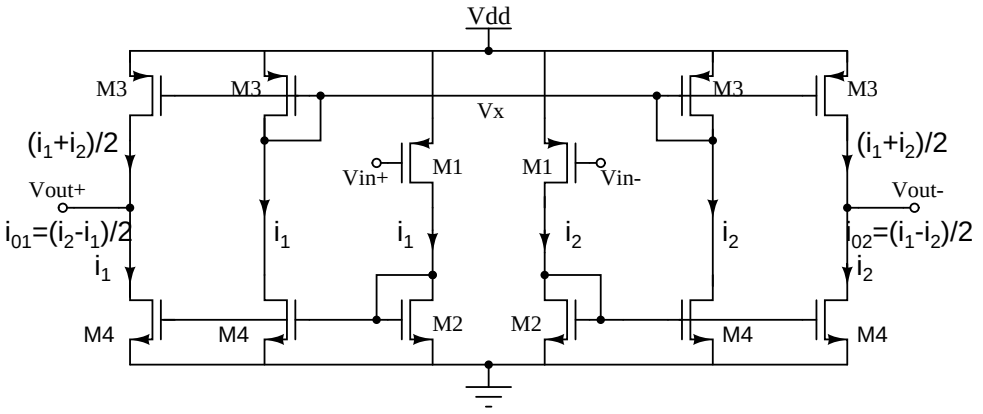


Figure 3.1: The low voltage, pseudo differential OTA architecture with CMFF.

$$A_{CM} = \frac{V_{outCM}}{V_{inCM}}, \tag{3.1}$$

$$= \frac{g_{m1} - (g_{m1}g_{m2})/(g_{m2} + g_{ds1}g_{ds2})}{g_{ds1}g_{ds2}}, \tag{3.2}$$

$$= \frac{g_{m1}}{(g_{m2}g_{ds1}g_{ds2})} \approx \frac{g_{m1}}{g_{m2}}. \tag{3.3}$$

The proposed OTA architecture is reproduced in Fig. 3.1 [13]. It uses the same differential transconductance to detect the common mode too, essentially by making copies of the individual currents and subtracting the common mode component at the output. The proposed OTA structure is a three current mirror, single ended OTA, without the tail current source. Thus the OTA becomes fully balanced and fully symmetric.

In Fig. 3.1 the current $I_1 + I_2/2$ provides the information of the common mode level of the inputs V_{inCM} as follows (neglecting short channel effects):

$$I_1 + I_2 = K_p(W/L)_1[(V_{dd} - V_{inCM} - \mid V_{TP} \mid)^2 + 0.25V_{diff^2}], \tag{3.4}$$

$$= \beta[V_{ov}^2 + 0.25V_{dd}^2], \tag{3.5}$$

where $V_{inp} = V_{iCM} + V_{diff}/2$, $V_{inn} = V_{inCM} - V_{diff}/2$, $\beta = K_p(W/L)_1$ and $V_{ov} = V_{dd} - V_{inCM} - |V_{TP}|$.

The current $I_1 + I_2/2$ gets mirrored at the output, extracting the desired common mode component V_{inCM}. This common mode current is subtracted at the OTA outputs and is referred to as 'feedforward cancellation' of the common mode signal. The concept is explained in Fig. 3.2.

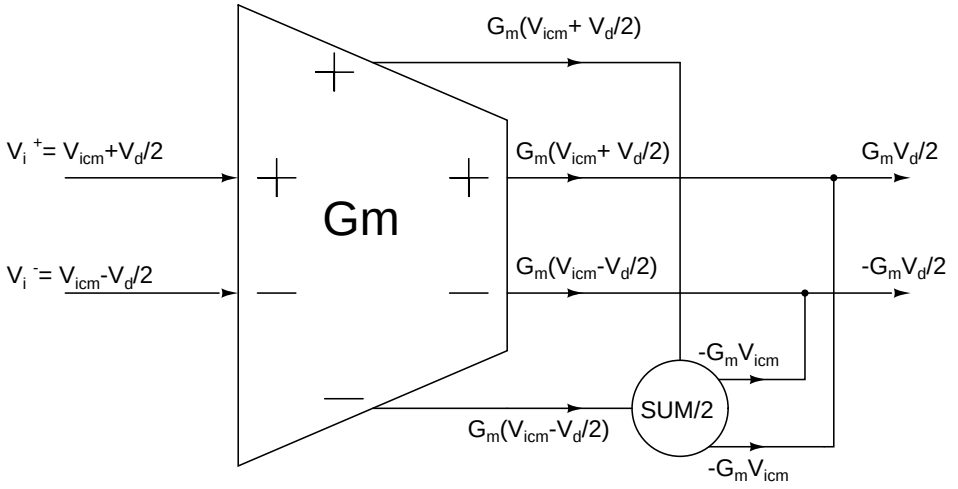


Figure 3.2: Conceptual implementation of OTA feedforward cancellation.

3.2 Common Mode Feedback using Cascaded OTA Structures

The common mode feedforward mechanism employed so far, helps suppress the common mode component at the output, but in order to fix the output DC common mode voltage properly, the CMFB is still required.

The OTA architecture makes the CMFB available, if at least two similar OTA structures are utilized, and feedback transistors are added in first OTA. The output common mode level of each stage is then sensed by the V_x node of next cascaded OTA structure. The CMFF and CMFB technique can be used simultaneously by addition of four transistors as shown in Fig. 3.3. This approach helps prevent loading at the output due to additional CMFB block, as is the case of some conventional CMFB architectures.

One wonders how the typical comparator operation of a CMFB block, highlighted in Fig. 3.4, is achieved here. Figure 3.5 shows this, and drawn is one half of the fully symmetric OTA with CMFB block. A reference current I_{ref} is mirrored in the lower CMFB transistor M_{4a}, which sets the required DC point at output whereas M_{3a} takes its input as a feedback V_{cmfb} from the 2^{nd} cascaded OTA. V_x is extracted input common mode of 2^{nd} OTA, which of course is the output common mode V_{outCM} of 1^{st} OTA.

If the output DC point of $Vout_p$ is at its optimum, I_x and I_{ref} are equivalent. If in case its higher, then I_x, which is essentially common mode point of this very OTA, but sensed in, and fed back from the next cascaded OTA, it will increase, lowering the common mode output. Hence a stable common mode is achieved.

One clear advantage of this scheme is the shared path for the differential and common mode signals which helps to achieve similar bandwidths for both common

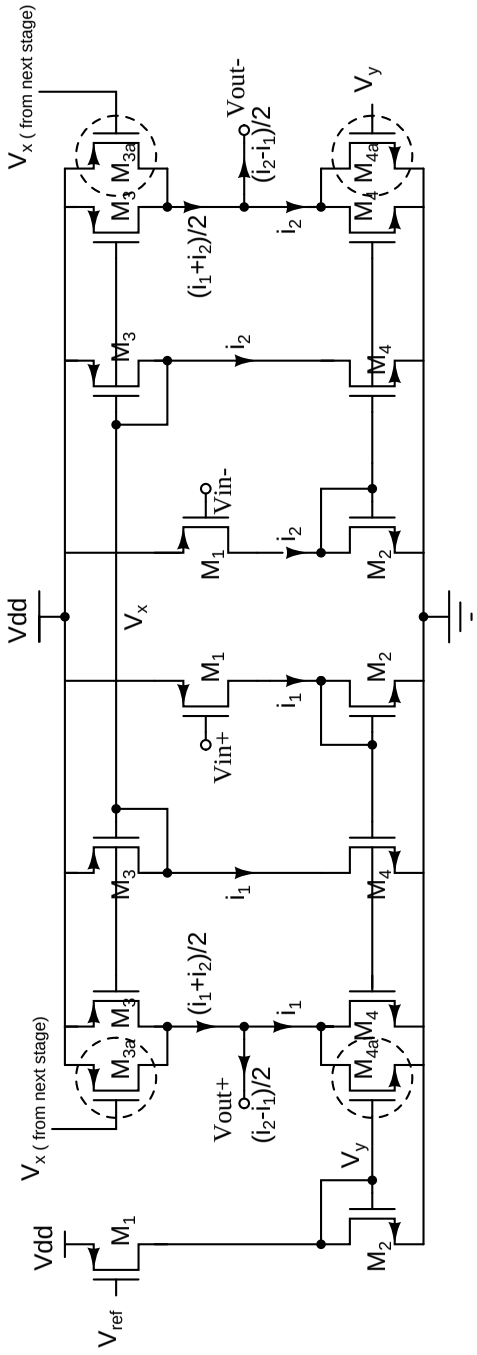


Figure 3.3: The pseudo differential OTA architecture with CMFF and CMFB.

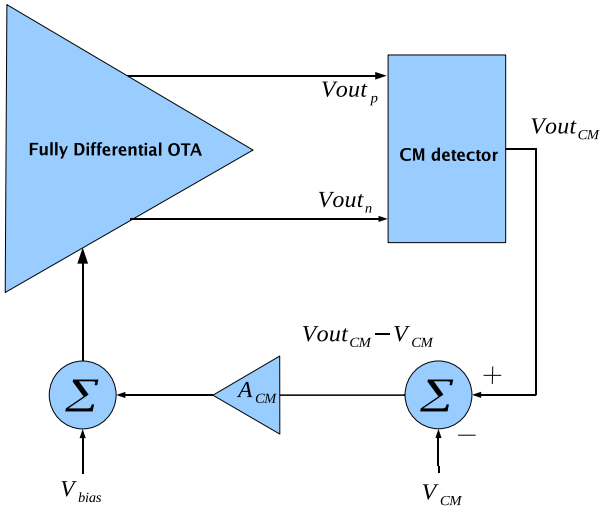


Figure 3.4: The generalized CMFB block for a fully differential OTA.

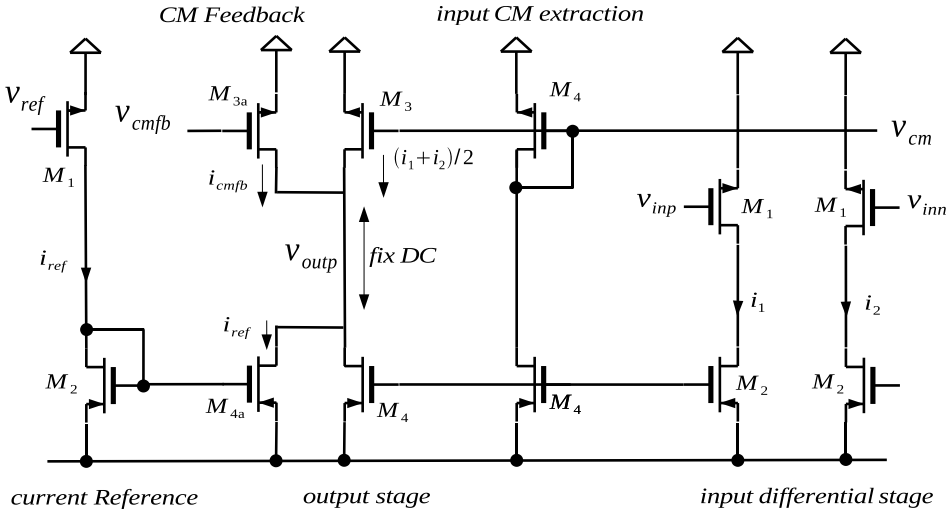


Figure 3.5: One half of the fully symmetric OTA with common mode feedback mechanism.

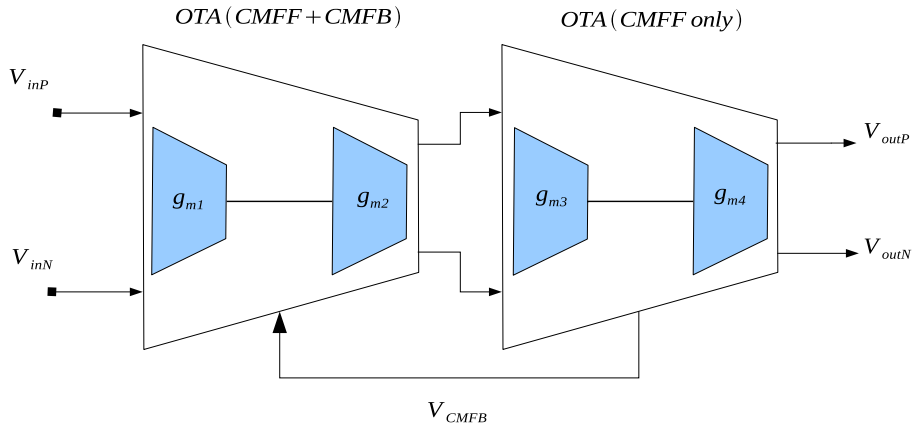


Figure 3.6: A pair of cascaded OTA required to provide CMFB.

mode and differential paths. This is required, as ideally one needs to suppress common mode disturbances over the entire band of differential mode input signal by achieving similar unity gain frequencies [11].

3.3 Frequency Response

The OTA encounters one parasitic pole in the differential signal path and two parasitic poles in the common mode path. The overall transfer function of the OTA and the two poles is given by the following expressions:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m4}}{(g_{m2} + g_{ds1} + g_{ds2} + sCz)(g_{ds3} + g_{ds4} + sC_L)}, \tag{3.6}$$

$$\omega_{p1} = \frac{g_{m2} + g_{ds1} + g_{ds2}}{C_z}, \tag{3.7}$$

$$\omega_{p2} = \frac{g_{ds3} + g_{ds4}}{C_L}, \tag{3.8}$$

where C_z is the total output node capacitance of input differential pair and C_L is the load capacitance. The DC gain of the amplifier is:

$$A_{DC} = \frac{g_{m1}g_{m4}}{(g_{m2} + g_{ds1} + g_{ds2})(g_{ds3} + g_{ds4})}, \tag{3.9}$$

$$= \frac{\sqrt{(W/L)_1}\sqrt{(W/L)_4}}{[\sqrt{(W/L)_2} + \sqrt{I_{din}}(1/L_1 + 1/L_2)]\sqrt{I_{dout}}(1/L_3 + 1/L_4)}, \tag{3.10}$$

where I_{din} and I_{dout} are input and output stage currents.

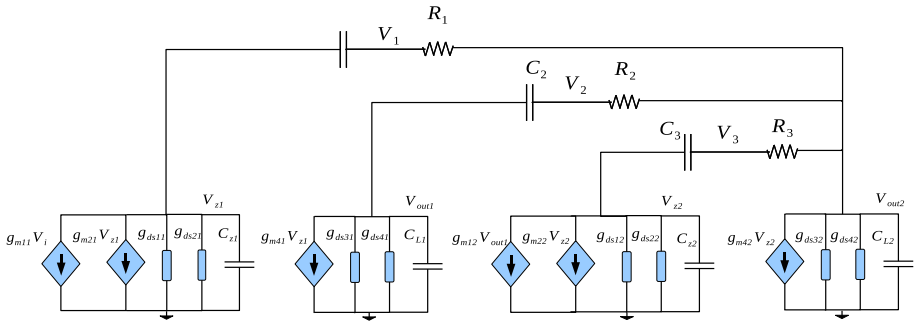


Figure 3.7: Small signal model with Nested Miller compensation.

3.3.1 Cascaded OTA structures and Compensation

Upon cascading the two OTA structures, as highlighted in Fig. 3.6, four nearby poles are likely to keep the amplifier unstable, unless it is compensated.

One needs to identify a suitable compensation scheme. Even with multi stage cascaded amplifier one can resort from simple Miller compensation to more novel ways to compensate like 'No Capacitor Feedforward Compensation' proposed in [16].

Since feedforward mechanisms may increase the power budget, and may also not suit the architecture, a Miller compensation has been resorted to, in this thesis. However, one needs to choose 'Nested Miller Compensation' with feedback to output from every amplification stage.

Upon applying Nested Miller compensation to the cascaded amplifier, the equivalent small signal model of the system is shown in Fig. 3.7.

One may derive a set equations for this amplifier to derive possible pole-zero expressions. The following equations were derived:

$$g_{m11}V_{in} + V_{z1}(g_{m21} + g_{ds11} + g_{ds21} + sC_{z1}) + sC_1(V_{z1} - V_1) = 0. \quad (3.11)$$

$$sC_1(V_1 - V_{z1}) + R_1(V_1 - V_{out2}) = 0. \quad (3.12)$$

$$g_{m41}V_{z1} + V_{out1}(g_{ds31} + g_{ds41} + sC_{L1}) + sC_2(V_{out1} - V_2) = 0. \quad (3.13)$$

$$sC_2(V_2 - V_{out1}) + R_2(V_2 - V_{out2}) = 0. \quad (3.14)$$

$$g_{m12}V_{out1} + V_{z2}(g_{m22} + g_{ds12} + g_{ds22} + sC_{z2}) + sC_3(V_{z2} - V_3) = 0. \quad (3.15)$$

$$sC_3(V_3 - V_{z2}) + R_3(V_3 - V_{out2}) = 0. \quad (3.16)$$

$$g_{m42}V_{z2} + V_{out2}(g_{ds32} + g_{ds42} + sC_{L2}) + (V_{out2} - V_3)R_3 + (V_{out2} - V_2)R_2 + (V_{out2} - V_1)R_1. \quad (3.17)$$

For the sake of solving the above expressions, the CAD tool Mathematica® was utilized for variable elimination. However the resulting expressions remained overly complex and would not get a simplified form.

3.4 Noise and OTA Nonlinearity

The possible sources of nonlinearities in the circuit include:

- Nonlinear behavior of transistor models.
- Imbalance in CM loop gain, mainly due to transistor mismatches resulting in 2nd and 3rd order harmonics at output.
- Additional HD components contributed by the cross product of differential and common mode signals.

Consider a common mode component V_{CM} at the frequency of the differential signal V_{diff}, then intermodulation term $V_{CM}V_{diff}$ would appear as a second order and differential component at the output.

The designed OTA strives to attain good common mode suppression, but the maximum common mode signal must be kept low. The cancellation of the quadratic components of the individual currents I_1, I_2 help to linearize the output current. However second order harmonics still arise due to transistor mismatches.

Odd order harmonics appear as a result of short channel effects, when effective carrier mobility is no more constant and becomes a function of longitudinal and transversal electrical fields. The MOSFET drain current in saturation region with short channel effects is then approximated [13] as:

$$I_D = \frac{\beta}{2}\frac{(V_{sg} - V_T)^2}{1 + \theta(V_{sg} - V_T)^2)}, \tag{3.18}$$

where $\beta = \mu C_{ox}(W/L)$, $\theta = (1/LE_c) + \theta_0$ and $E_C = \upsilon_{sat}/\mu$. L is MOS channel length, C_{ox} is oxide capacitance per unit area, μ_0 is low electric field mobility, υ_{sat} is carrier saturation drift velocity, and E_C is longitudinal channel's electrical field in saturation region. The addition of θ_0 models the effect of transversal electric field.

The third order distortion in the proposed OTA is approximated as:

$$HD_3 \approx \frac{\theta V_{peak}^2}{16V_{ov}(1+\theta)(2+\theta V_{ov})}. \tag{3.19}$$

Smaller θ provides wider linear range, which could be attained by increasing channel length at the expense of having more parasitic capacitance. Increasing V_{ov} on the other hand, improves the linearity but costs more power.

As mentioned above, third order harmonic distortion components arise also as a result of mixing of differential and common mode components. For the implemented cascaded OTA case, this HD_3 of the output currents is expressed [13] as:

$$HD_{3CMFB} \approx HD_3[1 + |\frac{L}{1+L}|\frac{1}{\theta V_{ov}(1+0.5\theta V_{ov})}] \tag{3.20}$$

$$= HD_3 \times F, \tag{3.21}$$

where $L = A.A_I B$, in which A is the DC gain $A_I = \frac{(W/L)_{3a}}{(W/L)_3} = \frac{(W/L)_{4a}}{(W/L)_4}$, and HD_3 is given by Eq. 3.19. Expression 3.20 shows that F would then be a factor worsening the linearity due to nonlinear components. F is reduced by increasing V_{ov}. Reduction in A_I, however, will also decrease gain of CMFB loop.

Considering only thermal noise from all transistors, the input referred noise density becomes:

$$V_{n-rms}^2 = \frac{16KT}{3g_{m1}} BW[1 + \frac{g_{m2}}{g_{m1}} + \frac{(1 + A_I)g_{m3}}{g_{m1}B^2} + \frac{(1 + A_I)g_{m4}}{g_{m1}B^2}], \tag{3.22}$$

where BW is the equivalent noise bandwidth.

3.4.1 Noise vs. Speed vs. Linearity

An increase in the B factor reduces the contributed noise of output transistors, which in turn increases the effective transconductance and hence the transconductance of CMFB (g_{cmfb}), but worsens phase as parasitic capacitance increases. Notice from Eq. 3.20 that increasing B increases F, which is a noise-linearity trade-off and is highlighted graphically in Fig. 3.8. Finally, maximizing the g_{m1} as well as ratio B, reduces the noise contribution, as evident from Eq. 3.22.

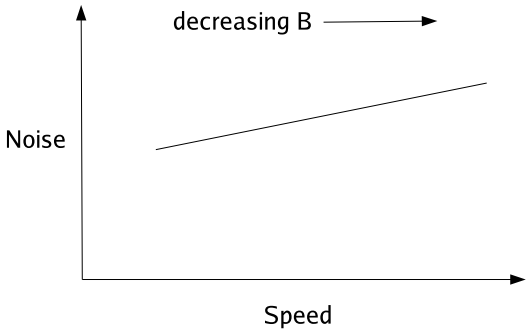


Figure 3.8: Increased sizing factor 'B' in OTA results in low speed, while reducing noise contribution.

Chapter 4

Behavior Level Video PGA Modeling

The PGA in consideration, needs to buffer, amplify or attenuate, maintaining a specific bandwidth and linearity that satisfies the targeted video standards. This underscores the need of a having an operational transconductance amplifier, which provides the required linearity and bandwidth among others. The fully differential implementation of this OTA, is programmable by means of external components.

The Fig. 4.1 shows a fully differential buffer in which gain is controlled by the input and feedback resistors. One finds out the following distinct disadvantages in a resistive architecture.

- Charge stored in input nodes of OTA would ultimately leak away through path provided by feedback resistors.
- The resistive load adds more to the total noise contributed.
- Bad accuracy of time constants.

Fortunately, since the early 70's analog sampled data techniques were introduced which emulated the resistor with MOS switches and capacitors [17, 18]. The replacing switched capacitor variants have several advantages, including:

- Compatibility with CMOS technology.
- Good accuracy of time constants.
- Better voltage linearity and temperature characteristics.

However SC circuits come at the cost of non-overlapping clock generator, clock feedthrough in switches and the condition on input signal to be less than the sampling clock frequency [20].

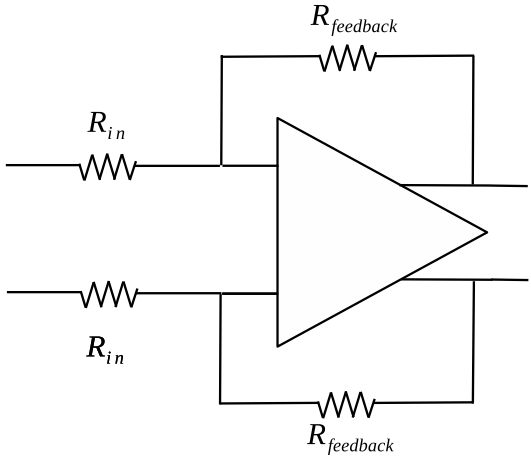


Figure 4.1: A fully differential amplifier with resistive feedback.

4.1 Resistor Emulation by Switched Capacitor Circuits

Its been established [20, 19] that a resistor can be emulated by a switched capacitor circuit, by concepts of charge transfer among capacitors.

Table. 4.1 summarizes the equivalent resistance of a series of switched capacitor variants providing resistor emulation. The emulated resistance in all cases is inversely proportional to the capacitance.

SC circuit	Equivalent Resistance
Parallel	T/C
Series	T/C
Series Parallel	$T/C_1 + C_2$
Bilinear	T/4C
Negative Transresistance	-T/C
Positive Transresistance	T/C

Table 4.1: Switch capacitor circuits providing resistor emulation.

When combined with an OTA to make an SC integrator, all of the above schemes realize the transfer function whose gain coefficient depends upon the capacitor ratios. However, the first four of the schemes used above are parasitic sensitive and may cause considerable inaccuracy in the final transfer function. Fortunately the 'negative transresistor' and 'positive transresistor' are switching schemes that realize parasitic insensitive buffers. The positive transresistor realizes an inverting delay-free buffer, whereas the negative transresistor is a non-inverting delaying buffer [20].

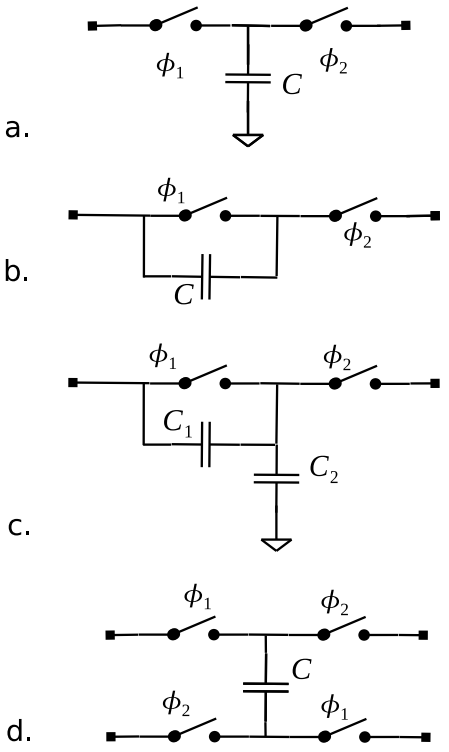


Figure 4.2: Switched capacitor circuits (a) parallel (b) series (c) series-parallel (d) bilinear.

4.1.1 Switches in Signal Path

One would want to remove as many switches from the video signal path as possible. So its more feasible to choose a negative transresistor switch, which has only one switch in the video signal path. Within the digitizing channel, one can further hope to merge or shift this switch towards the clamp circuit too, if possible.

Finally, the feedback loop SC scheme is a slightly modified version of series SC circuit. The clock ϕ_2 has been kept switched on, which means one can remove this switch altogether, finally creating a scheme shown in Fig. 4.4.

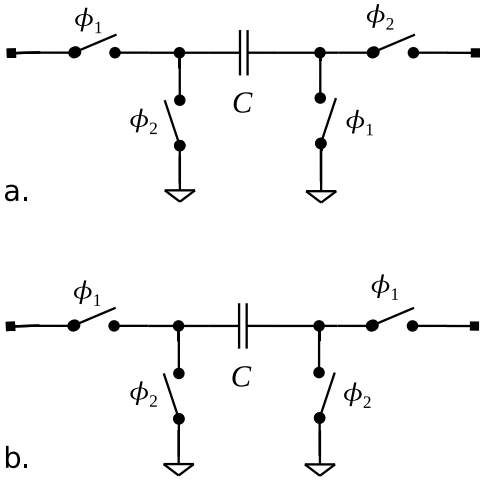


Figure 4.3: Parasitic insensitive switched capacitor circuits, (a) negative transresistor (b) positive transresistor.

4.2 Analysis of Switch Capacitor PGA Switching Scheme

It is imperative to analyze the identified SC switching scheme, with the intention to obtain a close loop transfer function.

Using charge analysis on the sampling and feedback capacitors at both clock phases, and starting at time period t (clock phase 1):

$$q_1(t) = C_1 \cdot (Vin(t) - 0), \tag{4.1}$$

$$q_2(t) = C_2 \cdot (0 - 0). \tag{4.2}$$

At time period $t + \tau$ (clock phase 2):

$$q_1(t + \tau) = C_1 \cdot (0 - 0), \tag{4.3}$$

$$q_2(t + \tau) = C_2 \cdot (Vout(t + \tau) - 0). \tag{4.4}$$

At time period $t + 2\tau$:

$$q_1(t + 2\tau) = C_1 \cdot (Vin(t + 2\tau) - 0), \tag{4.5}$$

$$q_2(t + 2\tau) = C_2 \cdot (0 - 0). \tag{4.6}$$

Due to charge conservation, the charge on the two capacitors cannot disappear, as the capacitors cannot discharge themselves via OTA terminals. Hence, we can

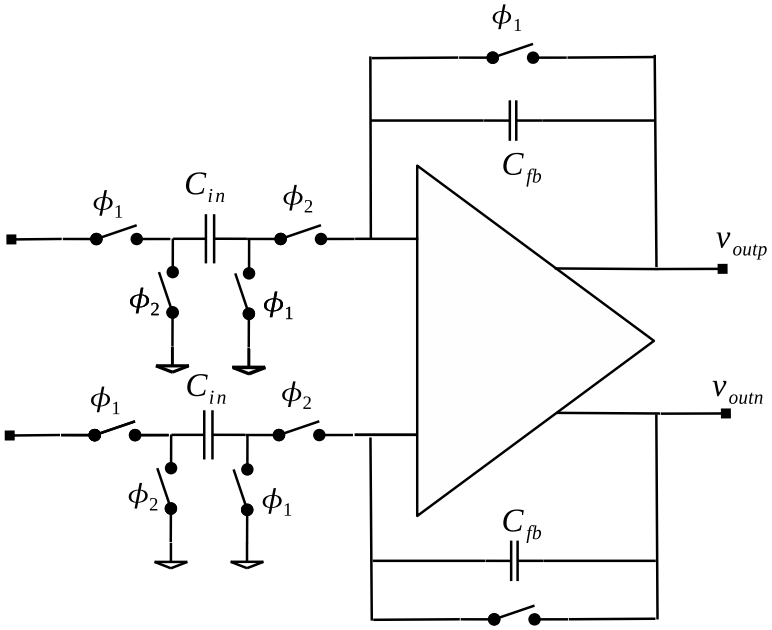


Figure 4.4: PGA refresh scheme.

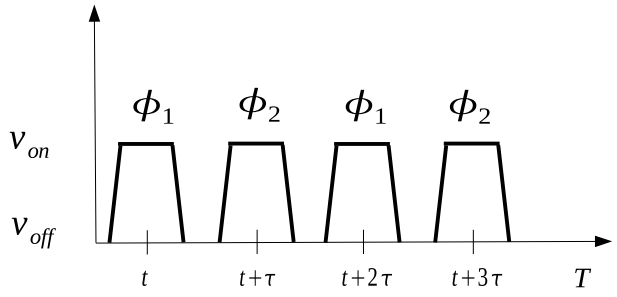


Figure 4.5: Clock phasing scheme used during charge analysis.

obtain another expression:

$$q_1(t) + q_2(t) = q_1(t+\tau) + q_2(t+\tau). \tag{4.7}$$

Since sampling period $T = 2\tau$ and $t = kT$. Substituting these into Eq. 4.7 yields,

$$C_1 \cdot \ Vin(kT) = C_2 \cdot \ Vout(kT + T/2). \tag{4.8}$$

Applying Z-transform on both sides of above expression:

$$C_1 \cdot \ Vin(z) = C_2 \cdot \ z^{1/2} \cdot \ Vout(z), \tag{4.9}$$

$$H(z) = \frac{Vout(z)}{Vin(z)} = \frac{C_1}{C_2} z^{-1/2}. \tag{4.10}$$

The delay in the transfer function of Eq. 4.10, delays the signal, but does not deteriorate the video quality and PGA gain setting depends solely on the values of the two capacitors.

The next sections look into sampling rates, the minimum capacitor size and finally a higher level OTA model, to successfully simulate the suggested PGA.

4.3 Oversampling in Video PGAs

The specific circuit being looked at, is a kind of pseudo switched capacitor. During the horizontal sync period amplifier is pre-charged to prevent drifting. After this, the amplifier is operated in continuous-mode over the entire horizontal line until next (horizontal) sync.

The PGA targets the highest video bandwidths up to 30 MHz from HD video specifications. By sampling at 300 MS/s, there is a 10× oversampling ratio.

From the linearity point of view, the system actually subsamples. By sampling at 300 MS/s, the high input bandwidth allows the signal above Nyquist to get folded. The reason for this high bandwidth is to guarantee a very low signal attenuation at signal frequencies below 300/2 MS/s (which is Nyquist for this case). A video system is sensitive towards group delay, phase delay and signal distortion through attenuation.

4.4 Noise Considerations and Minimum Size of Capacitor

Fig. 4.4 showed the switching scheme with sampling and feedback capacitors. A buffer could well be realized with capacitors on the order of a few femtofarads or as large as some pF. This section addresses limitations on the minimum capacitor size required, with the help of the example case.

The video PGA is going to feed the differential signal to the 12-bit TI-PSAR ADC, which, in the ideal case achieves a signal to noise ratio of 74 dB [19]:

$$SNR_{ideal} = 6.02N + 1.76 = 74\ dB. \tag{4.11}$$

where N denotes no. of bits deciding ADC resolution. In a real ADC, this could be less than 70 dB due to circuit limitations.

For a low voltage OTA, if the the output signal swing is 1 V for a 1.2 V supply, then RMS voltage would be:

$$V_{rms} = 1\ V/2\sqrt{2} = 0.35\ V. \tag{4.12}$$

The total RMS noise is then calculated as:

$$V_{n(rms)} = \frac{0.35}{10^{74/20}} = 69.8\ \mu V. \tag{4.13}$$

In a switch capacitor circuit, a sampling capacitor accumulates noise generated by the switch, as the inherent bandwidth is more than half the sampling frequency. The total noise power is equivalent to $K.T/C$, independent of the 'on' resistance of the switch, where K is Boltzmann's constant and T is temperature. Noise in the signal band is [15]:

$$V_n^2 = 2.\frac{K.T}{C}, \tag{4.14}$$

where, a multiplication by '2' indicates that $K.T/C$ noise within the signal band has been doubled, due to fully differential design [15].
Solving for C, yields a minimum bound on capacitor size and is calculated to be 1.69 pF for this example.

4.5 Developing a Higher Level OTA Model

Initially, a single pole simulation model of the OTA was developed, to keep the system simpler and stable under all conditions.

$$\omega_{p1} = \frac{1}{R_1 C_1}.$$

In this model, both the positive and negative input signals were multiplied to get the gain, as $A = g_m.R_1$, and was provided by the ideal voltage controlled current source ($vccs$). Resistor R_1 and capacitor C_1 provided the first pole on both ends. Finally, it was subjected to differential conversion, ridden on a common mode voltage of 0.6 V by a fixed DC source. The model is drawn in Fig. 4.6.

4.5.1 Single Pole OTA Model

This OTA model was further simulated as a 'multiply-by-2' SC circuit, to realize a higher output voltage, in a low voltage application. So a 2 V output voltage was possible at a 1 V supply. As a final step, the OTA model was simulated with much required switched capacitor CMFB circuit.

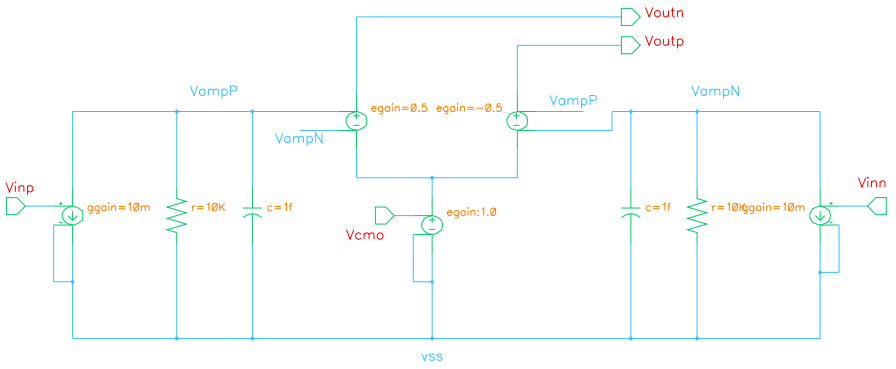


Figure 4.6: Single pole OTA model.

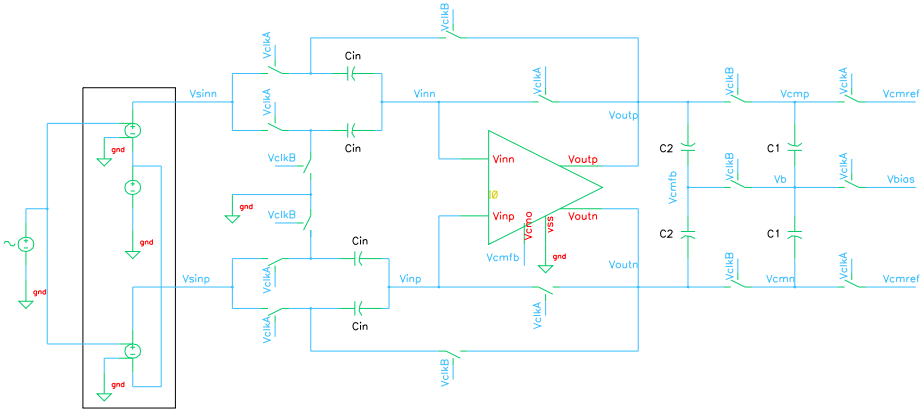


Figure 4.7: A testbench for the single pole OTA, with a 'multiply-by-2' and switched capacitor CMFB circuits.

The simulation results of the model at this point encountered convergence issues, giving incorrect output values. It was concluded, that the OTA model needed to realize common mode feedback control, to show better convergence. This gave rise to a more improved OTA model described below. The complete testbench used with the SC-CMFB block is shown in Fig. 4.7.

4.5.2 Enhanced OTA Simulation Model

Various approaches were tried to model the two pole OTA to include the CMFB characteristic. The model shown in Fig. 4.9 evolved as a series of improvements upon the basic model. It may be mentioned, that developing a model encompassing all real OTA characteristics such as voltage limiting, offset, etc., was not the intention, and a simpler working model with basic characteristics, enough as a proof of concept with the PGA switching scheme was required.

An improved simulation model of OTA comprised of the following additional features:

- Common mode feedback mechanism as a feedback input from the sensing block.
- Realization of a two pole OTA.
- Slew rate limitation.

4.5.3 The Current Limiting Model

Fig. 4.8 shows the subcircuit used in the new OTA model, to realize the slew rate limitation.

The four diode circuit defines a limit on the maximum current that can pass through the OTA. All the diodes conduct (forward biased) when input current I_o remains less than I_{limit} defined by fixed current source, and I_o appears at the output. When the input current $0.5I_{in}$ (in upper branch) becomes equivalent to $0.5I_{limit}$, the other two diodes D2 & D3 get reverse-biased, hence limiting the current at the output. When the current is negative, the pair of D2 & D3 conducts and D1, D4 pair becomes reversed biased.

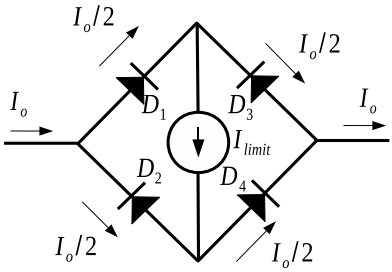


Figure 4.8: The current limiter model subcircuit in enhanced OTA model.

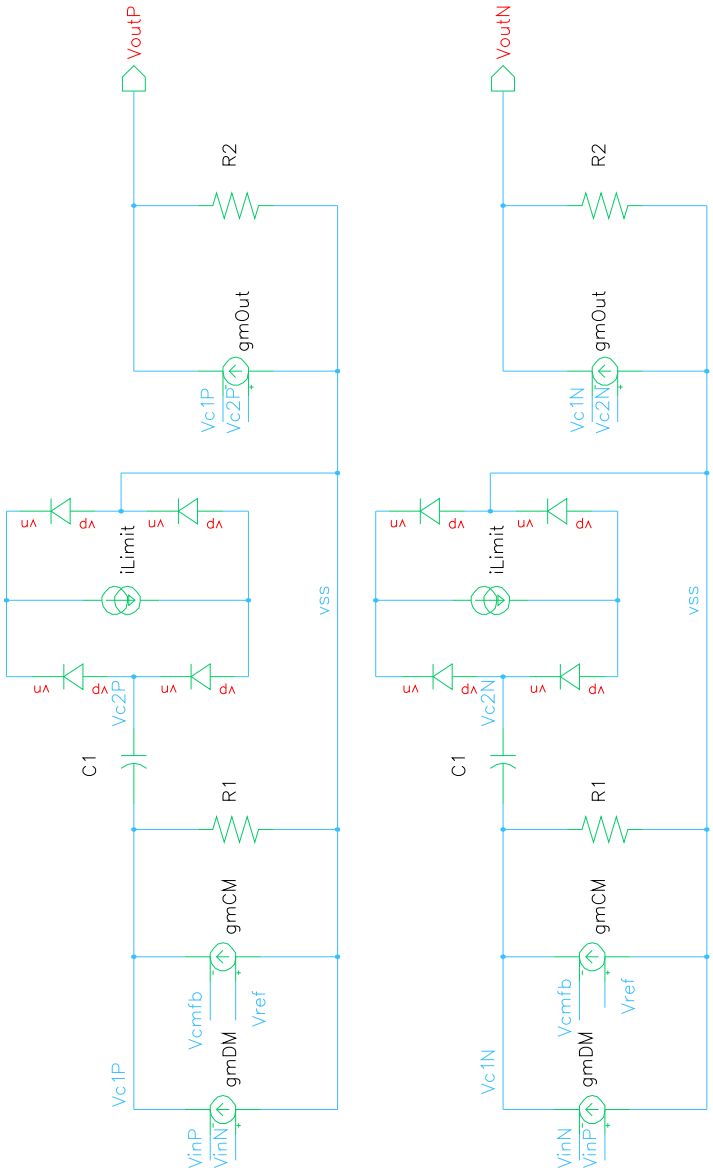


Figure 4.9: Enhanced OTA simulation model.

4.5.4 Designing Enhanced OTA Model

The model starts by fixing the capacitance value, to compute the slew rate of the OTA by the relation:

$$SR = I_{max}/C. \tag{4.15}$$

Hence for a slew rate of 250 V/μs, and a capacitance value (which will also influence the first pole), the value of fixed current source was determined. An I_{max} value of 250 nA was obtained for 1 fF capacitor.

The value of the resistor R_1 chose the gain as A_1=Gm_{DM}.R_1, as well as determining the location of the first pole for $\omega_{p1} = 1/R_1C_1$. The first pole was set at 500 KHz.

An ideal voltage controlled current source realized, what the common mode feedback does in a fully differential amplifier. The difference of ideal reference voltage V_{ref} and feedback common mode voltage V_{cmfb} (marked V_x) decided the additional amount of current, if any, to settle the output node. Common mode gain A_{cm} was determined by this differential gain and the pole resistor A_{cm}=Gm_{CM}.R_1

The gain in the second stage had been kept to unity, but one can also distribute the total gain in a series of two stages.

Finally, it may be noticed that gain to differential input signal $V_{inP} - V_{inN}$ was computed in both pairs (twice), adding a 6 dB to the gain computed above. Hence, one could keep the gain to half of desired gain in Gm calculation above.

Fig. 4.10 shows the transient and AC simulation plots for the designed OTA model with a 60 dB gain.

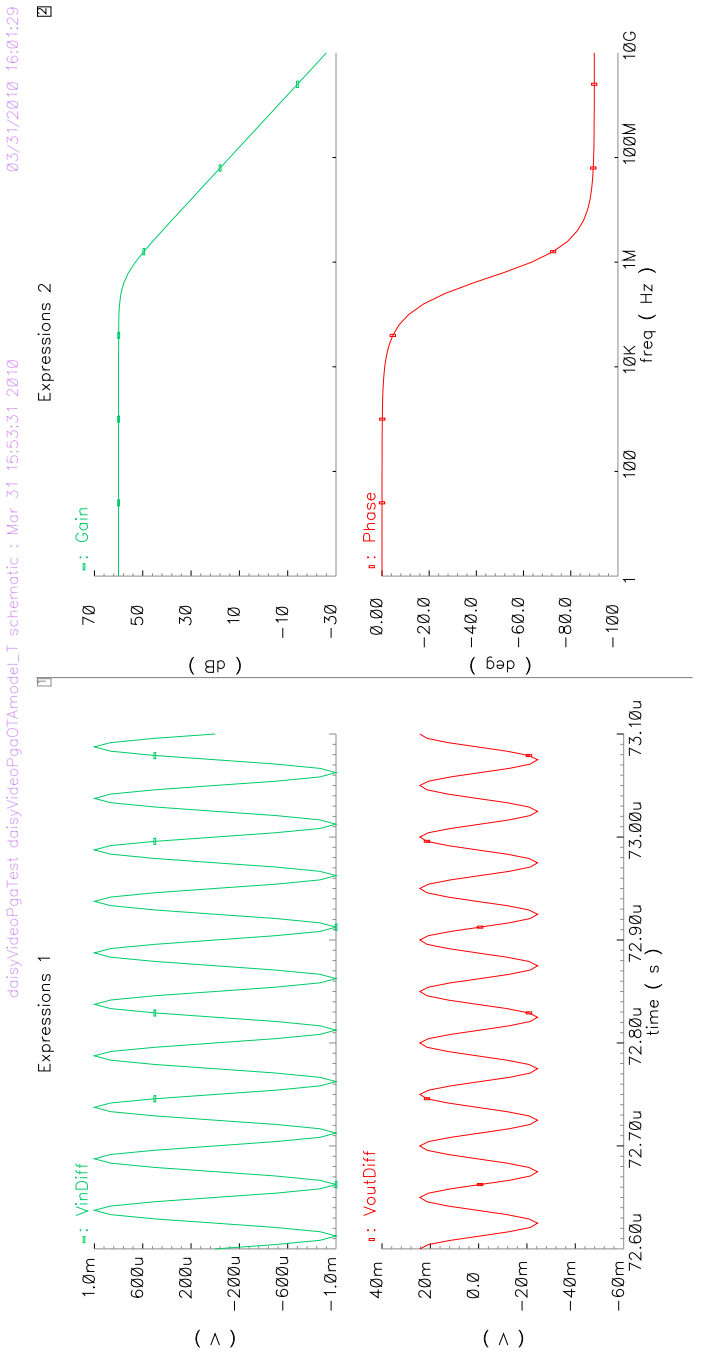


Figure 4.10: OTA model simulation.

4.6 Modeling a Switched Capacitor Video PGA

One needs to take into consideration how this SC OTA model could settle in a video AFE. A video signal has picture information during the active line duration of the signal which must be preserved without distortion. Hence, no switching may occur in the PGA scheme during the active signal, leaving behind the horizontal blanking interval only. As mentioned in Fig. 1.5, the back porch duration has color burst in some formats, so either the front porch or the sync-tip interval could be employed for switching and pumping in enough charge until the next sync pulse.

Then resulting PGA would act like a capacitive feedback amplifier during the active video line duration as shown in Fig. 4.11. During the sync-tip duration it pumps in charge, as derived earlier and shown in Fig. 4.4.

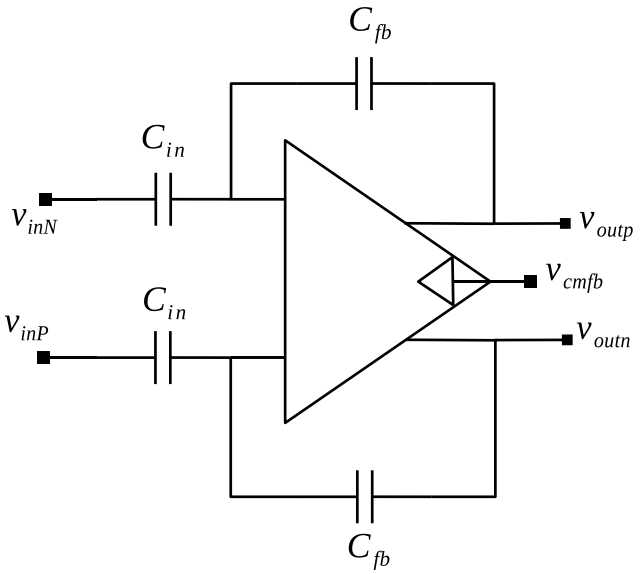


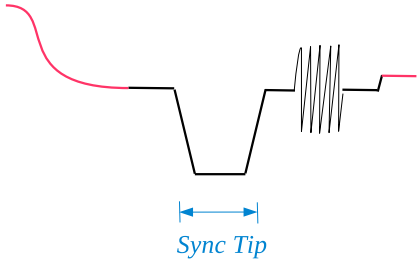
Figure 4.11: PGA as a capacitive feedback buffer during active video signal.

4.7 Sync-Tip Compensation - an SC Level Shifter

As a video AFE designer, one would want the ADC to avoid ever dealing with the sync-tip duration of the video signal. In other words, the ADC should only see the active video signal, which it has to digitize, omitting the 300 mV trench of sync pulse. This would help improve the dynamic range of the ADC.

One notices, that in the real world the input signal would be single ended, and non-inverting PGA input could be employed for this level shifting.

This is achieved in the following way:



- During the sync-tip interval an additional switch pulls the, say −40 IRE or −300 mV sync-tip, to an equal blanking level of 0 IRE.
- During active video time, instead of −300 mV level, a common mode voltage of 350 mV is ridden over the non-inverting PGA input. This is to provide the video signal (0−700 mV) an equivalent common mode point.

The testbench in the next section shows the switching scheme with the sync-tip compensation.

This voltage level of 300 mV needs to be specifically defined on the chip, and has been adjusted for, by a programmable DAC, generating the offset and sync-tip compensation voltage. The scheme has been implemented as one DAC generating both the offset voltage and the sync-tip voltage, and is reprogrammed during an interval shorter than the hsync pulse.

4.8 Simulation Testbench of the PGA Switching Scheme

The finally realized PGA switching scheme, is shown in Fig. 4.12. Notice that switched capacitor feedback has been utilized to arrange for CMFB. The simulation results of this testbench are presented in Fig. 4.13.

The input video signal (yellow) having a −300 mV sync-tip was generated using ideal components, while the equal amplitudes of input and output differential signals (represented in purple and orange) suggest a 1× gain setting. The two non-overlapping clocks ϕ_1 and ϕ_2, are visible only during the sync portion, as clocks must not switch during active video portion. Hence, one hopes that enough charge has been pumped in, during the sync interval to retain the correct level of the PGA circuit until next sync pulse.

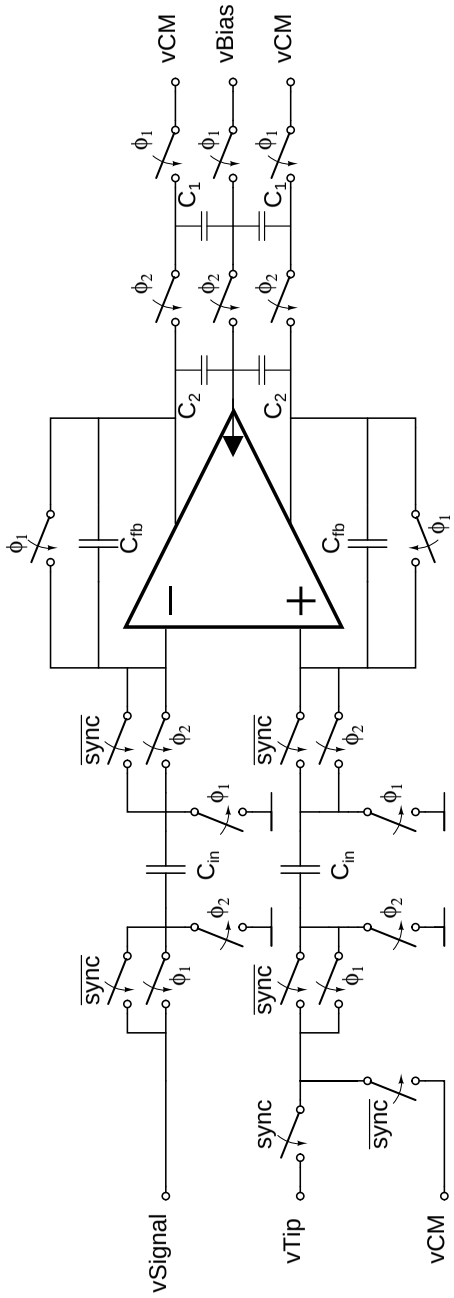


Figure 4.12: The final switching PGA with sync-tip compensation and SC-CMFB circuits.

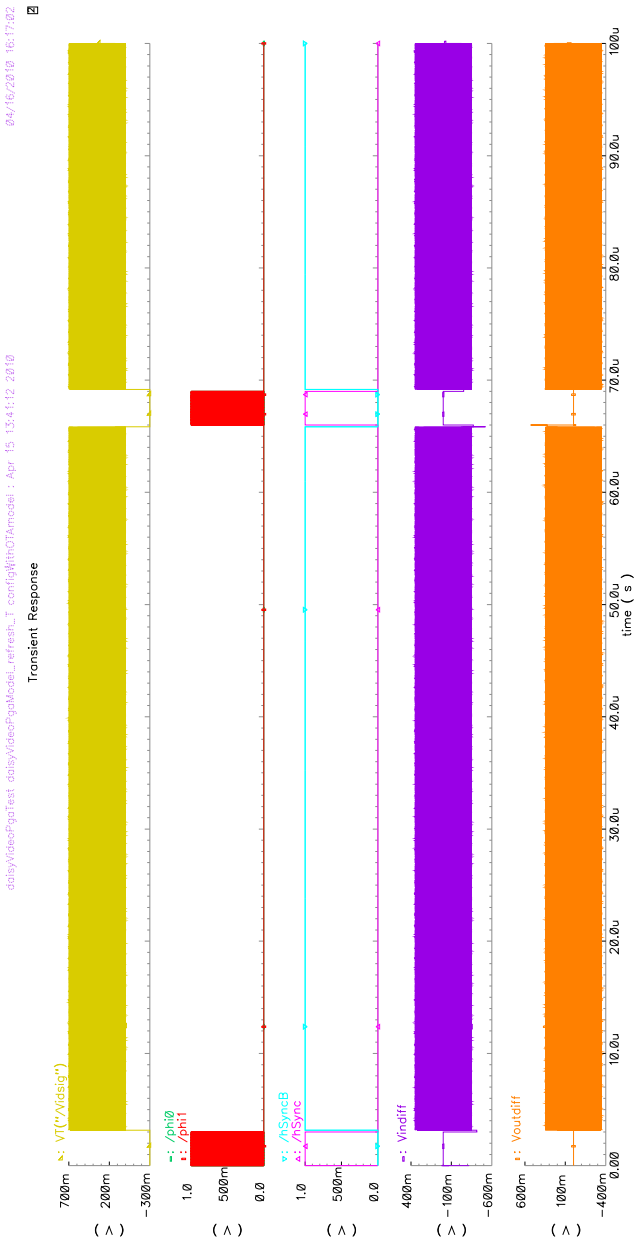


Figure 4.13: The final simulation results highlighting a sync-tip compensated buffered differential output, simulated input video signal, sync pulses and non overlapping clocks.

Chapter 5

Transistor Level Design

The primary motivation behind choosing the architecture proposed by AMSC group at Texas A&M [13], was to be able to reduce the supply voltage to 1.2 V or lesser and maintain high signal swing eventually. The target process was chosen to be an available 65 nm digital CMOS process. This section intends to address the implementation details of this OTA in the 65 nm CMOS process.

5.0.1 Modern Trends in Low Voltage Analog Design

Designing a low voltage OTA in a process where short channel effects change the known transistor expressions considerably becomes somewhat challenging. The cookbook methods of obtaining an OTA such as the V_{dsat} method [20], which are more applicable for long channel drain current expressions, no longer hold. This is especially true when the supplies are lower. The reason behind this problem is the reliance on common mode range (CMR), which in case of lower supplies, often become more than the supplies themselves. Hence it cannot be adopted for low voltage, short channel process.

Certain methods have been published such as g_m/I_D methodology [21] for the synthesis of CMOS analog circuits. However, it relies on the availability of 'early voltage' of transistors, whose accurate modeling itself has remained a topic of discussion and many models may deviate from the true early voltage [26]. Yet many have claimed better designs using this methodology on analog and RF blocks [22, 24, 23]. Regardless of this method, the g_m/I_D parameter itself, is indeed a strong candidate to classify the performance of analog circuits.

On the other hand 'inversion coefficient', originally introduced by the EKV MOS model [14], emerged as a strong parameter of a transistor, being able to express all transistor parameters in terms of one inversion coefficient. It covered all regions of operation of the transistor operating plane, suggesting its optimum use at a particular operating point.

Just like the traditional analog design hexagon Fig. 5.1 explains the analog performance of a MOSFET, having a particular channel length and drain current, operated at an optimal inversion coefficient accordingly with its application.

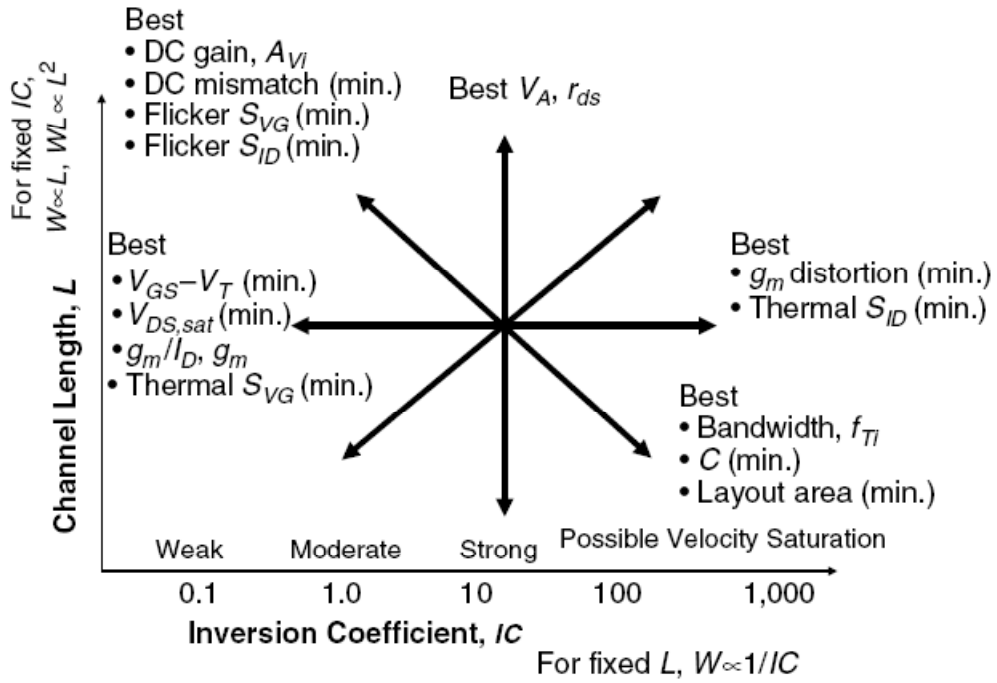


Figure 5.1: MOS analog performance trade-offs for any MOSFET of fixed current, channel length and selected inversion coefficient [25].

With the above mentioned limitations, we encounter our low voltage PGA design in a short channel process, starting from process features and addressing next, the implementation issues emanating within.

5.1 The 65 nm CMOS Process

The CMOS process offers the following distinct features:

- 65 nm poly length.
- Dual and triple V_t MOSFETs.
- Dedicated process options for low power and high speed.
- Core supply of 1 V and 1.2 V with available supply options of 1.8 V and 2.5 V.
- Six to ten metal interconnect layers.

As mentioned above, this 65 nm CMOS process library offers a range of MOS devices where apart from the standard versions are available MOS devices for high speed (low V_t), low power and variable supply options as well as RF, high voltage and unsalicided devices.

Choosing the right transistor

It was determined early during the design phase, that gain in MOS devices in this process was considerably low, hence the foremost target was to select a device with highest gain.

The choice of MOS model from CMOS device library was the 'high performance analog-low power', as an assumed model for showing better analog performance. However when gain becomes a bottleneck, to determine better gain characteristics in the absence of device datasheets, one can probably rely on a comparison of g_m/I_D vs. V_{eff} device characteristics, biased from a fixed current source with similar aspect ratios (W/L).

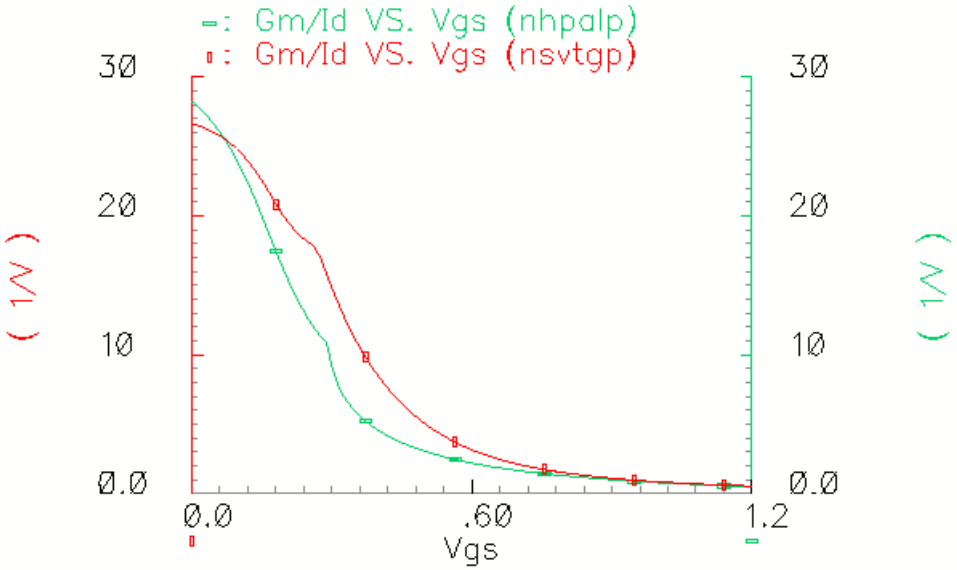


Figure 5.2: Comparison of g_m/I_D vs. V_{eff} curves of two MOS devices.

Device wrapper

The transistor model in the CMOS library is actually a subcell consisting one transistor and two diodes. Hence *m1* is vendor's internal notation for a transistor, whereas *d0* and *d1* are diodes. The reason for these is to have a subcircuit wrapper around the transistor model card call, such that one easily add default values and modify fingers, widths, diodes, etc.

5.2 OTA Design in 65 nm CMOS

The OTA architecture described in chapter 3, is implemented here. Initially, design of OTA with common mode feedforward is described, and later extra CMFB transistors are added. Finally the two cascaded blocks are integrated, and targeted simulation results are addressed.

5.2.1 Design of OTA with CMFF

One usually starts designing the OTA with the specifications on maximum allowed current consumption; then from the relation:

$$I_D = SlewRate \cdot C_{comp}. \tag{5.1}$$

The current consumption is decided first, which fixes the compensation capacitor C_{comp} early in the design procedure, to achieve required phase margin. However, in our case, it was initially not assumed that gain target of 60 dB would span on two cascaded stages. The need for compensation could have been circumvented if the parasitic capacitance C_z had kept the dominant pole away from the second pole, keeping the OTA stable.

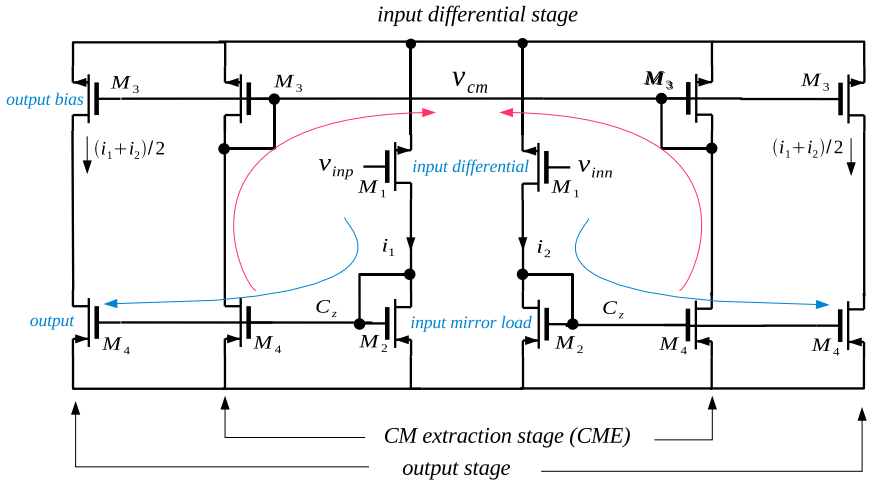


Figure 5.3: The low voltage OTA with CM extraction and differential path explained.

With a current budget of 10 mA, one can drain about 5 mA per OTA structure. To begin the design, a few considerations were kept in mind to keep the design simple:

- One can burn about 1 mA per gain stage initially and lower this consumption later in the input differential and common mode stages substantially.

- A large feedback inductor tied to the input fixes the output DC point which helps optimize the other parameters without worrying about DC levels.
- One may take similar sizes of all push and pull devices as a starting point.

Before furthering the design guidelines of the OTA, two distinct observations were:

- Due to the absence of tail current source, with fixed V_{eff}, the input width remains the sole current controller in the input stage.
- The mirror width of the input stage sets the V_{eff} of the common mode and output stages.

The considerations for the OTA design are as follows:

- The push currents in common mode extraction stage (CME) and output stage were eventually kept as ratios of the input current, set through input width.
  This is shown specifically in Fig. 5.4, where input stage current is I_x, the CME stage current is mirrorRatio1$\times$ I_x, while output stage push current is mirrorRatio2$\times$ I_x. If output bias device has a sizing ratio mirrorRatioP, then mirrorRatio2 is equivalent to mirrorRatioP $\times$ mirrorRatio1, which sets output stage pull current.
- Since $g_m/I_D \propto 1/V_{eff}$, to maximize the gain from the output stage one decreases the V_{eff} of the output device, while maintaining its operation in saturation.
- Gain can surely be improved by increasing channel length, but one needs to be careful for the reduced bandwidth with increasing lengths. With an initial $2.5L_{min}$, the eventual channel length was set at $10L_{min}$.
- Some output gain stages are of push-pull configuration. In such a case the total gain (g_m) of that stage is:

$$\frac{g_{m_p} + g_{m_n}}{g_{ds_p} + g_{ds_n}}. \tag{5.2}$$

  This particular output stage is not a push-pull configuration and since the g_m of the bias transistor does not play any role for gain, one could reduce size to minimize coupling from bias. Such a technique would have its typical trade-off in terms of reduced swing since $g_m \propto 2I_D/V_{eff}$

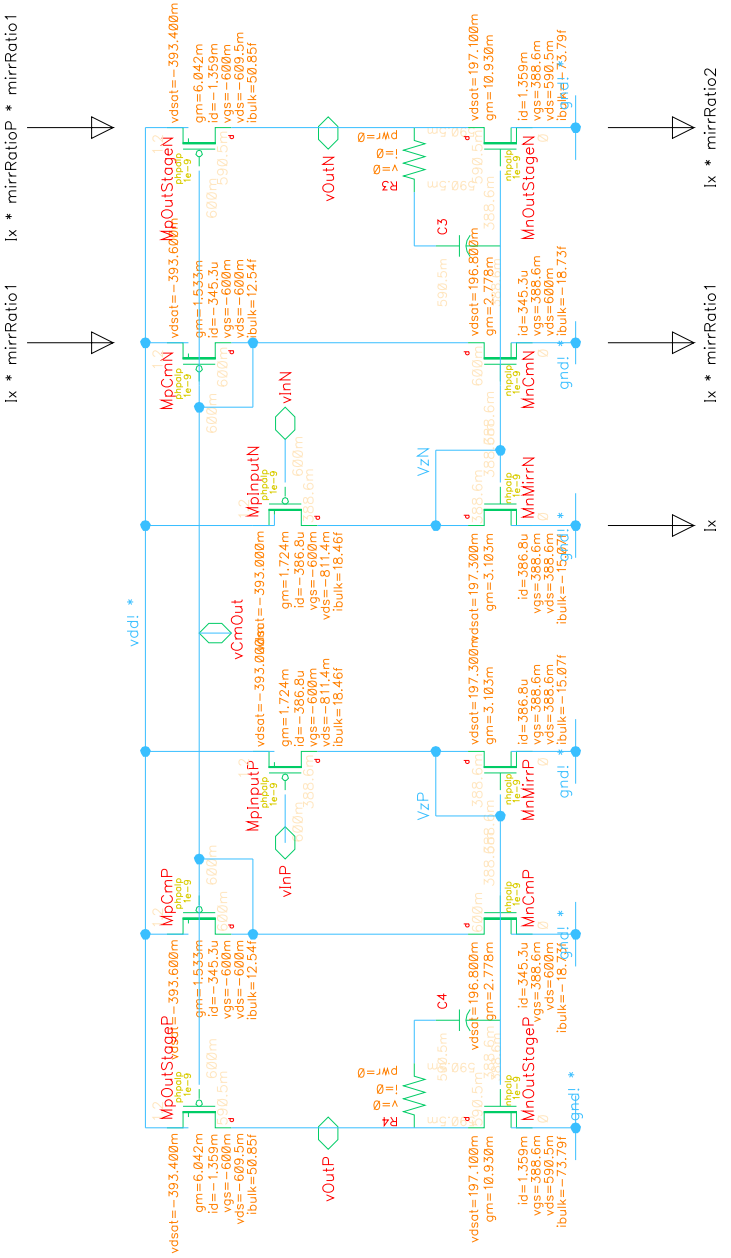


Figure 5.4: The designed OTA with annotated g_m, currents, and voltage levels.

5.2.2 Achieved Specifications for OTA (with CMFF only)

The specifications for the uncompensated OTA designed, are summarized in Table. 5.1.

Gain	28.5 dB
Phase Margin	36°
Unity Gain Frequency	767 MHz
Slew Rate	1240 V/μs

Table 5.1: Achieved specifications on low voltage OTA with CMFF.

As evident, the OTA's DC gain is far off from target and multiple stages are surely required to attain the target gain. A maximum of factor 8 gain is available per gain stage, in this process.

The two poles are fairly close by to destabilize the system. Bandwidth is also much less than the target.

Since the architecture already relies on another stage, we decide to first design the OTA with CMFB devices, cascade it with this block, and then re-address all issues in considerations with the target OTA specifications.

5.2.3 Designing the OTA Structure with CMFB Devices

The OTA structure with CMFB, as shown in the Fig. 5.6, is essentially the same with the exception of four added transistors to the previous OTA, and a reference current mirror.

While designing this stage, some distinct observations were:

- Stabilizing the output DC point here, is easier than previous OTA (with CMFF only), as it had no current control. In this structure one sets the optimum output DC point of the OTA by sweeping the width of feedback CMFB devices.
- The current mirroring devices controlled by voltage V_{ref} have been kept low on current, of the order 300 μA.
- The currents in the two feedback devices are similarly kept low at $\approx$ 300 μA.

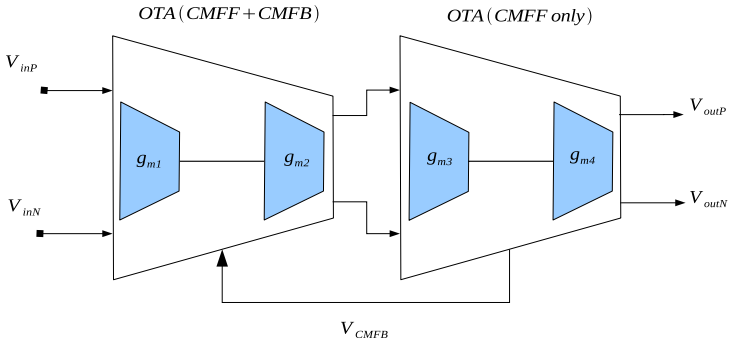


Figure 5.5: A pair of cascaded OTA required to provide CMFB.

5.3 Cascading OTA Structures

When the two blocks are cascaded, some immediate observations are:

- Gain target of 60 dB gets achieved, and one may target even higher.
- Due to four poles the system is highly unstable.

Of course the OTA was not yet compensated and a bad phase margin was expected.

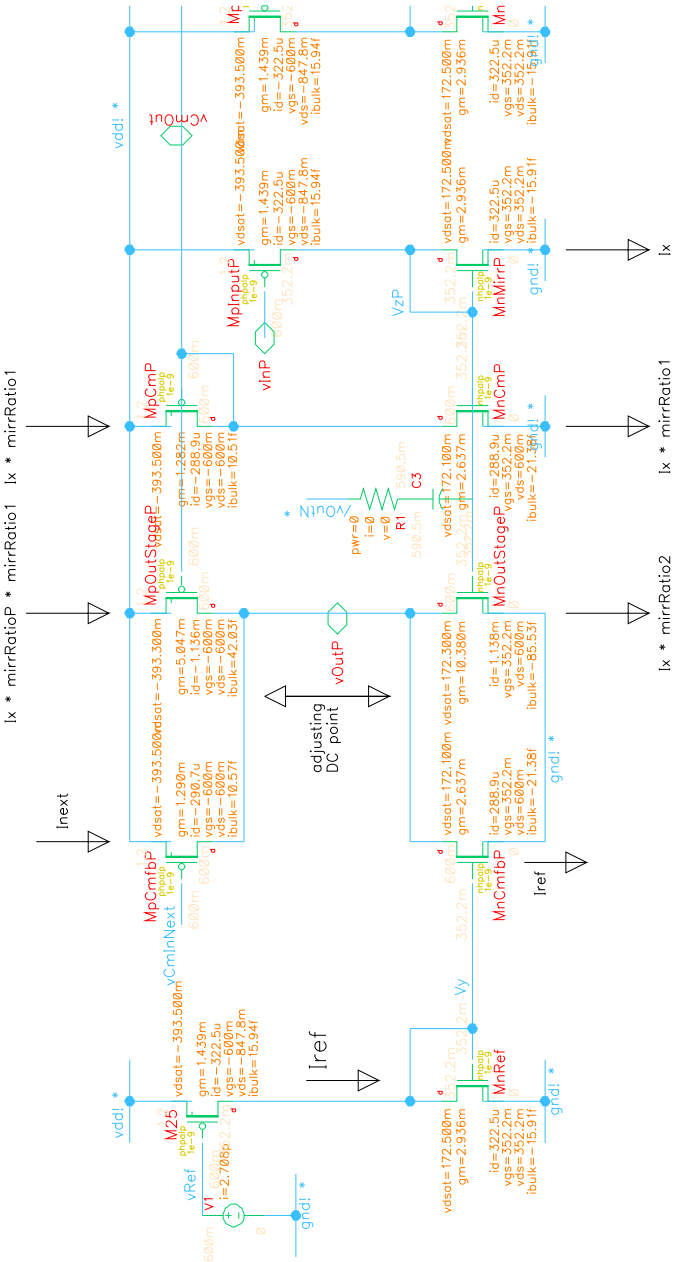


Figure 5.6: One half of OTA with added CMFB devices, with annotated operating points, currents, g_m of transistors.

5.4 Nested Miller Compensation

Two of the four poles are located close by and are contributed solely by parasitics in the mirror node. In case of cascaded stages, a third pole is also introduced by parasitics of first output stage, deteriorating the PM further. The fourth one is contributed by the load capacitance.

In order to stabilize the OTA, one needs to identify a compensation scheme. Even with multi stage cascaded amplifiers one can resort from simple Miller compensation to more novel ways to compensate like 'No Capacitor Feedforward Compensation' proposed in [16].

Since feedforward mechanisms may increase the power budget, and may also not suit the architecture, a simpler Miller compensation has been resorted to. However, one needs to choose nested Miller compensation with feedback to output from every stage.

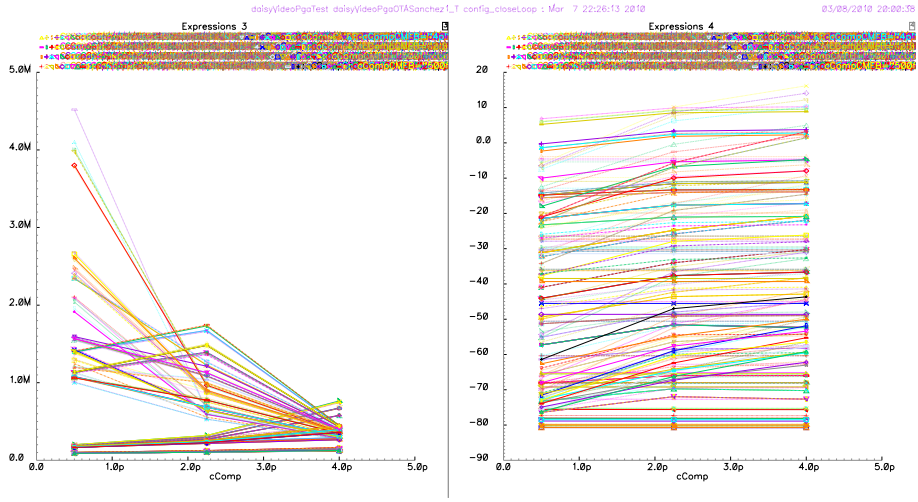


Figure 5.7: Parametric plot of phase margin and bandwidth.

A parametric analysis was run to check the architecture limits, if in case attaining a phase margin of 45° was ever reachable. A quick 729 points analysis over 6 variables of 3 Miller caps and 3 series compensation resistances revealed that larger caps up to 4 pF were not enough to guarantee a stable system. In this situation, some other tricks were needed to stabilize the system.

5.4.1 Reducing Output Capacitance

One could introduce a common drain type buffer, to reduce the load capacitance. This will shift one of the poles caused by output load capacitance to a new location, yet introducing another pole by input buffer capacitance.

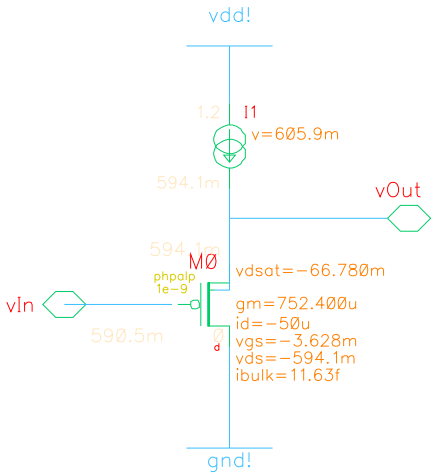


Figure 5.8: The common drain buffer used to reduce capacitance.

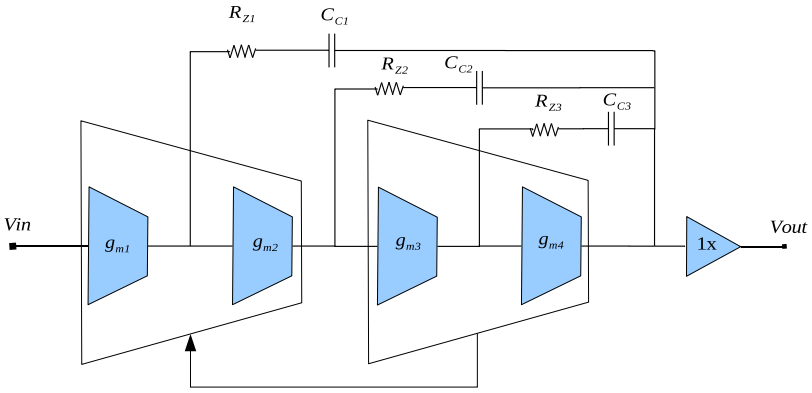


Figure 5.9: Nested Miller compensation with an output buffer.

Introduction of this technique worked well and without any other significant change the buffer guaranteed a stable system on the expense of bandwidth. This is shown in Fig. 5.10, where the dark green curve indicates bandwidth achieved after buffer addition, as against original purple curve.

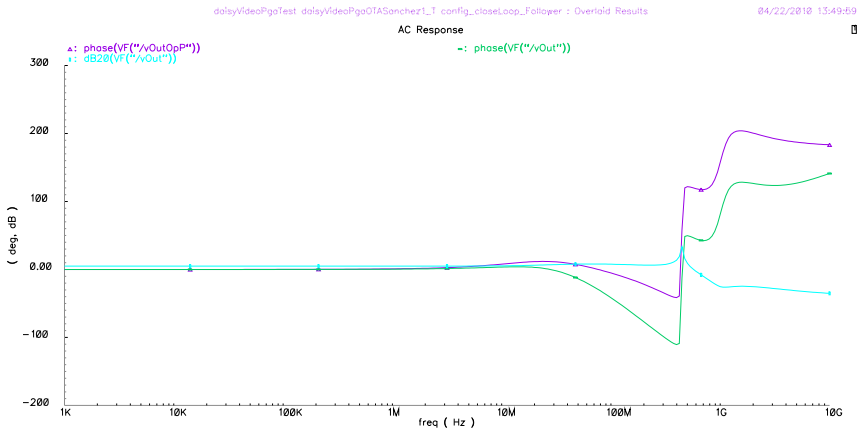


Figure 5.10: Reduction of significant bandwidth by source follower.

5.4.2 Standard Expressions - Unreliable

In the presence of several poles and zeroes, one needs to be careful before trusting the the standard expressions. For instance, reported phase margin may not be the correct measure. This is because, sometimes the phase margin actually becomes more than 90°, due to zeroes in the transfer function. The optimizer or parametric analysis results may also become less meaningful due to this. One should look at the phase curve instead of totally relying on expressions in such cases. An example of such results is shown in Fig. 5.11.

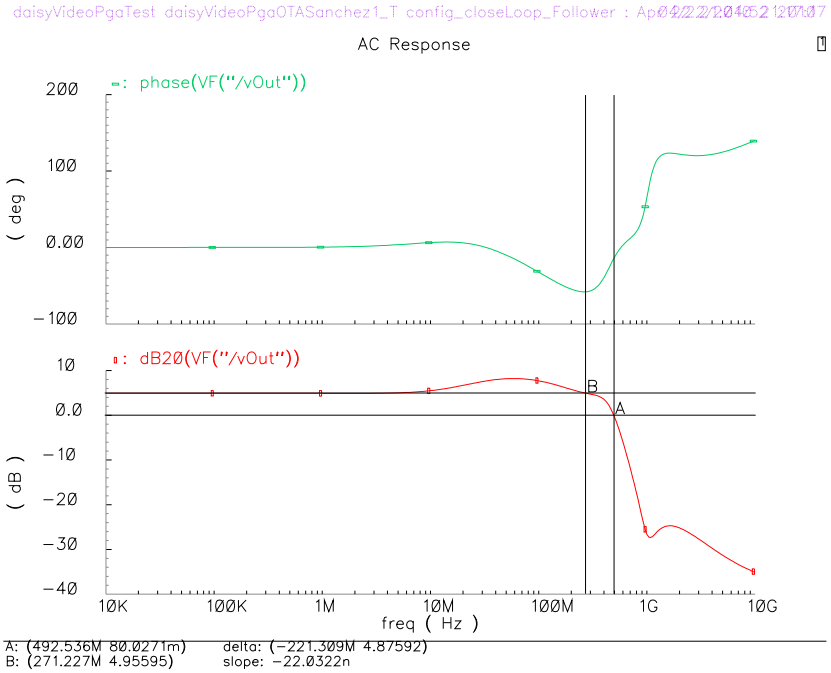


Figure 5.11: Reliance on expressions leading to wrong results.

5.5 Noise Analysis

The PGA specification puts a maximum limit to the noise that can be tolerated in the design. It should be less than 0.5 LSB. This suggests a maximum total integrated noise level of −88 dB. With this maximum limit, noise analysis was run over the entire design of 28 MOS transistors, three Miller resistors and ideal switches. The noise summary is as follows:

Total Integrated Noise = 0.39 $\mu V^2/Hz$ = −76 dB.
MOS noise contribution

MOS pair	OTA	Contribution
Input differential (M1)	CMFB	52.64%
Input mirror (M2)	CMFB	20.54%
Output bias (M3)	CMFB	3.46%
Output Stage (M4)	CMFB	7.58%
Miller Resistors	-	3.2%
Input mirror (M2)	CMFF	2.34%

Table 5.2: Major noise contributors in PGA design.

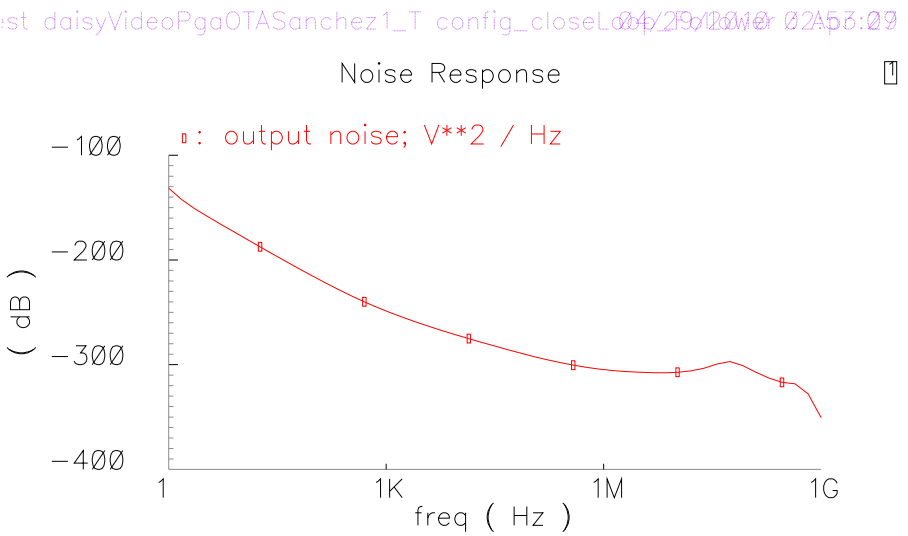


Figure 5.12: 1/f noise curve of the designed PGA.

The analysis results reveal significant contribution of input differential pair to the total integrated noise. This was also explained by Eq. 3.22 and is reproduced here for convenience.

$$V_{n(rms)}^2 = \frac{16KT}{3g_{m1}} BW[1 + \frac{g_{m2}}{g_{m1}} + \frac{(1 + A_I)g_{m3}}{g_{m1}B^2} + \frac{(1 + A_I)g_{m4}}{g_{m1}B^2}], \tag{5.3}$$

where $B = M_4/M_2$, BW is equivalent noise bandwidth.

It is obvious from this equation that increasing g_{m1} and B factor, will improve the noise performance. B was already more than 1, so one could increase g_{m1}. This is vital for decreasing the noise level to tackle the 73% noise contribution from the input differential and mirror pairs.

5.6 Non-Linearity and Distortion

Spectre® provides the periodic steady state analysis, which was utilized to check the distortive harmonic components affecting the system's linearity. It was found out that output buffer meant to stabilize the system, once again adds to the system nonlinearity. The strength of harmonics are summarized in Table. 5.3.

	HD2	HD3
Buffered	30.3 dB	41 dB
Unbuffered	98.7 dB	41 dB

Table 5.3: Second and third order harmonics.

Notice, that unbuffered HD components are listed against the buffered ones to show how non-linear the source follower is. One needs to re-address the source follower design to suppress HD2 components. On the other hand, third order components are also strong enough adding considerable non-linearity. To re-address the design one can seek help from Eq. 3.19 and Eq. 3.20.

5.7 Bandwidth vs. Stability

Finally, the bandwidth in the final OTA specifications have had a strong trade-off with stability. This is highlighted in Fig. 5.13. A better phase margin is marred by decreasing bandwidth and a high bandwidth amplifier is less stable. One needs to settle somewhere in the middle, perhaps at the minimum stability criteria of 45°, found to be near 200 MHz bandwidth.

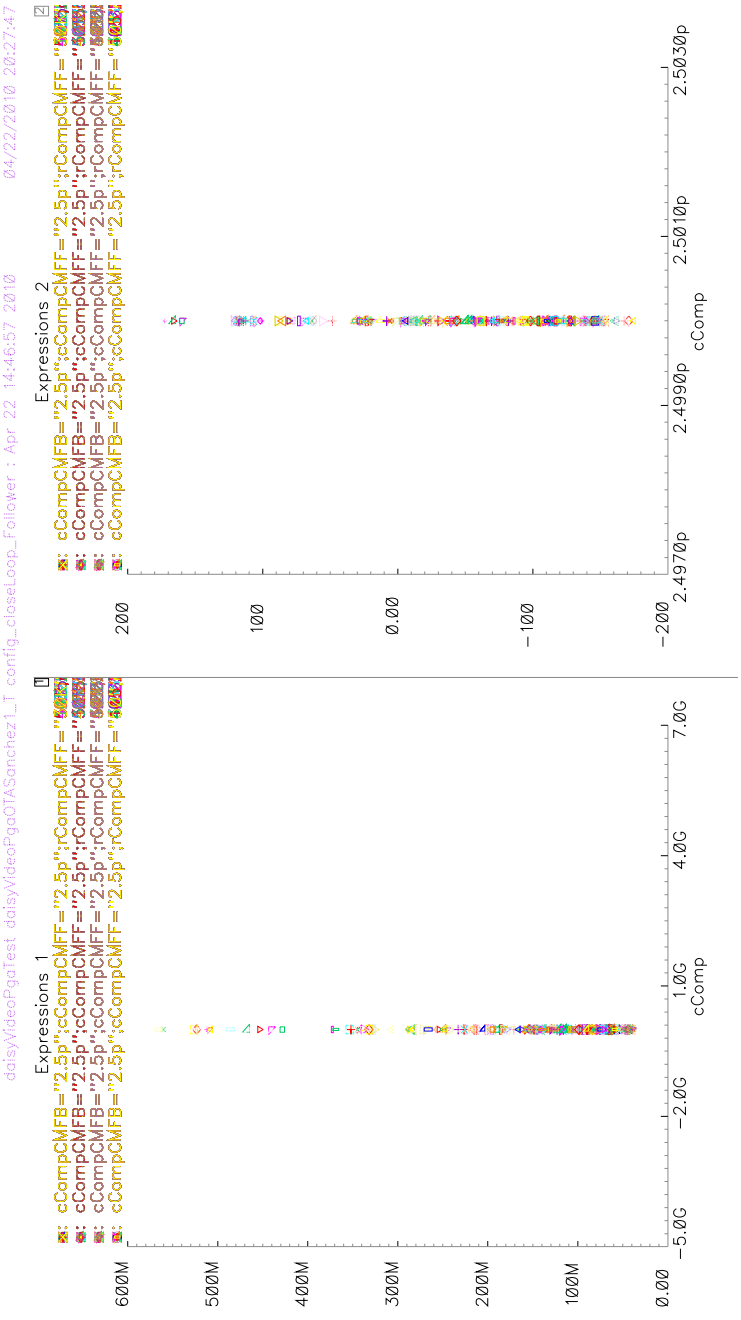


Figure 5.13: The bandwidth vs. phase margin trade-off, highlighted by parametric analysis.

5.8 Final OTA Specifications

The final OTA specification achieved, adjusted to compensated after all the various analog design trade-offs are summarized below.

Supply Voltage	1.2 V
Phase Margin	$\approx 45^{\circ}$
Bandwidth	193 MHz
Gain Settings	0.5, 1
Gain	60 dB
CMRR	292 dB
Linearity	30.3 dB
Slew Rate	1240 V/μs
Noise	-66 dB
Power Consumption	10.4 mW
OTA Architecture	low voltage
Process Node	65 nm

Table 5.4: Final PGA specifications.

Chapter 6

Conclusions and Future Work

This thesis presented a switched capacitor PGA realized using a novel OTA architecture, unique for excluding the tail current source, providing efficient common mode feedforward and inherent common mode feedback. The fully differential, fully symmetric architecture was implemented in a modern 65 nm CMOS implementation, using a 1.2 V supply.

The CMOS process limitations have been very evident at these low supply, and a total of four gain stages, comprising of two OTA structures were utilized to attain the targeted gain for required linearity. Nested Miller compensation was used with 2.5 pF capacitors to keep the amplifier stable.
The following conclusions are made:

- The Miller compensated amplifier with large 2.5 pF capacitors achieves up to 200 MHz (3 dB) bandwidth.
- A factor 8× gain per stage is available in this process.
- Targeted gain requires minimum of 3 stages in this process and voltage supply.
- Main specifications met for video standards up to HDTV 720p.
- Architecture requires careful OTA input stage design to minimize total noise contribution.

As a next step, one needs to further this design in the following possible ways:

- Re-design the input stage of the OTA to reduce the major noise contribution.
- Re-address the design for linearity, either by removing the buffer or improving its design.

- Optimize the design using a CAD optimizer to explore the limits of the design.
- Layout of the designed PGA block.
- Using this OTA, realize an active antialiasing integrated OTA-C filter, which was initially conceived in the second cascaded OTA.

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Appendix A

MATLAB Codes

The following MATLAB code snippet was used to estimate the required unity gain frequency, from the ADC no. of bits (NOB), beta factor and sampling frequency.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% User: syeaa775
% Project name: videoPga
% Project area: /site/edu/es/EXJOBB/videoFront/
% % Department of Electrical Engineering
% Linkoping University
% Tue Feb 17 CET 2010

% PGA transfer function Vout/Vin(z) = [C_in/C_f] · z^-1
% beta = C_f/(C_in+C_f)
%Capacitors:
% C_in = input capacitor
% C_f = feedback capacitor
% Set 'Cap' value and 'PGAgain' factor

Cap = 1e-12;
PGAGain = 2;

switch (PGAGain)
case 1
disp('****** 1X Gain *****');
C_f = Cap;
C_in = Cap;
case 2
disp(' *** 2X Gain ***')
C_f = 0.5 * Cap;
C_in = Cap;
```

```
case 0.5
disp('*** 0.5X Gain ***')
C_f = Cap;
C_in = 0.5 *Cap;
otherwise
disp('Gain not supported')
end

%Cc = 0.3*C_f;
beta = C_f / (C_in + C_f);
NOB = 12;
fSample = 300e6;
omegaUg = abs( log(2^-NOB)*fSample / beta )
f_ug = omegaUg / 2 / pi
```

Appendix B

Skill Scripts

This section contains Skill™ snippets used in different Spectre® simulations.

B.1 Pole and Zero Locations

The script below was used to compute poles, which were mainly caused by parasitic capacitances. The 'captab' simulation option was used to obtain the node capacitance.

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; User: syeaa775
;; Project name: videoPga
;; Project area: /site/edu/es/EXJOBB/videoFront/
;; Department of Electrical Engineering
;; Linkoping University

;; (if (loadi "daisyVideoPga/cds/OTASanchez1cascaded.il") 0)

resultsDir = "/tmp/daisyVideoPgaOTASanchez1_T/spectre/config_closeLoop"
cPar1 = pv( "I4.VzN : I4.VzN" "Total" ?result "capInfo_dc-info.captab" ?results-
Dir resultsDir)
cPar2 = pv( "I6.VzN : I6.VzN" "Total" ?result "capInfo_dc-info.captab" ?results-
Dir resultsDir)
cOut1 = pv( "VoutInN : VoutInN" "Total" ?result "capInfo_dc-info.captab" ?re-
sultsDir resultsDir)
cOut2 = pv( "vOutN : vOutN" "Total" ?result "capInfo_dc-info.captab" ?results-
Dir resultsDir)

gmMirrN = OP("/I4/MnMirrN" "gm")
gdsnOut = OP("/I4/MnOutStageN" "gds")
gdspOut = OP("/I4/MpOutStageN" "gds")
```

```
gmMirrN2 = OP("/I6/MnMirrN" "gm")
gdsnOut2 = OP("/I6/MnOutStageN" "gds")
gdspOut2 = OP("/I6/MpOutStageN" "gds")

fp12= gmMirrN / (2 * 3.14159 * cPar1)
fp11= (gdsnOut + gdspOut)/(2 * 3.14159 * cOut1)
fp22= gmMirrN2 / (2 * 3.14159 * cPar2)
fp21= (gdsnOut2 + gdspOut2)/(2 * 3.1459 * cOut2)

(printf "OTA Parameters" )
(printf "cPar1=%e cOut1=%e cPar2=%e cOut2=%e" cPar1 cOut1 cPar2 cOut2 )
(printf "gmMirrN=%e gmMirrN2=%e gdsnOut=%e gdspOut=%e gdsnOut2=%e
gdspOut2=%e " gmMirrN gmMirrN2 gdsnOut gdspOut gdsnOut2 gdspOut2)

(printf "fp12 =%3.2f MHz " fp12*1e-6)
(printf "fp11 =%3.2f MHz " fp11*1e-6)
(printf "fp22 =%3.2f MHz " fp22*1e-6)
(printf "fp21 =%3.2f MHz " fp21*1e-6)
```

B.2 Harmonic Distortion

This script prints the strength of HD2 and HD3 components, once the user has enabled the periodic steady state analysis.

```
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;; User: syeaa775
;; Project name: videoPga
;; Project area: /site/edu/es/EXJOBB/videoFront/
;; Department of Electrical Engineering
;; Linkoping University
;; if(loadi("/edu/syeaa775/vidPga/daisyVideoPga
;; /skill/displayResultsSanchezOTA.il") 0)

(printf "Loading the display results file for Sanchez OTA \n")

netName = "/vOut"

waveForm = (v netName ?result "pss-fd.pss")

firstHarmonic = (harmonic waveForm 1)

secondHarmonic = (harmonic waveForm 2)

thirdHarmonic = (harmonic waveForm 3)

(printf "Harmonics %f %f %f \n"

(float (dB20 firstHarmonic))
(float (dB20 secondHarmonic))
(float (dB20 thirdHarmonic)) )

HD2 = (dB20 firstHarmonic) - (dB20 secondHarmonic)
HD3 = (dB20 firstHarmonic) - (dB20 thirdHarmonic)

(printf "HD2 = %f dB and HD3 = %f dB \n"
(float HD2) (float HD3))

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
```