Analysis of the Formation Conditions for Large Area Epitaxial Graphene on SiC Substrates

Rositsa Yakimova, Chariya Virojanadara, Daniela Gogova, Mikael Syväjärvi,
D. Siche, Krister Larsson and Leif Johansson

Linköping University Post Print

N.B.: When citing this work, cite the original article.

Analysis of the formation conditions for large area epitaxial graphene on SiC substrates

R. Yakimova[1,a], C. Virojanadara[1,b], D. Gogova [2,c], M. Syväjärvi[1,d], D. Siche[2,e], K. Larsson[3,f], L. I. Johansson[1,g]

[1] Department of Physics, Chemistry and Biology, Linkoping University, SE-581 83 Linköping, Sweden

[2] Leibniz Institute for Crystal Growth, 12 489 Berlin, Germany

[3] Department of Materials Chemistry, Uppsala University, Box 538, 751 21, Uppsala, Sweden

[a]roy@ifm.liu.se, [b]chavi@ifm.liu.se, [c]gogova@ikz-berlin.de, [d]msy@ifm.liu.se, [e]siche@ikz-berlin.de, [f]karin.larsson@mkem.uu.se, [g]lejoh@ifm.liu.se

Abstract. We are aiming at understanding graphene formation mechanism on different SiC polytypes (6H, 4H and 3C) and orientations with the ultimate goal to fabricate large area graphene (up to 2 inch) with controlled number of mono layers and spatial uniformity. To reach the objectives we are using high-temperature atmospheric pressure sublimation process in an inductively heated furnace. The epitaxial graphene is characterized by ARPES, LEEM and Raman spectroscopy. Theoretical studies are employed to get better insight of graphene patterns and stability. Reproducible results of single layer graphene on the Si-face of 6H and 4H-SiC polytypes have been attained. It is demonstrated that thickness uniformity of graphene is very sensitive to the substrate miscut.

Introduction

The empirical "Moore's law", formulated by Gordon Moore in 1965 is about to fail. Moore predicted that the number of Si transistors per chip, the brain of today's computers, would increase exponentially every year. Following this tendency the number of transistors will reach one billion per chip by 2010. The current miniaturization cannot continue forever because of the limitations placed by the discreteness of matter itself. The small distances between transistors will result in parasitic resistance and capacitance that will be detrimental to the performance of any processing unit. The expected failure of Moore's low has triggered the search for alternative non-silicon based materials. Graphene has recently emerged as a new discovery and has attracted an avalanche attention because of the unique structural, physical and mechanical properties [1]. The availability of samples of graphene has led to extensive exploration of electronic properties and novel transport phenomena in this material [2]. Although several ways of producing graphene have been reported none of them can be qualified as a high yield method. Recent efforts on fabrication of epitaxial graphene on SiC have elevated the expectations towards large area homogeneous graphene [3, 4] and thus the feasibility of device processing by conventional microelectronics lithography techniques.

In this paper we summarize our recent achievements in growing large area epitaxial graphene with controlled number of monolayers on different SiC surfaces concerning the polytype and crystallographic orientation by applying high-temperature atmospheric pressure sublimation process. Calculations on the energetical stability of C attachment to SiC polar surfaces by Density Functional Theory (DFT) have been initiated.

Experimental

Substrates. When considering industrial applications, forming large area uniform epitaxial graphene on SiC is the most promising technique to prepare extensive graphene samples. Today SiC substrates have large area, up to 100 mm in diameter wafers are commercially available and exist as semiconducting (p- and n-type) and semi-insulating material, which allows different device designs. Moreover, SiC is a good template because of the similar hexagonal structure and the possibility to decompose SiC by leaving C to reside on the substrate. Under heating the formation of surface phases on Si-terminated SiC (0001) surface is well known to undergo the following modifications: from Si rich (3x3) structure – through the intermediate (1x1) and ($\sqrt{3}$ x$\sqrt{3}$) – R30^{o} structures, to the C-rich (6$\sqrt{3}$ x 6$\sqrt{3}$) phase, and finally epitaxial graphene. In our work the graphene deposition was made predominantly on Si-terminated surfaces. Some experiments were made with non-polar surfaces but graphene did not grow due to the mix of terminating Si and C-atoms.

Growth furnace and process. The equipment used for the graphene formation was modified from an earlier version which gave graphitic layers [5] having qualities quite well comparable with those recorded for natural single crystal graphite. Basically it is an inductively heated high temperature furnace but the crucible was specially designed so that the axial and radial temperature gradients were minimized in order to prevent mass transfer from and to the sample. The base pressure in the reactor was 5x10^{-6} mbar. The graphene growth was carried out under highly isothermal conditions at a temperature of 2000°C and at an ambient argon pressure of 1 atm. The process does not apply H_2 etching prior to graphitization nor does it use any Si flux to remove O_2, as the surface preparation and oxygen removal is built in during the initial stage of the graphene formation process. An advantage of this type of reactor is that a large area graphene can be grown on SiC substrates (ultimately 2").

Characterization. To confirm the graphene material and its thickness, the samples were assessed using angle resolved photoelectron spectroscopy (ARPES), low energy electron microscopy (LEEM), AFM and Raman spectroscopy.

Results and Discussion

In the applied isothermal annealing, the annealing temperature determines the kinetics of the elements involved. The surface mobility of carbon and the nucleation rate of the buffer layer are expected to increase considerably when raising the annealing temperature from 1200 to 2000°C. The sublimation rate of silicon, leaving carbon behind, should also increase with temperature. However, a surrounding ambient of Ar, instead of vacuum, is commonly used in sublimation growth experiments to suppress a too fast sublimation rate and provide a smooth decomposition of the SiC. In this particular case it results in desirable growth and morphology changes, the formation of larger terraces with single layer graphene sheets on top.

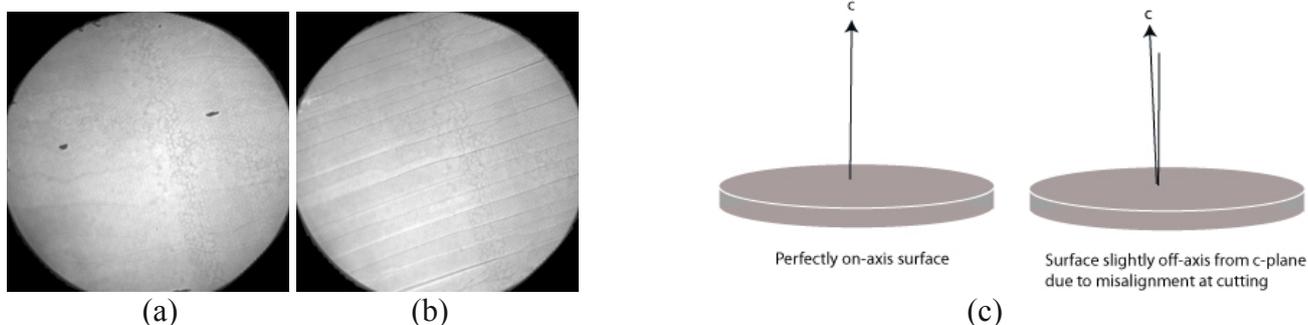| (a) | (b) | (c) |

Fig. 1. LEEM images taken from monolayer graphene grown on a) 0.03°-SiC, the field of view (FOV) is 50 μm and b) 0.25°-SiC, the FOV is 25 μm [6]. c) Illustration of wafer miscut.

We have grown large area homogeneous graphene on nominally on axis 6H-SiC wafers [3]. It was found that due to the step-bunching phenomenon on vicinal substrates, any small miscut is detrimental to the surface morphology of the epitaxial graphene, which is illustrated by Fig. 1. The LEEM images show surface morphology of graphene grown on substrates with different miscut: a) 0.03^o, where continuous graphene sheet with a size larger than 50 μm^2 was observed, and b) 0.25^o, where regular steps and smaller terrace widths (≈ 2 μm) appear.
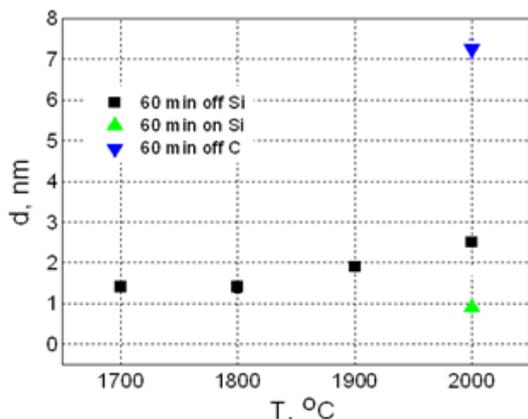

Fig. 2. Graphene/graphite thickness vs. temperature for different faces of 8° off-oriented 4H-SiC samples and identical deposition time of 60 min. An on-axis sample is shown for comparison.

We have studied thickness dependence of graphene grown on 4H-SiC on temperature (1700-2000^oC), face polarity and orientation (on-axis and with 8° off orientation), Fig. 2. The process thermodynamics is not expected to change significantly for the two polytypes (6H or 4H) because the enthalpy of sublimation and the surface free energy do not differ much. However, a pronounced difference may be observed between Si- and C-terminated face, as well between vicinal and atomically flat surfaces. While in the latter case surface kinetics may be facilitated by the presence of steps, the smaller surface energy of the C-face is determining in the former case. It was found that graphitization is more distinct on the C-face of off oriented substrates (layer thickness around 7 nm), while only a few monolayers of graphene were obtained on the Si-face of on-axis wafers at 2000^oC.

The thickness of epitaxial graphene in our process at this stage can be controlled by temperature, time and face polarity. The course of thickness vs. temperature dependence on the Si-face at a fixed time of growth is also indicative for a significant involvement of surface reconstruction and a buffer layer formation. The graphene deposited on off-axis substrates is carpet-like exhibiting step-wise morphology governed by the substrate off-cut, and a prominent step-bunching.
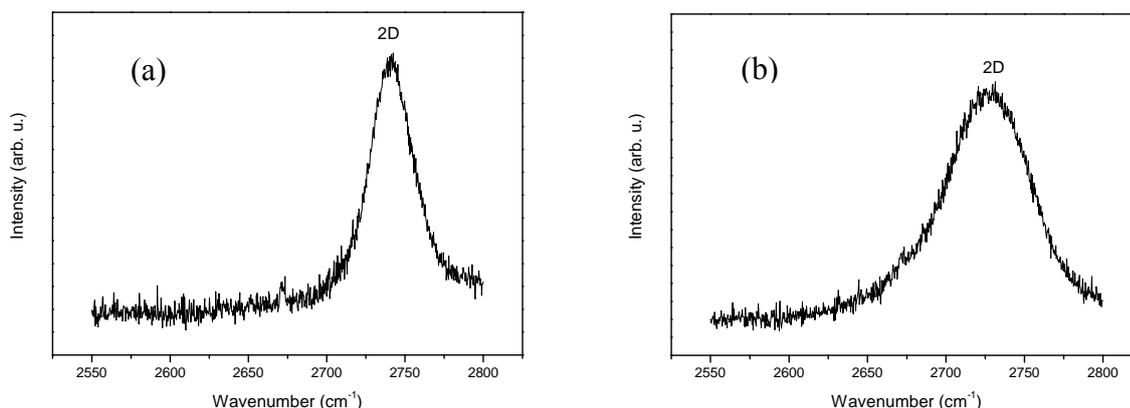

Fig. 3. μ-Raman spectra of graphene at 633 nm excitation wavelength: a) SLG b) 2D band becomes broader and blue-shifted (from 2692.5 cm^{-1} for a SLG to 2688 cm^{-1} for 2 LG) when the graphene thickness increases from SLG to multilayer graphene. This band can be fitted with 4 Gaussians.

Micro-Raman measurements show intense and narrow (FWHM ~26 cm-[1]) 2D peaks suggesting a single layer (SLG) of graphene (Fig. 3a) while the 2 monolayer graphene exhibits a broader peak that can be fitted with 4 Gaussians (Fig. 3b). The peak positions are shifted compared to the position of mechanically cleaved (stress-free) graphene, which demonstrates some compressive strain in our material due to the interaction of the epitaxial graphene with the SiC substrate. The strain changes the lattice constant of graphene, hence the Raman peak frequencies. The uniformity of the epitaxial graphene has been evidenced by mapping samples of 7x7 mm^2 area.

The cubic polytype is interesting because of the high electron mobility and similarity of the (111) surface with 6H (0001). The thermodynamic stability of graphene adhesion onto the Si-rich and C-rich surface of 3C-SiC (111) was theoretically investigated using DFT. Initial calculations based on periodic boundary conditions and plane-wave basis sets were performed. The graphene layer was found to chemisorb weakly to the surface Si atoms with on average bond strength of 1.1 eV (Si-face) and 1.6 eV (C-face) per binding graphene C atom. The new bond formations are highly polar with a partial electron transfer from the SiC surface to the graphene adlayer. These bonds have appreciably stronger than Van-der-Waals strengths, but at the same time small enough to be ruptured at e.g. higher temperatures.
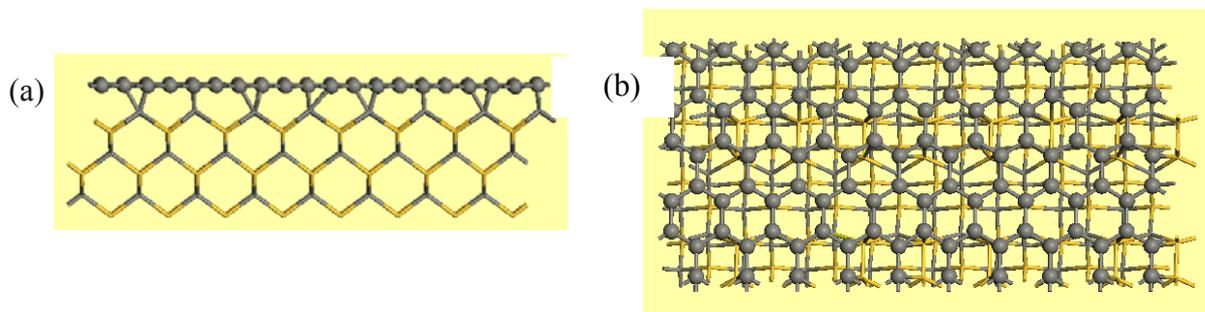
(a) (b)

Fig. 4. (a) Side view and (b) top view of the 3C-SiC (111) plane. The hexagonal lattice network, which can serve as a template for graphene growth, is displayed.

In summary, we have demonstrated a novel approach towards epitaxial graphene growth on SiC substrates. The method is based on high temperature (2000°) sublimation at 1 atm of Ar ambient, which yields SLG on a large area (~1 cm^2) and allows good control over the thickness uniformity. Recently, quantum Hall effect has been successfully measured on such samples [7].

References

[1] K.S. Novoselov, A.K. Geim, S.V. Morozov, D. Jiang, M.I. Katsnelson, I.V. Grigorieva, S.V. Dubonos, A.A. Firsov: Nature Vol. 438 (2005), p.197
[2] A. K.Geim and K. S. Novoselov: Nature Mateials Vol. 6 (2007), p.183
[3] C. Virojanadara, M. Syväjarvi, A. A. Zakharov, T. Balasubramanian, R. Yakimova, and L. I. Johansson: Phys. Rev. B Vol.78 (2008), p.245403.
[4] K.V. Emtsev at al.: Nature Materials Vol. 8 (2009), p. 203.
[5] T. Kihlgren, T. Balasubramanian, L. Walldén, and R. Yakimova: Phys. Rev. B Vol. 66 (2002), p. 235422
[6] C. Virojanadara, R. Yakimova, J. R. Osiecki, M. Syväjärvi, R. I. G. Uhrberg, and L. I. Johansson: Surface Science Lett. 603 (2009), p. L87-L90

[7] A. Tzalenchuk, S. Lara-Avila, A. Kalaboukhov, S. Paolillo, M. Syväjärvi, R. Yakimova, O. Kazakova, T.J.B.M. Janssen, V. Fal'ko, S. Kubatkin: arXiv:0909.1220