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A 3.3V 72.2Mbit/s 802.11n WLAN Transformer-Based Power Amplifier in 65nm CMOS

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Abstract-This paper describes the design of a power amplifier (PA) for 802.11n WLAN fabricated in 65nm CMOS technology. The PA utilizes 3.3V thick gate oxide (5.2nm) transistors and a two-stage differential configuration with integrated transformers for input and interstage matching. A methodology used to extract the layout parasitics from electromagnetic (EM) simulations is described. For a 72.2Mbit/s, 64-QAM, 802.11n OFDM signal at an average and peak output power of 11.6dBm and 19.6dBm, respectively, the measured EVM is 3.8%. The PA meets the spectral mask up to an average output power of 17dBm.

Keywords-CMOS, power amplifier, transformers, wireless LAN

Introduction

The power amplifier (PA) is a key building block in all RF transmitters. To lower the costs and allow full integration of a complete radio system-on-chip, it is highly desirable to integrate the entire transceiver and the PA in a single CMOS chip. However, integration of RF power amplifiers in low-cost CMOS technologies proves to be a challenging task [1].

While digital circuits benefit from the technology scaling, it is becoming significantly harder to meet the stringent requirements on linearity, output power, and power efficiency of PAs at lower supply voltages and in the presence of large on-chip parasitics [2]. This has recently triggered extensive studies to investigate the impact of different circuit techniques, design methodologies, and design trade-offs on functionality of PAs in deep-submicron CMOS technologies [3]. Particularly, the demand for higher data rates in wireless communication has led to an increased interest in modulation schemes utilizing both phase and envelope modulation, necessitating a special focus on design issues for linear CMOS PAs to amplify signals with high Peak-to-Average-Power Ratio (PAPR), as in 802.11n WLAN. Due to the large PAPR values, there is an inherent conflict between power-added efficiency and linearity, as the PA has to back-off significantly from

the maximum output power in order not to cause significant distortion. Assuming a signal with PAPR of 10dB, the efficiency of an ideal Class-A amplifier cannot be higher than 5% [4]. Nonetheless, it is important to minimize power consumption to increase battery operation time and also minimize heat dissipation.

Several high performance PAs for WLAN have been fabricated in 180nm [5], [6] and 90nm [7] CMOS technologies. In this paper, we present the design and evaluation of a linear 2.4GHz WLAN PA [8] in 65nm CMOS supporting the IEEE 802.11n draft standard. The PA utilizes 3.3V thick gate oxide CMOS transistors and integrated transformers for input and interstage matching. The output matching network is located off-chip, on a FR4 PCB, and is realized by lumped components. This paper discusses the design and implementation of the PA, including the circuit architecture, modeling and design of the transformers, the extraction of the layout parasitics, and the output matching network design, which is followed by the experimental results.

Design and Implementation of the Power Amplifier

The PA utilizes 3.3V thick gate oxide CMOS transistors with a gate length of 0.6μm and integrated transformers (T_1 and T_2) for input and interstage matching. Fig. 1 shows the differential design and the two amplifier stages, as well as the integrated transformers and tuning capacitors (C_1 and C_2). Transformers have not been commonly used in integrated CMOS PAs until recently, and it has been shown that they can provide sufficient performance for impedance matching purposes [9], [10]. Since the primary and secondary windings of the implemented transformers are galvanically isolated, we can use the center taps for either biasing of the input device in the cascode stage, as in the first transformer, or power supply of the cascode stage, as in the second transformer.

To ensure reliable operation and protect the transistors from hot electrons and breakdown due to high voltage peaks, each amplifying stage uses a pair of transistors in a cascode configuration, which also increases the output resistance and reduces unwanted capacitive feedback [11]. To provide highest protection for the transistors, the gates of the cascode transistors should be biased at VDD, but a lower bias level can provide better performance [10]. As the 65nm process was

still under development, information on reliability issues due to hot carriers in the thin oxide devices was limited, and a conservative approach, using a cascode structure with two thick oxide devices with long channel length, was taken. The minimum channel length of the thick gate oxide transistor was 0.6μm, which also leads to a low gain of the transistors. Therefore, to achieve a sufficiently high gain, large transistor widths were used, 0.8mm and 6mm for the first (M_1 and M_2) and second (M_3 and M_4) amplification stages, respectively. In [12] it is shown that a combination of a thin oxide and thick oxide device in the cascode structure can provide sufficient reliability for WLAN products in nanometer technologies. Using a combination of a thin oxide and thick oxide device could increase the gain of the PA, due to the shorter gate length, and lower the driving requirements of the first stage as the input impedance of the required thin oxide device can be higher.

Transformer Model and Losses

In [9] the relationship between the voltages and currents in the primary and secondary windings of an ideal transformer in Fig. 2 is described. Suppose that an impedance, Zs, is connected to the secondary side, then the primary side experiences an impedance, Zp, which relates to each other according to the turns ratio, n, as defined in (1).

$$n = \sqrt{\frac{L_s}{L_p}} = \frac{V_2}{V_1} = \frac{I_1}{I_2} = \sqrt{\frac{Z_s}{Z_p}} \quad (1)$$

Consequently, different winding schemes result in different impedance transformation ratios, which mean that the transformer can be used for impedance matching/transformation purposes. A more detailed analytical model of the transformer is the T-model, described in [13], where the efficiency was derived to be as follows (for optimum choice of L_p and consideration of tuning capacitors [14]):

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_P Q_S k^2}\right)\frac{1}{Q_P Q_S k^2}} + \frac{2}{Q_P Q_S k^2}} \quad (2)$$

In (2), Q_P and Q_S are the quality factors of the primary and secondary sides, respectively. From (2), we can see that the efficiency can be maximized by using a coupling factor, k, as close as possible to unity and making the Q of the

primary and secondary windings, as large as possible. However, the number of turns and the inductances are limited by the substrate and interwinding parasitic capacitances and operating frequency, making it challenging to find an optimum transformer design. Moreover, in this PA design the inductances of the transformers are limited by the large capacitances of the transistors since the transformers are used for input and interstage matching.

The designs of the planar square transformers are based on a model described in [15] and are implemented as coupled inductors. The model in Fig. 3 includes coupling to the substrate, inductances, and the coupling between the primary and secondary sides, parasitic capacitances, and the series resistance of the windings.

To reduce the resistive losses at primary and secondary sides, the two upper layers in the seven-metal stack are connected to form one conductor. The thicknesses of the aluminum and copper layers are 1.3μm and 0.6μm, respectively. The winding ratios of the transformers, in Fig. 1, are 2:3 (T_1) and 3:2 (T_2) with a coupling factor of approximately 0.7 for both transformers. Estimations of the power losses in the transformer can be calculated by the maximum available gain, G_{ma}, based on S-parameters for any termination impedances calculated according to (3) and (4), and is a measure of the gain of a system when the source and load reflection coefficients are conjugately matched to S_{11} and S_{22} [16].

$$G_{ma} = \left| \frac{S_{21}}{S_{12}} \right| \left(k_s - \sqrt{k_s^2 - 1} \right) \quad (3)$$

where k_s is the stability factor defined as:

$$k_s = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} \quad (4)$$

The simulated maximum available gain, G_{ma}, for the input and interstage transformers is approximately -2.2dB for both transformers at the target operating frequency of 2.45GHz. G_{ma} is plotted in Fig. 4 up to the approximate self-resonant frequency, which is close to 5GHz.

Besides biasing possibilities through the center taps of the transformer, the galvanic isolation also features an ESD protective function (for stand-alone

devices) at the input of the PA. LNA implementations have shown that protection up to 5kV is feasible [17] by using transformers.

Parasitics Extraction

Extraction of interconnect parasitics and inherited losses are used to predict the frequency behavior and gain of the PA. In our simulation model, the signal traces are approximated by series inductance and series resistance, which are extracted through electromagnetic (EM) simulations using Agilent Advanced Design System (ADS).

To meet the current density limitations, and to reduce the losses in the drain and source connections at the output transistors, several metal layers were stacked on top of each other in the structure, as shown in Fig. 5. For such a structure, the capacitive coupling between gate, source, and drain is increased. Since not all the metal layers are not included in the existing transistor model, we need to add the parasitic capacitances, while taking into account the associated dielectric losses [18], into our extended model. The values were extracted through EM simulations and added in the simulation model as series connections of capacitance and resistance between the gate, drain, and source, as seen in Fig. 6. Additionally, there will be an interconnect resistance between the drain (M_{input}) and source (M_{casc}). But by making the transistors wide with multiple fingers and using several metal layers as shown in Fig. 5, the resistive drop across this resistance was reduced to a few mV and therefore this resistance was omitted in Fig. 6. The large transistors were split into gate widths of 20μm (connected on both sides), resulting in 40 and 300 fingers for the transistors in the first and second amplifier stages, respectively.

The S-parameters were converted to Z-parameters [19] of the reciprocal network [18] into a T-type connection and by applying expression (5) and (6), the parasitic component values were approximated at the operating frequency. For differential signals, (5) was applied to calculate the differential impedance (Z_{dd}). For single-ended excitation, (6) was applied to calculate the input impedance at port 1 (Z_{se}) [20].

$$Z_{dd} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \qquad (5)$$

$$Z_{se} = Z_{11} - Z_{12}Z_{21}/Z_{22} \qquad (6)$$

To accurately model the gate resistance at high frequencies, we added a vertical gate resistance [21] as in Fig. 7, which due to dopant segregation during silicidation can be relatively high, and thus will influence the gain of the PA and f_{max} [22]. In Fig. 6, this resistance is denoted as R_{vgr}, inserted in series with the lateral gate resistance, $R_{lateral}$, which is calculated by the gate sheet resistivity and layout geometry. The sum of both resistance values for the first and second amplifier stages are approximately 1.6Ω and $250m\Omega$, respectively, and the vertical gate resistance represents ~20% of the total gate resistance in our design. The estimated impact of these resistances is a gain reduction of 1.6dB.

For evaluation of the PA design, the schematic from Cadence was simulated in ADS WLAN 802.11g testbench together with the layout of the fabricated testboard using RFIC Dynamic Link. In such a setup the influence of the parasitics can be evaluated.

Off-Chip Matching Network

The PA utilizes an off-chip lumped element balun [23] (Fig. 8) for differential-to-single-ended conversion and load impedance transformation. A pre-matching capacitor (C_P) was used before the balun to compensate for the bondwire inductance and interconnection lines from the PA to the balun. For simplicity we assume that the bond-wire inductance [24] and the interconnections from the PA to the balun can be represented by L_P, and that the balun makes an impedance transformation from a resistive value R_2 to a resistive R_L. As the pre-matching capacitor is added in front of the balun, two impedance transformations are performed. One impedance transformation is done at the immediate output of the PA, from a complex load Z_1 to R_2, and one transformation from R_2 to R_L. As we are adding matching components we may potentially lower the impedance transformation ratios from Z_1 to R_2, and R_2 to R_L ($Re\{Z_1\}<R_2<R_L$), such that the overall matching network become less sensitive to component variations and that a wider bandwidth can be achieved [25].

Based on these assumptions, a matching network with a complex load Z_1, the component values of C_P, L_{Bx}, and C_{Bx} can be calculated according to equation (7), (8), and (9).

$$C_P = \frac{2L_P\omega - \text{Im}\{Z_1\}}{\omega\left(\text{Re}\{Z_1\}^2 + 4L_P^2\omega^2 - 4L_P\omega\,\text{Im}\{Z_1\} + \text{Im}\{Z_1\}^2\right)} \quad (7)$$

6

$$R_2 = \frac{\operatorname{Re}\{Z_{11}\}^2 + 4L_P^2\omega^2 - 4L_P\omega\operatorname{Im}\{Z_{11}\} - \operatorname{Im}\{Z_{11}\}^2}{\operatorname{Re}\{Z_{11}\}} \quad (8)$$

$$\sqrt{R_2 R_L} = \omega L_{B1} = \omega L_{B2} = \frac{1}{\omega C_{B1}} = \frac{1}{\omega C_{B2}} \quad (9)$$

The differential output stage also implies some additional aspects, besides the available double voltage swing, as each amplifier stage can utilize a lower power enhancement ratio [3], [13] such that the efficiency can be higher than if a single-ended PA with a single L-match would have been used.

Experimental Results

Fig. 9 shows the photograph of the PA, with a size of 1x1 mm^2. The chip was directly bonded on the testboard, which was a two-layer 0.5mm thick FR4 PCB with ε_r of 4.2 and tan δ of 0.035 as shown in Fig. 10. The input power to the testboard was applied differentially with an external 50-to-100 Ohm balun connected to the signal source.

The target frequency of the PA was set to 2.45GHz in the design work. After tuning of the output matching network, the best performance in terms of power gain was found at 2.48GHz. For a frequency offset of ±30MHz around 2.48GHz, the drop in gain was measured to be 0.4dB (2.45GHz) and 0.2dB (2.51GHz), respectively.

The input and output 1dB compression points (P1dB) at 2.48GHz were found to be 2.6dBm and 19.6dBm, with a power-added efficiency (PAE) of 5.8%. Plots of the measured average output power, EVM, and gain are provided in Fig. 11 and Fig. 12 for a 72.2Mbit/s, 64-QAM, 802.11n OFDM signal, while using a supply voltage of 3.3V. Compared to 802.11g, the data rate of 802.11n is increased from 54Mbit/s to 72.2Mbit/s by the use of more subcarriers, shorter guard interval, and 5/6 coding rate [26].

For an input signal with PAPR of 9.1dB, the PA gave an EVM of 3.8% at an average output power of 11.6dBm, and 5.4% at 13.4dBm average output power with a PAE of 1.4%. Due to the high linearity requirements of OFDM modulation, the PA was biased in class-A which leads to large bias currents and low PAE [6]. Additionally, simulations indicate that there is design space for load impedance improvement to get a higher output power.

The measured output spectrum of a WLAN 72.2Mbit/s, 64-QAM, 802.11n OFDM signal for a 20MHz channel is plotted in Fig. 13. As seen in the figure, the PA meets the spectral requirements of the 802.11n draft 2.05 [26]. The PA showed an average output power of 17dBm with an EVM of 13.1%.

In Table 1 the performance of the implemented PA and some recently presented WLAN PAs is listed. The transformer-based PA in this work has similar average output power compared to recently presented WLAN PAs. However, our PA is capable of running at a lower supply voltage than [6], maintaining a low EVM for a 802.11n OFDM signal with more subcarriers than 802.11g [5], [6], and is implemented in a more advanced technology with increased resistances in the interconnects [2].

Table I. Performance Comparison of WLAN PAs

Reference	CMOS Technology	VDD [V]	Data rate [Mbit/s]	Pout [dBm]	EVM [%] @ Pout	PAE @ Pout
[5]	180nm	3.3	54	17.9	3	14
[6]	180nm	3.5	54	11.6	2.8	1.4
[7]	90nm	3.3	54	11.6*	3.6*	8**
This work	65nm	3.3	72.2	11.6	3.8	1.1

* RF performance without applying the implemented digital pre-distortion (DPD) algorithm.

**PAE at Pout when the DPD is used but with an EVM of 1.8%.

Summary

The paper has presented a transformer-based CMOS PA for WLAN 802.11n, fabricated in 65nm CMOS. A methodology to extract the layout parasitics from electromagnetic (EM) simulations was described. The PA meets the EVM and spectral requirements for a 72.2Mbit/s, 64-QAM, 802.11n OFDM signal, at an average output power of 11.6dBm, with an EVM of 3.8%.

Acknowledgment

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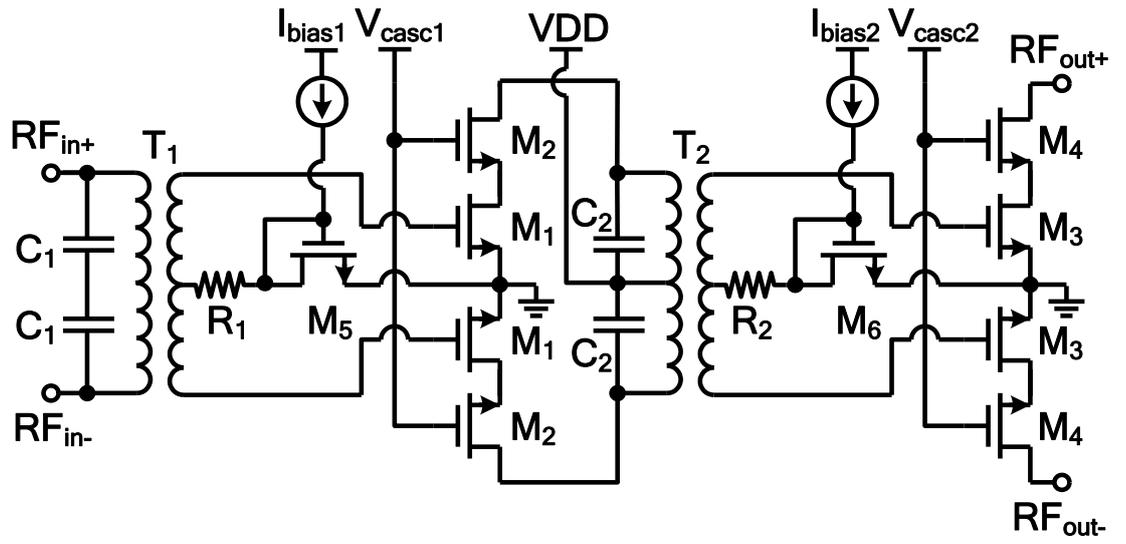26. IEEE P802.11n/D2.05, pp. 283-284, Jul. 2007.

Figures

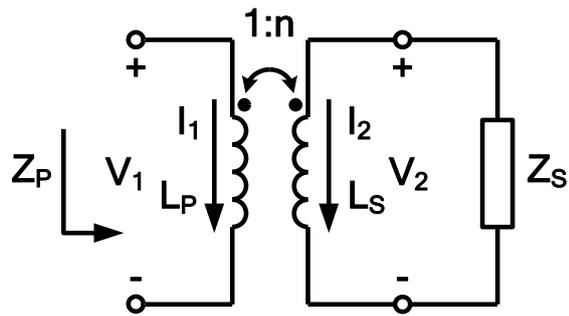**Fig. 1. Simplified schematic of the PA**
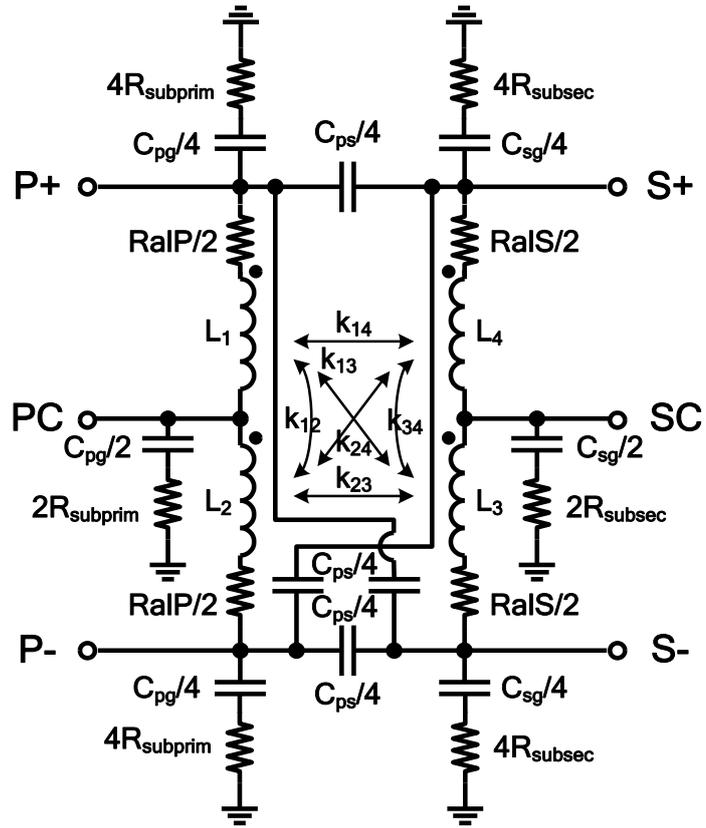

Fig. 2. Ideal transformer model
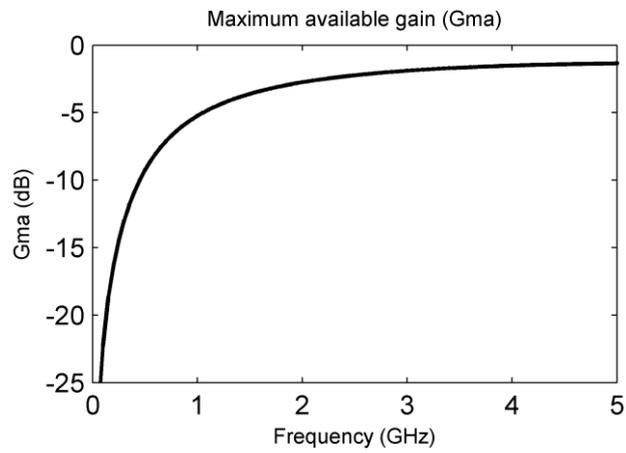
Fig. 3. Transformer model

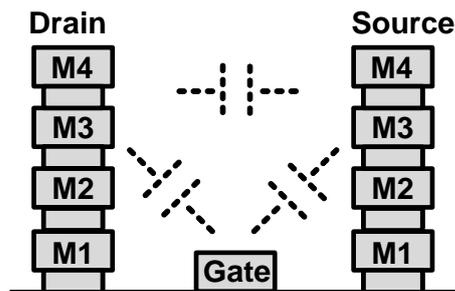**Fig. 4. Simulated maximum available gain**

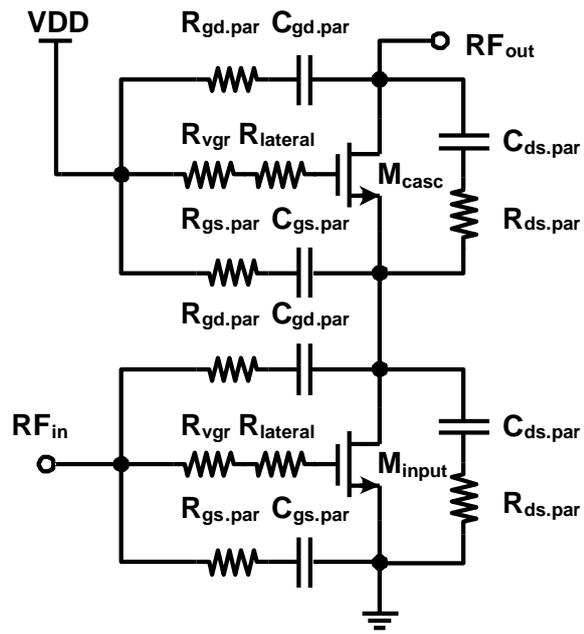**Fig. 5. Parasitic capacitances between gate, drain, and source**

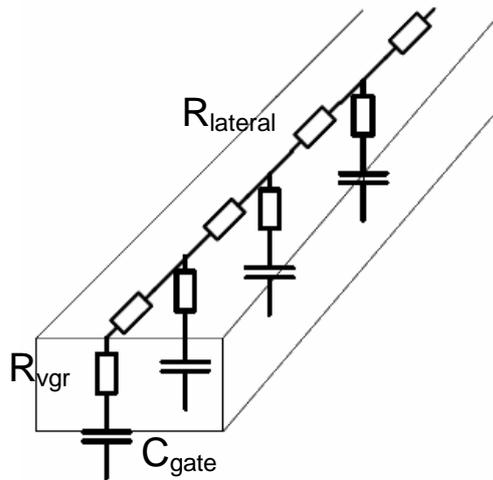**Fig. 6. Model of cascode stage with parasitics**

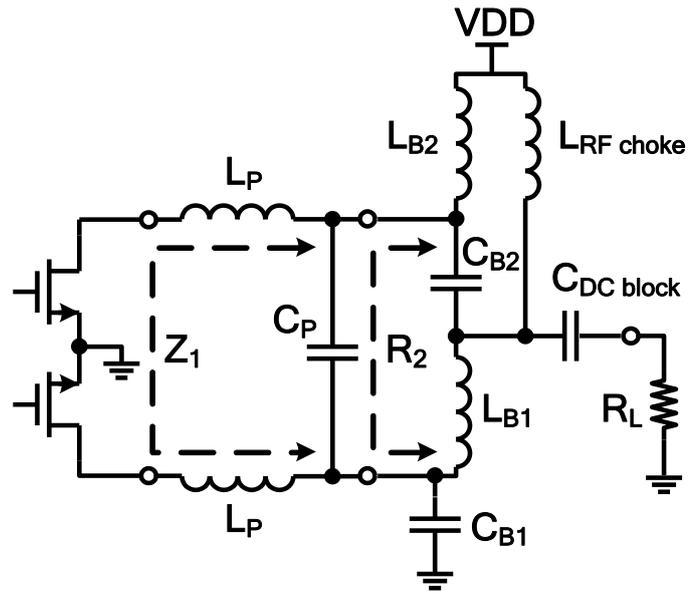**Fig. 7. Poly gate finger and gate resistance components**

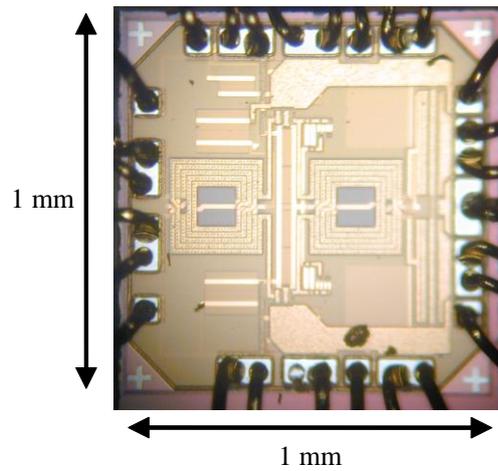Fig. 8. Simplified schematic of the output matching network
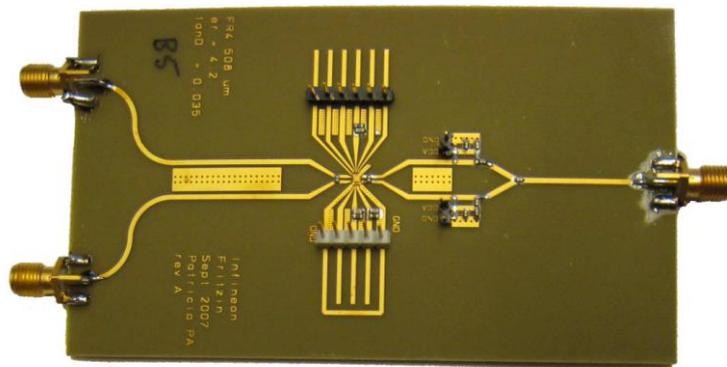

Fig. 9. Chip (1x1mm) photo of the PA

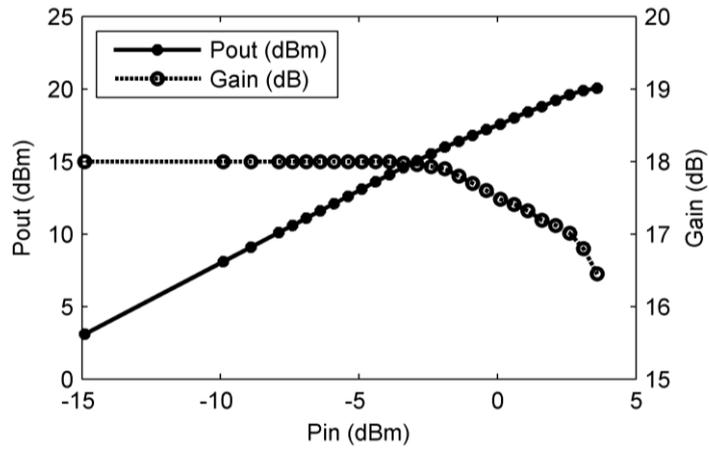Fig. 10. FR4 PCB: Input to the left and output to the right

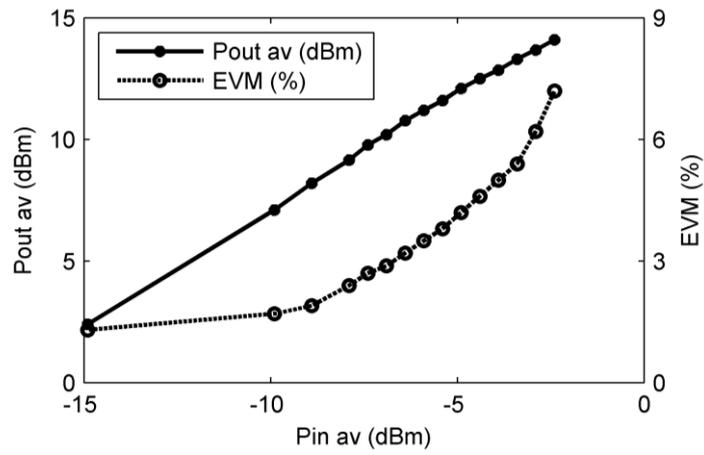**Fig. 11. RF performance (Pin, Pout, Gain)**

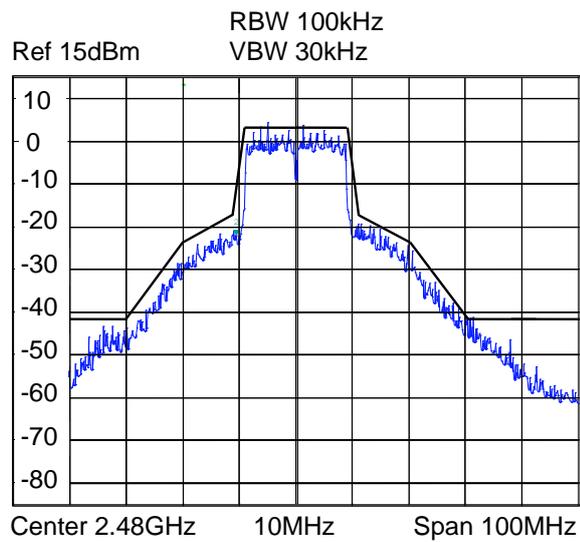**Fig. 12. RF performance (Pin,av, Pout,av, EVM)**

Fig. 13. Spectral mask and measured peak spectrum at an average output power of 17dBm with an EVM of 13.1%