Implementation of Low Power, Wide Range ADPLL for Video Applications

Examensarbete utfört i Elektronik System vid Tekniska högskolan i Linköping
av
Abdul Raheem Qureshi,
Haris Qazi
LiTH-ISY-EX--10/4407--SE
Linköping 2010
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Konstruktion av en bredbandig, heldigital, lågeffekts-PLL för videotillämpningar

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Abdul Raheem Qureshi, Haris Qazi

Sammanfattning
Phase locked loop (PLLs) are the keystone for the electronic as well as for the communication circuits. Without any exaggeration, PLLs are found almost in every electronic and communication devices. Countless research has been performed, for the modification and enhancement of the PLLs circuit. While, due to the numerous advantage of the digital circuitry, the recent research is focusing on the all digital implementation of the PLLs. Therefore, it was competitive to touch with burning research.

Low power and wide range all digital phase locked loop (ADPLL), for video applications is presented. ADPLL has an operating input frequency between 10 kHz to 150 kHz and output frequency between 10 MHz to 300 MHz. The phase frequency detector (PFD) is based on D-flip flops, having two output error and direction signal. The traditional charge pump (CP) is replaced by time-to-digital converters (TDC) and analog low pass filter (LPF) by digital low pass filter (digital-LPF). For completely digital architecture, voltage controlled oscillator (VCO) is replaced by the digitally controlled oscillator (DCO). In DCO, eleven bits are dedicated for controlling bits, two bits for biasing and one bit for enable the DCO. The designed steps for ADPLL were almost similar to the designed steps of a second order analog PLL. The ADPLL is implemented on a CMOS 65-nm technology.

Nyckelord
PLL, Digital, Low Power, Wide Range
Abstract

Phase locked loop (PLLs) are the keystone for the electronic as well as for the communication circuits. Without any exaggeration, PLLs are found almost in every electronic and communication devices. Countless research has been performed, for the modification and enhancement of the PLLs circuit. While, due to the numerous advantage of the digital circuitry, the recent research is focusing on the all digital implementation of the PLLs. Therefore, it was competitive to touch with burning research.

Low power and wide range all digital phase locked loop (ADPLL), for video applications is presented. ADPLL has an operating input frequency between 10 kHz to 150 kHz and output frequency between 10 MHz to 300 MHz. The phase frequency detector (PFD) is based on D-flip flops, having two output error and direction signal. The traditional charge pump (CP) is replaced by time-to-digital converters (TDC) and analog low pass filter (LPF) by digital low pass filter (digital-LPF). For completely digital architecture, voltage controlled oscillator (VCO) is replaced by the digitally controlled oscillator (DCO). In DCO, eleven bits are dedicated for controlling bits, two bits for biasing and one bit for enable the DCO. The designed steps for ADPLL were almost similar to the designed steps of a second order analog PLL. The ADPLL is implemented on a CMOS 65-nm technology.
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<td>5.5</td>
<td>Specification for the hsync = 107.184 kHZ</td>
<td>71</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter (circuit use to convert analog signal into digital signal)</td>
<td></td>
</tr>
<tr>
<td>ADDLL</td>
<td>All Digital Delay Locked Loop (a circuit that generates an output signal whose phase is aligned with the phase of input reference signal)</td>
<td></td>
</tr>
<tr>
<td>ADPLL</td>
<td>All Digital Phase Locked Loop (a circuit that generates an output signal whose phase is aligned with the phase of input reference signal)</td>
<td></td>
</tr>
<tr>
<td>AFE</td>
<td>Analog Front End</td>
<td></td>
</tr>
<tr>
<td>CDMA</td>
<td>Code Division Multiple Access (channel access technique)</td>
<td></td>
</tr>
<tr>
<td>CP</td>
<td>Charge Pump (a circuit used to provide controlling current according to the input voltage)</td>
<td></td>
</tr>
<tr>
<td>CSDCRO</td>
<td>Current Starving Digitally Controlled Ring Oscillator (a type of ring oscillator)</td>
<td></td>
</tr>
<tr>
<td>DCO</td>
<td>Digital Controlled Oscillator (change output frequency based on controlling bits)</td>
<td></td>
</tr>
<tr>
<td>DVD</td>
<td>Digital Video Disc (a kind of optical disc storage)</td>
<td></td>
</tr>
<tr>
<td>HDMI</td>
<td>High Definition Multimedia Interface (an interface used to transmit uncompressed digital data)</td>
<td></td>
</tr>
<tr>
<td>LF</td>
<td>Loop Filter (filter used in a loop)</td>
<td></td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator (an electronic circuit use to generate a signal)</td>
<td></td>
</tr>
<tr>
<td>LPF</td>
<td>Low Pass Filter (a kind of a filter)</td>
<td></td>
</tr>
<tr>
<td>NTSC</td>
<td>National Television System Committee (analog television system)</td>
<td></td>
</tr>
<tr>
<td>PD</td>
<td>Phase Detector (a circuit used to detect phase difference)</td>
<td></td>
</tr>
<tr>
<td>PFD</td>
<td>Phase Frequency Detector (a circuit used to detect phase and frequency difference)</td>
<td></td>
</tr>
<tr>
<td>PGA</td>
<td>Programmable Gain Amplifier (a kind of amplifier)</td>
<td></td>
</tr>
<tr>
<td>PAL</td>
<td>Phase Alternate Line (analog encoding system)</td>
<td></td>
</tr>
<tr>
<td>RGB</td>
<td>Red Green and Blue (Three components of color video signals)</td>
<td></td>
</tr>
<tr>
<td>SECAM</td>
<td>Sequential Colour with Memory (In French, Séquentiel couleur à memoire, Analog color television first used in France)</td>
<td></td>
</tr>
<tr>
<td>TDC</td>
<td>Time-to-Digital Converter (used to convert a timing information into digital bits)</td>
<td></td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
<td></td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator (used to change output frequency according to input controlling voltage)</td>
<td></td>
</tr>
<tr>
<td>VCR</td>
<td>Video Cassette Recorder (type of video tape recorder that uses removable video tapes)</td>
<td></td>
</tr>
</tbody>
</table>
Chapter 1

1 Background and Introduction

1.1 Introduction

To provide Industrial environment for graduating students, at the division of Electronics Systems, Department of Electrical Engineering, a video project is initiated under the supervision of Dr. J Jacob Wikner, where many students can be supervised in shared forum. This mega project is divided into multiple sub projects of which this thesis is a part. The project is carried out by combined effort of students and researchers in a shared forum. The target of the mega project is to implement a digitizing video device for hand held devices such as laptops and micro projectors.

In this project, we used software like Cadence and Matlab. Every week we had a joint meeting to discuss the achievements and hurdles of the week with other project fellows and supervisor.

1.2 Video AFE

Figure 1.1 shows the architecture of the video IC consisting of two different channels:

1. Digitizing channel, the main purpose of digitizing channel is to select the desired input from the multiple inputs of the video signal and converts into the digital format.

2. Time/Reference channel, which is used to provide the timing information or synchronizing signal to the ADC.

We are going to discuss digitizing channel and reference channel one by one.

1.3 Digitizing Channel

The video signal is digitized when passed through digitizing channel consisting of input multiplexer together with DC clamp and followed by filter, the output of filter is feed to a programmable gain amplifier (PGA) and this signal is passed through an analog-to-digital converter (ADC) to get a digital output.
1.3.1 Input Multiplexer and DC Clamp

The input multiplexer is used for selection between different signals at the input of AFE. For high resolution formats it must guarantee high bandwidth and high linearity. Table 1.1, summarizes some of the specifications of the multiplexer.

<table>
<thead>
<tr>
<th>Item</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of inputs</td>
<td>8</td>
</tr>
<tr>
<td>Number of outputs</td>
<td>3</td>
</tr>
<tr>
<td>Linearity</td>
<td>60 dBc to 80 dBc</td>
</tr>
<tr>
<td>DC set time</td>
<td>1 frame</td>
</tr>
<tr>
<td>Isolation</td>
<td>70 dB</td>
</tr>
<tr>
<td>Min input voltage swing</td>
<td>200 mV&lt;sub&gt;PP&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

Table 1.1 Input multiplexer specifications [1]

1.3.2 Programmable Gain Amplifier

Filtered signal is given to programmable gain amplifier (PGA) to scale up or down the amplitude of the signal as desired by the ADC. To achieve a high output signal swing, high linearity and reduced noise fully differential amplifier architecture is used.

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Slew rate</td>
<td>5 mA/0.5 pF</td>
</tr>
<tr>
<td>Linearity</td>
<td>60 dB</td>
</tr>
<tr>
<td>Gain settings</td>
<td>0.5, 1, 2</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.2 V</td>
</tr>
</tbody>
</table>

Table 1.2 Programmable gain amplifier (PGA) specifications [2]

1.3.3 Input Low Pass Filter

The output of the multiplexer is feed to anti aliasing filter to reduce noise bandwidth and to band limit the ADC input signal.
1.3.4 Analog to Digital Converter

The differential output of the PGA is applied to a 12-bit, 300 MS/s time-interleaved successive approximation register (SAR) architecture based ADC. According to the project requirements, all components should be as digital as possible therefore the ADC design is based on SAR architecture.
<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of bits</td>
<td>12</td>
</tr>
<tr>
<td>Sampling frequency f-s</td>
<td>300 MHz</td>
</tr>
<tr>
<td>Input bandwidth</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Gain error, GE</td>
<td>1%</td>
</tr>
<tr>
<td>Offset error, OE</td>
<td>1%</td>
</tr>
<tr>
<td>SFDR/IMD</td>
<td>60 dBC</td>
</tr>
</tbody>
</table>

Table 1.3 Analog-to-digital converter (ADC) specifications [3]

1.4 Time/Reference Channel

The time channel is used to extract the timing information needed to control the digitizing channel as shown in Figure 1.1. The input video reference is fed to a multiplexer which selects the source of synchronization signal, which is passed on to the phase locked loop (PLL) and then the output of PLL is fed to a delay locked loop (DLL). As shown in Figure 1.1, the output of the DLL is then used as a sample signal to digitizing channels.

1.4.1 Phase Locked Loop

The objective of this thesis is to design all digital phase locked loop (ADPLL) to align the higher frequency signal at the output of the PLL with its input. The frequency range at the input is from 10 kHz to 150 kHz, at the output, we generate between 10 MHz to 300 MHz.

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input frequency</td>
<td>10 kHz to 150 kHz</td>
</tr>
<tr>
<td>Output frequency</td>
<td>10 MHz to 300 MHz</td>
</tr>
<tr>
<td>Jitter</td>
<td>2%</td>
</tr>
<tr>
<td>Output duty cycle</td>
<td>50%</td>
</tr>
<tr>
<td>Latency</td>
<td>2 clock cycles</td>
</tr>
</tbody>
</table>

Table 1.4 All digital phase locked loop (ADPLL) specifications [5]

Poor design of PLL may increase the cycle to cycle jitter, which will create variation in the starting point and will directly affect the video picture as shown in Figure 1.2.
1.4.2 Delay Locked Loop

The high frequency signal at the output of the ADPLL is fed to the delay locked loop (DLL), to generate 32 different phases. The DLL aligns the output clock with the input clock but with a controlled delay. The signal is delayed by passing through a delay line and controlling the delay line with some logic.

The table 1.5 summarizes some of the specifications of ADDLL

<table>
<thead>
<tr>
<th>Item</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>10 MHz to 300 MHz</td>
</tr>
<tr>
<td>Number of phases</td>
<td>32</td>
</tr>
<tr>
<td>Jitter</td>
<td>2%</td>
</tr>
<tr>
<td>Latency</td>
<td>2 clock cycles</td>
</tr>
</tbody>
</table>

Table 1.5 All digital delay locked loop (ADDLL) specifications [4]
1.5 Reference


Chapter 2

2 Analog Front End (AFE)

2.1 Introduction

Despite the increased and emerging role of digital interfaces, the analog video interface still provides a backbone in multimedia applications. This is due to their better image quality and also the low power consumption when compared to some digital video interfaces. So, one cannot avoid the role of video analog front end (video AFE) to input signal port for variety of high-quality display devices. It also increase the number of possible signal sources in home entertainment, computer graphics etc.

2.2 Simplified Video AFE Block Diagram

Consider the very basic video AFE, it may comprise one or more analog to digital converters (ADCs) and a bundle of circuits for clamping, signal conditioning and filtering. In most of the cases the video AFE also requires some sync processing block. The purpose of this sync processing circuitry is to extract timing and frame sync from the analog signal.

![Simplified video AFE block diagram](image)

In the diagram shown in Figure 2.1, the ADC is one of the important parts. According to the application, the sampling frequency and resolution varies. These variations are comparatively small to the variation in analog portion of the video AFE’s signal path. For example, SDTV requires 10-12 bit at the sampling rate of 27/25 MS/s, 1080p HDTV required 10-bit at 148.5 MS/s.
Computer display application requires resolution of 8-10 bit. As to fulfill the requirement of WUXGA/60 Hz or UXGA/75 Hz resolution display, the sampling frequencies increase to 205 MS/s. Other than the requirement of ADC, the video signal chain is complicated to its overall performance. In most cases it is more critical to design that signal chain than the ADC. Since, the signal that has to be digitized by the ADC must be conditioned and passing through a certain steps so that it can be digitized correctly.

Voltage clamping is one of the steps through which the signal has to be passed before it reaches the ADC for digitizing. Mostly the video signal has some DC component and before digitizing the signal, it is necessary to scale down or scale up the signal to its original state or at least to the acceptable level of the ADC. There are numerous methods for clamping available depending on situation and requirement. For example, in SDTV a charge pump is used, while in computer monitors and HDTVs more complicated method are introduced.

Programmable gain amplifier (PGA) is used to control the gain of the incoming signal. It adjusts the swing of the signal to meet the requirements of the input range of the ADC. It is also used to control the saturation of each color component or brightness/contrast.

Clock recovery and sync generation are used to extract the sync signal from video signal as the sync signal can be embedded with the analog video signal. The performance of this circuitry significantly contributes the overall performance of the video AFE.

2.3 Video Data Concept [1]

There are many techniques and methods of transferring the video data from one place to another. The visual data may be from video cassette recorder (VCR), digital video disc or digital versatile disc (DVD) players, broadcasted channel, satellite television and many others. The main purpose is to transfer video data from one point to another safely. It sound very easy but too many requirements make it complex and there are several ways.

In general, there are two options, digital or analog. Historically, most of the equipments were analog and digital video was confined to rare applications like video editing, but now digital applications are moving towards average consumer, which decreases the cost up to significant levels; for example HDMI (high definition multimedia interface).

Once upon a time, the video signal contained only the black and white information. Gradually video signal became colorful. In colored video signals the data is transmitted using RGB that is red, green and blue components. The main disadvantage of this technique was bandwidth. RGB occupies three times larger bandwidth than current gray-scale (black and white). To solve this problem; a technique was developed instead of RGB, YIQ or YUV data were transmitted as a color signal. In YIQ or YUV only one signal is transmitted instead of three different signals and
mainly it requires same bandwidth as a traditional gray scale format. NTSC, PAL and SECAM video standards are also based on this technique.

For connecting consumer equipment together, S-video was developed. This S-video signal is comprised by two analog signals. One signal carries Y and another carries U and V information in a particular format; also called C or chroma. Previously, the S-video was only available on S-video home system (S-VHS) machines, but now it is found in many televisions, settop boxes and DVD players. The YPbPr is a slight modification in analog YUV video signal and is also used for connecting equipment together.

2.4 Video Image

The video signal consists of a number of still images that rapidly change, so that a continuous motion is sensed. This motion occurs 50 or 60 times per second for consumer video and 70 to 90 times for computers graphics. Therefore a video display device requires timing information for when a new image is starting, which is called vertical sync.

Figure 2.2 Still image composed of multiple individual lines & video consist of multiple still images [1]
There is also so-called horizontal sync. The horizontal sync has information about when every new scan line starts. Each still image also consists of scan lines, these lines of data come in sequential fashion down the display. A combination of both horizontal and vertical syncs is known as a composite signal.

There are three different ways of transfer vertical and horizontal information:

a) By transferring horizontal and vertical sync signal separately. Computers and consumer devices that use analog RGB video transmit horizontal and vertical sync separately.
b) By transferring composite sync signal without video signal.
c) By transferring composite sync signal embedded within video signal. The devices that are based on analog YPbPr video normally rely on this technique.

2.4.1 Interlaced and Non-Interlaced

The video is a series of stagnant pictures so each full video is displayed in a sequential order. This basic technique is known as progressive or non-interlaced technique. In this technique, the CRT starts from the top left corner and is gradually moved towards right edge of the image, this movement is known as horizontal scanning as shown in Figure 2.3 and when it reaches to extreme right corner, it moves down to second line (known as vertical scanning) and again started from the extreme left corner of image. This whole mechanism is repeated again and again until the entire screen is refreshed. It can be shown in Figure 2.3.
Another technique is interlacing, where the amount of information sent for the image is reduced. In interlacing, we define two fields for horizontal scanning i.e., horizontal scanning field 1 and horizontal scanning field 2, as shown in Figure 2.4. The odd-numbered lines are transferred followed by the even-numbered lines. Hence by doing so, the amount of sent information for each image is halved. Although, interlacing is not using for computer monitors and few new digital formats television, it is still used in a number of consumer application; for example cathode ray tube (CRT) television.
2.5 Video Resolution

The video resolution is one of the important aspects of video signal; for example, 720 x 480 or 1920 x 1080. This information explains the number of horizontal samples and vertical scan lines in visible field. Let us consider an analog signal that can be sampled at 13.5 MHz to generate 720 samples per line. By sample the same signal at frequency of 27 MHz it can generate 1440 samples per line.

2.5.1 Standard Definition Video

The NTSC, PAL and SECAM video formats all belongs to the same standard definition family. The bandwidth of standard definition has about 6.75 MHz and the active resolution of 720 x 480 or 720 x 576 interlaced. While, in broadcasting of NTSC 330 lines of resolution is require at a maximum bandwidth of 4.2 MHz.

Figure 2.4 Example on interlaced display of a video signal [1]
2.5.2 Enhanced Definition Video

Enhanced definition is one of the most recent categories having an active signal of 720 x 480 progressive or greater. The main difference between standard definition and enhanced definition is that enhanced definition is comprised on non-interlaced or progressive while the standard definition is interlaced.

2.5.3 High Definition Video

High definition video has two possibilities of active signal. One has an active signal of resolution of 1920 x 1080 interlaced and another possibility is 1280 x 720 progressive.

2.6 Color Spaces

There are three dominating models for the mathematical representation of a set of colors depending upon their applications. They are also known as color spaces. These color spaces are not associated to intuitive notions of saturation, hue and brightness.

a) RGB (represented by three dimensional Cartesian coordinate system).

b) YIQ (required bandwidth equal to the traditional gray scale).

c) YCbCr or YUV (in YUV, Y used for Lumina while U and V are used for color information. YCbCr is also known as a scaled or offset version of YUV).

Let's consider, the RGB color space first.

2.6.1 RGB Color Space

RGB stands for red, green and blue. These components are three primary additive colors and can be added together with a fixed proportion to form the desired color. Typically, RGB increases the easiness of the architecture and design of the system. The systems that are designed on the basis of RGB are more flexible. They can benefit from a large number of present software routines. RGB is represented in a three dimensional Cartesian coordinate system and can be explained as a three dimensional cube as shown in Figure 2.4.
The main disadvantage of RGB is that all three components need equal bandwidth to represent the desired color within the RGB color cube. That is why RGB is not very effective and beneficial for real world images. If one wants to change the intensity or a color of a pixel all the three RGB values must be updated; the new desired intensity and color of pixel is calculated, then modification are accomplished and the new RGB values are written back to frame buffer. Hence processing an image in this color space is not a suitable task.
The 100% amplitude and saturation of an ordinary video signal can be shown in Table 2.1.

<table>
<thead>
<tr>
<th></th>
<th>Red</th>
<th>Green</th>
<th>Blue</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Range</td>
<td>0 to 255</td>
<td>0 to 255</td>
<td>0 to 255</td>
</tr>
<tr>
<td>White</td>
<td>255</td>
<td>255</td>
<td>255</td>
</tr>
<tr>
<td>Yellow</td>
<td>255</td>
<td>255</td>
<td>0</td>
</tr>
<tr>
<td>Cyan</td>
<td>0</td>
<td>255</td>
<td>255</td>
</tr>
<tr>
<td>Green</td>
<td>0</td>
<td>255</td>
<td>0</td>
</tr>
<tr>
<td>Magenta</td>
<td>255</td>
<td>0</td>
<td>255</td>
</tr>
<tr>
<td>Red</td>
<td>255</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Blue</td>
<td>0</td>
<td>0</td>
<td>255</td>
</tr>
<tr>
<td>Black</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2.1 In a video signal 100% RGB color bars [1]

2.6.2 YUV Color Space

The phase alternation line (PAL), National Television System Committee (NTSC) and sequentiel couleur avec mémoire (SECAM) composite color video standards used YUV as a color space. In YUV the Y is used for luma and U and V is used for color information. Therefore, the black and white (gray scale) has only luma (Y) information. The information is sent just a way so that black and white receiver can receive Y information and decode it while only the color receivers and decode the additional color information to display a color picture [1].

2.6.3 YIQ Color Space

In YIQ, I and Q stand for in-phase and quadrature phase, respectively. Here IQ is the modulation method, used to transmit the color information. YIQ is also used by NTSC.

2.6.4 YCbCr Color Space

During the development of world-wide digital component video standard YCbCr color space was developed as part of international telecommunication unit – recommendation (ITU-R BT.601).
In YCbCr, Cb and Cr are defined to have eight bit range of 16-240 and Y has nominal range of 16-240. YCbCr is also known as a scaled and offset form of the YUV color space [1].

Table 2.2 and Table 2.3 are the lists of the YCbCr values for 75% amplitude and 100% saturated color bars for SDTV as well as HDTV.

### SDTV

<table>
<thead>
<tr>
<th></th>
<th>Y</th>
<th>Cb</th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Range</td>
<td>16 to 235</td>
<td>16 to 240</td>
<td>16 to 240</td>
</tr>
<tr>
<td>White</td>
<td>180</td>
<td>128</td>
<td>128</td>
</tr>
<tr>
<td>Yellow</td>
<td>162</td>
<td>44</td>
<td>142</td>
</tr>
<tr>
<td>Cyan</td>
<td>131</td>
<td>156</td>
<td>44</td>
</tr>
<tr>
<td>Green</td>
<td>112</td>
<td>72</td>
<td>58</td>
</tr>
<tr>
<td>Magenta</td>
<td>84</td>
<td>184</td>
<td>198</td>
</tr>
<tr>
<td>Red</td>
<td>65</td>
<td>100</td>
<td>212</td>
</tr>
<tr>
<td>Blue</td>
<td>35</td>
<td>212</td>
<td>114</td>
</tr>
<tr>
<td>Black</td>
<td>16</td>
<td>128</td>
<td>128</td>
</tr>
</tbody>
</table>

Table 2.2 Seventy-five percent YCbCr bars for SDTV and HDTV [1]
## HDTV

<table>
<thead>
<tr>
<th></th>
<th>Y</th>
<th>Cb</th>
<th>Cr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal Range</td>
<td>16 to 235</td>
<td>16 to 240</td>
<td>16 to 240</td>
</tr>
<tr>
<td>White</td>
<td>180</td>
<td>128</td>
<td>128</td>
</tr>
<tr>
<td>Yellow</td>
<td>168</td>
<td>44</td>
<td>136</td>
</tr>
<tr>
<td>Cyan</td>
<td>145</td>
<td>147</td>
<td>44</td>
</tr>
<tr>
<td>Green</td>
<td>133</td>
<td>63</td>
<td>52</td>
</tr>
<tr>
<td>Magenta</td>
<td>63</td>
<td>193</td>
<td>204</td>
</tr>
<tr>
<td>Red</td>
<td>51</td>
<td>109</td>
<td>212</td>
</tr>
<tr>
<td>Blue</td>
<td>28</td>
<td>212</td>
<td>120</td>
</tr>
<tr>
<td>Black</td>
<td>16</td>
<td>128</td>
<td>128</td>
</tr>
</tbody>
</table>

Table 2.3 Seventy-five percent YCbCr bars for SDTV and HDTV [1]
2.7 References

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Chapter 3

3 Phase Locked Loop

The concept of phase locked loops (PLLs) was described in 1932, when British researchers found homodyne direct conversion receiver as an alternative to the superherodyne receiver. In the homodyne system, a local oscillator was used to multiply and tune the input signal. There might be a problem that the local oscillator would swiftly drift in frequency, therefore, a self balancing signal was applied to the oscillator to keep the same frequency and phase of the signal as the desired signal. This concept was defined in 1932, by French research Henri de Bellescize in the L’onde Électrique journal [9].

Phase locked loops can be generalized as a control model whose major task is to generate a signal at its output whose phase is aligned to the phase of the input signal or reference signal. PLLs compare the output waveform to the input waveform and generate a phase error, which drives the oscillator. According to the phase error, the oscillator increases or decreases the oscillation frequency and tries to match the phase of the output waveform to the input waveform.

In most communication or controlling ICs, PLLs and DLLs are found where they are used to align the input and output clock phases. To accomplish this task the PLL uses a voltage controlled oscillator (VCO) to generate the desired output frequency by integrating frequency and continuously comparing the input and output clock phases using a phase detector. Taking the advantage of its integrating nature, the PLLs are widely used for frequency multiplication.

While on the other hand, DLLs align the reference clock or input clock and output clock by a delaying mechanism. DLLs compare the input clock to the output generated clock and generate a phase skew. According to the phase skew the delay of a delay line is controlled. The delay may increase or decrease according to the nature of the phase error.

PLLs are abundantly used in telecommunication, computers, televisions, radio applications and many other electronic applications. It can be used to generate stable frequencies from the distorted channel and recover a desired clock signal. According to the application, the phase locked loop can be used for demodulation as well as frequency synthesis. As we know that, phase is the integral of frequency, by holding the input and output phase in locked state indirectly means that the input and output frequencies in a lock condition. On the other side, PLLs can be used as frequency synthesizers because it can track an input frequency or can generates the multiple of input frequency by simply multiplying by a number.
3.1 Applications of PLL

There are many variations in PLLs architectures. Architecture is dependent on the applications, but the basic PLL has remained nearly the same since 1932. PLLs found in synchronization applications. PLLs are also used for the synchronization of bits or symbol and for the extension of threshold in space communication.

3.1.1 Recovery of Clock

In high streams of data, such as data from the magnetic head of a disk drive, serial data streams are sent to the receiver without any synchronization of clocks. At the receiving side, a clock is generated whose frequency is almost equal to the frequency of the reference signal and then the task of the PLL is to aligned the transitions in data stream. The whole process is known as clock recovery. There is a restriction in this process: to work properly the stream of data must have a transition frequency which is sufficient high enough to correct any drift in the PLL oscillator.

3.1.2 Deskewing

Due to process variation, like temperature and voltage drift, there is a finite delay between the detected clock edge and the received data. Specially, in case when a clock is sent in parallel with data, this clock received and amplified before it can be further used to drive the flip-flop, also increased the delay. To eliminate this delay a deskew PLL on the receiver side is introduced such that clock sampling is in phase with the received clock.

3.1.3 Clock Distribution

In Figure 3.1, a reference clock is applied to the chip and to the PLL. The PLL generates an output clock which is actually the input clock for the coming block on the chip which is clock distribution. The main idea is to keep the clock distribution in balance state so that at the output of the clock distribution and each clock generated should be synchronized. Hence, one of the output clocks of clock distribution block is applied to the feedback terminal of phase locked loop. The phase locked loop varies the phase and frequency of the output clock until the phase of the feedback clock is aligned to the phase of reference clock. At this state, the frequencies of the reference and feedback clock are equal.
PLLs can be considered as omnipresent in electronic systems. PLLs can be used to tune the clock in a small part of each individual IC but can also tune separate ICs which might be at far distance. There might be a case that reference clock may not be in good shape, so the responsibility of the PLL is to recover a regular clock. Depending on the applications, on some occasion the reference clock is exactly the same as the output clock, or it might be the case that output of distributed clock may be a rational multiple of the reference clock. PLLs tackle both cases efficiently.

3.1.4 Frequency Synthesis

In digital communication systems the PLL is widely used. Especially in wireless communication system like global system for mobile (GSM), code division multiple access (CDMA), etc, PLL is one of the most essential parts. The PLLs are used for up conversion and down conversion. In most cellular handsets, the purpose of local oscillator (LO) is achieved by PLL and it reduces the cost and size of the handset significantly. In GSM, the desired channel is selected by up and down conversion of the frequency which increased the complexity in architecture. While, in PLL by simply change the division ratio (M) as shown in Figure 3.2, frequency can be increased or decreased very easily. Therefore, in GSM the LO modules are designed with a frequency synthesizer IC.
3.1.5 Reduction of Noise and Jitter

The most abundant property of all PLLs is to align the reference clock and feedback clock edges as close as possible but still there is a difference in phase. Here static phase offset appear, which can be defined as the average time difference between reference and output clocks phases. The static phase offset also known as steady state phase error. This variation in phases is also known as tracking jitter. Practically, there are static phase offset error and tracking jitter problems, but ideally the steady state phase error should be equal to zero and the jitter should take as small values as possible.

Due to jitter a related phase-noise problem is created. The main reason for the phase noise is the amplifier block in the system. To keep this phase noise at a minimum one solution is to design the digital PLLs with emitter coupled logic (ECL) blocks but it may increase the power consumption. The property, which distinguishes PLL from other electronic blocks is higher noise rejection. As the phase and frequency of generated clock is unaffected by the sudden variations in the voltages of the supply lines and ground. This property is known as supply and substrate noise rejection.
3.1.6 Generations of Clock

Microprocessors are typically operated at different frequencies. Usually, a PLL is used to provide clock to these processors. The PLLs multiplies a reference with a particular multiplication factor or ratio. The ratio can be large or may be unity.

3.1.7 To Reduce Interference

Interference is one of the major problems in modern electronic systems. Almost all electronic equipment has an interference problem as they emit unwanted radio frequency energy. Many agencies such as FCC put limits on this wasted energy. Normally, at the operating frequency and on few harmonics this emitted noise is strong. To minimize this effect a designer can used spread spectrum PLLs. Due to the PLL the interference is reduced significantly with high-Q receiver. PLLs can be used to spread the energy over a larger portion of the spectrum due to which interference is reduced.


PLLs are widely used for frequency control as they can be utilized as frequency multipliers, demodulation, clock recovery and as tracking generators. Although each application has its own features and requirement but all unite on a single basic principle of PLLs.
Figure 3.3 shows the basic block diagram of PLL frequency multiplier. PLLs are a feedback control system that controls the phase of a voltage controlled oscillator (VCO). The phase detector (PFD) takes two inputs $f_{\text{ref}}$ and $f_{\text{back}}$. One input is the reference frequency input and the second is the feedback clock which is actually the output of the divider. Now at working condition the phase and frequency of phase detector’s input should be the same, but in starting condition they could be far apart. The working of the phase detector is to generate an error signal by taking the difference of reference signal and feedback signal. This error signal is the voltage proportional to the phase difference between inputs of phase detector. The larger the phase difference the larger will be the error signal similarly on other hand smaller the phase difference smaller will be error signal.

The error signal is applied to the charge pump (CP) as shown in Figure 3.3. The CP controls the charging and discharging of the loop filter. After the CP, we have loop filter. The main purpose of this loop filter is to determine the dynamic characteristic of the PLLs. The loop filter also plays an important role in the stability of the whole PLL. It provides a smooth output which is directly applied to the input of the VCO. VCO oscillates according to the voltage. Normally, the larger the input voltage, larger the oscillation of the VCO and the output frequency of the PLL increases. While on the other hand, if a small voltage is applied to the input of the VCO then the oscillation is slow and the output frequency is comparatively low. The oscillation increases or decreases according to a particular proportion of the increase or decrease in input voltage. This proportion is known as VCO gain. VCO are considered to be the heart of the PLL.

It is worthwhile to mention, that the output frequency of the VCO $f_{\text{out}}$ is $N$ times input reference frequency $f_{\text{ref}}$. This output $f_{\text{out}}$ is sent to the divider block which is normally $N$ counter. The divider block divides the $f_{\text{out}}$ signal and generates $f_{\text{back}}$ signal. The $f_{\text{back}}$ divided signal is sent back to phase detector (PFD).

### 3.3 PLL Architecture

The PLLs can be categorized as

- Analog PLLs, most of the components are analog. For example, charge pump, loop filter, VCO etc.
- Digital PLLs, still few components are analog. For example VCO etc.
- All digital PLLs, each component in architecture is digital.

In section 3.4, we have explanations for the analog PLLs.

### 3.4 Analog PLLs

It is discussed in section 3.2, PLL generally comprise on phase detector, charge pump, loop filter, voltage controlled oscillator and optional divider no matter its analog or digital PLLs.
- Phase detector (use to compare phase between reference signal and feedback signal)
- Charge pump (use to control the current in loop filter)
- Loop filter (use to provide sufficient phase margin for stability)
- Voltage controlled oscillator (used for frequency oscillation)
- Divider (used when PLL is used as multiplier)

Let consider, the first component of the PLL.

### 3.4.1 Phase Detector [2]

PLLs are feedback systems that compare the input reference frequency with the feedback frequency. Therefore, PLLs require some kind of comparator that performs the comparison, and phase detectors are used. By comparing the two signals, i.e., the reference and feedback signals, the phase detector generates an output which is directly proportional to the phase error as shown in Figure 3.4.

![Phase Detector](image)

**Figure 3.4** Block diagram and characteristics of a phase detector [2]

Ideally, the average output voltage of the phase detector is directly proportional to the phase difference $\Delta \Phi$ between the two input signals $V_1(t)$ and $V_2(t)$ as shown in Figure 3.4. The slope of this line is $K_{PD}$, which is the gain of the phase detector. It is illustrated in the Figure 3.4, that the gain of the phase detector ($K_{PD}$) is also zero when the phase difference ($\Delta \Phi$) between the two signals is zero. If $\Delta \Phi$ is positive, the average output voltage is also increased with positive slope of $K_{PD}$.
3.4.1.1 XOR Gate

The simplest phase detector is a simple exclusive-OR (XOR) gate as shown in Figure 3.5. But, there are some limitations for this kind of a phase detector. The XOR gate generates a pulse at the output without any information about which waveform is leading and which one is lagging. Also the XOR gate produces the pulse at both the rising and falling edges of the signal as shown in Figure 3.5.

![Figure 3.5 Waveform of the XOR gate as a phase detector](image)

Figure 3.5 Waveform of the XOR gate as a phase detector [2]

Figure 3.5 shows the waveforms when the XOR gate acts as a phase detector. \( V_1(t) \) and \( V_2(t) \) are the two signals applied the input of the phase detector. There is a phase difference between these two input signals which is denoted as \( \Delta \Phi \). According, to the width of the phase error, the XOR gate generates the output pulse \( V_{out}(t) \) at rising edge as well as on falling as shown in Figure 3.5.

The consequences of this problem will be severe. Since, in lock condition when the reference signals and feedback signals are in phase there may be a slight variation in duty cycle of the feedback waveform, and then ideally there should be zero phase error. In the XOR gate implementation a phase error is generated output at both rising and falling edge. This phase error may destroy the locking condition.

3.4.1.2 D Flip Flop

A single D flip flop as shown in Figure 3.6 can be used as a phase detector. It will generate the pulse at the output irrespectively of the duty cycle of the reference signal.
3.4.1.3 Dynamic Phase Detector

Dynamic phase detector is widely used in both PLLs and DLLs circuits. The main advantage of the dynamic phase detector is that it can generate two kinds of signals; up and down which gives information about which waveform is leading and which one is lagging. Due to the generation of up and down signal the design of charge pump which are normally right after phase detector in PLLs and DLLs circuit become easy.
Figure 3.7 shows the schematic of dynamic phase frequency detector [1].

3.4.2 Charge Pump [2]

After the phase detector, typically charge pump is found in PLLs as shown in Figure 3.2. Whenever the phase detector generates error signals, normally up or down (having information of leading or lagging), these signals are sent to the charge pump. The charge pump consists of a couple of on-off switches and current sources. These on-off switches are used as controlling devices and control the current to the loop filter.
The basic architecture of the charge pump is shown in Figure 3.8. The loop filter is charged or discharged by the charge pump. When the upper switch $S_1$ is on, the loop filter is charging through the current source. When the upper switch $S_1$ is off and lower switch $S_2$ is on then loop filter is discharge.

3.4.3 Shortcomings of Charge Pump [7]

Normally, the $S_1$ and $S_2$ switches are transmission gates or simple a transistors that are on or off by an applied controlling voltage at gate. One problem could be mismatch. Due to this mismatch the charging and discharging current for the loop filter will not be equal.
Therefore, phase error due to current mismatches can be expressed by following formula.

\[
\Phi_e = 2\pi \frac{\Delta_{\text{ton}} |I_{\text{UP}} - I_{\text{DN}}|}{T_{\text{ref}} I_{\text{CP}}}
\] (3.1)

where,

|\(I_{\text{UP}} - I_{\text{DN}}|\) is the change of charging and discharging currents

\(\Delta_{\text{ton}}\) is the duty cycle of down/up signal

\(T_{\text{ref}}\) is time period for the reference signal

\(I_{\text{CP}}\) is current from the charge pump

### 3.4.4 Loop Filter [8]

Loop filter is found after the charge pump in PLLs circuits as shown in Figure 3.3. The purpose of the loop filter is to provide a voltage to the voltage controlled oscillator.

![Figure 3.9 RC filter (loop filter) for analog PLL [1]](image)

The loop filter can be a simple capacitor or may be with more passive elements as shown in Figure 3.9. The architecture of the loop filter depends on the application and the order of the filter.

### 3.4.5 Loop Filter Design Issues

In the following text, the design issues or important parameters that have to be kept in mind by the designer while designing a loop filter for particular application are described.
3.4.5.1 Loop Bandwidth

One of the main issues with the loop filter is the tradeoff between spur level and lock time. Loop filters with low loop bandwidth will have lower spurious noise but lower locking time. On the other hand, high loop bandwidth has faster locking time but poor spurious noise performance. So, good knowledge of designing is required to keep the balance between spur level and locking time.

3.4.5.2 Phase Margin

The phase margin strongly relates to the stability of the system. If the loop filter is unstable the whole PLL will be unstable. The designer has a range for selecting the phase margin. Typically, the phase margin is selected between 40 to 55 degrees or sometimes 40 to 60 degrees, but it may change dependent on the applications. The higher the phase margin, the system will be more stable. If the phase margin is zero then the system will completely unstable.

Consider the transfer function $G/ (1+GH)$, if the phase margin is zero, then the denominator of the transfer function will become zero, and making it infinite and function become unstable. The optimal value of phase margin can gives the fastest locking time.

3.4.5.3 Filter Order

To improve the spurious performance, the order of the filter is also important. If the filter has higher order then the main advantage is lower spur levels and better spurious free dynamic range (SFDR).

Filters with higher order have disadvantages as well. First of all, higher order filter has more passive components. Resistors introduce noise inside or outside the loop bandwidth. It may result in serious consequences, depending upon the application. Area is also increased with the increased order of filter since the number of capacitors increase and which occupy larger area.

3.4.6 Charge Pump with Phase Frequency Detector

To understand the complete mechanism of the charge pump, let consider a charge pump combined with a phase frequency detector and a simple loop filter as shown in Figure 3.10.
When the signal A is leading from the signal B, then the phase frequency detector will generate and $Q_A$ signal and the $Q_B$ signal is almost zero (a small glitch appears due to reset which is almost negligible). This $Q_A$ signal will turn on the $S_1$ switch and $Q_B$ signal will turn off the $S_2$ switch.

Figure 3.11 Timing diagram of phase frequency detector and charge pump [2]
Hence, there is a path of charging for the loop filter (a capacitor $C_p$). Due to charging of capacitor the output voltage ($V_{out}$) is increased. It will increase the oscillation of the VCO ($VCO \text{ gain} > 0$) and hence the phase difference will decrease. The voltage at the output will increase up to the maximum limit of the capacitor and/or switches until up signal is generated and it will be the case when signal A lagging behind B. The Figure 3.11 shows this mechanism for the charge pump together with phase frequency detector and loop filter.

### 3.4.7 Voltage Controlled Oscillator (VCO)

The voltage controlled oscillator (VCO) defines the output frequency of the PLL, and thereby known as heart of the PLL. The VCO oscillating frequency depends on its input voltage [1]. The oscillators must be tunable by any controlling bits or controlling voltage to cater for variations and applications.

![Figure 3.12 Block diagram of voltage controlled oscillator (VCO) [2]](image)

Ideally, the output oscillation frequency is a linear function of the controlling input voltage, and the relation can be described by [2]

$$\omega_{out} = \omega_0 + K_{VCO} \cdot V_{cont}$$  \hspace{1cm} (3.2)

Here $K_{VCO}$ represents the gain or the sensitivity of the VCO. The unit for $K_{VCO}$ is Hz/V. In Figure 3.13 $\omega_0$ is the intercept corresponding to $V_{cont} = 0$. The tuning range is described by the difference between the frequencies $\omega_2 - \omega_1$. 

3.4.8 Performance Parameters of VCOs [2]

In the following subsections are some important parameters of the VCO.

3.4.8.1 Center Frequency

The center frequency is the midrange value of the tuning range. It is chosen according to the environment in which VCO is working. In clock generation circuits of microprocessor, it might be possible that VCO run at the clock rate or may be at twice. Nowadays, the center frequency of CMOS based VCOs can be as high as 10 GHz [2].

3.4.8.2 Tuning Range

The tuning range is the range in which VCO oscillates. When VCOs are used in PLLs circuits, the output frequency depends on the VCO oscillation frequency, and the oscillation frequency of VCO depends on the tuning range. Therefore, the tuning range is one of the most important parameters of the VCO. The required tuning range depends upon two parameters [2].
a) Change in center frequency of VCO with process and temperature.
b) The required range of frequency. As different frequency range is required for different applications. In some applications, required clock frequencies that have to be scaled up in magnitude by one or two orders, depends upon the mode of operation, eventually require wide range of tuning.

### 3.4.8.3 Linearity in Tuning

Due to non-idealities, the gain of the VCO is not constant and the tuning behavior of the VCO becomes non-linear. Such kind of non-linearity creates big hurdles in settling behavior of the phase-locked loops. That is why it is desirable to keep gain variations as small as possible across the tuning range.

Practically, the VCO characteristic is shown in Figure 3.14. The VCO shows a high gain region in the centre of the range and low gain at the two extreme corners.

![Figure 3.14 Nonlinear characteristics of a voltage controlled oscillator [2]](image-url)
3.4.8.4 Amplitude of Output Waveform

To make the output oscillation waveform more immune to noise, it is desirable to achieve higher amplitude. The waveforms with higher amplitudes are less sensitive to noise. There is a tradeoff between power dissipation, voltage supply and also tuning range.

3.4.8.5 Power Dissipation

Power dissipation is one of the most important issues in any circuits. The output oscillation of the VCO is affected by the tradeoff between speed, power dissipation and noise.

3.4.9 Divider

The divider is an optional part of the PLL circuit. It is specially required when PLLs are used as frequency multipliers. If a divider with value N is used in PLL circuit, then the output frequency of the PLL is described:

\[ F_{\text{out}} = N \cdot F_{\text{ref}} \]  \hspace{1cm} (3.3)

where,

- \( F_{\text{ref}} \) is the reference frequency of the PLL
- \( F_{\text{out}} \) is the output frequency of the PLL
- N is the division ratio.

3.4.10 Varieties of Dividers

There are many options for dividing the frequency, which one to use depends on the application.

The simplest type of divider is D-flip flop as shown in Figure 3.15. The D-flip flop is known as a transparent flip flop. Because at rising or falling edge of clock, whatever at the input is passed to the output. By using this property simple D-Flip flop can be used as divider [3].
The Figure 3.15 is dividing the frequency by a factor two. While, in Figure 3.16 there is a waveform for the input and output frequency. For the dividing factor of four or greater number, multiple D-flips flop can be use in cascaded state.

3.5 Digital PLLs and All-Digital PLLs [5]

In the system on chip (SOC) era, it is very easy to design a chip embedded with its own clock generator. Phase locked loops are used for this purpose. Previously PLLs were partially analog as few components such as charge pump or voltage controlled oscillators were analog. Designer has to face digital switching noise in mixing analog control signals. Therefore, design efforts
increased in a noisy digital environment. While on other side all digital PLLs (ADPLLs) are more immune to noise, better testability, programmability, stability and especially easy integration into a digital system.

3.6 Basic Architecture of ADPLL

The purpose of PLLs are almost same whether its analog, semi digital or all digital. Although in architecture there are some changing and replacements as shown in Figure 3.17. The time to digital converter (TDC) is introduced instead of charge pump. While the analog filter is replaced by digital filter and the VCO is replaced by digitally controlled oscillator (DCO) as shown in Figure 3.17.

![Basic block diagram of the digital phase locked loop](image)

Figure 3.17 Basic block diagram of the digital phase locked loop [6]

3.7 Different Approaches

There are many different approaches to design digital PLLs. These are as follows.
The block diagram shown in Figure 3.18, architecture is a proposed in [4]. Here the pre-divider is used to slow down its frequency [4]. The PFD performs almost the same task as in previous architecture. Here controller block is used. The purpose of the controller block is to perform the locking algorithm by changing the controlling code once in a number of cycles. Here the purpose of filter is also performed. The controlling block also filtered out some glitches by averaging algorithm. After performing the controlling algorithm, the controller block provides controlled codes to DCO and then DCO oscillates accordingly.

Figure 3.18 All digital phase locked loop architecture [4]

Figure 3.19 shows architecture of a PLL, proposed in [6]. Here the PFD detects the frequency and phase difference between the input and feedback signals, and results in an error pulse signal and the direction signal. The error pulse signal is further quantized by the TDC. The TDC generated digital bits, which are sent to the DCO, after passing through the digital filter. There are two arrangements for the filter and TDC as shown in Figure 3.19. The upper chain is known as coarse TDC and filter while the lower one is known as fine TDC and filter.
Figure 3.19 All digital phase locked loop (ADPLL) architecture [6]
3.8 Why Digital PLL

Although analog PLLs exhibit good jitter performance compared to digital PLLs, they are more immune to noise and better skew suppression but despite all these advantages they are more sensitive to process variations. In deep submicron the complexity for designing a PLL increases. In the analog filter the capacitor occupies too much space. This problem becomes more critical when the PLL requires a higher order filter.

The digital circuitry has many advantages over an analog circuitry and almost all these advantages are justified by digital PLL over an analog. Therefore, it confers more benefits to make the circuits more as digital as possible. In addition, the digital PLL can operate at a lower voltage supply, even at a voltage of 0.9-1 V. Digital has shorter lock time compared to the analog PLLs and are easier to migrate from one process to another in the same or different IC. On the other side digital PLLs has poor jitter compared to analog PLLs.
3.9 References


[5] H.J.Hsu, C.C.Tu and S.Y Huang, “A High-Resolution All-Digital Phase-Locked Loop with its Application to Built-In Speed Grading for Memory”, Department of Electrical Engineering National Tsing-Hua University, Taiwan.


[10] Application notes, “The PLL and Early History”, from a University of Guelph course, including an IC PLL tutorial.

4 Behavioral Model

System/circuit design is a step by step process and professionally every designer follow these set of steps. A designer starts with a vague idea of functionality and time constraints from customer and then keeps the time limitation in mind. He develops a behavioral model of the required system. After completing the first steps the model is presented before the customer, to ensure the functionality. At this stage if the customer is satisfied by the functionality of the system, the designer jumps to gate level implementation or redevelops the behavioral model with desired changes. Do designers go for behavioral/functional models and not on schematic directly? The most common and suitable answer is, that it is easy to debug the behavioral model of the system than schematic.

In the same way we implement the behavioral model of our thesis project all digital phase locked loop (ADPLL). The chapter is divided into two portions:

1- Architecture selection.
2- Behavioral model of selected architecture.

In section 4.1, we are going towards architecture selection first and then behavioral model of selected architecture.

4.1 Architecture Selection

When we started our thesis work we selected the architecture shown in Figure 4.1. In this architecture we have a phase frequency detector (PFD), two parallel connected time-to-digital converters (TDC), two parallel connected digital loop filters, 1-1-1 MASH structure base fractional – N PLL used as DCO and a counter for frequency division [1].

The PFD compares the phase and frequency of the hsync (incoming signal to ADPLL) with the Fback (feedback signal) and generates error and direction signals. The error signal tells about the magnitude of phase difference between hsync and Fback, and direction signal is to increase or decrease the frequency. The error signal is passed to the TDC where it is converted in digital format which is used for manipulation in filter. TDC is followed by a digital filter which is simple bilinear transformation of a first order low pass filter. We will have detailed discussion on all these components in chapter 5.

The architecture is composed of two parallel paths i.e. coarse and fine path. Both contains same components but the difference can be seen in there frequency resolution. The coarse path is
active when error is greater than a certain value, with having high gain it can increase and decrease the frequency with large steps. On the other hand, the gain of fine path is lower and is used for fine resolution of frequency.
Figure 4.1 ADPLL architecture selected at start [1]
The problem with the architecture shown in Figure 4.1, is the DCO, which is not completely digital and according to our project specification all components should be digital to reduce space and enhance performance.

Then we thought to replace the DCO with a current starving digitally controlled ring oscillator (CSDCRO), but again we were unable to complete because the output of a single (coarse / fine) path was 16-bit and the combine output of 32-bit was a too large number of bits for the DCO. The working of DCO will be discussed in chapter 5. Although, this architecture would be more accurate and fast enough than several other ADPLL architectures, it was not fully digital.

4.2 Behavioral Model of Selected Architecture

The selected architecture of the ADPLL shown in Figure 4.2 is composed of similar components that were used in previous architecture but this time it is single path and consist of current starving digitally controlled oscillator (CSDCRO).

The complete block diagram of all digital PLL is shown in Figure 4.2.
Figure 4.2 Block diagram of the selected ADPLL architecture [2]
The phase frequency detector (PFD) is shown in Figure 4.3, is used to compare the phase difference between hsync and Fback signal. It calculates the difference between the rising edges of both signals and then outputs the magnitude of this difference as an error signal as shown in Figure 4.3. The second output of this block is direction signal which directs the DCO to either increase or decrease (depending upon direction signal) the frequency according to the magnitude of error provided by the PFD.

![Figure 4.3 Block diagram of the phase frequency detector (PFD) for the ADPLL [2]](image)

The PFD is followed by a time-to-digital converter (TDC) which converts the time magnitude of error into a 15-bit thermometer code. As shown in Figure 4.4, the input to the TDC block is an error signal and the same error signal is used as TDC clock signal. The internal structure of TDC will be explained in detail in later chapter 5.

To reduce the number of bits at the output of the TDC a thermometer to binary converter (T2B) is used which converts this 15-bit thermometer code into 4-bit binary number.
This 4-bit binary number is then feed to the loop filter to filter out the undesired high frequency signals, to preserve the frequency response and stability of the system [2]. Digital loop filter is used and is a bilinear transformation of a resistor in series with a capacitor. The functionality and transformation of an RC filter into digital filter is explained in chapter 5. As shown in Figure 4.5 there are the four inputs from In[0] to In[3] and a clock signal which define the sampling period of the discrete time system.

Figure 4.4 Block diagram of time-to-digital converter (TDC) for the ADPLL [2]

Figure 4.5 Block diagram of digital low pass filter (digital LPF) for the ADPLL [2]
This 11-bit output of the filter will decide the output frequency of the current starving digitally controlled ring Oscillator (CSDCRO). Frequency increases with decrease in delay and this delay is set by the magnitude of the bits at the input of CSDCRO. The functionality of the CSDCRO and the relation between frequency and input bits is explained in chapter 5.

To achieve frequency multiplication, the frequency of the signal generated by the CSDCRO is divided using a frequency divider circuitry and then fed back to the PFD as shown in Figure 4.2.

Figure 4.6 Block diagram of digitally controlled oscillator (DCO) for the ADPLL [2]
4.3 References


Chapter 5

5 Schematic Level Description of the ADPLL and Simulation Results

In this chapter, the schematic level of ADPLL is described. In addition, almost all the important individual blocks of the ADPLL are explained: phase detector, time to digital converter, digital low pass filter, DCO (the most important part of ADPLL) and the divider will be explained according to their individual functionality as well as duties and participation in whole ADPLL.

5.1 Circuit Components

The important components of circuit are.

1. Phase and frequency detector (PFD)
2. Time-to-digital converter (TDC)
3. Digital loop filter (digital LPF)
4. Digital controlled oscillator (DCO) and divider

Let us, briefly discuss these circuit components one by one.

5.2 Phase and Frequency Detector (PFD)

The phase detector is used to compare the phase and frequency of the input reference with the feedback clocks and generate the error and a direction signal. Before deep analysis of the PFD circuit, it is important to give a slight introduction of the D-flip flop here, because the PFD circuit is consists on D-flip flop.

5.2.1 D-Flip Flop

Figure 5.1 shows the block diagram of the D-flip flop. The D-flip flop has four important terminals: D, Clk, Q and Qbar. Reset terminal is an optional. The D-flip flop is also known as a delay flip flop because whatever the data at the D terminal, reaches the output Q at a delay of maximum one clock cycle. The D-flip flop used here are the positive edge triggered.
5.2.1.1 Schematic of D-Flip Flop

Figure 5.2 shows the schematic of D-flip flop using NAND gates. The schematic of the D-flip flop is almost same as the RS-latch. The only difference is that the two inputs of the RS-latch, R and S are combined as a single input and the R input has the inverted version of the S input which is known as D. These changes are only performed in the master section while the slave latch section remains unchanged.
5.2.1.2 Operation of D-Flip Flop

By considering a positive edge trigger, when the rising edge of clock appears at the clock input CLK of the D-flip flop, whatever at the input of D, it appears at the output terminal Q and its inverted output is appear at the Qbar terminal. On the contrary when the falling edge of clock is appear at the Clock input CLK there is no change at the output of D-flip flop, that means D-flip flop has keep its previous state unchanged.

The mechanism is for positive edge trigger D-flip flop. Negative edge triggered D-flip flop works on the negative edge of the clock and rest of the functionality is same as a positive edge trigger.

<table>
<thead>
<tr>
<th>Clock</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising edge</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Rising edge</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Non-rising edge</td>
<td>X</td>
<td>$Q_{\text{prev}}$</td>
</tr>
</tbody>
</table>

Table 5.1 Truth table for the D flip-flop [1]

5.2.1.3 Types of D-Flip Flop

According to the timing characteristics, D-flip flops can be classified into two categories.
1. Synchronous D-flip flop (dependent on clock edge)
2. Asynchronous D-flip flop (independent of clock edge)

Let have a look on the two mentioned types of D-flip flop.

5.2.1.4 Synchronous D-Flip Flop

In synchronous D-flip flop the reset signal is synchronized with respect to clock edge. In synchronous D-flip flop, if the reset signal enable, the D-flip flop will wait until the rising edge of clock will appear at the clock input and when the rising edge of clock appears at the Clk input the whole D-flip flop will reset as shown in Figure 5.3.

![Waveform of the synchronous D flip-flop](image)

**Figure 5.3 Waveform of the synchronous D flip-flop [5]**

5.2.1.5 Asynchronous D-Flip Flop

In asynchronous D-flip flop, the reset signal is not synchronized with respect to clock. This means that if the reset signal is enabled, no matter what is the condition or state of clock signal, the whole D-flip flop will reset, de asserting the Q output as shown in Figure 5.4.
Figure 5.4 Waveform of the asynchronous D flip-flop [5]

5.2.2 Schematic of Phase Frequency Detector (PFD)

Schematic of the phase and frequency detector (PFD) consists of three D-flip flops, one NAND gate, one AND gate, one inverter and one OR gate. The PFD generates an error signal and a direction signal by comparing the phase and frequency of hsync and Fback clocks, respectively. Error and direction signals are the representation of phase error and the DCO frequency control direction.

The PFD circuit is, to some extent, a modified circuit of tri state phase frequency detector [2]. As it is shown in Figure 5.5 instead of up and down signals here error and direction signals are the final output of the PFD. The output of NOR gate is an error signal, with the input signals: up and down, while the direction signal is taken from the D-flip flop, where up signal is applied at the input and down signal is applied at the CLK input of the D-flip flop as shown in Figure 5.5.
The D input of first two D-flip flops are connected to the $V_{dd}$ as shown in Figure 5.5. When the rising edge of the hsync (input reference signal) arrives at the clock input of D-flip-flop, the output of D-flip flop will become high and up signal will appear at the output of D-flip flop. As the D-flip flop used here is positive edge triggered. And this intermediate up signal is applied to the input of NAND gate. Similarly, on the lower side Fback signal is applied at the clock input of the D-flip flop and down signal is the output. This down signal is applied at the second input of the NAND gate. According to the functionality of a NAND gate, whenever both inputs are high, the output of the NAND gate becomes zero. The output of this NAND gate is actually the reset signal for the first two D-flip flops as shown in Figure 5.5. It will be worthwhile to mention here that both D-flip flops are synchronous D-flip flops and are active low. Hence, when up and down signals become high, both flip flops will be reset. In such a case, the error signal will suddenly go down to zero as the error signal is the output of a NOR operation between up and down signals [2].

Direction signal directs the DCO frequency. The DCO should increase or decrease the frequency according to the nature of the direction signal. When the direction signal becomes high, the DCO will increase its oscillations and when the direction signal becomes low, the DCO will decrease its oscillations. By increasing or decreasing the oscillation of the DCO, the output frequency of the PLL will increase or decrease respectively [3].
<table>
<thead>
<tr>
<th>Direction</th>
<th>Oscillation of the DCO</th>
<th>PLL output frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (Logic high)</td>
<td>Increase</td>
<td>Increase</td>
</tr>
<tr>
<td>0 (Logic low)</td>
<td>Decrease</td>
<td>Decrease</td>
</tr>
</tbody>
</table>

Table 5.2 Behavior of the direction signal in proposed ADPLL [3]

5.3 Time-to-Digital Converter (TDC) [3]

As mentioned earlier, the PFD has two output signals, an error signal and a direction signal. The error signal is converted into digital bits by TDC which is comprised of a series of switches, inverters and D-flip flops as shown in the Figure 5.6.

There is a couple of inverters for every stage. The delay of both inverters is equal to ΔTDC, which is the resolution of TDC. When the error signal becomes high, all switches will close and the V_{dd} signal will directly appear at the D input of D-flip flop. On the contrary, when the error signal becomes low, all switches will open. In this case, the error signal appears at D input of the D-flip flop after passing through two inverters, having a particular delay. When the error signal again goes back to high, these D-flip flops will triggered and the outputs will appear at the output of the D-flip flop as TDC[14] to TDC[0].

The output bits of TDC, from TDC[14] to TDC[0] are in thermometer-code format. Hence, it is necessary that the rest of the blocks of PLL should support this code format. In our design the digital low pass filter supports the binary format code. Therefore, a decoder is used to convert the thermometer code into the binary code.
Figure 5.6 Block diagram of time-to-digital converter (TDC) [3]
5.4 Digital Loop Filter (DLPF)

The main purpose of the loop filter in PLLs is to provide a competent amount of phase margin for stability [3]. Stability is the back bone of any PLL circuit. By considering an ordinary charge pump PLL, the simplest loop filter consists of a resistor in series with a capacitor as shown in Figure 5.7. The value of resistor and capacitor decides the filter phase margin.

![Figure 5.7 Schematic of the low pass filter (LPF) [3]](image)

Let $Z(s)$ be the transfer function of a circuit shown in Figure 5.7, in $s$-domain. Then the value of $Z(s)$ is [3]

$$Z(s) = \frac{V(s)}{I(s)}$$

$$= R + \frac{1}{sC}$$

For the transfer function of the digital filter, the equation 5.1 is converted from $s$-domain to $z$-domain by applying bilinear transformation.

$$H(z) = |Z(s)|_{s=\frac{2(1-z^{-1})}{Ts(1+z^{-1})}}$$

Hence, by taking $s$ tends to $z$, the equation 5.3 becomes.

$$= \frac{\left(\frac{Ts}{2C}+R\right) + z^{-1}\left(\frac{Ts}{2C}-R\right)}{1-z^{-1}}$$

(5.4)
where, $Ts$ is the sampling period of a discrete-time system. In our case this is equal to the time period of the input reference signal $h_{sync}$.

Suppose $\alpha$ and $\beta$ are two coefficients. Then the transfer function in $z$-domain of the digital filter will be

$$H(z) = \alpha + \beta \frac{1}{1-z^{-1}}$$

(5.5)

$$= \frac{(\alpha+\beta)-\alpha z^{-1}}{1-z^{-1}}$$

(5.6)

Where the values of $\alpha$ and $\beta$ are

$$\alpha = R - \frac{Ts}{2C}$$

(5.7)

$$\beta = \frac{Ts}{2C}$$

(5.8)

After considering $\alpha$ and $\beta$, the schematic of the digital LPF is shown in Figure 5.8. The clock signal of the digital LPF is equal to the input reference frequency i.e., $h_{sync}$.

![Digital LPF Schematic for ADPLL](image-url)

Figure 5.8 Implementation of the digital LPF for ADPLL [3]
Where, $\alpha$ represents the proportional part of the loop filter.

$\beta$ represents the integral part of the loop filter.

In the schematic of digital LPF, there is an accumulation between D-flip flop and adder as shown in Figure 5.8. Since, in digital LPF addition and multiplication are performed on bits, there will be a definite case of saturation during accumulation. To counter this, there is an extra box, which performed saturation.

### 5.4.1 Multiplier

In the design of digital LPF, there are two multipliers. The input is a stream of bits, which is the output from the time-to-digital converter. It will be multiply by a coefficients $\alpha$ and $\beta$ as shown in Figure 5.8.

For the selection of multiplier architecture, it is most important that the multiplier should support signed multiplication. This is because the DCO oscillating frequency increases or decreases according to the controlling bits provided by the digital LPF and the direction signal. When the direction signal is at logic high, hsync is leading from Fback signal. Therefore, in this case, DCO oscillation should be increased and when Fback signal is leading from hsync, the frequency of oscillation should be decreased [3].

#### 5.4.1.1 The Array Multiplier [4]

The architecture of an array multiplier is shown in Figure 5.9. For the N partial products $N \times M$ 2-bit AND gates is required where M is the size of the number. Hence, in this way most of the area of the multiplier is consumed by the adding of the N partial products which requires $(N – 1)$ M-bit adders. Here, one left shifting is performed by simply routing as shown in Figure 5.9. Therefore, no special algorithm or logic is required for shifting. Finally at the time of fabrication whole layout of array multiplier is in the form of rectangle, resulting in a very compact layout.
From Figure 5.9, it can be observed that the direct calculation for the propagation delay for this circuit is not an easy task because of the partial sum adders, which are implemented in the ripple carry fashion. For the best performance, critical path are required. The critical path of ripple carry structure circuit shown in Figure 5.9 can be written as

$$t_{\text{mult}} = [(M - 1) + (N - 2)t_{\text{carry}} + (N - 1)t_{\text{sum}} + t_{\text{AND}}] \quad (5.9)$$

where,

$t_{\text{mult}}$ is the execution/computation/delay of multiplier.

$t_{\text{carry}}$ is delay of carry propagation.

$t_{\text{sum}}$ is delay of results generated by an full adder.

$t_{\text{AND}}$ is delay introduced by AND gate.
The schematic shown in the Figure 5.9, is the carry-ripple multiplier for unsigned numbers. There is a slight modification for signed multiplier. When direction signal becomes high, multiplication of signed number is performed. The schematic for the signed number multiplier is shown Figure 5.10. Therefore, we used signed multiplier to achieve both signed and unsigned multiplication.

![Figure 5.10 Four-bit array multiplier for signed numbers](image)

### 5.5 Digital Controlled Oscillator (DCO)

DCO is the most important part of the ADPLL. DCO decides the frequency of the ADPLL. In our case, DCO oscillation frequency is determined by the eleven controlling bits. The architecture of the DCO comprises of two different cells, known as DCO delay cell A and the DCO delay cell B. These cells are connected in cascaded fashion. The number of cells depends upon the output frequency of the ADPLL as well as the DCO. The architecture of the DCO is shown in Figure 5.11, which consists of 5 stages. Controlling bits are provided directly from the digital LPF to the lower string of transistors, which are actually the chain of NMOS transistors. The complement logic of these controlling bits are applied to the upper string of PMOS transistors as shown in Figure 5.11 [3].

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5.5.1 DCO Delay Cell A

The delay cell A of DCO consists of a string of NMOS transistors as well as PMOS transistors. These strings of transistors are used to control the current through the DCO cell by keeping transistors on and off, according to the bit pattern provide by the digital LPF. The DCO delay cell A schematic is shown in Figure 5.12 [3].
As shown in Figure 5.12, there is a NAND gate between the rails of NMOS and PMOS transistors. In a NAND gate, if one input is fixed at logic high, then the output will be the complement logic of second input. This means NAND gate will act as an inverter (NOT gate). This DCO delay cell A is used only for the first stage. Therefore, one input of the NAND gate is used for enable signal and the other input of NAND gate has the feedback signal connected to it so that it become ring oscillator. The left most corner transistors in NMOS and in PMOS rails are used for biasing and are known as biasing transistors. Their inputs are biasn and biasp respectively. They are used to prevent the circuit from current starving and named as Mp and Mn [3].
5.5.2 DCO Delay Cell B

DCO delay cell B is almost identical of the DCO delay cell A. The only difference is in the logic between the rails of NMOS and PMOS transistors. In delay cell A, inverter i.e., NOT gate is implemented as shown in Figure 5.13 [3].

![DCO Delay Cell A Diagram](image)

Figure 5.13 DCO delay cell A for the DCO [3]

In both cells of DCO, the rail of NMOS and PMOS transistors are binary weighted. The size of the right corner most transistor, PMOS or NMOS is equal to $2^0 \times \frac{W}{L}$ then second has $2^1 \times \frac{W}{L}$ and it increases in this pattern such that nth transistor has a size of $2^{n-1} \times \frac{W}{L}$. The size of the capacitor $C_p$ is selected according to the output frequency of the DCO [3].

A divide-by-N divider is used in the loop of the ADPLL. The divider is designed using verilog-A. Divider divides the frequency by factor $N$, consequently the DCO oscillates at $N$ times higher the frequency than the input reference frequency i.e., hsync.
5.6 Stability Analysis

The approximate s-domain model of second order charge pump PLL is shown in Figure 5.14.

![Figure 5.14 The laplace-domain (s-domain) model of a second order charge-pump PLL [3]](image)

In case of all digital PLL, the approximate model will be

![Figure 5.15 The approximated laplace-domain (s-domain) model of a second-order ADPLL [3]](image)
Both models will exactly be the image of one another, if the following criteria hold [3].

\[
I_{CP} = \frac{T_{REF}}{\Delta_{TDC}} \quad (5.10)
\]

\[
K_{VCO} = K_{DCO} \quad (5.11)
\]

\[
Z(s) = H(s) \quad (5.12)
\]

where,

- \(I_{CP}\) is the charge-pump current in case of PLL.
- \(T_{REF}\) is the period of the input reference clock \(h_{sync}\).
- \(\Delta_{TDC}\) is the resolution of the TDC or delay of both inverters in TDC
- \(K_{DCO}\) is the gain DCO.

Therefore, the loop gain of the charge-pump PLL, is

\[
\text{Loop Gain } |_{s-domain} = L_G(s) \quad (5.13)
\]

\[
L_G(s) = \frac{I_{CP}}{2\pi} \frac{K_{VCO}}{s} \frac{1}{N} \frac{s + \omega_z}{s} \frac{1}{R} \quad (5.14)
\]

Where,

\[
\omega_z = \frac{1}{RC} \quad (5.15)
\]

One of the most important stability parameter phase margin (PM), can be found as,

\[
\text{PM} = \tan^{-1}\left(\frac{\omega_{UGBW}}{\omega_z}\right) \quad (5.16)
\]

In the equation 5.16, \(\omega_{UGBW}\) is the unity gain-bandwidth of the system which is normally \((1/10)\) or \((1/20)\) of the input reference frequency [3].

Hence, the value of loop filter components, \(R\) and \(C\) can be calculated as.

\[
R = \frac{2\pi N}{I_{CP}K_{VCO}} \frac{\omega_z^2}{\sqrt{\omega_z^2 + \omega_{UGBW}^2}} \quad (5.17)
\]
5.7 Simulation Results

The output range is from 10-300 MHz and is divided into three regions. For each region, simulation is carried out at its extreme values. Following are the results.

5.7.1 For hsync = 15.625 kHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input frequency</td>
<td>15.625 kHz</td>
</tr>
<tr>
<td>Division ratio</td>
<td>864</td>
</tr>
<tr>
<td>Output frequency</td>
<td>13.5 M</td>
</tr>
<tr>
<td>Width of PMOS transistors for DCO controlling bits ($W_p$)</td>
<td>135 n</td>
</tr>
<tr>
<td>Width of NMOS transistors for DCO controlling bits ($W_n$)</td>
<td>135 n</td>
</tr>
<tr>
<td>Length of PMOS and NMOS transistors $L_n$ &amp; $L_p$</td>
<td>60 n</td>
</tr>
<tr>
<td>Rise time of supply voltage (trise)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Fall time of supply voltage (tfall)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Frequency for the filter (xtal-filter)</td>
<td>15.625 kHz</td>
</tr>
<tr>
<td>Capacitor for the DCO (Cp)</td>
<td>60 fF</td>
</tr>
<tr>
<td>Width of transistors for DCO center logic</td>
<td>9.45 n</td>
</tr>
</tbody>
</table>

Table 5.3 Specification for the hsync = 15.625 kHZ
5.7.2 For hsync = 67.5 kHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input frequency</td>
<td>67.5 kHz</td>
</tr>
<tr>
<td>Division ratio</td>
<td>2200</td>
</tr>
<tr>
<td>Output frequency</td>
<td>148.5 MHz</td>
</tr>
<tr>
<td>Width of PMOS transistors for DCO controlling bits (W_p)</td>
<td>135 n</td>
</tr>
<tr>
<td>Width of NMOS transistors for DCO controlling bits (W_n)</td>
<td>135 n</td>
</tr>
<tr>
<td>Length of PMOS and NMOS transistors L_n &amp; L_p</td>
<td>60 n</td>
</tr>
<tr>
<td>Rise time of supply voltage (trise)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Fall time of supply voltage (tfall)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Frequency for the filter (xtal-filter)</td>
<td>67.5 kHz</td>
</tr>
<tr>
<td>Capacitor for the DCO (C_p)</td>
<td>60 fF</td>
</tr>
<tr>
<td>Width of transistors for DCO center logic</td>
<td>81 n</td>
</tr>
</tbody>
</table>

Table 5.4 Specification for the hsync = 67.5 kHz

5.7.3 For hsync = 107.184 kHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input frequency</td>
<td>107.184 kHz</td>
</tr>
<tr>
<td>Division ratio</td>
<td>2624</td>
</tr>
<tr>
<td>Output frequency</td>
<td>148.5 MHz</td>
</tr>
<tr>
<td>Width of PMOS transistors for DCO controlling bits (W_p)</td>
<td>135 n</td>
</tr>
<tr>
<td>Width of NMOS transistors for DCO controlling bits (W_n)</td>
<td>135 n</td>
</tr>
<tr>
<td>Length of PMOS and NMOS transistors (L_n &amp; L_p)</td>
<td>60 n</td>
</tr>
<tr>
<td>Rise time of supply voltage (trise)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Fall time of supply voltage (tfall)</td>
<td>1 psec</td>
</tr>
<tr>
<td>Frequency for the filter (xtal-filter)</td>
<td>107.184 kHz</td>
</tr>
<tr>
<td>Capacitor for the DCO (C_p)</td>
<td>60 fF</td>
</tr>
<tr>
<td>Width of transistors for DCO center logic</td>
<td>180 n</td>
</tr>
</tbody>
</table>

Table 5.5 Specification for the hsync = 107.184 kHz
Following are the simulations results for the input frequency (hsync) equal to the 67.5 kHz, multiplying with N equal to 2200 and producing an output frequency of 148.5 MHz.

Figure 5.16 Frequency v/s time plot of output frequency of the ADPLL after DCO

The frequency v/s time plot shown in Figure 5.16, is the output of the ADPLL with input frequency (hsync) equal to 67.5 kHz with a division ratio 2200. At the start, the DCO increases or decreases the oscillation frequency to reach the desired frequency. Finally, with some small variations the output frequency reaches the desired level of frequency i.e., 148.5 MHz.
The frequency v/s time plot of feedback signal after the frequency divider is shown in Figure 5.17. The feedback signal is the output of the divider. The frequency divider divides the output frequency of the DCO (148.5 MHz) with a division ratio of 2200 and generates a feedback signal of frequency equal to 67.5 kHz. This feedback signal is the other input of PFD as discussed in chapter 5. When ADPLL is in stable condition, the output frequency of the divider equals to the hsync frequency as shown in Figure 5.17.
Figure 5.18, shows the jitter analysis of the ADPLL at the highest frequency, according to the specification. The jitter analysis is performed by considering all possible noises in a circuit. The width of the falling edge as shown in Figure 5.18, are the long term jitter values of the ADPLL.
5.8 References


Chapter 6

6  Conclusion and Future works

This thesis presented a low power all digital phase locked loop (ADPLL) for the video applications. The ADPLL has wide range of operating input frequency from 10 kHz to 150 kHz. The output range of ADPLL is from 10 MHz to 300 MHz can be used for a variety of applications. The circuit of ADPLL is implemented in a CMOS 65-nm technology using a supply voltage of 1 V.

By working on such a low supply voltage, it is marked the inadequacy of the CMOS process. The signals in a circuit are more sensitive to noise. As noise is one of the most critical harms in ADPLL. Secondly, there were some technical issues with 65-nm technology. Therefore, the circuit requires some more refinements and reflections. For moving towards next level for this design, a designer has following potential ways:

6.1 Circuit optimization

The circuit needs more optimization. The width of the transistors in a DCO can be selected more efficient manner so that amount of current in a controlling bits transistors are in more accurate amount. The size of the capacitor in a DCO and the delay of buffer in a TDC can optimized for better and smooth output of the ADPLL.

6.2 Single DCO

Due to wide range of output frequency, we divide the output range into three extreme boundaries. For each extreme value of the output frequency there is a separate DCO. There was an idea behind three DCOs, that according to the desired output frequency only one DCO should be selected. Meanwhile, remaining two DCOs will disable. But wide range at output can be achieved with a single DCO by a little bit sacrificing with a locking time.

6.3 Noise Analysis

There is a room for the noise analysis of the circuit. As the jitter value is slightly higher than the value of jitter given in specification. Therefore, requires more consideration and techniques for reducing substrate and supply noise in a circuit. Sigma delta modulator based divider can be a better option than presented divider.
6.4 Layout

Finally, a chip can be assembled after designing a proper layout of the ADPLL. While designing a layout there should be special concerns about the overall size of chip, proper placing of input and the output signals and clocking etc.