

Linköping University Post Print

On Minimization of Peak Power for Scan Circuit during Test

Jaynarayan T. Tudu, Erik Larsson, Virendra Singh and Vishwani Agrawal

N.B.: When citing this work, cite the original article.

©2010 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Jaynarayan T. Tudu, Erik Larsson, Virendra Singh and Vishwani Agrawal, On Minimization of Peak Power for Scan Circuit during Test, 2009, European Test Symposium (ETS 2009), Sevilla, Spain, May 25-29, 2009, 25-30.

Postprint available at: Linköping University Electronic Press

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-59591>

On Minimization of Peak Power for Scan Circuit during Test

Jaynarayan T. Tudu*, Erik Larsson†, Virendra Singh*, and Vishwani D. Agrawal‡

* Indian Institute of Science, Bangalore 560012, India

Email: jayttudu@csa.iisc.ernet.in, viren@serc.iisc.ernet.in

† Linköping University, SE-581 83 Linköping, Sweden

Email: erila@ida.liu.se

‡ Auburn University, Auburn, AL 36849, USA

Email: vagrawal@eng.auburn.edu.

Abstract

Scan circuit generally causes excessive switching activity compared to normal circuit operation. The higher switching activity in turn causes higher peak power supply current which results into supply voltage droop and eventually yield loss. This paper proposes an efficient methodology for test vector re-ordering to achieve minimum peak power supported by the given test vector set. The proposed methodology also minimizes average power under the minimum peak power constraint. A methodology to further reduce the peak power, below the minimum supported peak power, by inclusion of minimum additional vectors is also discussed. The paper defines the lower bound on peak power for a given test set. The results on several benchmarks shows that it can reduce peak power by up to 27%.¹

1. Introduction

Power consumption during testing of scan circuit is an important issue to address for today's very complex sequential circuits. It becomes especially important when chips are designed with small feature size and higher frequency; hence, at-speed test becomes necessary. Excessive average power results into burn out of chip whereas excessive peak power results into power droop problem which can falsely classify a good chip as a faulty chip. Average power can be reduced by reducing clock frequency. Reduction of peak power during test becomes very important for two reasons: 1. Higher peak power causes yield loss due to power droop and cross talk, 2. If the scan circuit is a module in an SoC then multiple module can be scheduled together to minimize test time. Our methodology shows that the test vector order under minimum achievable peak power, determined by our approach, would also smooth out the power profile. The smooth power profile can facilitate us to use box model [11] for test scheduling in an SoC. Otherwise, a more complex

cycle accurate model [12], [13] must be used for SoC test scheduling [14].

The problem of test power reduction is an active area of research for quite sometime. Most of the solutions [3], [8], [11] are aimed at average power reduction. However, they have also achieved small reduction in peak power as a by-product. Test vector reordering [8] is used to achieve average power reduction. Bonhomme et al. [10] used scan chain reordering technique to minimize the total number of transitions to reduce average power. The scan chain reordering leads to extra interconnect area and power dissipation. In [4] and [9], logic is added to hold the output of the scan cells at a constant value during scan shifting thereby reducing power dissipation. This approach greatly reduces average power, and will avoid peak power problems during scan shifting but these approaches lead to area overhead. Moreover, this approach degrades circuit performance because it adds extra logic in the functional paths. Another set of solutions which have been proposed in the literature are the low activity pattern generation using ATPG. Corno et al. [5] proposed a test pattern generation technique which modifies test sequence for sequential non-scan testing for reducing peak power. The approaches proposed by Shankarlingam and Touba [6] and Wen et al. [7] assign don't care bits of the deterministic test cubes used during test in such a way that it can reduce the peak power. Badereddine et al. [2] proposed a solution based on a power-aware assignment of don't care bits in deterministic test patterns. This solution proposes that X values of generated pattern is filled before doing the test pattern minimization, thereby the algorithm may put limits on the test pattern compaction and it may increase test time. This paper proposes methodology to minimize peak power by test vector ordering. We also provide the bound on the achievable minimum peak power for a given test set.

The rest of the paper is organized as follows. Section 2 presents the problem formulation where we formulated three problems and also describe the lower bound on peak power. Section 3 describes algorithms for all three problems. Section 4 presents the experimental results. The paper concludes Section 5.

1. This research is partly supported by The Swedish Foundation for International Cooperation in Research and Higher Education (STINT) through Institutional Grant for Younger Researchers for collaboration with Indian Institute of Science (IISc), Bangalore, India.

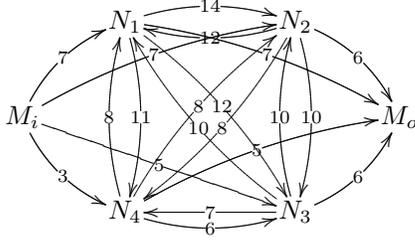


Figure 1. A weighted digraph for patterns in Example 1

2. Problem Formulation

Problem Statement: Determination of the minimum achievable peak power during test for a given test set and find out a test vector sequence which can support the minimum achievable peak power.

The proposed work formulates a graph theoretic problem by mapping test vector sequence to a complete weighted directed graph. The complete weighted directed graph D_c can be constructed in the following way: Each test pattern T_i corresponds to the node N_i of the digraph. There would be a directed edge, E_{ij} , from node N_i to node N_j if pattern T_i and T_j can be applied consecutively. The weight of the edge E_{ij} , EW_{ij} , is the maximum of number of transitions occurs in scan chain per clock cycle for complete scan operation including load/unload, and launch and capture cycles while applying test pattern T_i followed by T_j . Since any pattern can follow any other pattern, the constructed graph would be a complete graph. Example 1 helps understanding the graph construction. We use Example 1 as a running example in this paper.

Example 1: Let length of scan chain be 15 and test set size be 5. Test patterns and responses are listed below:

T_1 : 111111101010111	R_1 : 111010101111000
T_2 : 111111111010101	R_2 : 101010111111111
T_3 : 111111111110101	R_3 : 101011111111001
T_4 : 111111111111101	R_4 : 110111111110110

Figure 1 shows the weighted diagram for this test set. We introduce a dummy node M_i to scan in the first vector assuming scan chain is initially in reset state and M_o to scan out the last response.

We have formulated three problems to obtain the minimum peak power for a given test vector set and the order of test vectors. The first problem gives test vector sequence without time penalty and the other two problems give the test vector sequences with marginal increase in time. At the end we'll define the lower bound on the minimum achievable peak power.

2.1. Formulation of Problem-1

Definition 1. *path-weight* is defined as the maximum of weight of each edge in the path in a digraph.

Problem Statement: Given a complete weighted directed graph D_c , find out a Hamiltonian path which has minimum path-weight.

Consider three different Hamiltonian paths, Path1, Path2 and Path3 for the digraph shown in Figure 1:

$$\begin{aligned}
 &M_i \xrightarrow{7} N_1 \xrightarrow{12} N_3 \xrightarrow{7} N_4 \xrightarrow{8} N_2 \xrightarrow{6} M_o \\
 &M_i \xrightarrow{7} N_2 \xrightarrow{8} N_4 \xrightarrow{6} N_3 \xrightarrow{10} N_1 \xrightarrow{7} M_o \\
 &M_i \xrightarrow{5} N_3 \xrightarrow{10} N_1 \xrightarrow{14} N_2 \xrightarrow{8} N_4 \xrightarrow{5} M_o
 \end{aligned}$$

Let PW_1 , PW_2 and PW_3 be the corresponding path-weights. Then, we have $PW_1 = \max\{(M_i, N_1), (N_1, N_3), (N_3, N_4), (N_4, N_2), (N_2, M_o)\} = 12$. Similarly, $PW_2 = 10$ and $PW_3 = 14$. Thus,

$$\text{Minimum Peak Power} = \min(PW_1, PW_2, PW_3) = 10$$

To obtain a solution, we have transformed the problem to an unweighted directed graph problem. The transformation of a weighted digraph for a given threshold peak power value, P_{th} to an unweighted digraph is as follows:

- Every node in weighted graph has a corresponding node in unweighted graph.
- Remove all the edges whose weight is greater than P_{th} .
- Replace all other edges $EW_{ij} \leq P_{th}$, with unweighted edges.

The problem can be restated as: For a given complete weighted directed graph D_c , find out the minimum peak power P_{th}^1 , such that its corresponding unweighted graph, D_u has at least one Hamiltonian path.

The above problem formulation obtains minimum possible peak power P_{th}^1 . There may be more than one possible Hamiltonian paths in the unweighted graph. Although minimization of peak power minimizes average power, we can further optimize for given peak power P_{th}^1 by choosing a path that gives minimum average power. Note that we will visit every node only once and will not increase the test time.

2.2. Formulation of Problem-2

A directed graph, D , which does not contain any Hamiltonian path may have a possible walk [1] that visits each and every node at least once. This is illustrated by the following scenario shown in Figure 2.

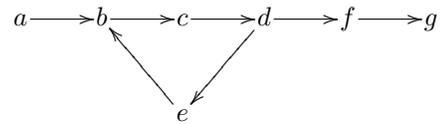


Figure 2. An unweighted digraph

It can be observed from Figure 2 that Hamiltonian path does not exist in the graph but there is a walk from node

a to node g which revisit node e, b, c and d and visit each node at least once.

Definition 2. We define **walk-weight** as the maximum edge-weight in the walk in a digraph.

Problem Statement: For a given complete weighted digraph D_c , find a walk which visits each and every nodes at least once with minimum **walk-weight**.

The problem can be redefined for unweighted graph as follows: For a given weighted directed graph D , find out the minimum peak power value, P_{th}^2 , such that its corresponding unweighted graph has at least one walk.

The possible walk will revisit a few nodes; hence, it will increase the test time. The increase in test time is proportional to the number of revisited nodes.

2.3. Formulation of Problem-3

Problem-1 obtains Hamiltonian path having minimum peak power P_{th}^1 and Problem-2 finds a walk having minimum peak power P_{th}^2 (less than P_{th}^1) at the cost of revisiting some nodes. If we further reduce P_{th} (minimum achievable peak power), the corresponding unweighted graph, D_u , will not have a walk to apply complete test set. Further reduction would result into disjoint paths. These paths can be joined to form a single walk by introduction of some extra low activity nodes (currently we consider only all 0's patterns and all 1's patterns whose corresponding nodes are N_{a0} and N_{a1}) to D_u . We refer, this walk with these additional nodes as *extended-walk* and the graph D_u with these additional nodes as *extended graph*. Note that we only scan in these patterns and will not apply so that scan out would have same value. The above stated scenario is illustrated in Figure 3.

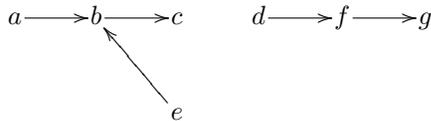


Figure 3. Disconnected unweighted digraph

In Figure 3, the possible disjoint paths could be $a \longrightarrow b \longrightarrow c$, $d \longrightarrow f \longrightarrow g$, and e . After interconnecting these paths the resultant will be as follows: $a \longrightarrow b \longrightarrow c \longrightarrow x \longrightarrow d \longrightarrow f \longrightarrow g \longrightarrow y \longrightarrow e$, where x and y are new nodes. Therefore, the problem can be defined in following way.

Problem statement: For a given complete weighted directed graph D_c , find the minimum peak power value, P_{th}^3 such that its corresponding unweighted *extended graph* has at least one *extended-walk*.

2.4. Lower Bound on Minimum Peak Power

Problem-3 can achieve the minimum possible peak power by inserting additional nodes N_{a0} (all 0's) and N_{a1} (all 1's).

Theorem 1. The lower bound on minimum achievable peak power for a test set is

$$\max_{\forall_i} [\max\{\min(EW_{a0i}, EW_{a1i}), \min(EW_{ia0}, EW_{ia1})\}] \quad (1)$$

Proof: In order to achieve the minimum peak power the graph should be augmented by additional nodes N_{a0} and N_{a1} to construct an extended graph. In extended graph, $EW_{ij} \geq \max\{\min(EW_{ia0}, EW_{ia1}), \min(EW_{a0j}, EW_{a1j})\}$. Therefore, it is guaranteed that visiting node j directly from node i would be expensive or equal to visiting through either node N_{a0} or N_{a1} . In worst case, we may always need to traverse through extended nodes while going from node i to node j . The minimum power to traverse node j from node i would be $\max\{\min(EW_{ia0}, EW_{ia1}), \min(EW_{a0j}, EW_{a1j})\}$. Hence, the minimum achievable peak power for a given test set would be the maximum of minimum peak power computed for all nodes, that is $\max_{\forall_i} [\max\{\min(EW_{a0i}, EW_{a1i}), \min(EW_{ia0}, EW_{ia1})\}]$.

Lemma 1. Let there be a test set of n vectors and scan chain length be l . The worst case test time to achieve the lower bound is $(3n - 1) \times l + n - 1$.

Proof: According to Theorem 1, we can always achieve minimum power by traversing through N_{a0} or N_{a1} . Hence, it adds one extra node in the traversal from node i to node j . However, it can be observed that to achieve minimum power, node j can be reached from node N_{a1} or N_{a0} , and N_{a0} or N_{a1} can be reached from node i . Therefore, in the worst case we need to take the following path to reach node j from node i : N_i to N_{a0} to N_{a1} to N_j . We walk through additional $(2n - 1)$ nodes in the worst case. Therefore, the worst case time would be: $(3n - 1) \times l + n - 1$.

Corollary 1. The minimum achievable peak power under maximum test time $(2n - 1) \times l + (n - 1)$ for a test set is $\max_{\forall_i} \{\max(EW_{a0i}, EW_{a1i}, EW_{ia0}, EW_{ia1})\}$.

Proof: A walk from node i to node j under power constraint $\max(EW_{a0i}, EW_{a1i}, EW_{ia0}, EW_{ia1})$ can be made by the following traversal: V_i to V_{a0} to V_j , or V_i to V_{a1} to V_j . Hence, the worst case test time under above stated power constraint would be $(2n - 1) \times l + n - 1$.

Note that the costs of walks N_{a0} to N_{a1} to N_j , and N_i to N_{a0} to N_{a1} to N_j differ by at the most one transition as $\max\{\min(EW_{a0i}, EW_{a1i}), \min(EW_{ia0}, EW_{ia1})\} - \max(EW_{a0i}, EW_{a1i}, EW_{ia0}, EW_{ia1}) = 1$. Therefore, we can infer from Corollary 1 that we can reduce the test time significantly at the cost of one additional transition in the worst case.

3. Algorithms

3.1. Algorithm-1 for Problem-1

The following algorithm computes the Hamiltonian path and minimum peak power value P_{th}^1 .

```

AlgoMinHam(Input:  $D_c$ , Output: HamPath,  $P_{th}^1$ )
1 Let  $A$  be nondecreasing sorted array of edge-weight;
2 index = SelectInitialIndex;
3 while(TRUE)
4    $UpLimit = A(index)$ ;
5   RemoveEdge( $D_c$ ,  $UpLimit$ ,  $D_u$ );
6   found = SearchHam( $D_u$ , HamPath) ;
7   if( found == TRUE )
8     then
9        $P_{min}^1 = UpLimit$ ;
10      return HamPath and  $P_{th}^1$ ;
11    else
12      index = SelectNextIndex;
13      CONTINUE ;
EndofAlgo

```

The procedure *RemoveEdge* removes all the edges with edge-weight greater than $UpLimit$. *SearchHam* finds the Hamiltonian path if one exists. The following example illustrates this.

Example 2 : Let D_c be the digraph from Figure 1. The Algorithm-1 will return the following Hamiltonian path:
 $M_i \xrightarrow{3} N_4 \xrightarrow{8} N_2 \xrightarrow{10} N_3 \xrightarrow{10} N_1 \xrightarrow{7} M_o$
and minimum peak power value $P_{th}^1 = 10$.

3.2. Algorithm-2 for Problem-2

The following algorithm finds out a minimum-weight walk if exist which visits every nodes of given digraph at least once.

```

AlgoMinWalk(Input:  $D_c$ , Output: Walk,  $P_{min}^2$ )
1 Let  $A$  be nondecreasing sorted array of edge-weight;
2 index = SelectInitialIndex;
3 while(TRUE)
4    $UpLimit = A(index)$ ;
5   RemoveEdge( $D_c$ ,  $UpLimit$ ,  $D_u$ );
6   Success = AlgoConDag( $D_u$ , DAG);
7   if(Success == TRUE)
8     AlgoConIpath(DAG, Ipath);
9     AlgoConWalk(Ipath, Walk);
10     $P_{min}^2 = UpLimit$ ;
11    return Walk and  $P_{th}^2$ ;
12  else
13    index = SelectNextIndex ;
14    CONTINUE ;
EndofAlgo.

```

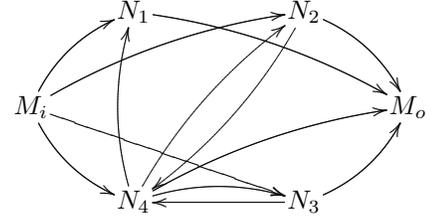


Figure 4. Unweighted digraph with edge-weights ≤ 8

The procedure *AlgoConDag* constructs a directed acyclic graph (DAG) from given digraph D_u by forming each cycle into corresponding *supernode* [15] if it can be constructed. *AlgoConIpath* constructs an intermediate path *Ipath* from a given DAG by using the concept of acyclic ordering [1]. Finally, *AlgoConWalk* procedure constructs a walk from a given *Ipath* by unrolling *supernodes* into cycles and connecting the nodes. The complexity of the algorithm would be $O(nodes^3 + edges^2)$, which is polynomial. Following example illustrates this.

Example 3: Let D_c be complete digraph from Figure 1. Then unweighted digraph D_u after RemoveEdge() is shown in Figure 4. After obtaining this digraph, resultant Walk and P_{th}^2 are obtained. The Walk is:
 $M_i \xrightarrow{7} N_2 \xrightarrow{8} N_4 \xrightarrow{6} N_3 \xrightarrow{7} N_4 \xrightarrow{8} N_1 \xrightarrow{7} M_o$
and $P_{th}^2 = 8$ which is $< P_{th}^1$.

3.3. Algorithm-3 for Problem-3

This algorithm find a minimum-weight, $P_{th}^3, walk$ in an extended graph.

```

AlgoMinEWalk(Input:  $D_c$  Output: EWalk,  $P_{th}^3$ )
1 Let  $A$  be nondecreasing sorted array of edge weight;
2 index=SelectInitialIndex;
3 while(TRUE)
4    $UpLimit = A(index)$ ;
5   RemoveEdge( $D_c$ ,  $UpLimit$ ,  $D_u$ );
6   FindDisjointPath( $D_u$ , C);
7   JoinPath(C, EWalk);
8   TempWalk = EWalk;
9    $P_{th}^3 = UpLimit$ ;
10  if(LowerBound <  $P_{th}^3$ )
11    index=SelectNextIndex;
12    CONTINUE;
13  else
14    return TempWalk and  $P_{th}^3$ ;
EndofAlgo

```

Procedure *FindDisjointPath* finds the directed path cover. Then procedure *JoinPath* introduces new nodes to interconnect paths. Here we are using all 0's N_{a0} or all 1's N_{a1} nodes to connect. The use node N_{a0} or N_{a1} depends upon the

Table 2. Results for Algorithm-2

Bench mark	#test pattern	scan length	Peaktran GivenOrder	Peaktran Algo-2	Improve ment%	improve% overAlgo-1	testtime overhead	Avgtran GivenOrd	Avgtran Algo-2	Improve ment%
s838	75	32	16	12	25.00	0.00	0.00	4.61	4.59	0.43
s838	75	32	16	11	31.25	08.33 ²	1.33	4.61	4.57	0.80
b19	628	215	171	162	5.26	0.00	0.00	98.12	97.96	0.17
b22	622	215	172	158	6.97	0.00	0.00	98.23	98.07	0.16

Table 3. Results for Algorithm-3

Bench mark	#test pattern	scan length	Peaktran GivenOrder	Peaktran Algo-3	Improve ment%	improve% overAlgo-2	testtime overhead	Avgtran GivenOrd	Avgtran Algo-3	Improve ment%
b19	628	215	171	161	5.84	0.61	0.63	98.12	97.50	0.63
b22	622	215	172	157	8.72	0.63	0.64	98.23	97.61	0.63

achieve minimum peak power without increase in test time. We also present two approaches that can further reduce the peak power at a cost of increase in test time. Finally, we have presented a lower bound on the minimum achievable peak power for a given test set. The results indicate that we can achieve up to 27% peak power reduction without increase in test time. We can also reduce average power by up to 4.96%. The proposed algorithms Algo2 and Algo-3 are polynomial complexity algorithms, hence the methodology is scalable. In the future, Algo-1 can be implemented as an approximation algorithm to reduce the time complexity. Note that the proposed method can be applied with the existing X-fill based approaches because it uses fully specified vectors. Hence, we can achieve more power saving in combination with the existing techniques. It could also be more effective if integrated with ATPG.

6. Acknowledgment

The authors thank to Prof. Michiko Inoue, NAIST, Japan and Prof. Tim Cheng, UCSB, USA for their valuable suggestions. The authors also thanks to Prof. Sunil Chandran, IISc, Bangalore for helping in understanding graph theoretic concepts, and Prof. Seiji Kajihara, KIT, Japan for providing test pattern file for d695.

References

- [1] J. Bang-Jensen and G. Gutin, *Digraphs Theory, Algorithms and Applications*, Springer-Verlag, 2006.
- [2] N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel, and H.-J. Wunderlich, "Minimizing Peak Power Consumption during Scan Testing: Test Pattern Modification with X Filling Heuristics," *Proc. Int'l Conf. Design and Test of Integrated System in Nanoscale Tech.*, pp. 359–364, 2006.
- [3] R. Sankaralingam, R. Oruganti, and N. A. Toubia, "Static Compaction Technique to Control Scan Vector Power Dissipation," *Proc. of VLSI Test Symposium*, pp. 35–40, 2000.
- [4] A. Hertwig and H.-J. Wunderlich, "Low Power Serial Built-In Self-Test," *Proc. European Test Workshop*, pp. 49–53, 1998.
- [5] F. Corno, M. Rebaudengo, M. Sonza Reorda, and M. Violante, "On Reducing the Peak Power Consumption of Test Sequences," *Proc. European Conf. Circuit Theory and Design*, pp. 247–250, 1999.
- [6] R. Sankaralingam and N. A. Toubia, "Controlling Peak Power during Scan Testing," *Proc. IEEE VLSI Test Symp.*, pp. 153–159, 2002.
- [7] X. Wen, Y. Yamashita, S. Kajihara, L.-T. Wang, K. K. Saluja, and K. Kinoshita, "On Low-Capture-Power Test Generation for Scan Testing," *Proc. IEEE VLSI Test Symposium*, pp. 265–270, 2005.
- [8] V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. M. Reddy, "Techniques for Minimizing Power Dissipation in Scan and Combinational Circuits During Test Application," *IEEE Trans. Comp.-Aided Design*, Vol. 17, No. 12, pp. 1325–1333, Dec. 1998.
- [9] S. Gerstendörfer, and H.-J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST," *Proc. Intl. Test Conf.*, pp. 77–84, 1999.
- [10] Y. Bonhomme, P. Girard, C. Landrault, and S. Pravossoudovitch, "Power Driven Chaining of Flip-Flops in Scan Architectures," *Proc. Intl. Test Conf.*, pp. 796–802, 2002.
- [11] R. M. Chou, K. K. Saluja, and V. D. Agrawal, "Scheduling Test for VLSI Systems under Power Under Power Constraints," *IEEE Trans. VLSI Systems*, Vol. 5, No. 2, pp. 175–185, June 1997.
- [12] S. Samii, M. Selkälä, E. Larsson, K. Chakrabarty, and Z. Peng "Cycle-Accurate Test Power Modeling and Its Application to SoC Test Architecture Design and Scheduling," *IEEE Trans. Comp.-Aided Design*, Vol. 27, No. 5, pp. 973–977, May 2008.
- [13] S. Samii, E. Larsson, K. Chakrabarty, and Z. Peng "Cycle-Accurate Test Power Modeling and its Application to SoC Test Scheduling," *Proc. Intl. Test Conf.* pp. 1–10, 2006.
- [14] J. Pouget, E. Larsson, and Z. Peng "Multiple-constraint driven system-on-chip test time optimization," *Journal Electronic Testing: Theory and Application*, Vol. 21, No. 6, pp. 599–611, 2005.
- [15] H. Gabow, Z. Galil and T. Spencer, "Efficient Implementation of Graph Algorithms Using Contraction," *Proc. 25th Annual Symp. Foundation of Computer Science*, pp. 347–357, 1984.

2. when Algo-2 is used as approximation of Algo-1 - as in previous row