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Advances in SiC growth using chloride-based CVD

Stefano Leone

Linköping University
INSTITUTE OF TECHNOLOGY

Semiconductor Materials Division
Department of Physics, Chemistry and Biology
Linköpings Universitet
SE-581 83 Linköping - Sweden

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Cover: Microscope image of an epitaxial layer grown on a 4H-SiC on-axis substrate, where growth occurs by islands. On the back cover a high magnification atomic force microscopy image of the center of an island is shown.

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If I speak with the languages of men and of angels, but don't have love, I have become a sounding brass, or a clanging cymbal.
If I have the gift of prophecy, and know all mysteries and all knowledge; and if I have all faith, so as to remove mountains, but don't have love, I am nothing.

Paul's First Letter to the Corinthians 13,1-2
The Holy Bible

To my mother and my father

Table of contents

Abstract

Silicon Carbide (SiC) is a wide band-gap semiconductor. Similar to silicon it can be used to make electronic devices which can be employed in several applications. SiC has some unique features, such as wide band-gap, high hardness, chemical inertness, and capability to withstand high temperatures. Its high breakdown electric field, high saturated drift velocity and high thermal conductivity are some of the most important characteristics to understand why SiC has superior electrical properties compared to silicon, and make it very attractive for power devices especially at high voltages and high frequency. The gain in reduced device sizes, reduced cooling requirements, and especially in improved energy efficiency for AC/DC conversion are a very important reasons to keep working in improving the material quality. Yet several issues still limit its full employment in all its potential applications, and many more steps have thus to be done for its complete success.

The core of an electric device is the epitaxial layer grown on a substrate by chemical vapor deposition (CVD). Gases containing silicon and carbon atoms, such as silane and ethylene, are often used to grow SiC, but limits in high growth rate are given by silicon cluster formation in the gas phase which is detrimental for the epitaxial layer quality. High growth rates are needed to deposit thick layers (> 100 μm) which are required for high power devices. Chloride-based CVD, which is usually employed in the silicon epitaxial growth industry, is based on the presence of chlorinated species in the gas mixture which prevent the formation of silicon clusters, therefore resulting in very high growth rates. This chloride-based CVD process was first started to be investigated a few years ago and then only at typical growth conditions, without exploring all its full potential, such as its performance at low or high temperature growth. In addition important parameters affecting the epitaxial layer quality in terms of defect formation and electrical characteristics are the substrate orientation and its off-cut angle. Standard processes are run on substrates having an 8° off-cut angle towards a specific crystallographic direction. On lower off-cut angles, such as 4° or almost 0° (also called on-axis) which would be more economical and could resolve problems related to bipolar degradation, many typical issues should be solved or at least minimized. For 4° off-cut angle the main problem is the step-bunching resulting in high roughness of the epi surface whereas for nominally on-axis the formation of 3C inclusions is the main problem.

In this thesis we discuss and present results on the use of the chloride-based CVD process in a hot-wall reactor to further explore most of the above mentioned topics. On-axis substrates are used to grow homopolytypic epitaxial

layers; detailed experiments on the gas phase composition adopting high contents of chlorine made it possible (**Paper 1**). Optimization of the on-axis surface preparation prior to the growth in combination with a correct choice of chlorinated precursors and growth conditions were required to reach a growth rate of 100 μm/h of 100% 4H polytype (**Paper 2**). Substrates with a 4° off-cut angle could be grown free from step-bunching, one of the most common morphological issue and usually detrimental for devices. Both the standard and chlorinated-process were successfully used, but at different growth rates (**Paper 3**). Also for this off-cut substrate a specific surface preparation and selected growth parameters made the growth possible at rates exceeding 100 μm/h (**Paper 4**). The benefit of the chlorinated chemistry was tested under unusual growth conditions, such as under a concentrated gas mixture (*i.e.* at very low carrier gas flow) tested on different off-cut substrates (**Paper 5**). A great advantage of chloride-based chemistry is the feasibility of growing at very low temperatures (1300 to 1400 °C compared to the 1600 °C standard temperature). At such low temperatures 4H-SiC epitaxial layers could be grown on 8° off-axis substrates (**Paper 6**), while high quality heteroepitaxial 3C-SiC layers were grown on on-axis 6H-SiC substrates (**Paper 7**). Finally, the very high growth rates achieved by the chloride-based CVD were applied in a vertical hot-wall reactor configuration, demonstrating the ability to grow very thick SiC layers at higher rates and lower temperatures than what is typically used for bulk growth (**Paper 8**). This work demonstrated that a new bulk growth process could be developed based on this approach.

Sammanfattning

Kiselkarbid (SiC) är en halvledare med ett stort bandgap och precis som den mycket vanliga halvledaren kisel kan SiC användas till elektroniska komponenter för många olika tillämpningar. SiC har unika materialegenskaper så som dess stora bandgap, dess höga hårdhet och motståndskraft både mot kemiskt aggressiva miljöer och höga temperaturer. Det som framförallt gör SiC så mycket bättre än kisel är främst den höga genombrottsfältstyrkan som gör att SiC klarar höga spänningar vilket är särskilt intressant för kraftkomponenter, för användning vid höga spänningar och höga frekvenser. Med elektroniska komponenter av SiC kan man, jämfört med samma komponenter av kisel, minska komponenternas storlek och kylbehov, men den huvudsakliga vinsten är en högre energieffektivitet vid AC/DC-omvandling. De minskade energiförlusterna är ett mycket starkt argument för att fortsätta att förbättra materialkvalitén på SiC. Det är materialrelaterade problem som idag håller tillbaka SiC-teknologin och ett antal problem måste lösas för att SiC ska få sitt stora genombrott.

Kärnan i en elektronisk komponent är det epitaxiella skikt som har växts ovanpå ett substrat. Ordet epitaxi kommer från grekiskans epi, som betyder ovanpå, och taxis, som betyder i ordning, så ett epitaxiellt skikt har alltså odlats på ett substrat och kopierat substratets kristallstruktur. Den vanligaste tekniken för att odla epitaxiella skikt i halvledarindustrin kallas på engelska chemical vapor deposition. Någon bra svensk översättning finns inte men tekniken innebär att man deponerar ett tunt skikt via kemiska reaktioner mellan gaser. Tekniken förkortas generallt för CVD från dess engelska namn. För att odla ett epitaxiellt skikt av SiC använder man gaser med kisel och kol, så som silan (SiH_4) och eten (C_2H_4), som späds ut kraftigt i vätgas. För att öka tillväxthastigheten i processen måste man öka mängden silan och eten i gasblandningen. Ett problem är dock att vid höga koncentrationer av kisel bildas kiseldroppar som regnar ner på substratytan och förstör det epitaxiella skiktet. Detta faktum gör att man inte kan odla epitaxiella skikt av SiC snabbare än ca 5-10 μm i timmen. För många kraftkomponenter krävs epitaxiella skikt med en tjocklek på 100 μm, eller mer och för att kunna odla sådana skikt på rimlig tid används kloridbaserad CVD. Kloridbaserad CVD är idag standard i kiselindustrin och bygger på närvaron av klorföreningar i gasblandningen. Eftersom klor binder starkare till kisel än vad kisel gör, hindrar närvaron av klor bildningen av kiseldroppar och man kan öka koncentrationen av kisel i gasblandningen och därmed öka tillväxthastigheten betydligt. Kloridbaserad CVD för kiselkarbid började på allvar undersökas för snart tio år sedan och då var fokus främst på redan välkända tillväxtförhållanden,

men den fulla potentialen hos kloridbaserad CVD, så som dess effekt på låg- eller högtemperatur tillväxt har ännu inte studerats. Inte heller har grundliga undersökningar gjorts av vad det är i processen som har betydelse för det epitaxiella skiktets elektriska egenskaper eller för bildandet av olika defekter under tillväxten.

När man kapar upp en kiselkarbidkristall i tunna skivor för att kunna odla epitaxiella skikt på dem, kapar man ofta kristallen lite snett i förhållande till hur atomplanen ligger i den. Detta gör att man får en kristallyta som ser ut lite som en trappa på atomär nivå. Detta är bra eftersom atomer som ska bygga upp det epitaxiella skiktet gärna binder till ytan vid ett sådant trappsteg eftersom de där kan binda till flera atomer samtidigt. Substrat som har kapats snett på det viset kallas off-axis substrat och för 4H-polytypen av SiC kapar man vanligen substraten 8 eller 4° snett. Substrat som kapats helt parallellt med kristallplanen kallas on-axis substrat, dessa är generellt sett svåra att odla bra epitaxiella skikt på, men man får inga spillbitar när man kapar kristallen och vissa kristalldefekter i substratet tränger inte igenom till episkiktet vilket ger bättre livslängd för de elektroniska komponenterna.

För att kunna odla på on-axis substrat gjordes detaljerade undersökningar av olika gasblandningar för processen och en hög klorhalt i gasblandningen möjliggjorde en process med hög tillväxthastighet på on-axis substrat (Artikel 1). Ytterligare optimering av både gaskemin och etsning av substratytan innan tillväxt gjorde att tillväxthastigheter på 100 μm i timmen kunde användas (Artikel 2). För substrat med 4° off-axis-vinkel utvecklades en process för odling av epitaxiella skikt där vanliga kristalldefekter, som är förödande för en elektrisk komponent, eliminerades och tack vare den kloridbaserade kemin kunde skikten odlas med relativt hög hastighet (Artikel 3). Även denna process utvecklades så att tillväxthastigheten överskred 100 μm i timmen (Artikel 4). Den kloridbaserade processen testades även under mera ovanliga tillväxtförhållanden, så som under väldigt lågt vätgasflöde, alltså väldigt hög koncentration av både kisel och kol i gasblandningen (Artikel 5). Den kloridbaserade kemin möjliggjorde även tillväxt vid låga temperaturer, 1300-1400 °C i stället för 1600 °C vilket är av stort intresse för vissa applikationer. Epitaxiella skikt hög kvalité av både hexagonal 4H-SiC (Artikel 6) och kubisk 3C-SiC (Artikel 7) odlades vid låga temperaturer på substrat av hexagonal SiC. Slutligen användes även den kloridbaserade kemin för att odla tjocka epitaxiella skikt vid högre temperaturer, 1700-1800 °C, med en mycket hög tillväxthastighet (Artikel 8). Detta är ett första steg mot en kloridbaserad process för att odla SiC bulkkristaller som sedan kan kapas till SiC substrat. Tack vare den kloridbaserade kemin kan betydligt lägre temperaturer än standard bulkprocesser användas som har en process temperatur på ca 2100-2400 °C.

List of publications included in the thesis

1. Thick homoepitaxial layers grown on on-axis Si-face 6H- and 4H-SiC substrates with HCl addition.
   S.Leone, H. Pedersen, A. Henry, O. Kordina, E. Janzén;
   J. Cryst. Growth, 312 (2009), p. 24-32.

2. High growth rate of 4H-SiC epilayers grown on on-axis substrates with different chlorinated precursors.
   S. Leone, F. C. Beyer, H. Pedersen, O. Kordina**,** A. Henry, and E. Janzén;
   Submitted to Crystal Growth & Design.

3. Improved morphology for epitaxial growth on 4° off-axis 4H-SiC substrates.
   S. Leone, H. Pedersen, A. Henry, O. Kordina and E. Janzén;
   J Cryst. Growth 311 (2009), p. 3265-3272.

4. Growth of step-bunch free 4H-SiC epilayers on 4º off-axis substrates using chloride-based CVD at very high growth rate.
   S. Leone, F. C. Beyer, H. Pedersen, O. Kordina, A. Henry, and E. Janzén;
   Submitted to Solid State Communications.

5. Optimization of a concentrated chloride-based CVD process of 4H-SiC epilayers.
   S. Leone, A. Henry, S. Andersson, O. Kordina, and E. Janzén;
   J. of Electrochem. Society, 157 (10) (2010), p. H969-H976.

6. Chlorinated precursors study in low temperature CVD of 4H-SiC.
   S. Leone, F.C. Beyer, H. Pedersen, S. Andersson, A. Henry, O. Kordina and E. Janzén.;
   Submitted to Thin Solid Films.

7. Chloride-based CVD of 3C-SiC epitaxial layers on 6H (0001) SiC.
   S. Leone, F.C. Beyer, A. Henry, O. Kordina and E. Janzén;
   Phys. Status Solidi (rapid research letter) 4 (11) (2010), p. 305-307.

8. Chloride-based SiC epitaxial growth toward low temperature bulk growth.
   S. Leone, F. C. Beyer, A. Henry, C. Hemmingsson, O. Kordina, E. Janzén;
   Crystal Growth and Design, 10 (8) (2010), p. 3743-3751.

List of publications not included in the thesis

(in reverse chronological order of publishing)

- Chloride-based CVD at high rates of 4H-SiC on-axis epitaxial layers.
  S. Leone, Y. C. Lin, F.C. Beyer, S. Andersson, H. Pedersen, O. Kordina, A. Henry, and E. Janzén;
  Presented ECSCRM2010 Oslo, to be published in Mater. Sci. Forum.

- Chloride based CVD of 3C-SiC on (0001) α-SiC substrates.
  A. Henry, S. Leone, F.C. Beyer, S. Andersson, O. Kordina and E. Janzén;
  Presented ECSCRM2010 Oslo, to be published in Mater. Sci. Forum.

- Chloride-based CVD of 3C-SiC Epitaxial Layers on On-axis 6H (0001) SiC Substrates.
  S. Leone, F.C. Beyer, A. Henry, O. Kordina and E. Janzén;
  Presented at E-MRS 2010, to be published.

- Deep levels in hetero-epitaxial as-grown 3C-SiC.
  F. C. Beyer, S. Leone, C. Hemmingsson, A. Henry and E. Janzén;
  Presented at E-MRS 2010, to be published.

- Concentrated chloride-based epitaxial growth of 4H-SiC.
  A. Henry, S. Leone, S. Andersson, O. Kordina and E. Janzén;
  Mater. Sci. Forum 645-648 (2010), p. 95-98.

- Chloride-based CVD at high growth rates on 3" vicinal off-angles SiC wafers.
  S. Leone, A. Henry, O. Kordina and E. Janzén;
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  Mater. Sci. Forum 615-617 (2009), p. 93-96.

- Growth of 4H-SiC epitaxial layers on 4° off-axis Si-face substrates.
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PART 1:

Introduction to SiC properties, growth and characterization

1

Silicon Carbide power devices for higher efficiency electronics

Will SiC save the world?

"The world is waiting for solutions to global warming and we have silicon carbide in our hands."
In 2007 Dr. D. Peters started his talk with this sentence at the International conference on Silicon Carbide and related materials held in Otsu (Japan). That talk was promptly commented with the following: "We thought we had enough to do getting defect levels down and making devices, and now we have to save the world?"
These sentences are a good introduction to the topic of this thesis.
Silicon Carbide (SiC) is a semiconductor material suitable for those electronic devices which are usually employed in applications where large amounts of energy are used (AC-DC converters, inverters in motors for industry, power grid transmission, etc.). SiC has those characteristics which potentially could reduce the energy losses usually occurring with Silicon (Si) devices, the most used semiconductor material for electronic applications nowadays. A very tiny increase in efficiency in any of these high power consumption applications would translate in a dramatic reduction of required energy; consequently less fossil fuel power plants would be needed, and tons of CO_2 emissions in the atmosphere could be avoided.
The equation "SiC devices = Reduce energy consumption" is definitively correct, but the route to get high quality and reliable SiC devices is still long, practical and economical reasons still hide the finishing line.
Although SiC has been investigated in academic institutions and at an industrial level for decades, its usage is still far below the expectations for two main reasons: the quality and the high cost both of the material and of the final electronic devices. SiC should replace some Silicon (Si) devices used today, but Si technology has been developed since half of the last century, and today its technology is very mature: very big (30 cm in diameter) circular substrates (so called wafers) of very high crystal quality are produced at a moderately low price. On the other side, commercial SiC wafers are today produced with an area 1/3 of that of the largest Si substrates with a questionable crystal quality, and at a significantly higher price than that of the bigger Si wafers. This shows the importance to further develop the SiC material so that less expensive substrates of higher quality and size can be produced. Such substrates would not only be

more convenient from an industrial point of view but also generate subsequent benefits on the worldwide energy consumption and reductions of CO_2 emissions. This thesis and all the efforts put into it are here to demonstrate that SiC can be manufactured at a reduced cost and with a higher quality. Thus SiC will outperform Si in some applications; it will be competitive and advantageous and it will be used for the sake of energy saving and, hopefully, in part "…to save the world"!

1.1 SiC physical properties

Silicon Carbide is a covalent crystal based on the covalent bond between a silicon and a carbon atom, having sp^3 hybridization. Each atom can form 4 bonds with the other element in a tetrahedral arrangement. The way the tetrahedrons stack on each other leads to different crystalline organization, also called polytype. More than 200 different polytypes can be formed in SiC according to calculations, but the polytypes observed in nature are much fewer than what has been calculated. According to Ramsdell´s notation [1] the different stacking sequences of the Si-C atoms can be described by a number, indicating the number of Si-C layers in the unit cell, and a letter, describing their geometrical arrangement (H for hexagonal, C for cubic, R for rhombohedral). The hexagonal arrangements 4H and 6H are the most known, together with the cubic 3C polytype. 4H is the most used polytype at an industrial level for device applications; 6H is widely used as a substrate for other semiconductor materials; 3C has some characteristics which make it attractive for MOSFET devices and as substrate for other semiconductors. SiC has many characteristic which makes it suitable and more advantageous to use for several devices, especially those involving high blocking voltages, as compared to narrower band-gap materials like Si. The main advantages of SiC are the high breakdown electric field strength, high thermal conductivity, and high saturated electron drift velocity.

A high breakdown electric field strength (E_{max}) makes possible to have unipolar devices which can handle very high voltages. Unipolar SiC power devices are efficient even at blocking voltages of more than 1 kV. E_{max} in SiC is about ten times higher than in Silicon. This means that a rectifying device made from SiC will require one tenth of the same epilayer thickness than what is needed for a Si device. Consequently, the doping of the SiC active layer will be ten times higher than that of the comparable active layer for a Si device. In theory this would mean a 100 times advantage in on state resistance if the devices were both unipolar. In the case of Si, nobody would design a unipolar device at voltages in excess of 1 kV, instead one would go to bipolar device structures where a plasma of electron and holes can be created.

Unipolar devices are however very advantageous to use in power circuitry since the switching speed is so fast. Switching losses in unipolar devices are small compared to those of bipolar devices and generally much higher switching speeds can be obtained.
The higher thermal conductivity of SiC also plays an important role because the heat produced through on-state and switching losses (reverse losses are generally very small) can be dissipated more easily. The produced heat will lower the mobility and hence increase the losses further. A high thermal conductivity is therefore paramount for good device performance. In practice it is the thermal conductivity that governs the power density one can use per unit area, or simply speaking, the thermal conductivity determines the chip size of the device.
High thermal conductivity and stability are very important features which make SiC not only resistant to high temperatures (like those in car engines) but also efficient in dissipating heat which consequently allows for much smaller and lighter cooling systems than those commonly used for Si. This last characteristic is one of the more attractive features making SiC interesting for use in hybrid-electric vehicles where light components are required.
The energy difference between the valence and conduction bands (band-gap) in SiC is very wide: between 2.4 and 3.3 eV, depending of the polytype. SiC is one of the semiconductor materials with the widest band-gap existing in nature.
Some of the main parameters of the most used semiconductors are reported in Table 1.1.

Table 1.1. Basic parameters of some semiconductors [2, 3, 4]

Material	Band gap eV	T_w K	λ W cm^{-1} K^{-1}	E_{cr} x10^5 V cm^{-1}	V_s x10^7 cm s^{-1}
Si	1.12	410	1.35	2.5	1
GaAs	1.43	570	0.45	2.6	1
3C-SiC	2.2	840	3-5	12	2.5
6H-SiC	3	1200	5-7	21	2
4H-SiC	3.2	1230	5-7	30	2
GaN	3.45	1250	1	40	3
Diamond	5.45	2100	14	190	2.7
AlN	6.2	2100	2	-	1.5

Note: T_w = working temperature; λ = thermal conductivity; E_{cr} = critical electrical breakdown field; V_s = saturated carrier velocity.

As may be seen from the table, diamond outperforms SiC in every aspect making it the clearest choice for power device applications. However, SiC is nevertheless the material of choice since it can readily be grown and processed into large, high quality, single crystal substrates, it can be doped both n- and p-type, and high quality epitaxial processes exist which enables accurate control of the active electronic properties.
From a material point of view, SiC has several physical properties which make it even more interesting for applications in harsh environments. SiC is a quite inert and hard material (second to diamond) which can withstand high temperature and harsh environments. Yet it is not easy to find an inexpensive and reliable material to be used for the packaging of these devices, which can work at the same operating temperature as the device made of SiC. Apparently packaging issues are the last frontier to cross in order to unleash the industrial commercialization of 4H-SiC MOSFET devices.

1.2 SiC for higher efficiency electronic

Today 40 % of all energy consumption is used for electricity. This share is forecasted to increase to 60 % within the next thirty years which creates problems due to the use of energy resources (fossil fuels and renewable energy sources) and subsequent greenhouse gases (GHG) emission [5]. From this 40 % of worldwide energy usage, more than 50 % goes into motion [6] which includes mainly motors for household and for industrial applications (Fig. 1.1) [7]. Electronic devices regulate the flow of energy for all the electronic systems which could be designed to have a high power rating (the rate at which energy is converted or work is performed, given by the product of current and voltage passing through a device).
The adoption of SiC devices can potentially affect almost every electronic system: industries, which use motors with variable speed; people, who use tools such as computers with power supplies; municipalities, which could get advantage of a more efficient and reliable power grid system; transportation, with hybrid cars and with every other mean of transportation which could rely on SiC-based sensors for a faster, cheaper and more reliable control of the main engine parameters.
Efficient power electronics enables energy savings in all applications where electricity is used. Power efficient motor control contributes with the biggest share of possible savings. Its application range from the industry sector (especially in engine at fixed and variable speed), to electricity driven transportation, and to home appliances requiring a motor (i.e.: washing machines, refrigerators, ventilation, …). By analyzing the details of the industry

sector, it can be calculated that one the biggest energy savings would come from this sector. In industry whatever moves needs a motor: fans, conveyors, winders, roller tables, spinning, pumps, cranes, paper machines, debarking drums, centrifuges, drilling, decanters, etc. Usually motors are kept running at 100 % of their power capability regardless of the requirement which is barely close to the motor maximum speed. By using a variable speed motor, which is run at 10 % above of the required power, an average of 40 % in energy is saved. Although they constitute for a smaller share in the motor control energy consumption, household appliances are also good candidates for energy savings by the use of efficient power devices controlling the motor speed. There are many motors in the appliances that we have at home, they require a consistent amount of energy, which could be reduced to 60% of actual consumption by using power devices.

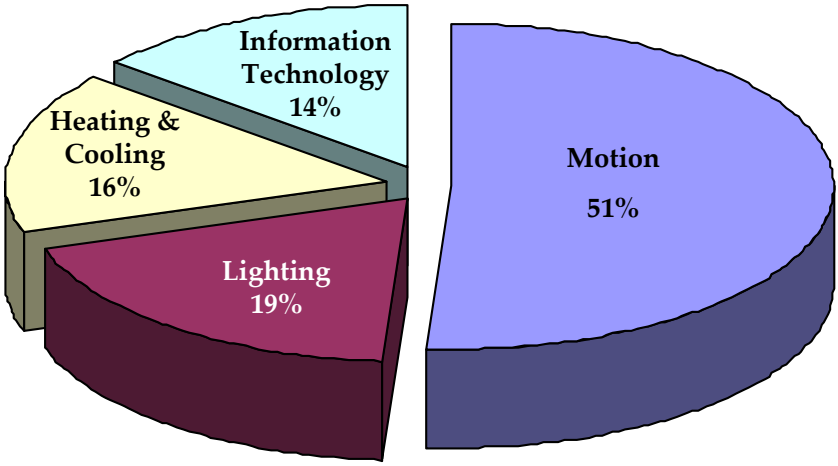

Fig. 1.1: Worldwide electricity usage by application area [7].

In addition the transportation sector can get several advantages from higher efficiency motors which use efficient power devices. SiC has the great advantage compared to other semiconductors to achieve the same power performance with much smaller area devices and without needing special cooling requirements. This means that traction drivers for trains and trams can get the benefit of more energy efficient tractions which are also lighter [8], however the technology is still not developed or reliable enough.

1.3 The green contribution from SiC

It has been calculated that in the German industry 12 % of all the motors could be run with power devices for electronic speed control making potential energy

saving possible that would amount to at least 20 %, which equates to about 9 fossil power plants (22 TWh). On a global scale, energy efficient motor drives alone can potentially save 202 billion kWh/year and avoid 75 million tons of CO_2 emission, leading to a staggering 45 GigaWatt reduction for new power plant capacity over the next 20 years! [9]

The case for green technologies such as solar and wind power is very important. Both techniques can produce energy at high voltage which must be stored to have it available as backup when no energy is produced (no sun or wind). Often storage must be done in low voltage batteries, and then converted back in AC to put it back in the distribution line, or it can be supplied directly to the grid, but still several conversion steps will be involved. SiC can play a very important role in all these AC/DC conversions, which can ultimately result in a 10 % higher efficiency for these green technologies (Fig. 1.2) [10].

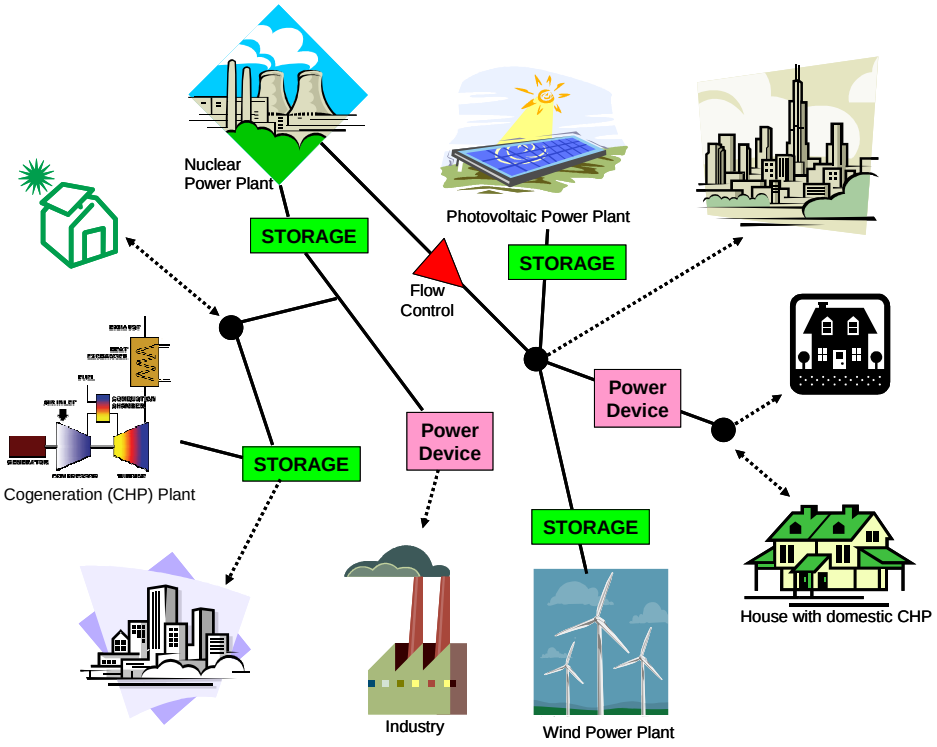

Fig. 1.2: Architecture of future distributed network of smart grid management. Example of decentralized network with power variation [10].

It is not easy to estimate the saving in energy if SiC power devices would be used also in household appliances, because this depends on their market which is believed to increase widely in next decades especially in Asiatic countries. The

same can be said for the transportation sector where the technology has to be developed, therefore no estimate can be done but that the whole electricity driven transport would benefit of a 25 % saving from the actual typical losses (estimated to be about 20 %) [9].
SiC can help to save energy, but the manufacturing cost (in energetically and economical terms) of SiC itself is quite high. The chloride-based CVD process, discussed and developed in this study, has the advantage of a great reduction in energy consumption to manufacture SiC. In the case of the epitaxial growth of a thick layer, a growth rate 10 times faster than the standard process would require very short production cycles with a reduction of one order of magnitude on all the consumables.
As it can be seen from Table 1.2, the saved time is enormous: about 9 hours for a 100 μm thick SiC epitaxial layer deposition. Such a large time saving results in many benefits in terms of the production cost and the environmental impact: the chilled water, power supply for all the reactor's components, the ventilation and exhaust gas treatment consumed per hour can be now reduced by more than 80 %! Typical consumables, such as carrier gas (hydrogen) and the power consumption keeping the process temperature at 1600 °C, are reduced by about 90 %! The lifetime of the reaction chamber can be significantly prolonged since it is only affected by the time of usage, which in this high growth rate process will be used 10 times slower.

Table 1.2. Cost comparisons between the standard and chlorinated-CVD process.

Materials and time consumption for a 100 μm thick SiC epilayer	Cycle time -no growth (min)	Epilayer deposition (min)	Hydrogen consumption (cubic meter*)	Power consumption (kW**)
State of the art reactor with standard CVD process at 10 μm/h	120	600	90	300
CVD reactor with Cl-CVD process at 100 μm/h	120	60	9	30
Saving	0	540	81	270

Note: * = typical consumption of 9 cubic meter/h; ** = typical consumption of 30 kW/h.

We can conclude that the development of the chloride-based CVD process of SiC would allow growing high quality SiC epitaxial layers while reducing its production cost to 80-90 % of the non-chlorinated state-of-the-art process. This

saving would give a tremendous impact/push to the development of SiC technology due to the availability of much cheaper material produced with an environment-friendly process.

There are still some barriers to be overcome for SiC to gain full acceptance in the market. Basically the first one regards the cost of these devices. As discussed above, the cost of SiC devices is too high compared to standard devices or power devices made of Si. Furthermore, the reliability of SiC devices is not yet high enough to convince users to invest in them, especially when taking into account the high standards of quality and safety which are required nowadays. A second limitation is the practical cost and time needed to implement this new technology. As an example it falls as natural that the use of variable speed motors in industries will probably happen gradually: when an equipment is too old and it is no longer worth doing maintenance on, it is replaced for a more efficient equipment with efficient motor control. The same accounts for household appliances, which will enter the market slowly, especially if governments give incentives to buy them.

My personal opinion is that the gain in terms of saved energy and reduced CO_2 emission could be so high that it motivates further efforts to develop SiC to make it less expensive and of higher quality. The focus of this thesis which is the advancement of the chloride-based CVD process may be the key technology to make the green-SiC-dream to come true!

2

Silicon Carbide growth

Setting the right oven temperature and the right ingredients… almost like making a pizza!

In 1824 SiC crystals were observed for the first time by J. J. Berzelius in Sweden [11]. Since then SiC has gone through intense research activity characterized by periods of dark and bright years. In the first half of the twentieth century it was discovered that SiC was more than just abrasive material known as Carborundum. In 1906 H. Dunwoody made a device of SiC which is considered to be the first diode, and in 1907 H. J. Round noticed electroluminescence from SiC [12]. Yet dark years came due to the boom of Si technology in the sixties, but SiC came back on the stage when Tairov and Tsvetkov managed to grow SiC crystals with high quality at the end of the seventies [13]. Nowadays the American company Cree Inc. markets 100 mm diameter wafers of very high crystallographic quality, and 150 mm diameter wafers are realized at an R&D stage [14].
Gemstones of SiC are also appreciated in the jewelry business where it is featured under the name of moissanite after the French mineralogist H. Moissan who found the first natural SiC crystal in a meteorite in 1905. [15].

2.1 Bulk growth

In 1892 Acheson managed to set up a process in a big furnace to grow SiC polycrystals of different sizes, and small monocrystalline platelets were formed in the voids of the charge material [16, 17]. The quality of those crystals was good enough to be used either as an abrasive material or for cutting tools. In this very simple process a big furnace was electrically heated up to 2700 °C to form SiC crystals starting from a mixture of silica, coke, and small percentages of saw dust and salt (NaCl, acting as a purifying material through the formation of chlorinated volatile species).
In 1955 Lely developed the growth process to a stage where crystalline platelets of higher crystalline quality and larger size were formed. A vacuum-tight furnace containing polycrystalline SiC and resistively heated to 2600 °C led to the growth of crystals of high quality due to a small temperature gradient [18].
Lely platelets had such a high quality that they were used as seeds in the modified-Lely-process, also called seeded sublimation growth, introduced by Tairov and Tsvetkov in 1978 [13]. The process consists of heating a

polycrystalline SiC source to a temperature where SiC sublimes appreciably, similar to the Lely process, but the vapor is condensed on a slightly colder seed, thereby realizing the growth of a thick single crystal grown at an appreciable rate. High purity graphite, growth in vacuum or in an inert gas atmosphere, and an accurate control of axial and radial temperature gradients were the key innovations in this process, more properly called physical vapor transport (PVT). In 1987 Cree Research Inc. was founded with the aim of developing the PVT process to grow thick and large diameter SiC crystals, which could be cut into wafers for semiconductor device applications [19]. Soon after the first Cree wafers were available on the market and the era of SiC as an industrial semiconductor material had started.

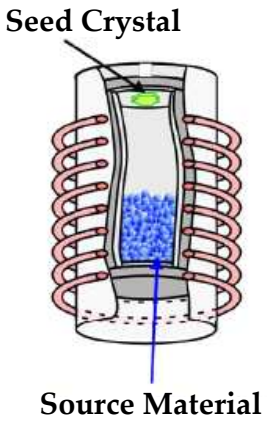

Fig. 2.1: A typical PVT system.

A PVT process is based on the physical process of sublimation, but many parameters have a very important effect on the final crystal quality. The furnace is usually a cylinder made from high purity graphite (Fig. 2.1) wrapped in insulating graphite felt and placed inside a quartz tube surrounded by a coil for radio-frequency heating. The process is run at temperatures up to 2400 °C under vacuum or under a low pressure of Argon, so that the SiC powder sublimes forming a vapor of SiC_2, Si_2C and Si. These vapors condense on a crystalline seed attached to the top part of the reaction chamber which is the coldest point. The growth rate and the shape of the grown crystal, as well as its quality, are chiefly determined by the axial and radial temperature gradients. The major advantages of this technique are the high growth rate achievable (even more than 1 mm/h), and the size of the crystals which can be grown and expand even more than the seed size. Important drawbacks of this process are the difficulty in growing very pure crystals and the very high operating temperature, which basically contributes to two main factors: the difficulty of keeping a low temperature gradient, with the risk of introducing of a lot of stress in the material (affecting the crystalline quality), and a high

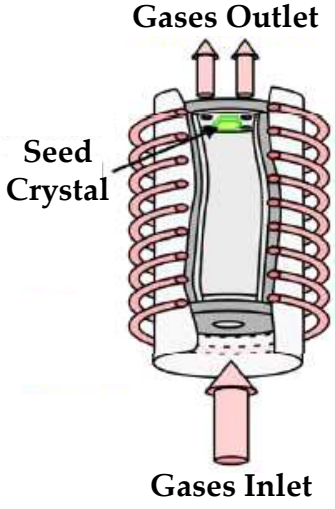

Fig. 2.2: A HTCVD reactor.

manufacturing cost (both in terms of lifetime of the furnace, and of energy requirement for heating and cooling unless a lot of insulating material is used).
At the end of the nineties a high temperature chemical-vapor-deposition process (HTCVD) was introduced [20, 21] (Fig. 2.2). The two main differences with the PVT system are: the source material, which now is made of high purity gases (such as silane, and ethylene); and the reactor is open instead of being a closed system. The deposition temperature might be lower than the PVT, but still above 2000 °C, otherwise the two systems are similar. In fact in the HTCVD process, non-stoichiometric SiC microcrystals are formed in the gas-phase which are brought to sublime and the resulting vapors condense on the seed resulting in the growth of a SiC crystal, exactly as in the PVT process. Besides, while in the sublimation process the growth is driven only by mass transport of the sublimed vapor, in HTCVD the process pressure can be adjusted in a broad range in order to affect the growth profile, speed and uniformity. The main advantage of the HTCVD process is the achievable purity of the crystals thanks to the pure gas source. Very high resistivity semi-insulating material needed for RF applications can be grown with this technique. The main drawbacks of this system are: the limited length of the crystal boule and growth rate, which are lower than in PVT; and the higher thermal gradient existing in the reaction chamber which results in a lower material quality, and causes a low reproducibility of the process and overall low production yield. Wafers produced in this way are available on the market [22].
More recently a new technique has been introduced, called halide CVD (HCVD) [23, 24]. The growth process is very similar to the HTCVD, the main differences are the adoption of chlorinated precursors and the reaction chamber geometry: a split gas injector for the carbon and silicon sources is used and the gas outlet is at the bottom of the reaction chamber. The silicon precursor is a chlorinated specie, tetrachlorosilane ($SiCl_4$), which avoids the formation of silicon clusters in the gas phase, as in the HTCVD process. In principle this should enable a lower deposition temperature, but this is normally kept above 2000 °C to minimize the formation of parasitic depositions at the inlet, which limits the duration of growth runs. Limits and drawbacks are similar to the HTCVD technique, but no commercial wafer has ever been available in the market manufactured with this process, to the best of our knowledge. A similar process, but run at a much lower

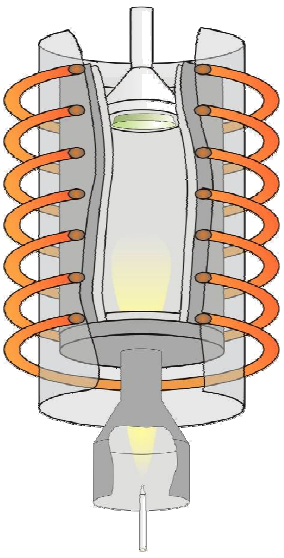

Fig. 2.3: Vertical reactor used for chloride-based CVD.

temperature of 1850 °C in a vertical reactor(Fig. 2.3), is described in this study in Paper 8.

2.2 Epitaxial growth

The electrical properties of the wafers cut out from a crystal boule are not good enough to be used directly as the active part of an electronic device. It is necessary to grow one or more layers (epitaxial layers) on top of the substrate. These layers must have an accurately controlled thickness, conductivity and dopant concentration, which are needed to get the electrical properties required for a specific electronic device.

The word epi-taxy come from the Greek words meaning "above" and "order", which indicate the process of growing a structure above a substrate keeping the same (crystallographic) order of the substrate itself. If the substrate and the epitaxial layer (epilayer) are exactly the same, both in terms of chemical and physical characteristics, the process can be also called homoepitaxial growth. If substrate and epilayer have a different chemical identity or a different crystallographic structure (*i.e.* 3C-SiC on 4H-SiC), then the process is called heteroepitaxial growth.

2.2.1 Epitaxial reactors

The SiC epitaxial growth process is usually made in a Chemical Vapor Deposition (CVD) reactor, where a mix of gases is flown inside a furnace. The laminar flow of the gas mixture forms a stagnant layer above the heated substrate. As the gas is heated, the reactive gases start to decompose (gas phase reactions). Some of the formed gaseous intermediates diffuse through the stagnant layer (also known as boundary layer) and may stick to the substrate where additional chemical reactions take place (surface reactions) leading to the growth of an epitaxial layer.

Many other epitaxial growth techniques exist. The ones which can alternatively be used for 4H-SiC epitaxial growth are: molecular beam epitaxy (MBE) [25]; sublimation epitaxy [26]; liquid-phase epitaxy (LPE) [27]; and some other minor techniques used for coating or other applications.

MBE is used to perform growth of SiC on Silicon substrates or to grow very thin layers where *in situ* characterization techniques (such as RHEED) may be used to monitor the initial stages of the epitaxial growth. MBE is done under high vacuum conditions with the precursors supplied through sputtering or heating of solid sources. Although it gives the advantage of controlling the growth in a very accurate way, it cannot be applied at an industrial scale due to the very low growth rate achievable (less than 1 μm/h) [25] and the very high production costs.

Sublimation epitaxy is based on the same principle as the PVT technique; the main difference is in the very close distance between the powder or polycrystalline SiC source and the substrate. High growth rates in excess of 200 μm/h can be achieved, but the source material is generally not pure enough to achieve a low background doping and high purity. The two major requirements of an epitaxial layer, which are the precise control of thickness and doping and their uniformity on the whole wafer, can neither be controlled with sufficient accuracy [26].

Liquid Phase Epitaxy (LPE) may be used to fabricate p-n junctions or to fill micropipes manifest in the substrate. The substrate is dipped in a graphite crucible filled with melt consisting of silicon with trace amounts of carbon dissolved in it. Usually, the melt also contains some chemical elements (scandium, lead, tin, germanium, …) added to improve the solubility of the carbon species. The achievable growth rate is higher than that of the standard CVD process but the inferior morphology and difficult doping control limits its practicality [27].

The CVD process is the most successful for growing device-quality epilayers; however several different reactor configurations may be used. Only a few of these configurations however can produce the quality and doping and thickness uniformity that is needed to obtain a high yield in the subsequent device processing. Reactors can have a horizontal or vertical configuration, depending on the gas flow direction and wafer position, and the flow can be directed parallel or perpendicular to the wafer surface. In cold wall reactors only the susceptor part where the wafers are placed is heated, while in the hot wall reactors all the walls and sides of the susceptor are heated. In case of the warm wall, the wafers are placed on heated susceptor, while the ceiling is a passively heated plate which reaches a lower temperature [28]. In some cases a part of the susceptor where the wafers are placed, or the whole susceptor, is continuously rotated during the growth assuring an improved uniformity. Nowadays one of the most commonly used reactor in industry is the horizontal hot-wall reactor setup developed by Kordina *et al* [29] at Linköpings University, which guarantees the best crystallographic quality and uniformity on multi-wafers systems [30] (Fig. 2.4).

Another category of reactors employed by industries is the planetary reactors. They are fundamentally similar to the horizontal hot-wall reactors, but both the susceptor and the smaller susceptor discs (satellites) supporting the wafers rotate to favor an improved uniformity, however the reactor cost and maintenance costs are significantly higher than those of the horizontal hot-wall reactors [31]. Horizontal reactors are usually run at reduced pressure under conditions where a laminar flow may be maintained more easily. A consequence of the laminar

flow is the rather thick stagnant layer which is formed on all the sides of the reaction chamber.As mentioned earlier, the gases have to diffuse through this layer before reaching the substrate and contribute to the growth. The thickness of the stagnant layer affects the growth rate, but its thickness is dependent on several parameters, mainly on the gas speed and therefore the process pressure [32].

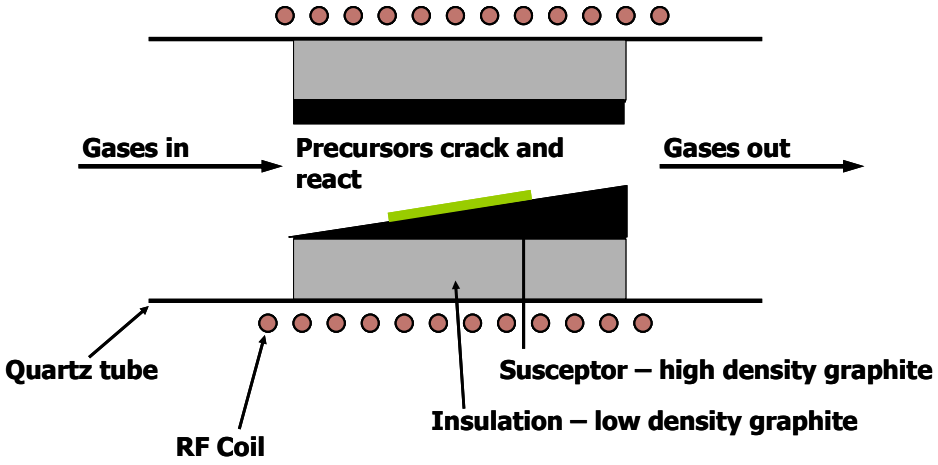

Fig. 2.4: Schematic of a horizontal hot-wall CVD reactor.

2.2.2 Growth regimes and modes

Thermodynamic and kinetic phenomena determine the growth process. Thermodynamic aspects are important mainly for the crystallographic nature of the epilayer and the achievable growth rate, while kinetic factors govern the speed of the gas-phase reactions and consequently impact the quality of the grown material. The main variables in a growth process are the temperature and pressure, which have to be controlled in such way that the main intermediates contributing to the growth are in a state of supersaturation. Different growth regimes and growth modes can occur on the surface depending mainly on the growth temperature and supersaturation conditions. In SiC epitaxy low temperatures (below 1300 °C) lead to kinetically controlled growth regimes which often result in amorphous growth. An intermediate regime between 1300 and 1500 °C is used for polycrystalline deposition or for monocrystalline 3C-SiC growth. At the typical growth temperature (1500 – 1600 °C) the mass transport regime regulates the amount of species diffusing on to the growth surface, where the temperature and substrate's surface morphology (*i.e.* flat terraces, stepped structures, …) will delineate the growth mode. At very high temperatures (above 1700 °C), like those used for bulk growth, the process is still under mass

transport regime, but it is mainly driven by thermodynamic factors, and partially by those parameters determined by the growth conditions, which will prevail in delineating the crystal growth process (Fig. 2.5).

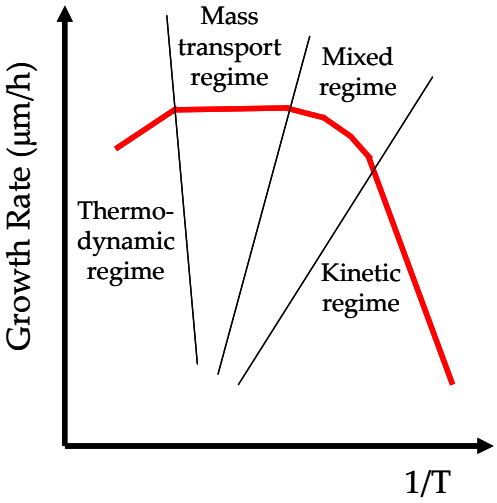

Fig. 2.5: Growth regimes dependence on growth temperature.

The most common epitaxial processes are based on a gas-phase system either by using gaseous precursors, or vapors obtained through sublimation of solid precursors, or by bubbling a carrier gas through a liquid precursor. In the case of SiC the CVD process is used. In such systems many steps are involved before a gas molecule contributes to the growth of a crystalline structure. These are: 1) mass transport of the gas species to the inside the reaction chamber; 2) gas-phase reactions; 3) diffusion of the reaction products to the crystal surface; 4) adsorption of some species on the substrate's surface; 5) diffusion of the adsorbed atoms on the surface; 6) incorporation of the atoms on the surface (by different growth modes as described later) or desorption of the adsorbed species from the solid to the gas phase; 7) mass transport of the non-adsorbed byproducts and the desorbed species away from the reaction chamber [33].

These mechanisms are depicted in Fig. 2.6. The parameters affecting each of these steps are many, spanning over parameters such as the reaction chamber geometry and heating profile, the gas dynamic and speed, and also the surface morphology and precursors´ concentration and ratio.

Three different growth modes can take place on the surface: i) island growth (Volmer-Weber); ii) layer-by-layer (Frank-van der Merve); and iii) a combination of layer- and island- growth mode (Stranki-Krastanov) [34]. The first or second modes prevail when the bonding between the adsorbing atoms and the substrate is weaker or stronger, respectively, than the bonding between adsorbed atoms. The third mode occurs when an initially formed layer changes its surface energy promoting island growth for the following adsorbed atoms. These phenomena are very important to control in the case of SiC growth. The width of the terraces where the atoms land after gas diffusion can favor one mode over the other, as well as the ratios of the main precursors intermediates can promote different islands shape (pillar, hillock, …) or steps advancing faster than others. In the case of SiC the two first modes are the ones which are more likely to occur. Island

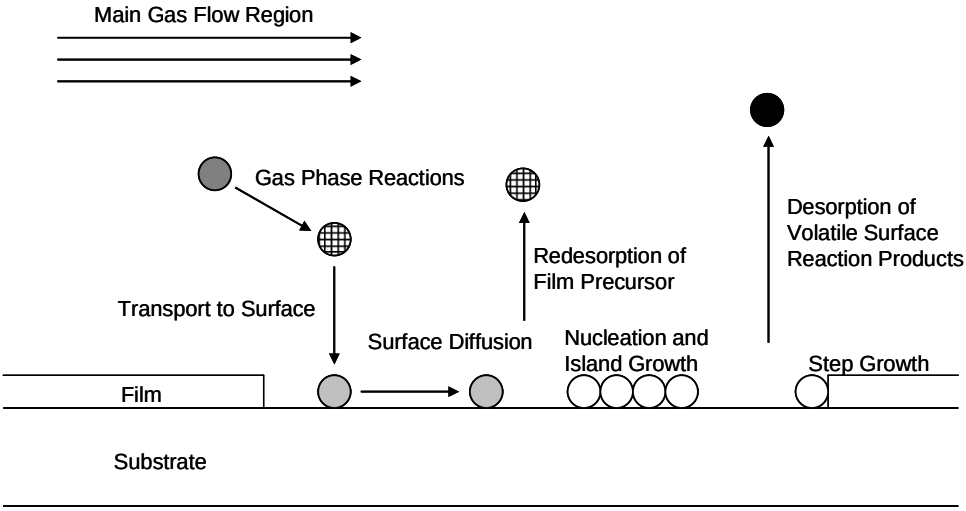

Fig. 2.6: Gas phase reactions and solid phase processes leading to the growth of an epitaxial layer [33].

growth usually occurs when the epitaxial growth is made on substrates cut parallel to the basal plane (0001). When atoms are adsorbed on a flat and wide terrace the 2D nucleation process is favored and is often initiated by spiral growth at dislocations manifest in the substrate. Due to the many different stacking sequences possible for SiC, in the case of growth on hexagonal substrates like 4H and 6H, the occurrence of 3C-SiC nucleation is very high, unless the growth is performed at temperatures higher than 1800 °C whereas only thermodynamic factors determine the grown polytype. Matsunami *et al.* [35] introduced the use of substrates cut with a small off-angle with respect of the basal plane, so that the generated step-structures and the reduced terrace widths would promote the layer-by-layer growth mode. In this way even lower growth temperatures could be used without generating other polytypes formed by the island growth-mode. Yet the growth temperature has to be kept high enough to ensure sufficient adatom mobility on the surface, so that they can reach the kink at the steps.

2.2.3 Growth parameters

An easy, though overly simplistic, way to describe the epitaxial process and the importance of the numerous growth parameters is to use the analogy of making a good "*Italian pizza*", the difference being that the ingredients (precursors) are not put on the dough (substrate) before baking it, but they are flown as gases inside the oven. The "art" of making a pizza has many common features with the "art" of growing an epitaxial layer: setting the right temperature in the proper

oven, choosing the right ingredients (their amount and way of adding them). When the pizza or the epilayer is ready, the proper characterization tools have to be used by expert personnel to validate the quality of a real good Italian pizza or a good device-quality SiC epilayer.
The description of the right oven (a horizontal hot-wall reactor) and method to grow a SiC epilayer were described in the previous section. In this section a brief outline of the main growth parameters and their effect on the epilayer quality are given.

Substrate off-angle
Nowadays commercially available wafers are 100 mm diameter wafers cut with an 8° or 4° off-axis cut towards the [11 $\bar{2}$ 0] direction in case of 4H-SiC, while 3.5° off-axis are used for 6H-SiC. On-axis or low off-angle (such as 2° off-axis) are also available on request.
An 8° off-axis cut ensures a wide window of operating parameters. Homoepitaxial growth has been demonstrated even at very low temperatures, such as 1300 °C [36, Paper 6], and most of the parameters can be used in a range that otherwise cannot be employed for lower off-cut angles. Most of the epitaxial defects formed are the same as for the other off-cut substrates. There are two main drawbacks in using this off-angle though. The presence and propagation of basal plane dislocations (BPD) in the epitaxial layers, which gives rise to a drift of the forward voltage in bipolar devices during operation [37]; and the manufacturing cost, since crystal boules are usually grown on on-axis seeds and consequently when the crystal is cut at such an off-angle it can produce a waste of up to 50% of the grown material.
4° off-axis 4H-SiC substrates have become more used since 75 mm diameter wafers were available on the market, in order to reduce the waste generated from cutting crystal boules. However the step-bunching is one of the main concerns with these off-cut substrates (Fig. 2.7). It is due to the different energy of the two different single-bilayer terraces (also called steps)

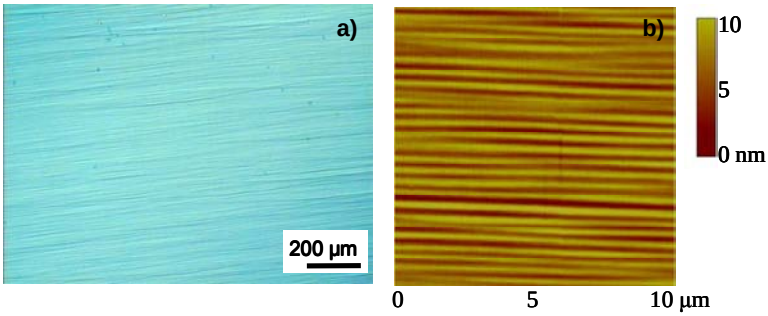

Fig. 2.7: Epilayer grown on 4° off-axis 4H-SiC: (a) Optical microscope image of a 10 µm thick layer; (b) AFM of a 10 x 10 µm^2 area with a RMS of 2.3 nm.

existing on 4H-SiC. At the typical growth temperatures (above 1500 °C) the energy difference is enhanced and causes one of the two terraces to grow faster than the other, so that bunches of steps higher than one unit cell are formed, resulting in a rough surface [38]. Lower temperatures can be used, but the probability of forming 3C-SiC inclusions and triangular epitaxial defects increases markedly [39]. A specific combination of growth parameters (*i.e. a* low temperature and low C/Si ratio) helps to avoid these issues but it limits the achievable growth rate, as described in Paper 3. Yet proper preparation of the surface may reduce the source of epitaxial defects even if the growth is performed at temperatures where step bunching is minimized, as shown in Paper 4. The remaining issues with 4° off-axis wafers are similar to those of 8° off-axis substrates, which are related to the presence of BPD and the waste of material when large diameter crystals are sliced at a 4° angle. With respect to BPD, it has been demonstrated that by growing layers thicker than 20 μm [40] or at high growth rates [41] BPD could annihilate by way of their image force converting into threading edge dislocations.

Lower off-angles, such as 2° off-axis, or wafers off-cut towards other crystallographic directions, such as $[1\,\bar{1}\,00]$, have been used to solve the problems of the BPD propagation and step-bunching [42] related to 4° off-axis substrates.

Nominally on-axis substrates have always been seen as the supreme choice to avoid BPD propagation. Preliminary results have confirmed very stable forward voltage operation in bipolar devices made on on-axis epilayers [43], which reveals a complete absence of the problems associated with the BPD. As an added bonus, no material will be wasted by slicing wafers out of crystal boules grown on on-axis seeds, as normally done.

In the past, the main difficulty was to perform homoepitaxial growth on on-axis substrates at temperatures not exceeding 1600 °C. This was because the nucleation of 3C-inclusions is very likely to occur on a non-stepped surface. Improvement of the polishing (as with CMP) and proper *in situ* etching conditions solved these problems [44, 45], as explained later. Yet the morphology obtained after growth on these surfaces is usually very rough [43, Paper 1 and 2] and unless chemical-mechanical-polishing (CMP) is performed, difficulties to process devices appear. Another approach is the use of very vicinal off-angles (between 0.3 and 1° off-axis) as proposed by Kojima *et al* [46] or in Paper 1. Even very small differences at such low off-angle can have a big impact on the growth mechanism which can vary from island growth, to spiral and step-flow, and eventually only step-flow (Fig.2.8).

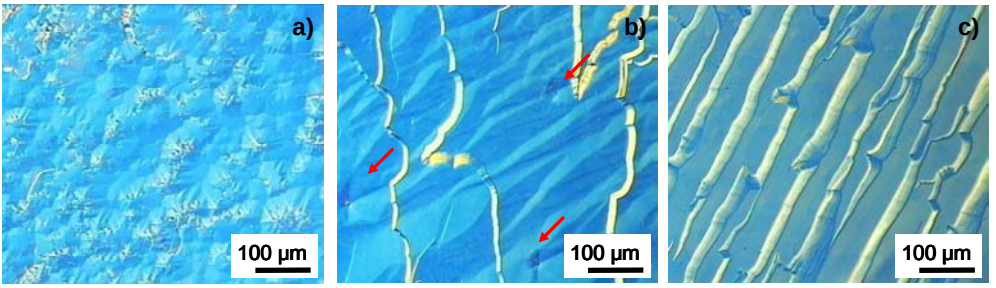

Fig. 2.8: Optical microscope image of a 20 µm thick epilayer grown on 4H-SiC with different low off-angles: a) 0.05°; b) 0.15° (island growth indicated by the arrows); c) 0.33°.

***In situ* etching**

One of the most important process parameter, though often neglected, is the preparation of the surface prior to the start of the epitaxial growth. As mentioned before, the epitaxial process tends to replicate the same order and structure of the substrate in the epilayer. It is wrong to assume that the substrate surface is unchanged during the temperature ramp up from ambient to growth temperature. The type of gas that is flown, the susceptor condition, the pressure, the time needed to reach the growth temperature are parameters which impacts the surface modifying it in several ways depending on the substrate polarity, off-angle and even polytype. Just the simple temperature ramp-up can be assimilated to an *in situ* etching unintentionally done on the surface which must be taken into consideration. In addition to this unintentional etching, under some conditions (*i.e.* on-axis homoepitaxial growth, or heteroepitaxial growth) a suitable etch step must be performed prior to the growth.

Several papers have been published to find out the optimal conditions for specific epitaxial processes yet only faint agreement can be found on which the best parameters are to be used simply because of the complexity of the several phenomena which are involved during the heat up. The main events which can occur on the substrate surface during unintentional or intentional *in situ* etching is desorption of silicon or carbon species at different rates and on specific areas of the surface. The vapor pressure of silicon is different from that of carbon. Silicon evaporates faster than the carbon species, especially at low pressure. On the other hand carbon atoms bind preferentially to hydrogen atoms forming hydrocarbons which desorb fast from the surface. The addition of another gas to the hydrogen such as hydrogen chloride (HCl) or/and a gas containing silicon or carbon can change the chemical equilibrium on the surface. The presence of chlorine will preferentially enhance the removal of silicon from the surface; a gas

containing silicon will suppress silicon evaporation, making faster carbon desorption, and vice versa in the case of flowing a gas containing carbon atoms. A small overpressure of one of the elements caused by silicon- or carbon-rich deposits on the susceptor, or uncoated parts of the graphite susceptor can affect the partial pressures of the carbon or silicon atom suppressing the desorption of one of them from the surface. The etching, or gas desorption is faster from areas with a higher surface energy, such as step edges, defects (dislocations), scratches due to polishing, and so on. This mean that aggressive etching conditions, such as very low pressure, the flow of an aggressive gas (like HCl), or a very slow temperature ramp up resulting in a long exposure to hydrogen could result in very non-uniform etching of the surface.
Extensive studies have been done on 4H- and 6H-SiC substrates with an off-cut [47, 48] and apparently a carbon overpressure during the temperature ramp-up leads to a better surface morphology in the case of higher off-angles, while in the case of 4° off-axis 4H-SiC, pure hydrogen is to be preferred [49, Paper 3]. Evidently high off-angles are subjected to a faster desorption of the carbon specie which leaves unpaired silicon atoms on the surface which eventually coalesce into silicon aggregates or droplets on the surface. These droplets can be buried by the subsequent epitaxial layer giving rise to epitaxial defects, or they can evaporate before the growth starts, leaving behind tiny pits. As said before these effects occur preferentially in combination with other defects such as scratches on the surface or dislocations. Carbon is needed to suppress the hydrocarbon species that may be formed through the interaction of the hot hydrogen with the carbon atoms from the substrate surface. In the case of 4° off-axis, it seems that the hydrocarbon formation is not so apparent, and in fact, a carbon overpressure may create a carbon-rich surface which could lead to a step-bunched epilayer or to a higher density of triangular defects. In the case of even lower off-angles (off-angle between 0.3 and 1°), such as vicinal on-axis substrates, the optimum conditions are reversed: a silicon overpressure is needed to prepare the surface at its best to favor homopolytypic growth [Paper 1]. For nominally on-axis substrates (off-cut angles lower than 0.1°) a dedicated *in situ* etching with silane at high temperature must be performed to ensure homopolytypic growth of thick layers [44] also at high growth rates [Paper 2]. 3C-SiC seems to be favored by carbon-rich etch conditions. Heteroepitaxial growth of 3C on hexagonal SiC on-axis substrates is favored by carbon-rich surface preparation.

Temperature (heating profile)
The epitaxial growth of hexagonal SiC is usually done at a temperature range between 1500 and 1600 °C where the growth regime is controlled by the mass transport. The introduction of off-cut substrates made possible to achieve

homopolytypic growth at these temperatures, otherwise special *in situ* treatment or growth temperatures of 1800 °C or more are needed [35]. Higher temperatures can be used for the epitaxial growth, but etching effects will be enhanced producing an etched surface and a decrease in growth rate. Lower temperatures could also be used. Homoepitaxial growth of 4H-SiC on 8° off-axis substrates has been demonstrated under several growth conditions and with different precursors at a temperature as low as 1300 °C [36, 50, Paper 6]. The drawback with low temperature operations is the low adatom mobility on the substrate's surface, which often results in an island-growth mode, and thereafter in extended defects organized with the 3C stacking sequence. Other defects, such as silicon aggregates and polycrystalline islands, or even complete polycrystalline or amorphous surfaces will ultimately be formed, especially at even lower temperatures.

The growth rate is affected by the temperature. The chemical reactivity of the gas species is enhanced at high temperature, but the growth rate does not always benefit of it, because etching is also enhanced at high temperatures counterbalancing the growth rate increase. Besides, the typical range of temperatures at which growth is done is selected for a good morphology control and the growth rate generally does not change appreciably in this range [51]. A temperature of 1300 °C can limit the growth rate to no more than 13 μm/h even when using the chloride-based CVD process [Paper 6], which usually allows substantially higher rates.

High temperature growth could be used to get very high growth rates, adaptable for a bulk growth CVD process. At temperatures above 1800 °C higher precursors concentrations can be used resulting in higher growth rates, especially if etching is minimized by using low hydrogen flows [Paper 8].

The doping (or incorporation of dopants) can also be affected by the temperature. This effect is moderate in the typical temperature window used for SiC epitaxial growth. In the case of n-type (nitrogen doped) layers grown with the standard CVD process [52] or with the chloride-based process [53], the doping increases moderately with the temperature when using Si-face substrates, while it decreases in the case of C-face substrates. P-type (aluminium doped) layers are affected in the opposite way compared to n-type layers, as demonstrated both with the standard process [54] and with the chloride-based process [55]. In both cases only small changes in the doping are noticed apart from a slight increase when going to low temperature (*i.e.* 1500 °C). Very low temperature growth (about 1300 °C) could favour much higher p-type dopant incorporation [56], since the evaporation rate of aluminium is much lower at a reduced temperature [54].

A last important consideration about temperature regards its distribution along the reaction chamber. It is not possible to keep exactly the same temperature along the susceptor length, especially at the inlet and outlet (Fig. 2.9), since some heat is lost through radiation, and they are colder than the central part of the susceptor.

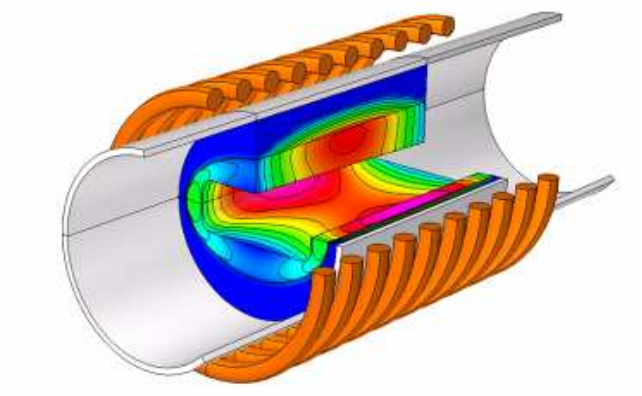

Fig. 2.9: 3D drawing of a heated hot-wall CVD reactor. Different colors indicate different temperatures of the heated susceptor. [51]

The RF coil position and geometry (distance between each turn of the coil, and the position of the coil relative the susceptor) can be properly tuned to achieve better temperature uniformity. Some process conditions, such as very low carrier flows and high gas speed, may require higher temperatures at the susceptor inlet, to guarantee a proper cracking of the precursors before they arrive above the substrate [Paper 5]. Another parameter affecting the heat distribution is the cooling of the incoming carrier gas which enters at a very low temperature.

Pressure

Reduced pressure is generally used in SiC multi-wafer reactors, because it helps in keeping a good gas flow uniformity in a larger sized reaction chamber. Pressures between 50 and 300 mbar are often used, depending on the reactor size and process. The pressure affects many parameters: the gas speed; the adsorption-desorption equilibrium of species between gas and solid phase; the thickness of the stagnant layer. Low pressure in general is advantageous for CVD processes mainly because of the stagnant layer reduction, thus gases can reach the substrate more easily, and adatoms may have a higher surface mobility [51]. A lower limit in the pressure is established due to some reasons: a too high gas speed results in a non-optimal gas concentration above the substrate [Paper 5]; a too fast precursor depletion; and adatom desorption will be intensified resulting in etching and faster evaporation especially of silicon species [51]. Higher limits in the pressure are set by either the formation of an undesired turbulent flow, which makes difficult to achieve high uniformity on large areas, and safety issues.

Recently a very low pressure (about 20 mbar) CVD process has been developed to achieve high growth rates (up to 250 μm/h), exploiting the suppression of silicon clusters at such low pressures [57].
Doping can be also affected by pressure. Nitrogen incorporation is proportional to the pressure, because the partial pressure of nitrogen containing species is directly affected by total pressure. The carbon coverage of the grown surface which influences the nitrogen incorporation into the layer, changes also with pressure [52]. Aluminum incorporation is generally also proportional to the pressure, but the overall mechanism is a result of a number of more complicated effects, especially the effective C/Si ratio existing in the gas phase. At a reduced growth rate the aluminum incorporation increases when reducing the pressure from atmosphere to about 300 mbar, but this tendency reverts at even lower pressures [54].

Carrier flow
Hydrogen is the most common carrier gas used in SiC CVD. It has been demonstrated that it can be incorporated easily both in the epilayer and in the substrate [58]. It can affect the electrical properties of epilayers, especially p-type SiC, because hydrogen forms complexes with p-type dopants [59]. In the case of boron incorporation, the passivation effect of hydrogen can be removed by annealing the material, in order to promote hydrogen diffusion and to make boron atoms active electrically [60].
Hydrogen is very active in the gas phase reactions and hence very important to achieve the proper gas-phase chemistry. As discussed in the previous paragraphs, it may also have very important effects on etching of the carbon species, or in the "cold finger" phenomenon which can impact the heat and gas-phase distribution inside the reaction chamber [61].
Argon may be added in the carrier gas at low percentage to improve the uniformity of the epitaxial layers. Helium is usually used in HTCVD systems not only to reduce the etching effect due to the hydrogen but also to have a good thermal conductivity. [62].

C/Si ratio
The ratio between the carbon and silicon precursors is one of the most important parameters in the growth of SiC layers. Carbon or silicon rich conditions have a direct influence on the polytype formation [63] with the 3C polytype becoming more likely to be formed at carbon rich conditions. In a very simple model it can be said that silicon-rich (Si-rich) conditions causes silicon droplets on the epilayer, while carbon-rich (C-rich) favours extended epitaxial defects (carrots and triangles) which often contain 3C-SiC inclusions (Fig. 2.10).

Eventually a too high C-rich input leads to polycrystalline or even amorphous layers. In the case of substrates with a high off-cut angle (4 or 8°) step-bunching can be generated at high C/Si ratios [64]. When nominally on-axis substrates are used, the C/Si ratio can influence the growth mode of spiral or hillocks starting from screw dislocations, and even the shape of islands (Fig. 2.11) [65, Paper 1].

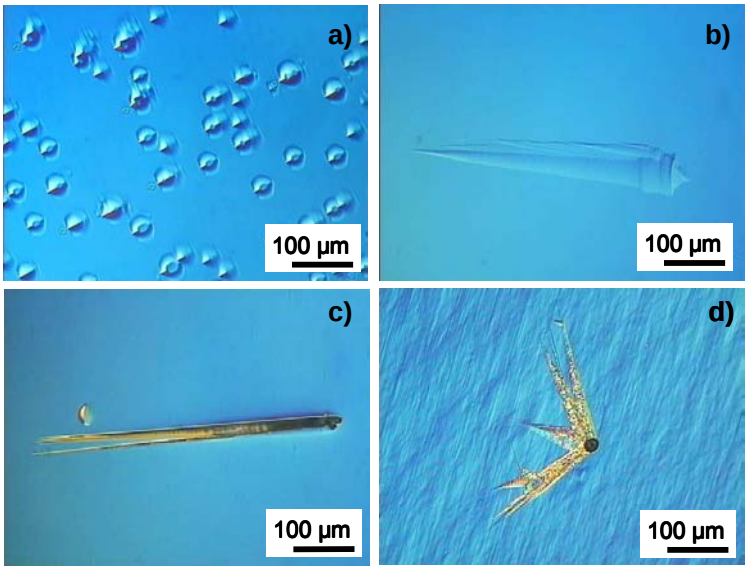

Fig. 2.10: Optical microscopy images of epitaxial layers grown with different C/Si ratios: a) 0.7; b) 0.8; c) 0.9; d) 1.

To obtain perfectly stoichiometric growth of SiC the C/Si ratio should be set at 1. The C/Si ratio is however usually set higher than 1 in standard growth conditions [35], due to the fact that the desorption of carbon species from the substrate is faster as compared to the slow gas diffusion of silicon species through the stagnant layer [51]. The validity of these assumptions is shown by the growth rate dependency which indicates a decrease of the growth rate at low C/Si ratios (typically below 1) and a saturation of the growth rate for higher C/Si ratios (as observed in Paper 3). It means that at high C/Si ratios the growth is steady and not limited anymore by the supply of one or the other of the two precursors. Adding more of both precursors will naturally increase the growth rate.

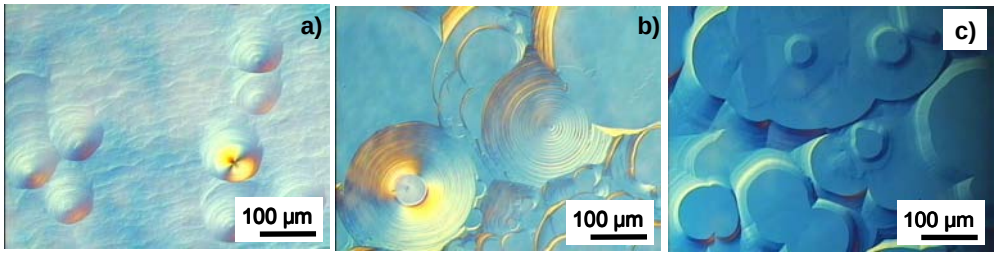

Fig. 2.11: Optical microscope images of epitaxial layers grown on on-axis substrates with different C/Si ratios: a) 0.6; b) 0.8; c) 1.

The values at which saturation is reached can easily change with any growth parameter, even the precursor concentration. In the case of chloride-based CVD with methyltrichlorosilane (MTS, CH_3SiCl_3) where growth rates of 100 μm/h and more can be reached, the plateau of the growth rate with respect to the C/Si ratio is reached at a C/Si = 1 [66], whereas values in the 0.3 to 0.4 range have been reported in a vertical hot-wall reactor [67].
Another very important effect related to the C/Si ratio is the site-competition epitaxy effect which determines the dopant incorporation [68]. It has been demonstrated that nitrogen atoms incorporation is inversely proportional to the C/Si ratio, because they occupy C-sites in the SiC crystal lattice, therefore a high carbon content renders nitrogen incorporation more difficult and vice versa. The opposite is valid for aluminium atoms incorporation, which is proportional to the C/Si ratio, since they occupy Si-site in the lattice.

Si/H_2 ratio

This is the typical parameter used to indicate the precursor concentration. The growth rate is directly proportional to this value when all the other parameters are kept fixed. The C/Si ratio is also kept fixed by scaling up the carbon source flow. If the standard CVD process is used, the Si/H_2 ratio is limited to values of less than about 0.1%; for higher values silicon clusters are formed in the gas-phase and they can fall on the epilayers as droplets, or they can form aggregates on the surface which can re-evaporate leaving a footprint behind. In all events the epilayer morphology will be severely damaged and no device can be processed on such layers. Under these conditions the growth rate is limited to values below 10 μm/h [69]. There are two main methods for the silicon clusters to be dissociated or not formed, so that the Si/H_2 ratio can be increased, and hence for the growth rate to be increased. One is to grow at very low pressure and at slightly higher temperatures [57], while the second is to add chlorine in the gas mixture

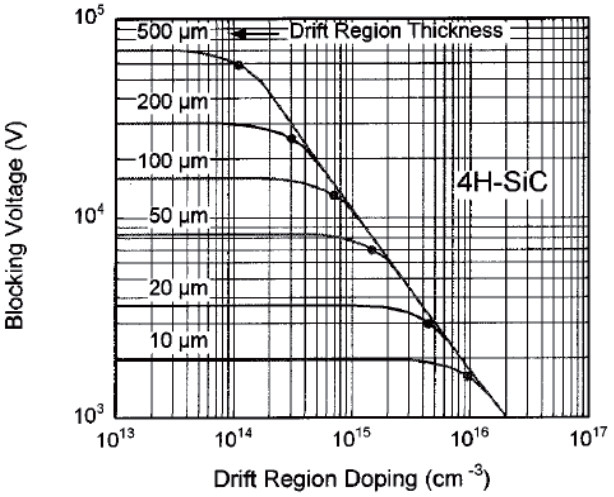

Fig. 2.12: Blocking voltage of a 4H-SiC epilayer as a function of doping and thickness.
[70 (© 2002 IEEE)]

since silicon atoms in the gas phase will bind preferentially to chlorine atoms instead of forming clusters, as it will be described later. In both approaches high Si/H_2 ratios (more than 0.5 %) can be used and growth rate of about 100 - 200 μm/h can be achieved [57, 66, 69]. Indeed it is very useful to have rates of about 100 μm/h, because this makes possible to grow the very thick (100-200 μm) layers needed for high power devices (10 kV and more) (Fig. 2.12) [70] in a reasonable production time.

Doping

The most typical dopants for SiC are nitrogen (N) for n-type and aluminum (Al) for p-type conductivity. Other elements can be used, such as phosphorus for n-type and boron for p-type, but they are not as convenient as N and Al [71]. Phosphorus can be added by using gaseous phosphine (PH_3) [71] or the liquid source tertbutylphospine ($C_4H_9PH_2$) [72]. Both chemical compounds are more expensive and dangerous than the inexpensive and inert nitrogen, which remains the most utilized n-type dopant. Boron contaminates the whole reaction chamber (including the quartz tube), which makes it highly unsuitable to use as it will be very difficult to obtain a low background doping again due to memory effects [55]. Molecular nitrogen (N_2) and liquid trimethylaluminum ($Al(CH_3)_3$) are two common sources for these dopants, employed also at an industrial level. Their incorporation is proportional to the amount introduced into the reactor, but it can be affected by many parameters (temperature, pressure, C/Si ratio, …).

Precursors

The standard process is based on silane (SiH_4) and a hydrocarbon, usually propane (C_3H_8) or ethylene (C_2H_4). Other silicon compounds have been tried, such as disilane and methylsilane [73], but silane remains the most used at an industrial level for the standard process. Chlorosilanes are discussed in the next section. Several hydrocarbons have been tested, but C_3H_8 and C_2H_4 are the ones used industrially because they guarantee a wider window of operating parameters and therefore a better morphology and higher growth rate for the epitaxial layers. C_2H_4 has a higher reactivity and can be used for growths at lower temperatures [74].

2.2.4 Chloride-based CVD

The very well developed industrial process for the production of silicon epitaxial wafers is based on the chloride-based CVD process. Chlorinated precursors are always used: trichlorosilane ($SiHCl_3$, or TCS); tetrachlorosilane ($SiCl_4$, ot TET); and occasionally dichlorosilane (SiH_2Cl_2, or DCS) [75]. As discussed in the section related to the Si/H_2 ratio, chlorine atoms have a high affinity with silicon

atoms in the gas phase, which prevents the formation of silicon clusters detrimental for the epilayer growth.

Chlorinated precursors were used for SiC growth in the previous century, mainly for heteroepitaxial growth of SiC on Si substrates [76] or for coating and other applications, but not so often for homoepitaxial growth of SiC [77]. The advantage of HCl addition to prevent silicon droplets to be formed on epilayers was reported in 1996 [47]. Dr. O. Kordina was the first to introduce chlorine (Cl) during the homoepitaxial growth of SiC to improve the morphology of epilayers by dissociating the clusters formed in the gas phase, as described in his patent filed in 2003 [78].

In the case of SiC growth, Cl can be introduced in the precursor mixture in several ways: by simply adding HCl or chlorine (Cl_2); by using chlorinated silicon precursors, like TET and DCS; by using chlorinated carbon precursors, like chloromethane ($CHCl_3$) or similar; or by having chlorine in a molecule containing both carbon and silicon atoms, like MTS (Fig. 2.13).

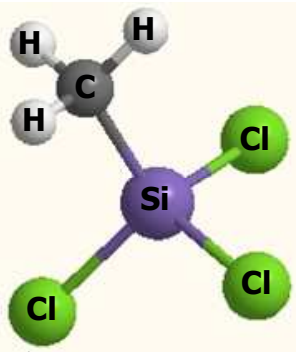

Fig. 2.13: The methyltrichlorosilane (MTS) molecule.

The addition of chlorine to the CVD process is not only fundamental to achieve very high growth rates, but in some cases it allows a wider operating window of the growth parameters which is particularly valuable when performing growth at temperatures lower than 1400 °C [Paper 6 - 7].

Chlorinated precursors

HCl can be added to the standard precursors, resulting in a very flexible process in terms of C/Si and Cl/Si ratios. The first publications on the chloride-based CVD applied for homoepitaxial growth of SiC were presented in 2004 [79, 80] exhibiting an increase in growth rate up to 30 μm/h, and later up to more than 100 μm/h [69, 81]. HCl has more benefits than dissociating silicon clusters, such as helping to prepare the substrate surface prior the growth [47, Paper 4] or to reduce the formation of 3C inclusions in the epilayer [82, Paper 1].

TCS and TET are the most used chloro-silane precursors. While TET has been proposed for growth at higher temperatures [24, Paper 8] but also for typical growth conditions [83], TCS has been more extensively used and some device material has also been demonstrated [84, 85]. The gas-phase chemistry of TCS and TET is different to that of the silane-plus-HCl-case resulting in a higher growth efficiency, which makes TCS and TET more attractive for industrial applications.

Chlorinated carbon precursors have not been explored so much, except chloromethane (CH_3Cl). It has been employed mainly for the growth at reduced temperature (1300 – 1400 °C) [36, 50], but also at higher temperature and growth rate [83]. A wider operating window of the growth parameters is found using it instead of normal hydrocarbons [86], but chlorinated silicon precursors are still to be preferred for the sake of high growth rate processes [83].
Methylchlorosilane, such as MTS, is very convenient to be used for SiC growth since it contains all the 3 chemical elements needed for the growth process, but their relative ratio is fixed, therefore other compounds have to be added for specific applications where those fixed ratios have to be changed. MTS was the first chlorinated precursor used for SiC epitaxial growth [76]. Homoepitaxial growths using MTS were done at the end of previous century [77] but only in the last years it has been successfully used to demonstrate very high growth rates of high quality homoepitaxial deposition of thick 4H-SiC layers [66, 87]. The gas-phase chemistry is similar to the case of chlorinated silicon precursors, except for the carbon species, which actually makes a difference in the precursor efficiency [81].

Precursor comparison
The gas-phase composition depends on the precursors used. A large difference of the main intermediates formed exists when comparing chlorinated silicon precursors with the standard silane chemistry with additions of any chlorine source. Chlorinated silicon precursors lead principally to the $SiCl_2$ intermediate, and partially to SiHCl. In the case of silane with chlorine additions, SiHCl is formed, and $SiCl_2$ is obtained only under certain conditions (Fig. 2.14) [88, 89]. This creates a very important difference in the growth efficiency which has been also confirmed experimentally [81], where chlorinated silicon precursors produce higher growth rates than silane plus HCl at the same Si/H_2 ratio. Apparently even chlorinated carbon precursors appear to be more efficient than non chlorinated carbon precursors even when HCl is added [86], however this result has not yet been explained by kinetic or thermodynamic calculations.
The difference in efficiency may also be perceived by the developed growth rate profile along the reaction chamber length [Paper 2]. MTS generates a much higher growth rate compared with $SiH_4 + C_2H_4 + HCl$, thanks to the higher efficiency. At the same time a higher depletion of the silane precursor is experienced on account of its reactivity. The silane decomposes and deposits silicon at the entrance of the susceptor [88].

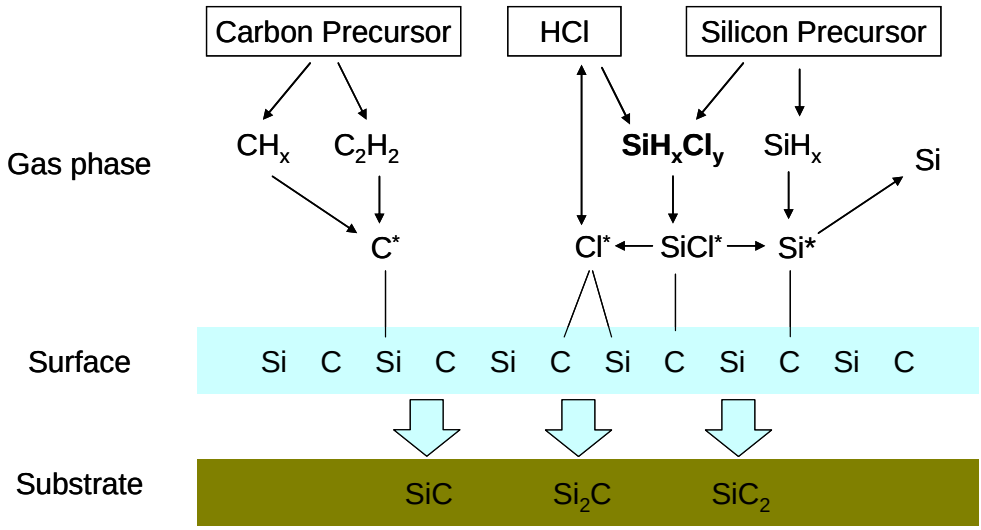

Fig. 2.14: Gas phase model in chloride-based CVD chemistry in the case of HCl addition [88].

Cl/Si ratio

Chloride-based CVD is not just a matter of adding chlorine into the reactor to avoid the formation of Si clusters. The addition of controlled amounts of chlorine in the system, *i.e.* controlling the Cl/Si ratio, can have very important effects on the epitaxial growth.

From a chemistry point of view a high input of chlorine in the system should result in a lower amount of silicon reaching the surface, which means a lower growth rate but also a higher effective C/Si ratio [90]. Thermodynamic calculations, based on growth parameters adopted in our setup, have showed that very high Cl/Si ratio (above 10) is needed to avoid the formation of liquid silicon. For a Cl/Si ratio above 10, it is possible to have an effective C/Si ratio below unity thereby establishing those Si-rich conditions which are essential for on-axis homoepitaxial growth [Paper 1]. Further experiments show however that in cases where on-axis substrates are treated with a Si-rich *in situ* etch, the produced Si-rich surface does not require such a Si-rich gas-phase [Paper 2].

The Cl/Si ratio affects the growth rate [66], but this dependence can change with different precursors [81, Paper 2]. The trend is that the growth rate increases with the Cl/Si ratio until a maximum is reached (between 3 and 5, depending on the precursors), and then it decreases. Probably the increase in growth rate is obtained as a result of an increasing concentration of the intermediate $SiCl_2$ with increasing Cl/Si ratio. The $SiCl_2$ is more efficient than SiHCl which is

predominantly formed at low Cl/Si ratios [91]. When the input of chlorine is too high, the etching effect of the chlorine becomes more significant resulting in a net decrease of the growth rate.
Doping experiments with the chloride-based process indicated that the Cl/Si ratio has a relevant effect on the two possible categories of dopants. N_2 incorporation in 4H-SiC Si-face epilayers is proportional to the Cl/Si ratio [53], as if higher Cl renders a lower C/Si ratio (more silicon reaches the surface). The opposite result is achieved in case of Aluminum incorporation in 4H-SiC Si-face epilayers, whereas it decreased by increasing the Cl/Si ratio [55], again as if the C/Si ratio is lowered.
The 3C polytype heteroepitaxial growth or 3C inclusion formation can be strongly affected by the Cl/Si ratio. Very high quality 3C-SiC heteroepitaxial layers could be grown at the low temperature needed for this polytype (below 1400 °C), because of the presence of chlorine which prevented the formation of Si clusters in the gas- and solid-phase. Furthermore, the morphology of the 3C layers is very dependent on the amount of added chlorine [Paper 7]. On-axis epitaxial layers could be grown homoepitaxially at high growth rates due to the use of high Cl/Si ratio. 3C-inclusions are limited or even suppressed when a high ratio is used [45, 82, Paper 1]. Even bulk growth at moderately high temperature (below 1900 °C) has been demonstrated to be possible when high Cl/Si ratio is used, because the formation of 3C inclusions can be prevented in that way [Paper 8].

2.2.5 Simulation of CVD process

A CVD process is a very complex system where chemical and physical phenomena are governed by macroscopic parameters. Growth temperature and pressure, gas inputs and the substrate's surface, gas speed and temperature distribution in the reaction chamber, are some of the main parameters which regulate all the processes occurring during an epitaxial layer deposition. Simulation software are used to calculate macroscopic phenomena occurring in a CVD reactor: temperature distribution, mass transport, and chemical reactions. Thermodynamic analysis can be sufficient to predict the main products which can be formed and at which rate. However kinetic parameters must be included on account of the rate at which different mechanisms can develop, in order to have a realistic picture of what really happens in a CVD process.
Simulations of SiC epitaxial growth have been done by several groups [51, 92, 93, 94], all of them are quite reliable and fit very well with experimental results. These achievements were employed to further develop the SiC CVD process even on larger area reaction chamber reactors.

Only preliminary simulations have been done based on the chloride-CVD process [88, 89, 95], which have shown that chlorinated-silicon precursors produce mainly the $SiCl_2$ intermediate, which has a faster gas-phase diffusion and results in a higher incorporation efficiency and therefore a higher growth rate, as confirmed by experimental results [81, Paper 2]. Those calculations showed also that the chloride-based CVD is a much steadier and uniform process than the standard chemistry based on silane and hydrocarbons, due to the different reactions occurring in the gas phase [89].
In this study several thermodynamic calculations have been performed to understand some experimental results. These were useful to get a hint on the importance of using very Si-rich conditions for the homoepitaxial growth on on-axis substrates [Paper 1], or on the improved growth efficiency in concentrated (low carrier flow) processes [Paper 5].
Still there are many unanswered questions on the chloride-based process. Further investigations should be performed to realize a model which fits on the vast amount of experimental data collected. The consequent advantages of its employment could be fundamental for the SiC chloride-based epitaxial process validation at an industrial level. The impacts of this research can be noteworthy on a worldwide scale, with enormous advantages for the industrialization of SiC high power devices but also for fundamental knowledge which could support other growth processes (*i.e.* nitride or graphene growth). This model could be used to study the possibility to adopt the chloride-based process for bulk growth of SiC in a horizontal-hot-wall configuration, performed at much lower temperatures than those exceeding 2000 °C in normal sublimation reactors, and probably resulting in much less stressed and consequently less defective material. Only a good model of the CVD process could make this further development feasible in a short time and at a reduced cost.

3

Characterization tools

The art of "tasting" the quality of the epitaxial layers

The growth of SiC epitaxial layer is a complicated process, but it can be claimed to be successful only if the epilayers quality is confirmed by several characterization techniques. There are several ways to investigate the physical and electrical properties of SiC epitaxial layers. A basic characterization consists of morphological and crystallographic analysis corroborated with electrical measurements. Epilayers morphology is evaluated by optical microscopy and by scanning electron microscopy (SEM); atomic force microscopy (AFM) can give the ultimate analysis at an atomic-scale. The crystallographic quality of the material can be assessed by X-ray diffraction (XRD), by low temperature photoluminescence (LTPL) from the UV to the IR region, and by Raman spectroscopy. Investigations on structural defects can be done by X-ray topography or by simply etching the epilayers (for example in molten potassium hydroxide at 500 °C) followed by a detailed analysis of the layer in an optical microscope. Identification and electronic structure identification of point defects is performed by electron paramagnetic resonance (EPR) and optical detection of magnetic resonance (ODMR). Electrical measurements, such as current-voltage (I-V) and capacitance-voltage (C-V), can give information on the conductivity, net carrier concentration, leakage current, and other electrical parameters. The existence of traps in the material band gap can be detrimental for device performance; they can be investigated by techniques like deep-level transient spectroscopy (DLTS) and minority carrier transient spectroscopy (MCTS), or by an indirect technique such as time-resolved photoluminescence (minority carriers lifetime measurement). Epilayer thickness measurements can be done by an optical technique, which is measuring the Fourier transform IR (FTIR) reflectance and by analyzing the inverse Fourier transform spectrum.

The epitaxial process cannot be validated if there is not a positive feedback from all of the above techniques. Only when a good epitaxial process is attained, yielding high quality epitaxial layers, these can be used for device applications. Device performance is the decisive test to assess the quality of the material and the growth process.

In this chapter the most used characterization techniques utilized in the present study are briefly introduced.

3.1 Optical Microscopy

Microscope analysis of the morphology of epitaxial layers is a very fast and informative tool. The quality of an epilayer can be evaluated in terms of surface roughness, epitaxial defects, and overall morphology uniformity. The thickness of epitaxial layers can be deduced with some approximation either by the length of extended defects (such as carrots, comets and triangular defects) assuming that they start at the substrate-epilayer interface, or by looking at the cross section of cleaved samples where a difference in doping between the epilayer and substrate makes their interface distinguishable.

Nomarsky differential interference contrast (NDIC) is frequently used to obtain a better contrast on the morphological features. NDIC makes use of a prism (called a Nomarsky prism), which polarizes the light and separates it into two orthogonally polarized components. These components are closely spaced (about 1 μm) when they reach the sample and are reflected back. Any difference in their path will result in an interference effect between the two beams, which are merged together when passing again through the Nomarsky prism. The final result is an image with enhanced contrast between areas of the surface with any different feature.

NDIC microscopy can be used to analyze etched samples and identify different dislocations existing in the material with sufficient accuracy. The etching can be performed by dipping a SiC sample in molten potassium hydroxide (KOH) at a temperature usually ranging from 450 to 550 °C, and a variable duration depending on etching temperature and purpose. Different defects, such as micropipes and dislocations (screw, edge, basal plane) can easily be recognized and distinguished with a NDIC optical microscope (Fig. 3.1).

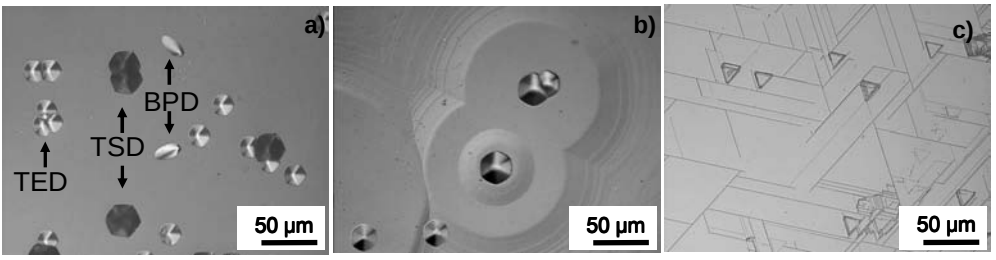

Fig. 3.1: Optical microscope images of epitaxial layers grown on different substrates etched with KOH at 500 °C for 90 seconds: a) 4H on 8 ° off-axis 4H-SiC, TED = threading Edge Dislocation, TSD = Threading Screw dislocation; BPD = Basal Plane dislocation; b) 4H on on-axis 4H-SiC, screw dislocations are at the center of each island; c) 3C on on-axis 6H-SiC, typical stacking faults of cubic polytype.

3.2 Atomic Force Microscopy (AFM)

Scanning probe microscopy, such us scanning tunneling microscopy (STM) and atomic force microscopy (AFM), are surface analysis tools able to reach a lateral resolution at an atomic level (even less than 1 Å). They are based on the concept of scanning a surface with a probe, and using the interaction (tunneling current, force interaction, optical interaction) between the probe and the atoms making up the surface. In the case of AFM a topography image of the sample can be obtained by the force interaction between the atoms on the sample surface and a finely shaped tip at the edge of a cantilever, for which movements are accurately controlled through a scanner made of a piezoelectric material. Any deflection of the cantilever caused by the interaction between surface atoms and tip atoms can be detected by the deflection of the cantilever. The accuracy of the scanner movements in the vertical and horizontal directions is fundamental to get information from the atomic-scale interactions. AFM can be operated mainly in two modes: contact and tapping mode. While in the first case the tip is dragged on the sample surface, in the second case the cantilever is kept tapping at a fixed frequency and distance from the surface in a way that its oscillations are constant. Any change in the deflection due to an interaction between *i.e.* a protuberance on the surface and the tip will produce a change in the cantilever deflection and a movement in the scanner, which is translated and detected as a change in topography. Short and long range forces (mainly Van der Waals) play an important role in the tip-surface interactions which are dependant on the characteristic of the analyzed material.

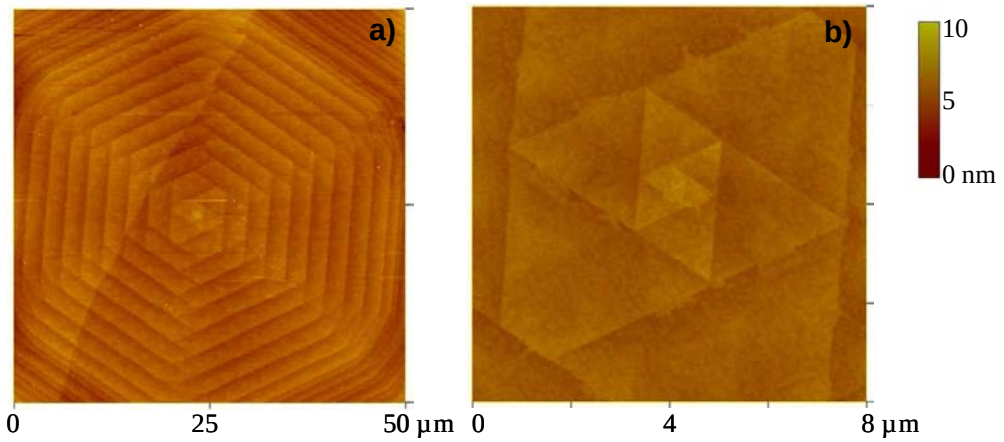

Fig. 3.2: AFM of a 4H-SiC epilayer grown on on-axis substrates. Island growth starting from a screw dislocation can be seen on different size images:
a) 50 x 50 µm^2; b) 8 x 8 µm^2. Step height is equal to the unit cell of 4H-SiC.

Many details and parameters can be varied and used to extract a lot of useful information for a very accurate surface analysis.
AFM in tapping mode is most commonly used on SiC samples. Very detailed topography maps of surfaces can be obtained, gaining information on the arrangement of atoms on the surface, presence of step-bunching, information on defects, and even clear images on spiral growth of islands (Fig. 3.2).

3.3 Low Temperature Photoluminescence (LTPL)

LTPL is a powerful technique which can give very important information about the quality of epitaxial layers. The different SiC polytypes can be recognized [96]. Features related to different dopants can be distinguished [97] and in the case of nitrogen and aluminum their concentration can be estimated [98]. Impurities (such as Titanium, Chromium, Vanadium, …) have been identified and their absence (or presence) may be verified. The presence of stacking faults and some intrinsic defects (such as the C-vacancy) can similarly be assessed [97]. Finally the purity and high crystalline quality of the epilayer result in a very intense photoluminescence spectrum characteristic of the material, the spectrum can be considered as a tool to assess material quality.
Photoluminescence is obtained by photo-exciting a sample with photons, usually emitted by a laser, at a well defined energy which is higher than the energy of the material band-gap (Fig. 3.3). Once the photons irradiate the sample, the electrons which are in the valence band (ground state) will be excited to the

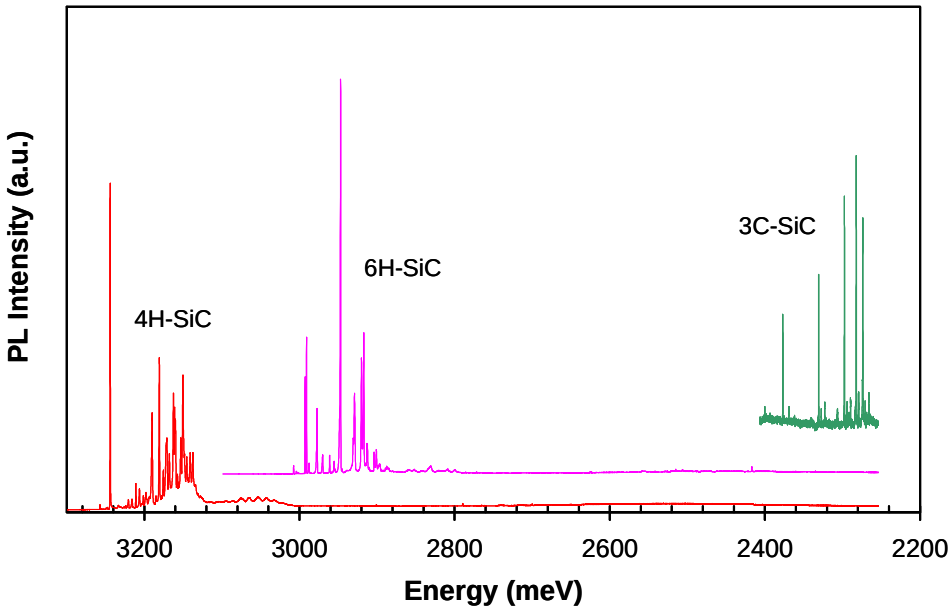

Fig. 3.3: LTPL recorded at 2K with an excitation of 244 nm on epilayers of different polytypes.

conduction band (excited state). As a result of this process, the free electron and hole formed in the conduction and valence band respectively relax into the band gap and can form an electron-hole pair bound by Coulomb interaction, called free exciton (FE). The free exciton has a high mobility and is free to travel in the crystal lattice until it either recombines radiatively thereby releasing a photon ($\hbar\omega$), or it is trapped at an impurity or defect forming a bound exciton (BE). The BE can also recombine radiatively releasing a photon of another wavelength characteristic of the defect involved in the BE complex.
In case of the FE the photon has an energy which is equal to the band gap energy (E_g) minus the binding energy (E_{FE}) required to form the free exciton:

$$\text{FE: } \hbar\omega = E_g - E_{FE}$$

While for the bound exciton even the binding energy to the impurity (E_{BE}) has to be considered:

$$\text{BE: } \hbar\omega = E_g - E_{FE} - E_{BE}$$

Since SiC is an indirect band gap material, excitons recombination has to be assisted by phonons to keep momentum conservation. In fact phonon-assisted recombinations are dominant in SiC. These recombinations can occur through different phonons, resulting in several phonon replicas with the following energy:

$$\text{Phonon-assisted bond exciton: } \hbar\omega = E_g - E_{FE} - E_{BE} - E_{Phonon}$$

A BE recombination can also occur without being assisted by a phonon if the impurity atom takes the excess momentum, which is a very rare event in indirect band-gap semiconductor as SiC, and often gives origin to a weak line in the PL spectrum, that is labeled as "no-phonon" line. In principle, in SiC a FE can not have no-phonon lines since there is no impurity atom to absorb the momentum in the exciton recombination process, as it happens for a BE. Conservation of momentum must always be maintained. In theory, the no-phonon line of the FE should never be observed however there have been reports where a weak no-phonon line of the FE has been seen, though this is a very rare event in SiC [99].
Another feature of PL observed in SiC arises from the way nitrogen impurities incorporate into the SiC lattice for different polytypes. Nitrogen atoms usually take place in a carbon site of the lattice, but this site can have different locations depending on the polytype. For 3C-SiC this site is uniquely a cubic site and consequently the spectrum of 3C only produces one no-phonon line due to N-BE (nitrogen-bond-exciton) and four phonon replicas (longitudinal acoustic and optical phonons, called LA and LO, and transversal acoustic and optical phonons, called TA and TO). The hexagonal polytypes can have both cubic and hexagonal

sites. 4H has one cubic and one hexagonal site, therefore two N-BE no-phonon lines can be found in the spectrum (P_0 and Q_0) having different energies due to different binding energies at the two sites. 6H has one cubic and two different hexagonal sites, and three no-phonon lines are originated (P_0, R_0 and S_0).
The amount of phonon replicas depend on the symmetry of the material. In 4H-SiC there are three equivalent minima of the conduction band located in the *M* point of the Brillouin zone. In 4H there are eight atoms per unit cell, which means that 24 (3x8) phonon assisted recombinations can occur, resulting in principle in 24 phonon replicas. Half of these have parallel polarization to the crystal axis, and the other half has perpendicular polarization. 22 out of these 24 replicas have been observed experimentally [99].
It is needed to keep the sample at liquid Helium temperature (2 K) to have all the electrons in the ground state and to reduce the possibility that thermally excited phonons may re-excite electrons into the upper states, which will cause broader or extra additional features in the spectrum.
At 77 K is still possible to distinguish the different SiC polytypes with good accuracy, while at room temperature it could be more difficult. At RT only a broad near band gap emission is observed from high quality epilayers. PL recorded at different temperatures can be useful to calculate the activation energy of a defect and to have information on its energy structure.
Measurements of the near band gap luminescence at 2K of SiC epilayers can be used to calculate the nitrogen concentration in uncompensated samples [98].

3.4 Thickness measurement by FTIR reflectance

The FTIR technique is very fast in measuring the thickness of epitaxial layers in a non-destructive way which is very important for industrial applications. With this technique it is possible to measure the thickness of a low-doped epilayer on top of a highly doped substrate. The difference in doping between the two layers results in a different dielectric constant and hence a different refractive index between them.
The core of an FTIR is the Michelson interferometer which in essence produces Fourier transformed light which is focused onto the layer and reflected both at the vacuum-epilayer and the epilayer-substrate interfaces. If both interfaces are smooth no problems with scattering of light will occur. The light beams reflected at the two interfaces will interfere and an interferogram will be obtained. After inverse Fourier transform a reflectance spectrum is obtained. In the obtained reflectance spectrum weak fringes will be detected in the infrared and in part of the visible range of the energy spectrum [100].

3.5 Current-Voltage (I-V) and Capacitance-Voltage (C-V) measurements by Mercury-probe

I-V measurements are used mainly to determine the conductivity of the epilayer, while C-V measurements are needed to calculate the amount of net carriers in the material. This may be done if a Schottky contact is applied on the epilayer by depositing a metal (Ni, Au, Cr, Mo, …), and an Ohmic contact on the backside of the substrate is made by depositing one metal or more or by simply putting a silver paste. A quicker and non destructive way consists in using mercury (Hg) for both contacts but of different size (bigger for the Ohmic), both can be realized on the epilayer surface.

When the current is measured at different voltages, electric characteristics of the epilayer can be extracted. Forward voltage characteristics show the series resistance existing in the material and its on-set voltage. Reverse voltage characteristics give information on leakage current and breakdown voltage.

In case of C-V measurements, once the conductivity and reverse voltage range (low leakage current) has been determined by I-V measurements, a reverse voltage is applied between the two contacts and the capacitance is measured. In this way the carriers are depleted and a depletion region of a certain width is formed and, by using some typical parameter (dielectric constant of the measured material, reverse bias used in the measurement, temperature and area of the contacts), the net doping concentration and its depth profile can be estimated [101].

Mercury is liquid and can easily be withdrawn from the epilayer. After the measurement the epilayer can be cleaned and used for further characterization and processing, although there are some controversial arguments on the possibility to completely remove mercury from the SiC surface.

The net doping concentration measured by Hg-probe is due to the amount of electrically active dopants incorporated in the material.

4

Main results

What we have "baked"…

In the work described in this thesis we have explored many of the borders related to the epitaxial growth of SiC. It has been done with the chloride-based CVD process in order to get as much as possible, in terms of achievable growth rates but also in opening the possibility to grow under very unusual conditions, which would not have been the case without adding chlorine in the gas-mixture.
The main topics of this study have been: the growth of SiC epilayer on substrates with different off-cut angles, with a focus on the *in situ* etching and growth parameters (Paper 1 to 5); the growth at unusual conditions, such as very low carrier gas flow (Paper 5) or very low temperature (Paper 6 and 7); the attempt of bulk growth at a much lower temperature than usual (Paper 8).
In short details the papers included in this thesis present the following results.

Paper 1: On-axis 4H- and 6H-SiC Si-face substrates were used to perform epitaxial growth with the $SiH_4 + C_2H_4 + HCl$ chemistry. Very high Cl/Si ratios and low C/Si ratios, rendering a Si-rich gas phase, resulted in the growth of 100 μm thick homoepitaxial layers at a rate of 25 μm/h. The effect of gas-phase chemistry and real off-angle of the substrate on the growth mechanism and 3C-SiC inclusions formation are discussed in detail.

Paper 2: Further experiments on on-axis 4H-SiC substrates were done. An accurate comparison between two different precursors approaches ($SiH_4 + C_2H_4 +$ HCl and MTS) and their growth efficiency along the susceptor length was performed. The introduction of a Si-rich *in situ* treatment of the surface combined with the MTS-chemistry lead to the achievement of a 100 μm/h growth rate.

Paper 3: The growth on 4° off-axis 4H-SiC substrates was studied in order to obtain high quality epitaxial layers with a smooth morphology. The standard process and the one with HCl addition were developed both resulting in the growth of step-bunch free epitaxial layers, but at different rates: 3 μm/h with the standard chemistry, and 28 μm/h with chloride-based chemistry. In both cases the C/Si ratio and temperature effects on the growth mode were changed similarly, and their effect is discussed in the paper.

Paper 4: A more detailed *in situ* etching procedure was developed for the epitaxial growth on 4° off-axis 4H-SiC substrates. An etching step with HCl at a higher temperature than that used for the epitaxial growth allowed chloride-based CVD to be performed at high growth rates (> 100 μm/h), without introducing step-bunching or triangular defects into the epilayer. The effects of surface preparation and growth temperature on the epilayer morphology are discussed.

Paper 5: A very low carrier flow (1/10 of the standard value) CVD process was developed on different off-cut substrates. A detailed study on the gas dynamics in the reaction chamber, setting different flows, pressure, reaction chamber heating and process parameters was performed. Growth rates up to 50 μm/h and excellent thickness uniformity on a 50 mm diameter wafer area were achieved. The effect of using different off-cut substrates (nominally on-axis, 4° and 8° off-axis) and the required different growth parameters for each of them were discussed.

Paper 6: Chloride-based growths at temperatures as low as 1300 °C were performed with two different precursors approaches (SiH_4 + C_2H_4 + HCl and MTS). The gas phase chemistry was quite different; MTS was more efficient and successful to grow high quality homo-epilayer on 8° off-axis substrates at a rate of 13 μm/h. High Cl/Si ratios were required to grow at such low temperatures. An accurate discussion on the different gas phase chemistry between the two precursor approaches is reported.

Paper 7: Low temperature CVD on 6H-SiC Si-face on-axis substrates was investigated with the SiH_4 + C_2H_4 + HCl chemistry. Several growth parameters were tested and finally very high quality single-domain 3C-SiC layers could be grown. A temperature of 1350 – 1400 °C, C-rich surface preparation, Si-rich growth conditions were needed to grow high quality 3C-SiC. If nitrogen was added during the growth single-domain 3C-SiC could be deposited.

Paper 8: The chloride-based process was used in a vertical hot-wall reactor at moderately high temperatures (1700 – 1900 °C) achieving growth rates of 300 μm/h and demonstrating that a bulk growth process is feasible at such temperatures. Different precursor approaches and substrate off-cuts were investigated and widely discussed. Limits in the growth process were due to the reactor geometry, but the overall results were quite promising to stimulate further research.

There are many important conclusions which can be deduced from this work.

- Substrate off-angle: It is possible to grow at high growth rates even on on-axis substrates, but the lower the off-angle, the more Si-rich conditions are needed (either in the gas-phase or in the *in situ* etching step)

- Surface preparation: it is a fundamental step which can never be neglected in CVD. Depending on the aim of the growth process and the substrate available, a proper *in situ* etching has to be performed.

- The growth temperature has obviously a great impact on the CVD process. As a rule of thumb, by increasing the temperature it is possible to use a wider range of parameters, and therefore to achieve higher growth rates.

- Chlorinated precursors are more efficient than the simple addition of chlorine to the gas mixture. The main intermediates which are formed in the gas phase are more efficient in bringing silicon to the surface, higher growth rate and better morphology control can be achieved.

- Cl/Si ratio allows growing SiC in a very broad window of conditions. The lower the temperature the higher the chlorine input has to be. 3C is affected by chlorine and probably etched at a different rate than the hexagonal polytypes. It affects the overall gas phase chemistry; the real C/Si ratio arriving on the substrate surface depends on the amount of chlorine in the gas phase.

In conclusion we have demonstrated that the chloride-based CVD is probably the best process to use for the epitaxial growth of SiC. High growth rates on different substrate off-angles and a very wide window of growth parameters are the main advantages of this technique. Thick epilayers for power devices can easily be grown in this way with a very efficient growth process.
The next bulk growth technique for SiC crystal could be based on the chloride-based CVD process.

Chlorine addition is beneficial for the epitaxial growth of SiC.
The same statement is not valid for baking a good pizza.

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