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Editorial Manager(tm) for Analog Integrated Circuits and Signal Processing
Manuscript Draft

Manuscript Number: ALOG1598

Title: Power Consumption of Analog Circuits - a Tutorial

Article Type: Manuscript

Keywords: Low power design; fundamental limits; dynamic range; technology scaling; analog building blocks

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Analog Integrated Circuits and Signal Processing manuscript No.
(will be inserted by the editor)

Power Consumption of Analog Circuits - a Tutorial

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Received: date / Accepted: date

Abstract A systematic approach to the power consumption of analog circuits is presented. The power consumption is related to basic circuit requirements, as dynamic range, bandwidth, noise figure and sampling speed and is considering basic device and device scaling behavior. Several kinds of circuits are treated, as samplers, amplifiers, filters and oscillators. The objective is to derive lower bounds to power consumption in analog circuits, to be used as design targets when designing power-constrained analog systems.

Keywords Low power design · fundamental limits · dynamic range · technology scaling · analog building blocks

1 Introduction

Power consumption is a very critical issue in modern electronic systems. For digital systems, power consumption research during the early 1990ies has lead to a very good understanding of this issue, and to good methods and tools for power savings [1],[2]. Analog systems are far more complicated, and there has been less dedicated research on the power consumption of analog circuits. Instead, textbooks concentrate on performance requirements rather than on power consumption as the primary design goal. We will here make an attempt to treat power consumption in analog circuits in a systematic way, with the objective to complement present performance-centric design methods with power-centric design techniques. An important element in a systematic treatment is to derive lower bounds to the power consumption of a circuit with defined task and performance. Such a lower bound can then be utilized as a design target for any low-power analog design task. It can also be used for the estimation of power consumption in early system design, or for comparisons between different approaches to solve a specific signal processing problem.

Eric Vittoz pioneered low power techniques already 1980 [3] and presented the first analysis of power consumption in analog circuits some 10 years later [4], [5]. This analysis of power consumption in analog circuits was further developed by Enz and Vittoz in [6]. Later, Bult [7] and Annema et. al. [8] looked into the effect of scaling on analog power consumption, an analysis which Bult then developed into a more comprehensive analysis of analog power consumption [9, (chapter by Bult)]. In addition, power issues in designing radio frequency circuits and systems has been discussed in [10] and [11]. More recently, Sundström, et. al., presented a more quantitative analysis of the lower power bounds in analog-to-digital converters [12]. The present work follows many of the ideas developed in [8], but aims at a more quantitative analysis with the objective to define lower power bounds related to requirements, as in [12].

As an introductory example, let us study the power consumption of an ideal sampler (sample-and-hold circuit) [4]. An ideal sampler will follow an analog signal and then sample and hold its value for a period of time. The main performance measures are sampling rate (number of sampling instances per unit time) and

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dynamic range (the signal-to-noise ratio at maximum input signal). Other performance measures are accuracy and signal bandwidth, which will be discussed later. See Figure 1. When the switching transistor is open, the noise voltage at the output can be estimated to ("classical kT/C-noise", assuming the only noise source being the amplifier output resistance and switch series resistance):

$$v_{nS}^2 = \frac{kT}{C_{Sn}}. \tag{1}$$

Assuming a full scale voltage (peak-to-peak voltage) at the input of V_{FS} will allow a maximum rms sine voltage of

$$v_s = \frac{V_{FS}}{2\sqrt{2}}. \tag{2}$$

This gives a dynamic range of the circuit of D:

$$D = \frac{v_s^2}{v_{nS}^2} = \frac{V_{FS}^2 \cdot C_{Sn}}{8kT} \tag{3}$$

In order to meet a certain D requirement, we thus need a capacitor C_{Sn} of

$$C_{Sn} = \frac{8kTD}{V_{FS}^2} \tag{4}$$

In order to charge this capacitor in time T to the full scale voltage V_{FS} we need a charging current of $I = C_{Sn}V_{FS}/T$. With a sampling frequency of f_s, we may assume that we use half a sampling period for capacitor charging, $T = 1/2f_s$. Finally, assuming that we have an ideal amplifier, with maximum output current equal to the supply current and maximum output voltage equal to supply voltage, we may calculate the power consumption of the sampler:

$$P_{Sn} = IV_{FS} = 16kTf_sD \tag{5}$$

This formula gives some insight in analog power consumption. We note that it is proportional to the dynamic range of the signal and the sampling rate (or signal bandwidth). The fact it is proportional to kT indicates that it is bounded by thermal noise. Furthermore, we note that this expression is independent of which technology is used.

So, what happens at very low dynamic ranges? Then the capacitance becomes very low. What can happen is that C_{Sn} in eq. (4) becomes lower that what can be implemented in a given technology. We thus need to replace C_{Sn} in the above formulas with C_S:

$$C_S = \max(C_{Sn}, C_{min}), \tag{6}$$

where C_{min} is the smallest capacitor which can be implemented. So, for low dynamic ranges, the power consumption will be technology dependent through C_{min} and V_{FS}:

$$P_{ST} = 2f_sC_{min}V_{FS}^2 \tag{7}$$

We may note that P_{ST} is strongly scaled with MOS technology, as both C_{min} and V_{FS} are scaled with feature size in new technology nodes. This is then very similar to the digital case, where power is proportional to CV_{dd}^2. See also Figure 2. This introductory example gives some basic insights in the lower bound for power consumption of analog circuits. We will come back to similar results later. In the following we will start to look at the transistor in section 2. We then discuss OTA and feedback in section 3, a single pole filter in section 4, and a comparison between a digital and an analog filter implementation in section 5. In section 6 we continue with low noise amplifiers and then we finish the circuit studies with voltage controlled oscillators in section 7. We finalize our paper with a discussion in section 8 and a conclusion, section 9.

2 The Transistor

Let us consider a simple transistor circuit, as in Figure 3. As in the above example, we start to look at the thermal noise. For an MOS transistor we normally express the drain noise current in terms of transistor transconductance, g_m as:

$$i_{dn}^2 = 4kT\gamma g_m B_n, \tag{8}$$

where γ is a noise factor (2/3 for a long channel MOS) and B_n is the system noise bandwidth [13]. In the following we neglect noise contributions from other sources than the transistor drain current (as the drain current noise normally dominates). The output noise voltage, v_{dn} will be $v_{dn}^2 = R^2 i_{dn}^2$. Again, assuming that the output full scale voltage is V_{FS}, corresponding to a maximum output as eq. (2), we may express the dynamic range, D, as:

$$D = \frac{v_s^2}{v_{dn}^2} = \frac{V_{FS}^2 \cdot g_m}{32kT\gamma A_v^2 B_n}, \tag{9}$$

where we introduced the DC gain of this stage, $A_{v0} = g_mR$. From eq. (9) we may now calculate the g_m needed to reach the dynamic range, D:

$$g_m = \frac{32kT\gamma A_{v0}^2 B_n}{V_{FS}^2} D. \tag{10}$$

To achieve a certain transconductance, g_m, we need to supply the transistor with a bias current $I_D = g_m V_{eff}$,

where we have introduced the parameter V_{eff} (of the order of 50 mV to 1 V, see below). Using I_D together with the supply voltage, again assumed to be V_{FS}, we can calculate the power consumption as:

$$P_{Tn} = 32kT\gamma A_{v0}^2 B_n \frac{V_{eff}}{V_{FS}} D \tag{11}$$

We may note large similarities to eq. (5), particularly considering the close relation between sampling frequency, f_s, and bandwidth, B_n.

Quite often the transistor will have a capacitive load. Assuming the circuit in Figure 3 has a capacitive load of C_{Ln} in parallel to R we have $B_n = 1/4RC_{Ln}$ (noise bandwidth of a single pole low-pass filter). Inserting this expression into eq. (9) gives the dynamic range:

$$D = \frac{V_{FS}^2 \cdot C_{Ln}}{8kT\gamma A_{v0}}, \tag{12}$$

where we again used $G = g_m R$. Then we need to choose C_{Ln} to meet the dynamic range requirement:

$$C_{Ln} = \frac{8kT\gamma A_{v0}}{V_{FS}^2} D \tag{13}$$

which is quite similar to eq. (4). In this case we need to consider the speed requirement in order to estimate power consumption. With a required gain of $A_{v0} = g_m R$ and bandwidth of $B = 1/2\pi RC_{Ln}$ we will have a requirement on g_m as:

$$g_m = 2\pi C_{Ln} A_{v0} B = \frac{16\pi kT\gamma A_{v0}^2 B}{V_{FS}^2} D, \tag{14}$$

which is the same expression as eq. (10) above (considering the difference between B and B_n). Therefore we will also have the same power consumption as above (eq. (11)).

We may also note that we have a possible scheme for low power design here. The required dynamic range sets a capacitance value (just as for the sampler). By then adding a gain and bandwidth requirement, we may set a value of g_m, which in turn leads to the (minimum) power consumption.

Let us now discuss the various parameters involved in the above discussion. Starting with V_{eff}, this parameter is just defined by [12]:

$$V_{eff} = \frac{I_D}{g_m}. \tag{15}$$

For a classical long channel MOST in strong inversion $V_{eff} \approx (V_G - V_T)/2$, where V_G and V_T are the gate voltage and threshold voltage respectively. For weak inversion, that is for $V_G < V_T$, $V_{eff} = mkT/q$, with m slightly larger than 1. For a modern submicron MOST V_{eff} tends to fall above these values, see Figure 4 [12].

Regarding γ, its value is 2/3 for a long channel MOST, whereas it is larger, 1.5 - 2, for a submicron device [13].

Returning to V_{eff}, from the above formulas (eq. 11) we can conclude that a small V_{eff} is preferred to save power. But, there are some constraints in how to choose V_{eff}. First, transistor speed depends on gate bias, so a low V_G (and low V_{eff}) will lead to reduced speed.

One measure of transistor speed is f_T, the frequency at which the transistor current gain equals unity. In Figure 5 we show typical values of f_T versus gate voltage for two process nodes. Compare Figure 4. We note quite a difference here between the two processes; in the 350-nm process we need to keep quite a large V_{eff} in order to keep transistor speed, however for the 90-nm process we do not gain much speed above $V_G \approx 100$ mV, corresponding to a $V_{eff} \approx 100$ mV.

Another constraint is related to input voltage amplitude. If the input voltage amplitude is large compared to V_{eff}, then we can expect a highly nonlinear response of the transistor. Without going too deep into nonlinear behaviors here, let us just conclude that for an input voltage swing of $V_{FS,in} = V_{eff}$ (where $V_{FS,in}$ is the peak-to-peak gate voltage), the transistor current will vary roughly between $I_{DC}/2$ and $3I_{DC}/2$ (assuming g_m constant in this region; I_{DC} is the DC drain bias). Thus limiting the input peak-to-peak swing to V_{eff} is a reasonable first attempt to relate V_{eff} to input swing.

A few final notes on the transistor. In the above text we assumed that the maximum output voltage swing, V_{FS} is equal to the supply voltage, V_{dd}. If this is not the case, it follows from the derivation of eq. (11) that the power consumption will increase by $1/\eta_v = V_{dd}/V_{FS}$, where we define η_v as the voltage efficiency. In a similar way, we may define a current efficiency $\eta_i = I_D/(I_D + I_b)$, where I_b is the current consumption of a possible bias circuit, needed to support the transistor with proper bias. It is important to note that also I_b may need to be chosen in such a way that the noise level meets the requirements. With these definitions, the power consumption will thus increase by $1/\eta_v \cdot \eta_i$.

Transistors are often used in a differential configuration, Figure 6. Let us combine two identical transistor stages (Figure 6 a) into one differential stage (Figure 6 b). The differential input voltage is then $2v_i$ and the differential output voltage $2v_0$. The output noise voltage squared will be $2v_{dn}^2$. As a result the differential circuit will have a dynamic range of

$$D_{diff} = \frac{(2v_0)^2}{2v_{dn}^2} = 2\frac{v_0^2}{v_{dn}^2} = 2D_{single}. \tag{16}$$

In the same time the power consumption is doubled, as we have two identical stages. However, if we now reduce each supply current in half, thus keeping the same power consumption, then we will also keep the dynamic range, as D is proportional to g_m and therefore to supply current (at fixed V_{eff}, eq. (9)). So, we can conclude that eq. (11) is valid also for a differential circuit. We may note that also the single stage capacitance is halved in a differential circuit, thus making the total capacitance the same. Another issue is current re-use, meaning that a bias current may be used by more than one transistor. An excellent example is the inverter amplifier, where one NMOS and one PMOS transistor contributes to the transconductance utilizing the same bias current, Figure 7 a). Here, both transistors contribute to g_m, so the total transconductance is $G_m = g_{mn} + g_{mp}$. The supply current is given by $I_{DC} = g_{mn}V_{effn} = g_{mp}V_{effp}$ making the supply current equal to:

$$I_{DC} = \frac{G_m}{\frac{1}{V_{effn}} + \frac{1}{V_{effp}}}. \quad (17)$$

So, for a given transconductance, we can expect only half of the power consumption compared to a single transistor stage. Another example of current reuse is the cascode stage (Figure 7 b), where one common source stage and one common gate stage share the same supply current. A cascade stage therefore has no power cost (except that it may reduce the voltage swing, thus reducing the voltage efficiency).

Now, do we have a technology effect similar to the minimum capacitor constraint described in the introduction? Of course, also here we have a minimum capacitance, C_{min}, corresponding to the minimum node capacitance which can be implemented in the particular technology used. We should then replace C_{Ln} in eq. (14) with $C_L = \max(C_{Ln}, C_{min})$. If C_{Ln} is the largest, power consumption is given by eq. (11); if C_{min} is the largest it is given by

$$P_{TC_m} = 2\pi C_{min} V_{eff} V_{FS} A_{v0} B. \quad (18)$$

Note that in the differential case each transistor requires C_{min}, so the total power will double compared to the single ended case when C_{min} controls power.

We may now give a more detailed scheme how to design a circuit with minimum power consumption. Starting with the dynamic range requirement, we calculate C_{Ln} from eq. (13). We then compare to C_{min} and choose $C_L = \max(C_{Ln}, C_{min})$. Then we calculate the required g_m from eq. (14). Next, we need to decide on V_{eff}. V_{eff} is constrained by the input voltage swing (which is a part of our requirements) and by f_T. f_T needs to exceed the gain-bandwidth product of the circuit, $A_{v0}B$. This can be concluded from the following argument. We expect that the drain capacitance, C_d, is somewhat lower than C_g, but follows C_g with changing transistor size (width; we assume length constant). In the same time we expect that the drain capacitance must be smaller than C_L, as it is a part of C_L. In conclusion, we expect that C_g must be smaller than C_L. Furthermore, $f_T = g_m/2\pi C_g$ (by definition). Inserting g_m from eq. (14) and $C_g < C_L$ we arrive to $f_T > A_{v0}B$.

So, V_{eff} thus have a lower bound given by V_{FSin} or $A_{v0}B$, whichever give the largest bound. Choosing V_{eff} equal to this lower bound gives minimum current consumption for achieving the required g_m calculated from eq. (14). Finally, we should strive for the largest possible voltage and current efficiencies (η_v and η_i), finally arriving to a minimum power solution meeting our requirements (D, B, A_{v0}, V_{FS} and V_{FSin}).

An interesting issue in this context is the effect of technology scaling. First considering the capacitance choice, it is in fact very similar to the sampling case. Either C_L is limited by the dynamic range (eq. (13)), or by C_{min}. In the first case, power consumption is given by eq. (11), in the second case by eq. (18), see also Figure 2. In the first case the power consumption is proportional to V_{eff}/V_{FS}, which is relatively independent of the process. Both voltages are expected to scale with the smallest feature size. However, for deep submicron processes V_{FS} tend to scale faster than V_{eff}, which may lead to an increased power with smaller devices (as pointed out in [8]). For the second case, we have a strong scaling effect as power is proportional to $C_{min}V_{eff}V_{FS}$, which is very similar to the sampling case (eq. (7)) and to the digital case, $C_{min}V_{dd}^2$.

3 OTA and Feedback

We will use a simple operational transconductance amplifier (OTA) as prototype stage for various circuit applications. A simple OTA could be just a differential stage as in Figure 6 b). Such a stage often has too low voltage gain due to a too low output impedance. It can be improved by adding a cascode stage, as in Figure 7 b, or by adding a second gain stage, as in Figure 8. For the first two cases, the above single transistor formulas are mainly valid. For the two-stage case, the first stage has a voltage gain of $A_{v1} = g_{m1}R_{L1}$ and the second stage has a transconductance of g_{m2}. Together we have a transconductance of $G = A_{v1}g_{m2}$. The output noise current of the OTA can be expressed:

$$i_{on}^2 = 4kT\gamma B g_{m1} R_{L1}^2 g_{m2}^2 + 4kT\gamma B g_{m2}, \quad (19)$$

where the two terms represents the contributions from the first and second stage respectively. The second term

divided by the first term can be expressed as $g_{m1}/(A_{v1}^2 \cdot g_{m2})$, indicating that this term may be discarded if the voltage gain in the first stage can be made high. So, if we have a reasonable voltage gain in the first stage, a lower g_{m2}, and therefore a lower bias current, is required for the second stage. On the other hand, there may be other requirements, controlling g_{m2} instead of noise. We will come back to these issues later. Let us now put the OTA into a feedback configuration, see Figure 9. It is easily shown that the voltage gain of this configuration is given by

$$A_v = \frac{v_o}{v_i} = -\frac{GZ_f - 1}{GZ_i + 1} \tag{20}$$

which for large G becomes $-Z_f/Z_i$. Note that for relatively large voltage gain, the input voltage swing is considerably smaller than V_{FS}, just relaxing the requirement on V_{eff}, which may save power. We may also use this expression for the case $Z_i = 0$ for which $A_v = -(GZ_f - 1)$. We may also calculate the output impedance for this stage:

$$Z_{out} = \frac{Z_i + Z_f}{1 + GZ_i} \tag{21}$$

and its input impedance:

$$Z_{in} = Z_i + \frac{1}{G}. \tag{22}$$

Let us now apply these results on a switched C amplifier with fixed voltage gain, A_{v0}. We are only interested in the relation between amplifier performance and power consumption here, so we therefore disregard switching schemes, switches, offset compensation schemes, etc.. We can then just replace the impedances with capacitors in the above expressions. The voltage gain is thus given by (from eq. (20) with Z_x replaced by $1/sC_x$):

$$A_{v0} = -\frac{C_i}{C_f} \tag{23}$$

and the output admittance in the Laplace domain:

$$Y_{out} = s\frac{C_i C_f}{C_i + C_f} + G \cdot \frac{C_f}{C_i + C_f}, \tag{24}$$

which is the same results as derived for a single stage amplifier in [12].

Following the scheme discussed in section 2, we start to calculate the output noise voltage from eq. (19):

$$v_{on}^2 = 4kT\gamma \cdot B_n g_{m1} R_{L1}^2 \cdot g_{m2}^2 \alpha R_L^2, \tag{25}$$

where we have introduced $\alpha = 1 + g_{m1}/A_{v1}^2 g_{m2}$, indicating the effect of the second stage noise. By comparing to our earlier results we note that by making $\alpha = R_{L1} g_{m2} = 1$ eq. (25) is valid also for single stage amplifiers. Introducing the noise bandwidth in this case, $B_n = 1/(4R_L C_L)$ we arrive to:

$$v_{on}^2 = \frac{kT\gamma}{C_L} \cdot \frac{C_i + C_f}{C_f} \cdot g_{m2} R_{L1} \alpha, \tag{26}$$

where we used the real part of eq. (24) as R_L and the imaginary part as C_L. Introducing the required dynamic range, as above, we may then arrive to a required capacitance

$$C_{Ln} = 8kT\gamma(C_i + C_f) \cdot g_{m2} R_{L1} \cdot \frac{\alpha}{C_f V_{FS}^2} \cdot D, \tag{27}$$

which expression is similar to eq. (13). Again, making $\alpha = R_{L1} g_{m2} = 1$ eq. (27) is valid for single stage amplifiers.

Next is to relate this expression to speed. As we are discussing a switched-C amplifier, settling time, related to sampling rate, may be a better parameter than bandwidth. We consider our amplifier to be dominated by the output pole with time constant $\tau = R_L C_{Ln}$ where R_L is found from eq. (24) . For a single pole amplifier, we expect the output to settle within 90% of its final value within the settling time $T_{se} = \tau \ln 10$. Starting with a single stage amplifier and following [12],we have with this criterion

$$g_m = (1 + \frac{C_i}{C_f})\frac{\ln 10}{T_{se}} C_{Ln}, \tag{28}$$

requiring a supply current of $I_D = g_m V_{eff}$. We also need to consider slewing, that is before entering the linear behavior the output voltage of the amplifier may be controlled by the maximum output current, I_D. The worst case slewing time, T_{sl}, is given by:

$$T_{sl} = \frac{C_{Ln} \cdot V_{FS}}{I_D}. \tag{29}$$

Let us set the total time for slewing and settling, $T_s = T_{sl} + T_{se}$ and note that I_D is the same for both criteria. We can then calculate I_D from these expressions:

$$I_D = \frac{V_{FS} C_{Ln}}{T_s} \cdot \left(1 + (1 + \frac{C_i}{C_f}) \cdot \frac{\ln 10 \cdot V_{eff}}{V_{FS}}\right) \tag{30}$$

Here the first term in the parenthesis corresponds to slewing and the second one to settling. By inserting C_{Ln} from eq. (27) we finally arrive to the current consumption and by multiplying with V_{dd} to the power consumption. Returning to the two-stage case, we have

$$\begin{aligned} G &= \frac{C_i + C_f}{C_f} \cdot \frac{\ln 10}{T_{se}} C_L \\ &= \frac{8kT\gamma(1 + \frac{C_i}{C_f})^2 g_{m2} R_{L1} \alpha \ln 10}{V_{FS}^2 T_{se}} D. \end{aligned} \tag{31}$$

As $G = g_{m1}R_{L1}g_{m2}$, eq. (31) reduces to:

$$g_{m1} = \frac{8kT\gamma(1+\frac{C_i}{C_f})^2\alpha\ln 10}{V_{FS}^2 T_{se}}D. \quad (32)$$

which equation is very similar to eq. (14), particularly if we consider that C_i/C_f is the voltage gain and T_{se} is proportional to the inverse of the sampling frequency. From this requirement of g_{m1} we can finally calculate the bias current of the first stage, I_{D1}.

Regarding the second stage, we need to make sure that its noise contribution is low enough, that is α is close to 1, and $g_{m2} \gg g_{m1}/A_{v1}^2$. This can hopefully be fulfilled without power penalty (keeping $g_{m2} < g_{m1}$) with a large enough voltage gain of the first stage. In addition, the second stage has to fulfill the slewing criterion, thus requiring the supply current (see eq. (29))

$$I_{D2} = \frac{C_{Ln}V_{FS}}{T_{sl}}. \quad (33)$$

4 A Single-Pole Filter Realization

Even though we do not intend to extend our tutorial to cover higher-order filters, we would like to touch upon a single-pole realization and what the impact on power dissipation is using our definitions found in the previous chapters.

We continue with the transconductance amplifier, OTA, as outlined in chapter 3, considering only the simplest possible implementation of such an amplifier, the single transistor. For a general transconductance amplifier, the output current is given by

$$i_{out} = g_m \cdot v_{in} \quad (34)$$

and the symbol is shown in Figure 10.

The first-order filter, i.e., the realization of a single, real-valued pole, can be implemented using a combination of transconductance elements together with a capacitor as illustrated in by the single-ended filter in Figure 11. The transconductance-C (or $G_m - C$) filter has the advantage on not relying on a resistance to set the pole, but instead a transconductance which quite often is somewhat simpler to tune. The filter transfer characteristics can be derived by summing the currents floating towards the output node:

$$i_1+i_2+i_C = -g_{m1}\cdot V_{in} - g_{m2}\cdot V_{out} - V_{out}\cdot sC_L = 0. \quad (35)$$

In the Laplace domain, the transfer function, $H(s)$, becomes

$$H(s) = \frac{-g_{m1}}{sC_L + g_{m2}} = -\frac{g_{m1}/g_{m2}}{1+\frac{s}{g_{m2}/C_L}} = -\frac{A_{v0}}{1+s/p_1} \quad (36)$$

from which we identify the voltage gain $A_{v0} = g_{m1}/g_{m2}$ and the real pole at $p_1 = g_{m2}/C_L$. In its simplest implementation the transconductor can be a common-source amplifier as illustrated in Figure 12. The transconductance of this particular topology is then given by the transistor transconductance itself. We assume also that the sketched load is large enough, preferably it is a constant current source, such that the delta current flowing out of the block is well defined. Figure 13 shows the transistor-level implementation of the first-order pole, where we have replaced the components with the corresponding subblocks using NMOS transistors as gain stages.

We start by applying the same reasoning as we did in the previous chapters. The drain noise current in terms of transistor conductance will now be:

$$i_{dn1}^2 = 4kT\gamma g_{m1}B_n \quad (37)$$

and

$$i_{dn2}^2 = 4kT\gamma g_{m2}B_n, \quad (38)$$

where B_n is the bandwidth of the common pole and the total noise current becomes

$$i_{totn}^2 = i_{dn1}^2 + i_{dn2}^2 = 4kT\gamma(g_{m1}+g_{m2})B_n. \quad (39)$$

The noise voltage on the output is determined by the load transconductance (assuming high output impedance in for example current sources if they would be used to form the load):

$$v_{totn}^2 = \frac{i_{totn}^2}{g_{m2}^2} \quad (40)$$

Further on, the noise bandwidth is also given by the filter bandwidth, i.e., $B_n = p_1/4 = g_{m2}/4C_L$. This gives us the following relation

$$\begin{aligned} v_{totn}^2 &= \frac{i_{totn}^2}{g_{m2}^2} = 4kT\gamma\cdot\frac{g_{m1}+g_{m2}}{g_{m2}^2}\cdot\frac{g_{m2}}{4C_L} \\ &= \frac{kT}{C_L}\cdot\gamma\cdot\frac{g_{m1}+g_{m2}}{g_{m2}} = \frac{kT}{C_L}\cdot\gamma\cdot(1+A_{v0}) \end{aligned} \quad (41)$$

where A_{v0} is the filter DC (absolute) gain. The dynamic range - assuming full-swing at the output of the filter - is once again

$$\begin{aligned} D &= \frac{v_s^2}{v_{totn}^2} = \frac{V_{FS}^2/8}{kT\gamma(1+A_{v0})/C_L} \\ &= \frac{V_{FS}^2\cdot C_L}{8kT\gamma(1+A_{v0})}. \end{aligned} \quad (42)$$

To continue our argument, we will revert back the expression by reinserting the pole, $p_1 = g_{m2}/C_L$, since from a filter design point of view, our specification points

are p_1 and A_{v0}. The dynamic range can therefore be expressed as:

$$D = \frac{V_{FS}^2 \cdot C_L}{8kT\gamma(1+A_{v0})} = \frac{V_{FS}^2 \cdot g_{m2}}{8kT\gamma(1+A_{v0})p_1}. \quad (43)$$

We can express the required transconductance as function of the desired dynamic range:

$$g_{m2} = D \cdot \frac{8kT\gamma(1+A_{v0})p_1}{V_{FS}^2} \quad (44)$$

The total current through the two branches, $I_D = I_{D1} + I_{D2}$, is given by

$$\begin{aligned} I_D &= g_{m1}V_{eff} + g_{m2}V_{eff} \\ &= (1+A_{v0})g_{m2}V_{eff} \\ &= 8kT\gamma \cdot (1+A_{v0})^2 \cdot \frac{V_{eff}}{V_{FS}^2} \cdot p_1 \cdot D. \end{aligned} \quad (45)$$

The power consumption can thereby be calculated as

$$P_F = V_{FS} \cdot I_D = 8kT\gamma \cdot (1+A_{v0})^2 \cdot \frac{V_{eff}}{\eta_v V_{FS}} \cdot p_1 \cdot D. \quad (46)$$

This result corresponds well to our previous results. With a higher filter bandwidth, more noise will be integrated and more power needs to be consumed to maintain the dynamic range. For example, for a $\gamma = 1$, a gain of $A_{v0} = 2$, a $V_{eff} = 0.5$ V, a supply voltage of $V_{dd} = V_{FS} = 1$ V, a bandwidth of 1 MHz, and a 60-dB dynamic range, we get the power consumption to be $P_F \approx 25$ nW.

Another, more power efficient solution is to use a PMOS transistor as gain stage in the second stage. Essentially, it boils down to the intuitive solution using a common-source stage with an active resistive load as shown in Figure 14. We can now save some power by re-using the current and we have the same set of derivations bringing us to eq. (44), where g_{m2} is our PMOS transconductance. The difference now though is that the current is given by

$$\begin{aligned} I_D &= g_{m1}V_{eff} = A_{v0}g_{m2}V_{eff} \\ &= 8kT\gamma \cdot (1+A_{v0}) \cdot A_{v0} \cdot \frac{V_{eff}}{V_{FS}^2} \cdot p_1 \cdot D \end{aligned} \quad (47)$$

and the power consumption becomes

$$P_F = V_{FS} \cdot I_D = 8kT\gamma \cdot (1+A_{v0}) \cdot A_{v0} \cdot \frac{V_{eff}}{\eta_v V_{FS}} \cdot p_1 \cdot D. \quad (48)$$

At a first glance, it does not seem to differ much between eq. (46) and (48), however assume we have a unity voltage gain, $A_{v0} = 1$, we will in eq. (46) have a factor 4 from $(1+A_{v0})^2$, and from eq. (48), we get the factor 2 from $(1+A_{v0}) \cdot A_{v0}$. The power consumption is only half compared to the two-stage version. With increased voltage gain, the amount of saved power is less. Analog filters can be characterized by a figure of merit, FOM_F [4]:

$$FOM_F = \frac{P_F}{N \cdot B \cdot D}, \quad (49)$$

where N is the number of poles in the filter, B is its largest bandwidth and D is the dynamic range. Using our eq. (48) above, with $N = 1$, $\eta_v = 1$, $A_{v0} = 1$ and $B = p_1/2\pi$ we can calculate a lower bound to the figure of merit as

$$FOM_F = 32\pi kT\gamma \frac{V_{eff}}{V_{FS}}. \quad (50)$$

Inserting $V_{eff} = V_{FS}$ (for large dynamic range) and $\gamma = 1$ gives a $FOM_F = 4.2 \cdot 10^{-19}$ J. This can be compared to the value estimated by Vittoz [4], $3 \cdot 10^{-20}$ J, very close to our value. Experimental results are considerably larger, in a compilation in [14] we see values from 0.22 fJ to 1.52 pJ. Part of this is caused by low voltage efficiency as $\eta_v = 1$ is not realistic when $V_{eff} = V_{FS}$. Another reason could be that most filter designs utilize large margins for easier specification control.

5 Comparison Between Analog and Digital

Following [4] we will make a simple comparison between a digital and an analog solution to the same problem. Let us thus compare the power consumption of a single pole analog low-pass filter and a single tap digital FIR filter. For the analog filter we use the results from section 4, eq. (46):

$$P_{F,\mathrm{An}} = 8kT\gamma \cdot (1+A_{v0})^2 \cdot \frac{V_{eff}}{V_{FS}} \cdot p_1 \cdot D. \quad (51)$$

For low dynamic range, we will use corresponding expression for $C_L = C_{min}$

$$P_{F,\mathrm{Ac}} = (1+A_{v0})V_{eff}V_{FS}C_{min}. \quad (52)$$

A digital, single-tap FIR filter performs the function $y(i) = a_0x(i) + a_1x(i-1)$, requiring an m-by-n bit multiplier plus an n-bit adder, where we have an m-bit coefficient and n-bit data (assuming $a_0 = 1$). n-bit data corresponds to a dynamic range of $D = 3/2 \cdot 2^{2n}$ [12]. In order to implement these arithmetic units, we need m n-bit adders for the multiplier and one n-bit adder for the adder, a total of m+1 adders. Each adder needs n full adders and each full adder can be implemented by 12 transistor pairs, corresponding to 12 equivalent inverters [15]. The total switched capacitance is then $12 \cdot (m+1) \cdot n \cdot C_{min}$, where C_{min} is the capacitance of

a minimum inverter. The total power consumption of the digital filter can thus be expressed as:

$$P_{FD} = \frac{1}{2}\alpha f_c 12 \cdot (m+1) \cdot n \cdot C_{min} \cdot V_{dd}^2, \quad (53)$$

where we used the standard formula for digital power, $\alpha f_c C V_{dd}^2/2$, where α is the activity (the probability that a node will move in a clock cycle) and f_c is the clock (or sampling) frequency. For a bandwidth of $p_1/2\pi$ we need a sampling frequency (Nyquist sampling) of $f_c = p_1/\pi$ Let us further assume $m = 6$ and $\alpha = 0.1$. We can now perform a quantitative comparison between the two filters, see Figure 15. Here we used $\gamma = 1$, $A_{v0} = 1$, $V_{eff}/V_{FS} = 1$ and $p_1/2\pi = 20$ MHz. For V_{FS} and V_{dd} we used 3 V and 1 V for the 350-nm and 90-nm process, resp. [12]. Corresponding values for C_{min} are 3 fF and 1 fF (Following [12] we use the minimum inverter capacitance also as minimum capacitance in the analog case). From Figure 15 we can note that analog power consumption rises steeply with the dynamic range, whereas the digital power consumption does not. Therefore, the digital filter uses much less power than the analog one for high dynamic range, whereas analog is preferred for low dynamic range. The crossing point is around 50 dB dynamic range in a contemporary process. Also, digital power is considerably reduced by scaling, whereas analog is not, as long as it is above its power floor. We also observe this analog power floor ($P_{F,Ac}$) due to C_{min}, which scales similarly to the digital power consumption. For the 90-nm process we estimate the crossing point between noise-limited capacitance and minimum capacitance at a dynamic range of about 40 dB.

6 Low Noise Amplifiers, LNAs

In the text above we have used the dynamic range as the main design target. In many applications the noise level is instead the main target, as for example in low noise amplifiers (LNAs) for RF frontends or IF amplifiers, or transimpedance amplifiers (TIAs) for optical detectors. We may use an OTA with feedback as prototype amplifier for these applications. A wide-band LNA is obtained by utilizing the circuit in Figure 16 with $Z_i = 0$ and a resistive feedback impedance, $Z_f = R_f$. For an RF LNA we normally need to adjust the input impedance to the source impedance, R_s, thus from eq. (20):

$$G = 1/R_s. \quad (54)$$

By choosing G according to eq. (54) we arrive to

$$A_v = \frac{GR_f - 1}{2} \quad (55)$$

and

$$Z_{out} = \frac{R_s + R_f}{2}. \quad (56)$$

The output noise voltage is found from multiplying the noise current from eq. (19) with the output impedance from eq. (56). Finally we can calculate the noise figure, F as:

$$F = 1 + \frac{v_{on}^2}{v_{sn}^2 A_{v0}^2} = 1 + \frac{\gamma\alpha}{g_{m1} R_s}, \quad (57)$$

where $v_{sn}^2 = 4kTR_sB_n$ is the source noise voltage. So, if we start with a requirement on F we can estimate g_{m1} to:

$$g_{m1} = \frac{\gamma\alpha}{(F-1)R_s}. \quad (58)$$

As we expect both γ and α to be close to 1 (say γ, α about 2), g_{m1} is directly controlled by the required noise figure and R_s. And, from g_{m1} we may estimate the power consumption as before. A further analysis shows that we can fulfill the criteria for G and α by proper choices of g_{m2} and R_{L1} for various values of g_{m1} (within reasonable limits). A similar relation is expected for most LNA topologies [16]. A very simple topology is the single common-gate stage for example, with input impedance $1/g_m$ and a noise figure as eq. (57) without α. We thus need to make $g_m = 1/R_s$ and we will have a fixed noise figure of slightly larger than 2 (3 dB).

So, is it possible to save power further with a given noise figure? On way is to perform a impedance transformation in front of the LNA. With an impedance transformation from R_s to R_s', larger than R_s, we may reduce g_m accordingly and thus save power, see [17]. The transformation can be accomplished through a transformer or via an LC matching network (in the case of a relatively narrow bandwidth). There may be various practical limits to how large transformation which can be accomplished, but it is outside the scope of this paper to go further into this topic. Moving to the other low noise amplifier example, the TIA, it again can be built as an OTA with feedback and $Z_i = 0$. A TIA is normally used to amplify the current (or charge) from a optical detector. In this case the source impedance is capacitive with capacitance C_d, see Figure 17. As above, the input impedance of the TIA is $1/G$ and the gain is expressed as the transimpedance, Z_t:

$$Z_t = \frac{v_o}{i_i} = -R_f(1 - \frac{1}{GR_f}), \quad (59)$$

where GR_f normally is very large making $Z_t = -R_f$. Normally, the pole formed by C_d and Z_{in} dominates this kind of design, why we have a bandwidth of:

$$B = \frac{G}{2\pi C_d}. \quad (60)$$

The output impedance can be found from eq. (21) (in Laplace domain)

$$Z_{out} = \frac{1}{G} \cdot \frac{1 + sR_f C_d}{1 + s\frac{C_d}{G}}. \quad (61)$$

The output noise voltage spectral density is calculated as in eq. (25) with R_L replaced by $|Z_{out}|$. A reasonable assumption is that we only consider the frequency range between $1/2\pi R_f C_d$ and $G/2\pi C_d$, thus using $|Z_{out}| = 2\pi f R_f C_d/G$:

$$S_{von}^2 = \frac{16\pi^2 kT\gamma R_f^2 C_d^2}{g_{m1}} f^2. \quad (62)$$

The full noise voltage is achieved by integrating this expression from 0 to B, thus:

$$v_{on}^2 = \frac{16\pi^2 kT\gamma R_f^2 C_d^2 B^3}{3g_{m1}}. \quad (63)$$

Finally, we calculate the equivalent input noise current by dividing eq. (63) by $|Z_t|^2 = R_f^2$

$$i_{in}^2 = \frac{16\pi^2 kT\gamma C_d^2 B^3}{3g_{m1}}. \quad (64)$$

This is a well known result from optical communications [18], and show again that the noise level is controlled by g_{m1}. In order to meet certain noise requirements, we need to chose a large enough g_{m1}, which is turn will set the power consumption as discussed previously. If we want a very low noise level, we may get into trouble with a too large input capacitance (as the gate capacitance of the input transistor is proportional to g_{m1} if g_{m1} is increased via increased transistor width). We can easily include the transistor input capacitance, C_g, by replacing C_d in eq. (64) with $C_g + C_d$. By further relating g_{m1} to C_g through $g_{m1} = 2\pi f_T C_g$, we find that i_{in2} is proportional to

$$i_{in2} \sim \frac{(C_d + C_g)^2}{f_T C_g}. \quad (65)$$

Changing C_g (through changing transistor width) this expression has a minimum for $C_g = C_d$, again a well known result. It is however quite expensive in power (for a given current noise we need 4 times larger g_{m1} than given by eq. (58)). If we for example instead optimize the target function $i_{in}^2 P$ and note that P is proportional to g_{m1}, there is no optimum, but the target function becomes lower for lower C_g. We also note that large f_T is preferred for low noise (and low power), so we should seek to maximize f_T through proper choice of bias point (V_{eff}) and fabrication process.

This discussion is also valid for so called charge sensitive amplifiers, where R_f is replaced by a capacitor, for example used in X-ray detectors [19].

7 Voltage Controlled Oscillators, VCOs

Voltage controlled oscillators, VCOs, are essential elements in most electronic systems. The most important target requirement on a VCO is its phase noise spectral density, $L(\omega)$. Let us therefore look for a relation between $L(\omega)$ and power consumption for a VCO. We use a simple oscillator model where signal and noise is generated by a transistor noise current, see Figure 18. See also [20]. For simplicity we use a single-ended version here with the expectation that a differential version will have the same power consumption as discussed above (the " -1" block is not needed in a differential version as both signal and its inverted value are available is such circuits). The output voltage spectral density can be expressed as:

$$S_v^2 = \left| \frac{Z_L}{1 - g_m Z_L} \right|^2 S_i^2 = \frac{R_L^2 \omega_0^2}{4Q^2 \Delta\omega^2} \cdot S_i^2, \quad (66)$$

where Z_L is the impedance of the L- R_L- C circuit, g_m is the transistor transconductance and S_i^2 its drain noise current spectral density. The latter transformation assumes that the oscillator barely oscillates ($g_m R_L = 1$) and is only valid for $\Delta\omega > 0$, where $\Delta\omega = \omega - \omega_0$, and ω is the angular frequency and ω_0 is the oscillating angular frequency (resonance angular frequency of the load). Q is the Q-value of the L- R_L- C circuit. Defining the transistor noise current spectral density as before (eq. (8))

$$S_i^2 = 4kT\gamma g_m \quad (67)$$

and the output power as (R_L includes the load to the oscillator and we define the power as the total power into R_L)

$$P_O = \frac{V_{FS}^2}{8R_L}. \quad (68)$$

We can then calculate the relative noise spectral density from eqs. (66), through (68)

$$S(\omega) = \frac{S_v^2}{R_L P_O} = \frac{\gamma kT\omega_0^2}{Q^2 P_O \Delta\omega^2}, \quad (69)$$

where we used $g_m = 1/R_L$. It can be shown that half of this noise is amplitude noise and half is phase noise. We therefore arrive to a phase noise spectral density of

$$L(\omega) = \frac{\gamma kT\omega_0^2}{2Q^2 P_O \Delta\omega^2}, \quad (70)$$

which is the well known Leeson formula [21]. This formula is intuitively very reasonable; the relative phase noise is proportional to the thermal energy (kT) divided by the energy stored in the resonator ($Q^2 P_o$).

Table 1 Examples on reported FOM compared to our bound.

Q	FOM_{osc}, our bound	FOM_{osc}, experimental
0.35	-159 dBm/Hz (-162 dBm/Hz)	-159 dBm/Hz [23]
8	-185 dBm/Hz (-188 dBm/Hz)	-185.5 dBm/Hz [22]

The power consumption, P_{DC}, is now given by $P_{DC} = I_{DC}V_{dd}$, where $I_{DC} = g_m V_{eff}$. Here $g_m = 1/R_L$ (see above) and $V_{eff} = V_{FS}$ as before. Finally we set $V_{dd} = V_{FS}/\eta_v$. Inserting these and eq.(68) into eq. (70) gives the oscillator power consumption

$$P_{DC} = \frac{4\gamma kT}{\eta_v Q^2 L(\omega)\left(\frac{\Delta\omega}{\omega_0}\right)^2}. \tag{71}$$

We note that the VCO power consumption is mainly controlled by η_v and Q for a fixed requirement on $L(\omega)(\Delta\omega/\omega_0)^2$. Lowest power consumption occurs for the largest η_v as usual, that is it is preferable to maximize V_{FS}. Furthermore, high Q resonators are preferable. However, this is not always easily obtained. Integrated inductors normally lead to Q-values of up to about 10 and if we want to avoid the use of inductors, which are very expensive in silicon area, we are left with Q-values below 1 (in RC or ring oscillators).

Let us compare to some experimental results. Following [22] we define an oscillator figure of merit, FOM_{osc} as:

$$FOM_{osc} = L\left(\frac{\Delta\omega}{\omega_0}\right)P_{DC} = \frac{4\gamma kT}{\eta_v Q^2}, \tag{72}$$

where we inserted our theoretical expression. So our lower bound to FOM_{osc} for two Q values are given in Table 1, together with two experimental results. Here we used $\gamma = 1$ and $\eta_v = 1$. The two experimental results represents among the best FOM_{osc} reported. In both cases current reuse is utilized, so we should reduce our theoretical FOM-values by half (-3 dB, in parenthesis). We note that the best experimental results are very close to our predicted values, indicating the usefulness of our prediction.

8 Discussion

The concepts for understanding power consumption in analog systems presented here are based on earlier work by Enz and Vittoz [6] and Bult [9], but also on the more quantitative work on analog-to-digital converters in [12]. The objective is to deepen the understanding of power consumption in analog systems and to introduce lower bounds to the power consumption which can be used as design targets when designing analog systems. We thus hope to offer the analog designer similar powerful tools as earlier available for the digital designer. We also believe that this paper will inspire its readers to further investigate the fundamental limits on performance as a design guidance rather than an obstacle.

As a tutorial, we have concentrated on understanding and only made very few comparisons to experimental results. As the concepts presented here are the same as used in [12], the quite comprehensive comparisons to experiments in [12] are a strong support to our concepts. Also, we have limited our effort to very simple, basic circuits. In practice the task of designing good analog circuitry is much more challenging, including system architecture, choice of circuit topology, choice of transistor bias points, etc. Still, we believe that by applying the concepts presented here, it is possible to adapt established analog design techniques to a power-centric methodology, particularly by utilizing lower power bounds as targets.

Certainly, many important issues are missing in this treatment. One such issue is matching between components (for minimizing offset, gain deviations, etc.). Here we judge that offset compensation is quite easy to implement, limiting the importance of matching. Regarding gain deviations it was found in [12] that its importance in fact is reduced by scaling. Also, various methods of digital error correction are often used, for example in ADCs, to counteract the effect of gain deviations. Of course, there are other impacts on performance due to mismatch such as worse supply rejection. We believe however that this can be catered for by adjusting design specification and tuning of topology.

Another important issue is linearity. There are many different requirements on linearity, depending on the various applications of the analog system. We found it too far reaching to treat this issue here. However, there is a close relation between linearity and the choice of effective transistor overdrive voltage, V_{eff}, and full-scale signal swing, V_{FS}, so we believe that our proposed concepts can be extended to include linearity effects. Also regarding radio frequency circuits our treatment is shallow. But again, we believe that our concepts can be extended to RF circuits by adding a comprehensive treatment of frequency matching networks.

9 Conclusions

We have introduced some basic concepts for understanding power consumption in analog circuits. These concepts are based on basic requirements, the most important being dynamic range (or noise level) and bandwidth (or sampling speed). We demonstrated how the dynamic range requirement sets a lower bound to the

capacitance in the signal path, independent on technology. For lower dynamic range requirements, the minimum capacitance implementable in the actual technology replaces this bound, thus making technology control the capacitance instead of dynamic range. Then next requirement, bandwidth or speed, will introduce a lower bound on the active device transconductance, g_m. To attain this g_m, we need to supply the active device with a bias current, I_{DC}, depending on the required g_m and the gate bias point, expressed as V_{eff}. Finally the lower power consumption bound is given by the supply voltage multiplied by this I_{DC}.

As a part of this scheme we also discussed several additional constraints, as the choice of bias (V_{eff}), signal swing (V_{FS}) and supply voltage. These choices are partly controlled by other constraints as required voltage gain, linearity, etc., and will therefore also influence the lower power bound.

We demonstrated how this scheme or very similar ones can be used to find a lower bound to the power consumption of many types of circuits, as samplers, amplifiers, filters, oscillators or analog-to-digital converters. In some cases our bounds are close to experimental results, in other cases they are not. This indicates large opportunities to further reduce power consumption of several classes of analog circuits.

Finally, we performed a comparison between a digital and an analog solution to the same problem and demonstrated that digital uses less power when high dynamic range is required and analog uses less power for low dynamic range. The crossover point moves towards lower dynamic ranges with process scaling.

Appendix: A Note on Flicker Noise

The flicker noise voltage spectral density on the transistor gate is often expressed as [13]:

$$S_{vgf}^2 = \frac{K_f}{C_g f}, \tag{73}$$

where K_f is the noise coefficient, C_g is the gate capacitance and f is the frequency. By integrating eq. (73) from a lower frequency limit, f_1, to the upper frequency limit (bandwidth), B_n, we arrive to:

$$v_{gf}^2 = \frac{K_f}{C_g} \ln \frac{B_n}{f_1}. \tag{74}$$

This gate noise is then amplified by the transistor to an output noise voltage of $A_{v0} \cdot v_{gf}$. Following the above procedure, we can then calculate the output dynamic range, D, and from that calculate the C_g required for achieving this dynamic range:

$$C_g = \frac{8K_f A_{v0}^2}{V_{FS}^2} \cdot \ln \frac{B_n}{f_1} \cdot D. \tag{75}$$

From this we can calculate g_{mf} through $g_{mf} = 2\pi f_T C_g$, and then estimate the power consumption as in section 2. In the same time we must make sure that we meet the speed requirement of the circuit, that is g_{mL} must fulfill eq. (14), $g_{mL} = 2\pi C_L B A_{v0}$, where C_L should meet the thermal noise and C_{min} requirement, and also accommodate the transistor drain capacitance, C_d, which increases with C_g, if a large C_g is achieved through a large transistor width. These two requirements are met through

$$g_m = \max(g_{mf}, g_{mL}). \tag{76}$$

A possible scheme to manage all these variables could be as follows. Starting with the scheme sketched in section 2, we arrive to g_{mL} (taking into account that C_d related to C_g must be accommodated in C_L). In order not to increase g_m further, we try to keep $g_m = g_{mL}$. The requirement of C_g is then achieved by reducing f_T until C_g is large enough. f_T can be reduced without changing g_m by increasing transistor width and length simultaneously ($g_m \sim W/L$ and $C_g \sim WL$, where W and L are transistor width and length respectively). After finding the appropriate g_m we can estimate the power consumption as in section 2. A possible problem with this scheme is that we decrease f_T of the input transistor when increasing the transistor length, which may give us problems with bandwidth. Also, we increase the input capacitance of the transistor stage, which may affect the power consumption of the previous stage.

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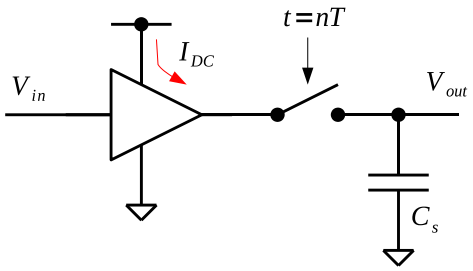

Fig. 1 Simple sampler.

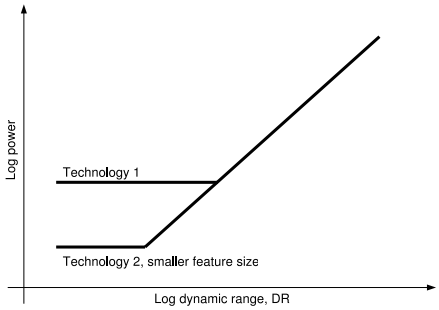

Fig. 2 Power vs dynamic range.

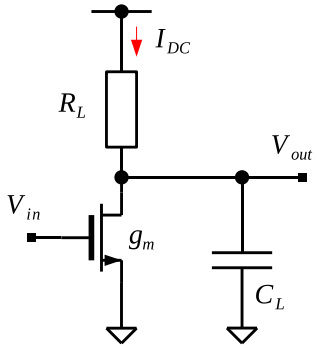

Fig. 3 Simple transistor stage.

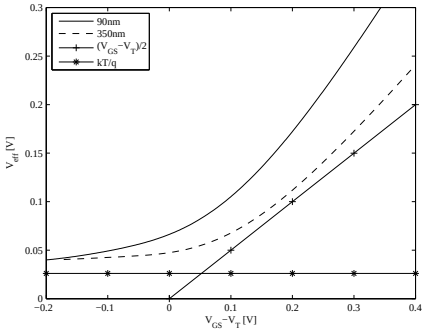

Fig. 4 V_{eff} vs gate voltage for NMOS transistors in two different processes.

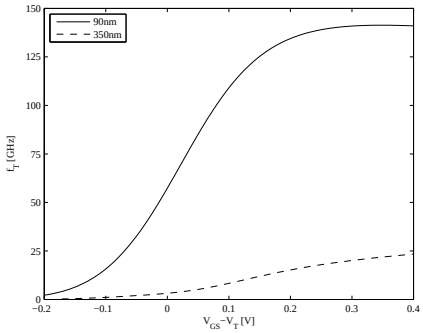

Fig. 5 f_T vs gate voltage for NMOS transistors in two different processes.

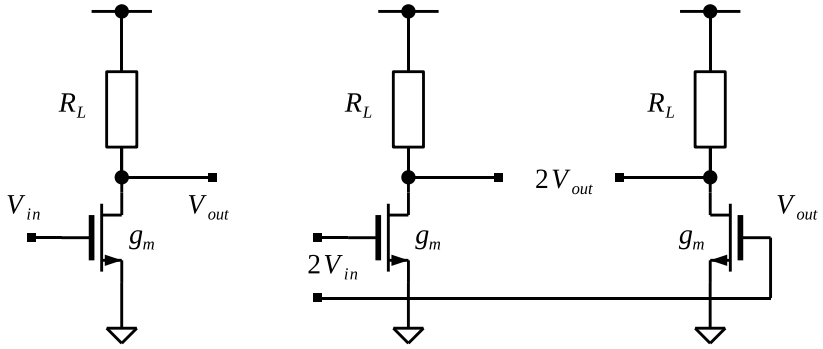

Fig. 6 Comparison of a single-ended and a differential stage.

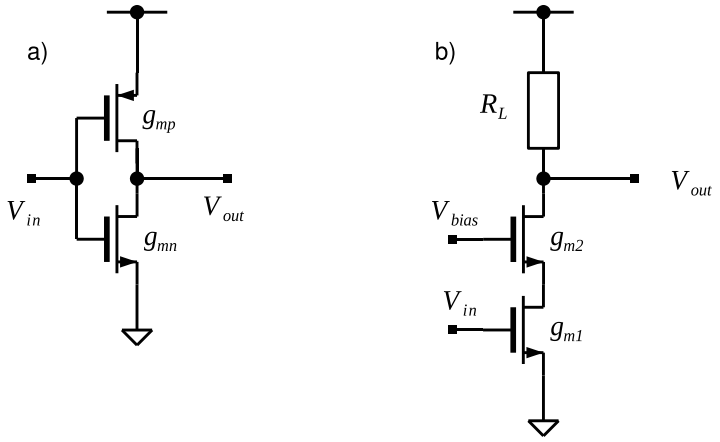

Fig. 7 An inverter (a) and a cascode amplifier (b).

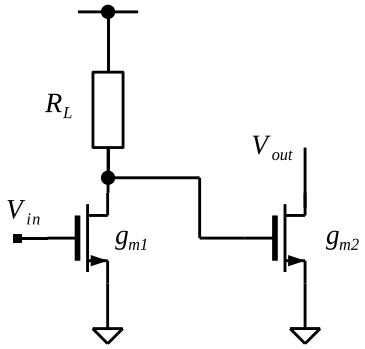

Fig. 8 A two-stage amplifier.

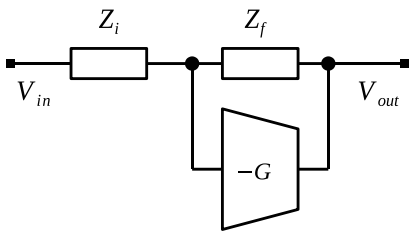

Fig. 9 A feedback operational transconductance amplifier (OTA).

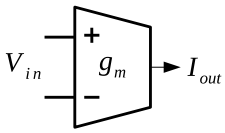

Fig. 10 Transconductance element.

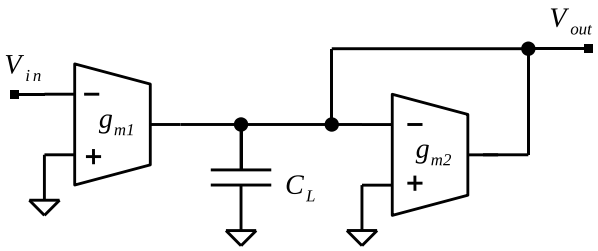

Fig. 11 A single-ended first-order filter

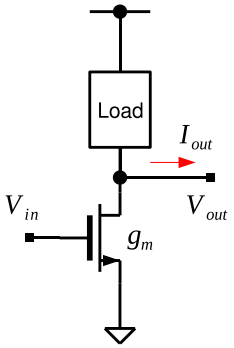

Fig. 12 First-order implementation of the transconductor

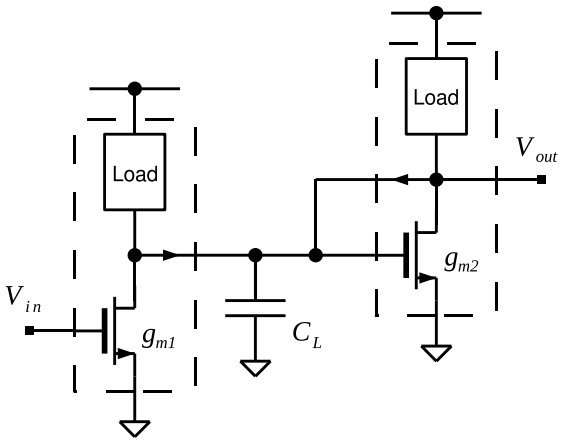

Fig. 13 Transistor implementation of the first-order filter.

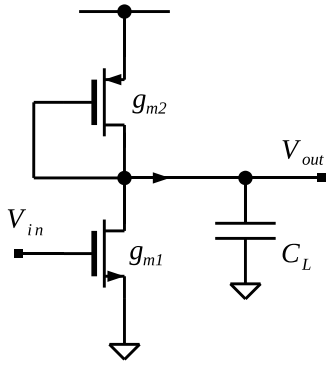

Fig. 14 Current re-use implementation of the single-pole stage

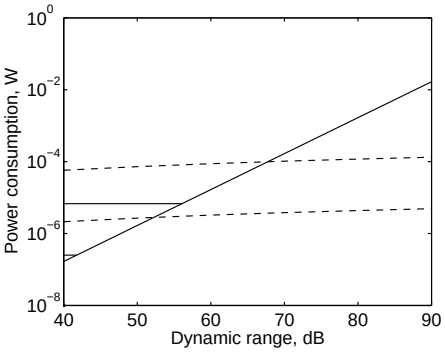

Fig. 15 Power consumption versus dynamic range for an analog (solid) and a digital (dashed) filter. The two horizontal solid lines represent power floors for analog 350 nm and analog 90 nm, respectively.

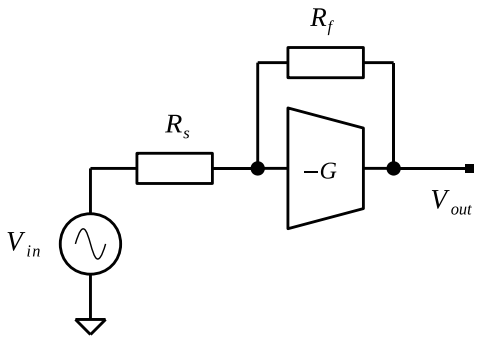

Fig. 16 LNA in resistive feedback configuration, similar to Figure 9, but with $Z_i = 0$, $R_f = Z_f$ and source resistance, R_s included.

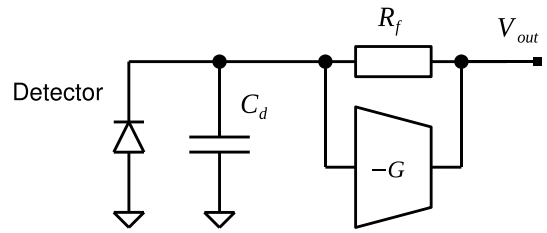

Fig. 17 Transimpedance amplifier (TIA) as low noise optical detector.

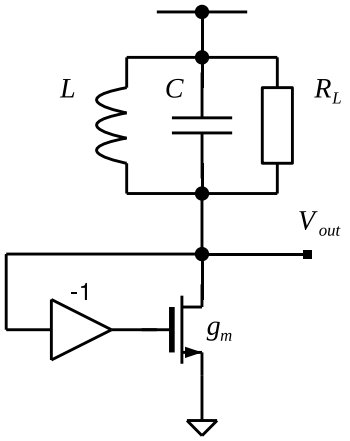

Fig. 18 A voltage-controlled oscillator (VCO).

***Author Biographies**

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Christer Svensson received the M.S. and Ph.D. degrees from Chalmers University of Technology, Gothenburg, Sweden, in 1965 and 1970, respectively. He joined Linköping University, Sweden 1978, where he became Professor in Electronic Devices 1983 and initiated a new research group on integrated circuit design. He pioneered the fields of high-speed CMOS design in 1987, and low-power CMOS 1993. Prof. Svensson was awarded the Solid-State Circuits Council Best Paper Award for 1988-1989. He is a member of the Royal Swedish Academy of Sciences and the Royal Swedish Academy of Engineering Sciences and was awarded Fellow of IEEE 2003.

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Christer Svensson Photo

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