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Role of graphene/substrate interface on the local transport properties of the two-dimensional electron gas

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The electron mean free path (l_{gr}) is "locally" evaluated by scanning capacitance spectroscopy on graphene obtained with different preparation methods and on different substrates, i.e., graphene exfoliated from highly oriented pyrolitic graphite (HOPG) and deposited (DG) on 4H-SiC(0001) and on SiO_2 and epitaxial graphene grown on 4H-SiC(0001) (EG). l_{gr} in DG on SiC was more than four times larger than in DG on SiO_2. The improved mean free path is explained by the higher permittivity of SiC compared to SiO_2, yielding a better dielectric screening of charged-impurities, and by the weaker coupling of graphene two-dimensional-electron-gas with surface polar phonons of SiC. On the other hand, l_{gr} on EG is on average ~0.4 times that on DG-SiC and exhibits large variations from point to point, due to the presence of a laterally inhomogeneous positively charged layer at EG/SiC interface. © *2010 American Institute of Physics*. [doi:10.1063/1.3489942]

Graphene, a planar one-atom thick layer of sp^2-bonded carbon atoms,[1] is the object of many research interests, especially due to its remarkable electronic transport properties making it a potential candidate for "post-Si" technology.[2] Ideally, in a very clean graphene sheet (i.e., with no adsorbed impurities) sufficiently isolated from its environment to be considered free standing, charge carriers can exhibit a giant intrinsic mobility[3] and can travel for micrometers without scattering at room temperature. Indeed, very high values of mobility ($>2\times10^5$ cm^2 V^{-1} s^{-1}) and electron mean free path have been observed in vacuum and at low temperature (5 K) in "suspended" graphene, after a cleaning by current-induced heating.[4] However, graphene for electronics applications is commonly supported by a dielectric substrate (typically SiO_2 or high-κ dielectrics) or by semi-insulating SiC. The values of the electron mean free path and mobility observed in supported graphene layers are usually significantly lower than in suspended ones. So far, graphene on silicon dioxide substrate has shown field-effect mobility ranging from 0.1 to 2×10^4 cm^2 V^{-1} s^{-1}.[5,6]

Several factors affecting the transport of carriers in graphene have been identified and are still under active debate. Carrier scattering with charged impurities[7–15] (either adsorbed on graphene surface or trapped at the interface with the substrate) is typically indicated as one of the main mechanisms limiting mobility of graphene two-dimensional-electron-gas (2DEG). Since charged impurities interact with graphene 2DEG by a screened Coulomb potential, the strength of the interaction is expected to decrease significantly with increasing the permittivity of the substrate and/or of the dielectric layer deposited on graphene. To date, contrasting experimental results have been reported in the literature on the effect of increasing the "environment" permittivity on graphene transport properties. As an example, Jang *et al.*[16] observed an improvement in mobility placing solid ice on the surface of graphene (on SiO_2) due to increased dielectric screening of long-range impurity scattering. On the contrary, Ponomarenko *et al.*,[17] observed no significant changes in carrier mobility, placing graphene on various substrates and in high-κ media. They also suggested that scattering by charged impurities is not the only mechanism that limits the mean free path attainable for substrate-supported graphene. Inelastic scattering by surface polar phonons (SPP) of the substrate[18] has been indicated as an additional mechanism limiting the carrier mobility in graphene. It has been shown theoretically that, due to the polar nature of the substrates commonly used for graphene (like SiO_2 and SiC), a long-range polarization field is associated to the thermally induced lattice vibrations at the surface of the substrate (i.e., the SPP).[18] This field electrostatically couples with the 2DEG, resulting in a sizeable degradation of mobility at room temperature. Recently, the experimental evidence of such SPP scattering at room temperature has been reported, based on temperature dependent transport measurements performed on devices in graphene deposited on SiO_2 substrate.[4] It has also been predicted that for graphene on SiC, the SPP scattering has a weaker effect on the electron mobility than for graphene on SiO_2, due to weaker polarizability of SiC and relatively high phonon frequencies associated with the hard Si–C bonds.[18] However, this beneficial effect of SiC substrate has not been shown experimentally to date.

In this work, "local" measurements of the electron mean free path have been carried out by scanning probe microscopy[6] in graphene on most relevant substrates for electronic applications: (i) graphene exfoliated and deposited on 4H-SiC (0001) (henceforth DG-SiC), (ii) graphene epitaxially grown on 4H-SiC (0001) (henceforth EG-SiC), and (iii) graphene deposited on SiO_2 (henceforth DG-SiO_2). The experimental results have been explained considering significant effects of the substrate permittivity and of substrate SPP on electron dynamics in graphene.

The DG-SiO_2 sample was prepared by mechanical exfoliation of graphene from highly oriented pyrolitic graphite (HOPG) and deposited on 100 nm SiO_2 thermally grown on

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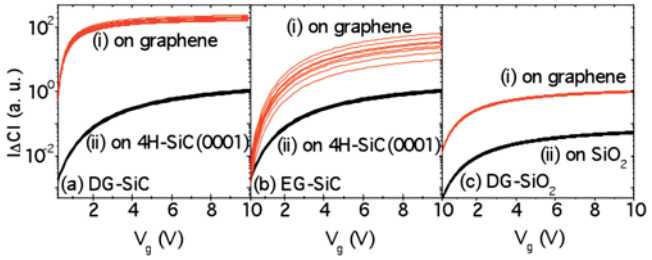

FIG. 1. (Color online) Representative characteristics obtained by SCS on (a) graphene deposited on 4H-SiC(0001) (DG-SiC), (b) graphene epitaxially grown on 4H-SiC(0001) (EG-SiC), and (c) graphene deposited on SiO_2 ($DG\text{-}SiO_2$). Two distinct families of curves correspond to tip placement (i) "on graphene" and (ii) "on substrate" are indicated. A typical scan comprises of an array of 5×5 positions with an interstep distance of 1×1 μm^2.

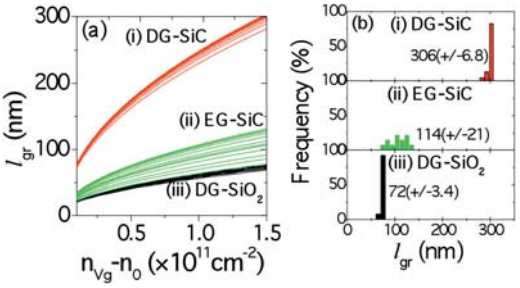

FIG. 2. (Color online) Evaluated electron mean-free path in graphene (l_{gr}) for (i) DG-SiC, (ii) EG-SiC, and (iii) $DG\text{-}SiO_2$ is depicted in (a). In (b) are depicted the corresponding histograms plotted at $n_{Vg}\text{-}n_0=1.5\times10^{11}$ cm^{-2}. An average increase of $>4\times$ and $>1.5\times$ can be seen in l_{gr} for DG-SiC and EG, respectively, as compared to l_{gr} for $DG\text{-}SiO_2$.

degenerately doped n^+ Si. For the DG-SiC sample, the substrate used for graphene deposition was 3.5 μm lowly n-doped 4H-SiC(0001) (concentration $10^{13}-10^{14}$ cm^{-3}) epitaxially grown on n^+ 4H-SiC(0001), whereas EG is prepared on a separate piece of the same 4H-SiC(0001) wafer used for DG-SiC. EG growth was carried out in an inductively heated reactor, operating at a minimal pressure of 5×10^{-6} mbar. The growth temperature was 2000 °C, in a confining Ar pressure of 1 atm to reduce the Si out-diffusion process.[19] We used optical contrast microscopy and atomic force microscopy to identify single layers of graphene (SLG) on $DG\text{-}SiO_2$ and on DG-SiC,[20] while micro-Raman spectroscopy along with conductive atomic force microscopy was used to identify SLG in EG-SiC.[21]

The electron mean free path at room temperature was "locally" evaluated at different positions on the SLG by a recently demonstrated approach based on capacitance measurements made with the probe of a scanning capacitance microscope.[6] In the case of $DG\text{-}SiO_2$, the SiO_2 film works as the gate dielectric and the n^+ Si substrate works as the semiconductor of a metal-insulator-semiconductor capacitor. Notably, the topmost graphene film does not behave as a "classical" metal film, but manifests itself as a capacitor, whose capacitance (the quantum capacitance C_q) adds in series to the insulator and semiconductor capacitance contributions.[22] Similarly, both in the case of DG-SiC and of EG-SiC, the very lowly doped SiC film works as the gate dielectric, whereas the n^+ SiC substrate works as the semiconductor back gate of the capacitor. Capacitance measurements were carried out using a Veeco DI3100 atomic force microscope with Nanoscope V controller and scanning capacitance microscopy (SCM) application module. A Pt coated n^+ Si tip was placed in Ohmic contact with graphene and a modulating bias $\Delta V=V_g/2[1+\sin(\omega t)]$ was applied between the back side of the sample and the tip. Bias amplitude V_g was varied from 0 to 10 V at bias frequency of $\omega=100$ kHz. For each tip position the absolute values of the induced capacitance variation were measured.

In Fig. 1 are reported representative capacitance-voltage characteristics obtained on DG-SiC (a), EG-SiC (b), and $DG\text{-}SiO_2$ (c) on arrays of 5×5 positions with an interstep distance of 1×1 μm^2. For reference, SCS measurements were carried also on bare SiO_2 and SiC regions of the samples. Distinctly higher capacitance values were measured on the graphene/substrate stack than on the bare substrate.[22] The signal measured on the bare substrate is the absolute value of the capacitance variation in a tip/insulator/semiconductor capacitor with area corresponding to the tip contact area A_{tip}. Upon application of a positive bias, an accumulation of electrons is induced in the graphene sheet. These electrons spread over an area A_{eff} around the tip/graphene contact. A_{eff} represents the effective area of the graphene/insulator/semiconductor capacitor and can be evaluated as $A_{eff}=A_{tip}(|\Delta C_{gr}|/|\Delta C_{sub}|)$ where $|\Delta C_{gr}|$ and $|\Delta C_{sub}|$ are the absolute values of capacitance variations measured on graphene/substrate and on substrate not covered by graphene, respectively. A_{eff} is related to the local electron mean-free path (l_{gr}) in graphene by the relation, $A_{eff}=\pi l_{gr}^2$, where l_{gr} is the length over which the electrons diffuse in graphene under biased conditions following "few" subsequent scattering events.[6]

Figure 2(a) shows the evaluated l_{gr} for DG-SiC, EG-SiC, and $DG\text{-}SiO_2$. l_{gr} is reported versus $n_{Vg}\text{-}n_0$, being n_{Vg} the carrier density induced in graphene by the gate bias V_g and n_0 the carrier density at $V_g=0$. The values of $n_{Vg}\text{-}n_0$ are obtained as $n_{Vg}\text{-}n_0=\varepsilon_0\varepsilon_{ins}V_g/(qt_{ins})$, where q is the electron charge, ε_0 is the vacuum permittivity and ε_{ins} and t_{ins} are the relative dielectric constant and the thickness of the insulating layer under graphene. The histograms of the l_{gr} values at a fixed value of $n_{Vg}\text{-}n_0=1.5\times10^{11}$ cm^{-2} are reported in Fig. 2(b). It is worth noting that l_{gr} in EG-SiC is on average 37% of l_{gr} in DG-SiC, but the spread of the l_{gr} values in EG-SiC is much larger than in DG-SiC. These differences can be explained in terms of the peculiar structure of EG/4H-SiC (0001) interface. Both experimental and theoretical studies have shown that EG synthesis on the Si face of SiC occurs through a series of complex surface reconstructions.[23–25] The precursor of graphene formation is a C-rich layer with $(6\sqrt{3}\times6\sqrt{3})R30°$ reconstruction. This layer is an intermediate buffer layer (zero layer) between the Si face of SiC and the first graphene layer, which subsequently grows on it. The ZL may be more or less defective with more or less dangling bonds at the interface with the Si face. Recent nanoscale measurements of the current transport across EG/4H-SiC (0001) interface indicated that a laterally inhomogeneous distribution of positive charge is associated to these dangling bonds between the ZL and the bulk substrate.[21] This interface charge can explain both the lower average value and the larger spread in the local l_{gr} values in the case of EG-SiC than in the case of DG-SiC. It is also worth noting that l_{gr} on DG/SiC is on average $\sim4\times$ than on DG/SiO_2 and the spread of the l_{gr} values are comparable in the two cases. This difference can be explained in terms of the higher permittivity of SiC ($\varepsilon_{SiC}=9.7$) than SiO_2 ($\varepsilon_{SiC}=3.9$) and of the lower

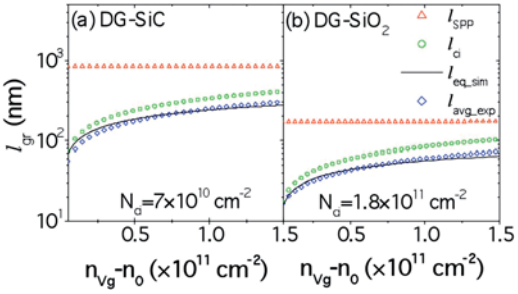

FIG. 3. (Color online) A representative graph of prominent limiting contributions to the room temperature electron mean free path in graphene evaluated for the cases of (a) DG-SiC, and (b) DG-SiO_2: l_{SPP} (up-triangles), l_{ci} (circles). The l_{ci} is simulated by varying the charged-impurity density N_{ci}. The best match between l_{eq_sim} (solid line) and l_{avg_exp} (diamonds) was found for $N_{ci}=7\times10^{10}$ cm^{-2} (DG-SiC), 1.8×10^{11} cm^{-2} (DG-SiO_2).

coupling of the 2DEG with SPP in SiC than in SiO_2.

The electron mean-free path limited by scattering on charged impurities (l_{ci}) in graphene could be expressed as a function of the carrier density as,[26]

$$l_{ci}(n)=\frac{16\varepsilon_0^2\varepsilon^2\hbar\nu_F^2}{Z^2q^4N_{ci}}\left(1+\frac{q^2}{\pi\hbar\nu_F\varepsilon_0\varepsilon}\right)^2\sqrt{\pi n}, \tag{1}$$

where $\hbar$ is the Planck's reduced constant, ν_F is the electron Fermi velocity in graphene ($\nu_F=1\times10^6$ m/s), Z is the net charge of the impurity (assumed to be 1 for this study), N_{ci} is the impurity density, and ε is the average between the relative permittivity of the substrate (ε_{ins}) and of vacuum permittivity ($\varepsilon_{vac}=1$). The electron mean free path limited by scattering with a SPP phonon mode of characteristic frequency ω_v can be expressed as[27]

$$l_{SPP,v}=\sqrt{\frac{\beta}{\hbar\omega_v}}\frac{\hbar\nu_F 4\pi\varepsilon_0}{q^2}\frac{q\nu_F}{F_v^2}\frac{\exp(k_0z_0)}{N_{SPP,v}}\frac{\hbar\sqrt{\pi}}{q}, \tag{2}$$

where $k_0\approx\sqrt{[(2\omega_v/\nu_F^2)^2+\chi n]}$, $\chi\approx10.5$, $\beta\approx0.153\times10^{-4}$ eV,[28] and $z_0\approx0.35$ nm is the separation between the polar substrate and graphene flake. $N_{SPP,v}$ is SPP phonon occupation number. The magnitude of the polarization field is given by the Fröhlich coupling constants, F_v^2.[28]

In Figs. 3(a) and 3(b) the average of the l_{gr} versus n_{Vg}-n_0 curves measured on different tip positions on DG-SiC and DG-SiO_2 are fitted with the equivalent mean free path obtained by,

$$l_{eq\_sim}^{-1}=l_{ci}^{-1}+\sum_v l_{SPP,v}^{-1}. \tag{3}$$

The SiO_2 substrate has two characteristic SPP frequencies at 58.9 meV and 156.4 meV with corresponding coupling constants F_v^2 of 0.237 meV and 1.612 meV; whereas the characteristic SPP frequency for SiC substrate is at 116.0 meV with F_v^2 of 0.735 meV. The only fitting-parameter used in Eq. (3) is N_{ci}. We found the charged-impurity density limiting the mean free path to be $\sim7\times10^{10}$ cm^{-2} for DG-SiC, and $\sim1.8\times10^{11}$ cm^{-2} for DG-SiO_2. The calculated l_{SPP} and l_{ci} versus n_{Vg}-n_0 curves are also reported in both cases. It is worth noting that l_{SPP} for DG-SiC is more than five times l_{SPP} for DG-SiO_2. As a result, scattering by charged impurities is the limiting scattering mechanism in DG-SiC [see Fig. 3(a)], whereas a significant contribution is played by scattering with SPP in the case of DG-SiO_2, especially at higher carrier densities [see Fig. 3(b)].

In this study we probed the local electron mean-free path (l_{gr}) in graphene deposited on 4H-SiC(0001) (DG-SiC), graphene epitaxially grown on 4H-SiC(0001) (EG-SiC) and compared it with graphene deposited on SiO_2 (DG-SiO_2) with method based on Scanning Capacitance Spectroscopy (SCS). We observed a $\sim>4\times$ increase in l_{gr} for DG-SiC compared to DG-SiO_2 owing predominantly to lesser SPP phonon scattering ($\sim<5\times$) and better dielectric screening of charged-impurities compared to SiO_2 substrates. On the other hand, l_{gr} on EG is on average ~0.4 times than on DG-SiC and exhibits large variations from point to point, due to the presence of a laterally inhomogeneous positively charged layer at EG/SiC interface.

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