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On-Chip Stimulus Generator for Gain, Linearity, and Blocking Profile Test of Wideband RF Front Ends

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Abstract—This paper presents the design and measurement of a stimulus generator suitable for on-chip RF test aimed at gain, 1-dB compression point (CP), and the blocking profile measurement. Implemented in a 90-nm complementary metal-oxide-semiconductor (CMOS), the generator consists of two low-noise voltage-controlled ring oscillators (VCOs) and an adder. It can generate a single- or two-tone signal in a range of 0.9–5.6 GHz with a tone spacing of 3 MHz to 4.5 GHz and adjustable output power. The VCOs are based on symmetrically loaded double-differential delay line architecture. The measured phase noise is -80 dBc/Hz at an offset frequency of 1 MHz for the oscillation frequency of 2.4 GHz. A single VCO consumes 26 mW at 1 GHz while providing -10 -dBm power into a $50\text{-}\Omega$ load. The silicon area of the complete test circuit including coupling capacitors is only 0.03 mm^2 , while a single VCO occupies 0.012 mm^2 . The measured gain, 1-dB CP, and blocking profile of the wideband receiver using the on-chip stimulus generator are within $\pm 8\%$, $\pm 10\%$, and $\pm 18\%$ of their actual values, respectively. These error values are acceptable for making a pass or fail decision during production testing.

Index Terms—On-chip RF testing, RF design for testability (DfT), RF test, stimulus generator, voltage-controlled oscillator (VCO).

I. INTRODUCTION

WIDE BAND RF front ends have the potential to meet the demands of future multiband and multistandard receivers. The advantage is smaller silicon area and lower power consumption compared to the solution employing multiple front ends (one for each band) or a tunable front end for a group of frequency bands [1]. For the production testing of such a receiver, a bandwidth of several gigahertz is needed from the signal source to the on-chip front end under test. This makes the design of the chip package and printed circuit board (PCB) transmission lines a challenging task. Due to the extremely large bandwidth, the use of lumped elements on a PCB to tune out the parasitics, which is a common practice in

narrow-band designs, is no longer an option. Moreover, the test methodologies like probe testing used to characterize the circuit during the design phase are very expensive in volume production in terms of setup time, cost, and complexity. One possible solution to these problems is the use of on-chip test circuitry for test measurements. In nanometer CMOS technologies, the circuit dimensions are small compared to the wavelength of interest. Therefore, the signals do not suffer from transmission line effects on a chip.

To test the gain, linearity, and blocking profile of an RF front end, two voltage-controlled oscillators (VCOs) with a wide tuning range and an adder with power control are needed. These components should feature a performance good enough for test, i.e., a small chip area overhead and low phase noise, but there is no stringent limit on the power consumption, since the circuit will be only used during the test mode.

The straightforward approach to build an on-chip oscillator is to use either an LC -tank-based or delay-cell-based circuit (ring oscillator). LC -tank-based oscillators have excellent phase noise performance, but the tuning range is usually not more than 20%–25%, and high- Q inductors are mandatory in this case. To realize such high- Q inductors, a large chip area and special enhancements within the CMOS process are needed. On the other hand, ring oscillators are better suited for on-chip integration using a standard CMOS process and occupy a small chip area that improves both the yield and the cost of the chip. In-phase and quadrature-phase components can easily be generated [2]. However, the phase noise performance of ring oscillators is, in general, poorer compared to LC oscillators.

In this paper, we present a stimulus generation circuit with a small chip area that achieves a wide tuning range of 0.9–5.6 GHz, low phase noise, and variable output power. The core of this circuit is a modified voltage-controlled delay line (VCDL) capable of providing a wide tuning range and low phase noise at all oscillation frequencies. This circuit is successfully used to test the gain, 1-dB compression point (CP), and blocking profile of wideband RF front ends.

The stimulus generation circuit consists of two VCOs, an adder, coupling capacitors, and switches, as shown in Fig. 1. Each VCO has nine VCDLs, which are designed such that they can seamlessly be switched to provide either a five- or nine-VCDL ring architecture, thus covering the complete frequency range of interest. The design and operation of the basic VCDL is discussed in Section II. The adder circuit is used to generate two tones with an adjustable output power level while driving a $50\text{-}\Omega$ load. The design of the modified VCDL, VCO, and adder circuit is discussed in Section III. Section IV presents the stimulus generator performance in terms of its tuning

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Fig. 1. Block diagram of the wideband radio receiver with on-chip test stimulus generator.

range, phase noise, dynamic range, and power consumption. In Section V, a wideband RF front end is demonstrated under test for the gain, 1-dB CP, and blocking profile using the on-chip stimulus generator, and the measurement results are compared with actual values. Section VI concludes with a summary and some future direction.

II. DESIGN OF THE BASIC DELAY LINE (VCDL)

VCOs based on the ring architecture fall in two categories, i.e., saturated and nonsaturated, according to the behavior of the delay line transistors. In the nonsaturated-type VCO, the transistors do not completely switch, and all devices are in the active region during the oscillation period. On the contrary, in the saturated-type VCO, the transistors completely switch, resulting in a larger oscillation amplitude. It is well known that the phase noise performance improves with the increase in oscillation amplitude [3].

Another important requirement is the large tuning range of more than 80% to cover the frequency band of 1–5.4 GHz for multistandard applications. There are several different types of delay line circuits reported in the literature, i.e., source-coupled delay line, cross-coupled delay line, and inverter-based delay line [4]. However, none of aforementioned is appropriate for the large tuning range and good phase noise performance at same time.

The circuit schematic of a VCDL, which is similar to the one presented in [5], is shown in Fig. 2. These delay line simulations show acceptable phase noise performance, a large bandwidth, and a large tuning range at the same time. It consists of an input n-type MOS pair (Mn1–Mn2) and a p-type MOS (PMOS) positive feedback pair (Mp1–Mp2), which helps to maintain a large oscillation amplitude at higher frequencies.

The VCO frequency can be tuned using a variable capacitor (varactor) or a variable load. A varactor, which is typically implemented by a p-n junction, limits the frequency tuning range to 10%–20%. In this design, the frequency tuning is obtained by tuning the conductance of the diode-connected PMOS load (Mp3–Mp4). This conductance can be controlled

Fig. 2. Circuit diagram of a basic VCDL.

by changing the bias voltage of PMOS transistor Mp5. The delay line can be enabled or disabled by applying a control signal (high or low) at the gate of transistor Mn3.

A simple analysis of the basic delay line shows that the tuning range of an oscillator based on a VCDL is mainly dependent upon the ratio of the transconductance of the input pair Mn1–Mn2 and positive feedback pair Mp1–Mp2 [5].

$$\begin{aligned} f_{\max} &\approx \frac{1}{2\pi N} \frac{g_{mn1}}{C_L} \\ f_{\min} &\approx \frac{1}{2\pi N} \sqrt{\frac{g_{mn1}^2 - g_{mp1}^2}{C_L^2}} \end{aligned} \quad (1)$$

$$f_{\min} \approx \frac{1}{2\pi N} \sqrt{\frac{g_{\text{mn}1}^2 - g_{\text{mp}1}^2}{C_L^2}} \quad (1)$$

$$f_{\text{range}} \approx f_{\text{max}} \left(1 - \sqrt{1 - \frac{g_{\text{mp1}}^2}{g_{\text{mn1}}^2}} \right) \quad (2)$$

where N is the number of VCDL stages, and C_L is the cumulative parasitic capacitance of gate, drain, or source of transistors Mn1–Mn2, Mp1–Mp2, and Mp3–Mp4 attached to the output node.

The phase noise in a ring oscillator comes from three fundamental noise sources, which can be attributed to the transistor white noise, flicker noise, and coupled noise from substrate, control, and supply lines. The low-frequency flicker noise of the differential input pair is not responsible for the phase noise; rather, the flicker noise of tail transistors Mn3 and Mp5 modulates the VCO with random frequency modulation [6].

As the single-ended ring oscillators are extremely sensitive to the supply noise, a differential structure is a natural choice. Ideally, in differential structures, the supply noise appears in common mode and is rejected by the next delay stage in the chain. However, in practice, the direct parasitic coupling between the supply line and the output cannot be eliminated, and its effect becomes even worse at high frequencies.

The phase noise of a ring oscillator increases with the number of stages for a given fixed frequency and power. This effect, as verified by simulations, can be mitigated by keeping the total phase noise almost constant at the expense of elevated power consumption.

Fig. 4. Block diagram of a switchable five-/nine-stage wide-tuning VCO.

Fig. 5. Circuit diagram of variable output adder with 50-Ω drive capability.

Fig. 7. VCO tuning characteristic versus V_{Ctrl} in slow and fast modes.

Fig. 6. Macrograph of a wideband RF front end with the on-chip stimulus generator.

substrate coupling (see the micrograph in Fig. 6). To avoid injection locking, the oscillator outputs are heavily buffered, and power supplies are carefully decoupled using large parasitic gate capacitances of the transistors, which are particularly laid out for this purpose. During measurement, any symptoms of injection locking are not observed for a tone spacing as small as

Fig. 8. VCO tuning characteristic versus V_{Fine} for different oscillation frequencies.

3 MHz. A tone spacing of less than 3 MHz cannot clearly be distinguished due to the phase noise of the VCOs.

A VCO in its slow mode, which is composed of nine VCDLs, achieves a tuning range of 65% (0.923–2.65 GHz). In the fast mode, the tuning range is 55% (2.52–5.61 GHz). Collectively, this covers the frequency band of interest (1–5.4 GHz) with a cumulative tuning range of 83.6%, as plotted in Fig. 7. As shown in Fig. 8, the control signal V_{Fine} brings variations

Fig. 9. Measured phase noise plot at 5.4 GHz.

Fig. 10. Phase noise of the test circuit at different oscillation frequencies.

(Δ frequency) in frequency mainly determined by signal V_{Ctrl} . V_{Fine} is used to adjust the VCO frequency in very small steps of a few megahertz, enabling us to generate two stable tones with a small frequency spacing.

The phase noise performance of the VCO at 5.5 GHz is shown in Fig. 9. At the offset frequency of 10 MHz, a phase noise of -85 dBc/Hz is measured. The VCO phase noise performance degrades at higher oscillation frequencies, as shown in Fig. 10. The use of a phase-locked loop (PLL) can improve the phase noise performance of the VCO, but designing a PLL with such a large bandwidth is an extremely challenging task. The output power of the test signal can be controlled using the bias currents (I_{bias1} and I_{bias2}) of the adder circuit. The plot in Fig. 11 shows that the output power of a single tone can be controlled from -36 to -3 dBm at 1 GHz. This dynamic range of the VCO drops by approximately 4 dB as the oscillation frequency increases from 1 to 5.5 GHz. For two tones, the dynamic range further reduces by approximately 3 dB. The power consumption of a single VCO including the adder circuit for an output power of -10 dBm is plotted in Fig. 12. The power consumption increases with the frequency for both slow and fast modes. Since the test circuit is operational only during the test mode, higher power consumption is acceptable.

V. WIDEBAND FRONT-END MEASUREMENTS

The gain, 1-dB CP, and blocking profile of a wideband front end consisting of an LNA and a mixer are measured using

Fig. 11. Single-tone VCO power at adder output versus adder bias current.

Fig. 12. VCO power consumption versus frequency.

Fig. 13. Error in gain and 1-dB CP measured using the on-chip stimulus generator compared to the actual values versus local oscillator (LO) frequency.

the on-chip stimulus generator. The stimulus is measured by a spectrum analyzer. The difference between the measured values and the actual values measured by standard RF instrumentation is plotted in Fig. 13. The maximum gain error is within $\pm 8\%$, while the maximum error in the 1-dB CP is within $\pm 10\%$. In production testing, the on-chip power detector can be used to measure power of the input and output signals [1]. The major challenge is to reduce or mitigate the effect of process variation on these simple on-chip detectors designed in nanometer CMOS technologies. There are techniques reported

Fig. 14. Comparison of blocker profiles of the front end using the on-chip stimulus generator and standard equipment.

Fig. 15. Percentage error in the blocker profile of the front end using the on-chip stimulus generator and standard equipment.

in the recent literature particularly focusing on the calibration of on-chip RF detectors [11].

The main advantage of the presented stimulus generator is the availability of two tones on a chip. These tones can be generated with an arbitrary frequency spacing (from a few megahertz to gigahertz) and independent power control, specifically when the low power tone mimics an in-band desired signal and the high power tone imitates an out-of-band blocker. The measured and actual blocking profiles are plotted in Fig. 14. The maximum error between these two plots is within $\pm 18\%$, as shown in Fig. 15.

The main source of the error in measurement is the fluctuation in the amplitude of the oscillator output signal. These amplitude variations originate from different sources like FM-AM noise folding or ripples present in the supply lines. These errors can be further reduced by using on-chip power supply regulators and a better decoupling scheme.

The third intercept point (IP3) is another measure of nonlinearity in addition to the 1-dB CP. This circuit metric can only be measured reliably when the IP3 of the stimulus generator is better than the IP3 of the circuit under test. In our case, the output IP3 of the adder circuit is -8 dBm, while the front-end IIP3 is close to 0 dBm, so the IP3 measurement is not feasible. However, it is possible to design a highly linear adder circuit to achieve this goal compared to the simple adder circuit used in this design at the expense of an increase in area overhead.

TABLE I
PERFORMANCE COMPARISON WITH RECENT PUBLICATIONS

	This Work	[7]	[8]	[9]
Technology	90nm	180nm ⁺	180nm	180nm
Freq Range (GHz)	0.9-5.6	2.7-4.1	4.3-6.1	0.5 – 5
Tuning Range	83.6%	34%	29.5%	90%
Fine Freq. Resolution (MHz/V)	≈ 100 @ 1.2GHz	-	-	-
Phase Noise (dBc/Hz) @ 1MHz	-80 (2.4GHz)	-70	-85	-75
Max. Output (dBm)	-3	-34	-15	-10
Dynamic Range (dB)	33	-	-	-
Power Dissip. (mW)	110 [¶]	14	80	10.5
Vdd (Volt)	1.3	1.5	2	1.8
Active Area (mm ²)	0.012 [*]	0.7	0.28	0.25

⁺ Thick top metal for inductor layout; [¶] including 50 Ω buffer (adder); ^{*} Effective chip area

VI. SUMMARY AND CONCLUSION

In this paper, a differential stimulus generation circuitry consisting of two VCOs and an adder with 50- Ω drive capability has been presented. The summary of the VCO performance and comparison with the published CMOS VCOs with wide and continuous tuning range has been provided in Table I. Our modified dual-VCDL-based VCO has a wide tuning range of 83.6%, close to 50% duty cycle, and low phase noise, and it occupies an area of 0.012 mm².

The VCO presented in [9] has the tuning range of 90%, but the used delay cell architecture and three-stage architecture cannot easily be modified to have an additional control to change the frequency in small steps of a few megahertz.

The proposed stimulus generator can generate a single- or two-tone stimulus with a dynamic range of more than 30 dB and occupies the total area of 0.03 mm² including the coupling capacitors.

This stimulus generation circuitry has been successfully used to test the gain, 1-dB CP, and blocking profile of a front end with an error of $\pm 8\%$, $\pm 10\%$, and $\pm 18\%$, respectively. In volume production, the pass/fail tolerance limits are very carefully chosen. If the pass/fail limits are stringent, yield loss will increase. Contrary to this, the defective parts per million (DPPM) will increase if the tolerance limits are too relaxed. Therefore, the best values of pass/fail tolerances are calculated based on the optimal compromise between DPPM, yield loss, and test time [12]. Keeping in mind the current industrial practices, the magnitude of the measured errors seems plausible for screening out faulty chips in volume production.

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