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Comprehensive Evaluation and Study of Pattern Dependency Behavior in Selective Epitaxial Growth of B-Doped SiGe Layers

Mohammadreza Kolahdouz, Julius Hållstedt, Ali Khatibi, Mikael Östling, *Fellow, IEEE*, Rick Wise, Deborah J. Riley, and Henry Radamson

***Abstract*—The influence of chip layout and architecture on the pattern dependency of selective epitaxy of B-doped SiGe layers has been studied. The variations of Ge-, B-content, and growth rate have been investigated locally within a wafer and globally from wafer to wafer. The results are described by the gas depletion theory. Methods to control the variation of layer profile are suggested.**

***Index Terms*—Loading effect, pattern dependency, selective epitaxy, SiGe.**

I. Introduction

IMPLEMENTATION of selective epitaxial growth (SEG) in recessed source and drain (S/D) junctions in CMOS structures has generated considerable interest in device technology during the recent years. The practice of embedding SiGe films in p-type MOS (pMOS) S/D regions increases carrier mobility by inducing uniaxial strain to the channel [1]–[3].

A major challenge for the integration of SEG is the pattern dependency of deposition. In these structures, high Ge content (18%–30%) and B concentration (1–3 $\times$ 10^{20} cm^{-3}) are used to obtain a considerable strain amount, low sheet resistance, and high thermal stability during silicidation of epilayers [4]. SEG of SiGe layers is usually performed on wafers containing chips with various size openings. The pattern dependency of deposition leads to variations in Ge content and growth rate across the chip and across the wafer, and this profile variation leads to variations in device performance [5]–[10]. Nonuniformity of epideposition will also cause differences from wafer to wafer as chip design or the architecture (oxide or nitride with a specific thickness) changes. Many studies have explored methods to improve layer profile uniformity over a wafer [5], [6], [9], [10]. Some of these reports show that the pattern dependency can be decreased (<5%) [9] but so far there is no remedy to totally eliminate the pattern dependency problem.

This paper studies the pattern dependency of SEG of B-doped SiGe layers and explains the results through gas depletion theory. The interaction between different chips on a wafer is discussed, and different ways to improve the uniformity of layer profile across a wafer are proposed.

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II. Experimental Detail

Epitaxial SiGe layers were grown on patterned Si (1 0 0) substrates in an ASM Epsilon 2000 reduced pressure CVD (RPCVD) reactor at 650 °C with growth pressures of 10, 20, and 40 torr. In order to achieve uniformity of epilayers, wafers were rotating during epitaxy (35 r/min). Dichlorosilane (SiH_2Cl_2), 10% germane (GeH_4) in H_2, and 1% diborane (B_2H_6) in H_2 were used as Si, Ge, and B sources, respectively. HCl was used as the etchant to obtain selectivity during epitaxy. The partial pressures of SiH_2Cl_2 (P_{DCS}) and HCl (P_{HCl}) were 60 and 20 mtorr, respectively, for all samples. The partial pressure of GeH_4 (P_{Ge}) varied from 0.5 to 0.9 mtorr, and B_2H_6 partial pressure (P_B) varied between 5.3 $\times$ 10^{-5} and 4.8 $\times$ 10^{-2} mtorr. The hard mask used in this study was 70–340 nm thermal SiO_2.

Substitutional B and Ge concentrations were measured directly by high-resolution X-ray diffraction (HRXRD). By introducing a mirror into the primary optics of the X-ray setup, high intensity was obtained that created the ability to perform direct measurements on an array of device openings. Atomic force microscopy (AFM) was used to measure surface roughness, layer thickness, and recessed junction depth.

III. Results and Discussions

A. Theory of Gas Boundaries and Gas Depletion in CVD

The kinetics of CVD growth can physically be described by classical boundary layer theory using the defining theory of laminar gas flow over the wafer. Fig. 1 illustrates a schematic view of the process description.

During gas flow, a stagnant boundary layer is established due to the frictional force between the gas steam and the stationary susceptor/substrate. The thickness of this boundary layer (β) as a function of the position above the susceptor/substrate x is written as

$$\beta(x) = C\left(\frac{\gamma x}{V}\right)^{1/2}$$

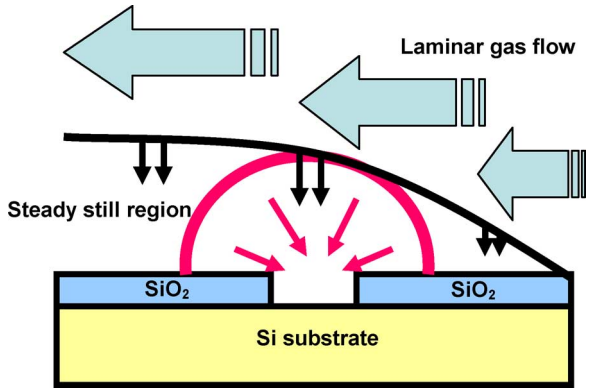

Fig. 1. Schematically illustration of how classical boundary layer forms from laminar gas stream flowing over the wafer in SEG during the CVD process. Black arrows in this figure are the gas molecules that diffused from the boundary and grey arrows show the depletion process inside the opening depletion volume (grey half circle) and afterward consumption of the diffused molecules by dangling bonds.

where γ is the gas kinematical viscosity, C is a constant, and V is the gas velocity. Beyond this boundary layer, the gas is assumed to be well mixed and moving at a constant speed. Gas molecules reaching the substrate surface have diffused through the gas boundary layer. When deposition occurs, the diffused gas molecules are consumed by dangling bonds. Gas molecules become depleted in the boundary layer if the reaction proceeds faster than diffusion.

Estimating the thickness of the boundary layer is not straightforward, but a rough calculation shows values on the order of centimeters. This means that growth molecules must diffuse vertically through a distance of about a centimeter. Diffusion will also occur laterally if there are concentration gradients across the wafer. This indicates that the gas phase depletion gradient will be significant (in the centimeter range) both vertically and laterally.

In gas depletion theory, two factors describe the growth kinetics that determine local pattern dependency: the amount of Si coverage of the chip (consumption term) and the gas velocity that controls boundary layer thickness over the wafer (diffusion term). A complete physical explanation of these factors is provided in the following sections.

B. Local Pattern Dependency: The Influence of Opening Size or Si Coverage of the Chips

Gas depletion theory indicates that Si coverage of the chip has a direct relation with the amount of gas consumption over a chip. Even if two chips on a wafer have openings with different geometries and sizes, they should have a similar layer profile if they have the same area of exposed Si. In order to verify this theory, two investigations were performed. The geometry and the density of chip openings were changed in each study, but the Si coverage of the chip was kept constant. Wafers were processed using a mask design containing three pairs of chips with identical coverage (0.83%, 2.8%, and 8.2%) but different geometry (see Fig. 2).

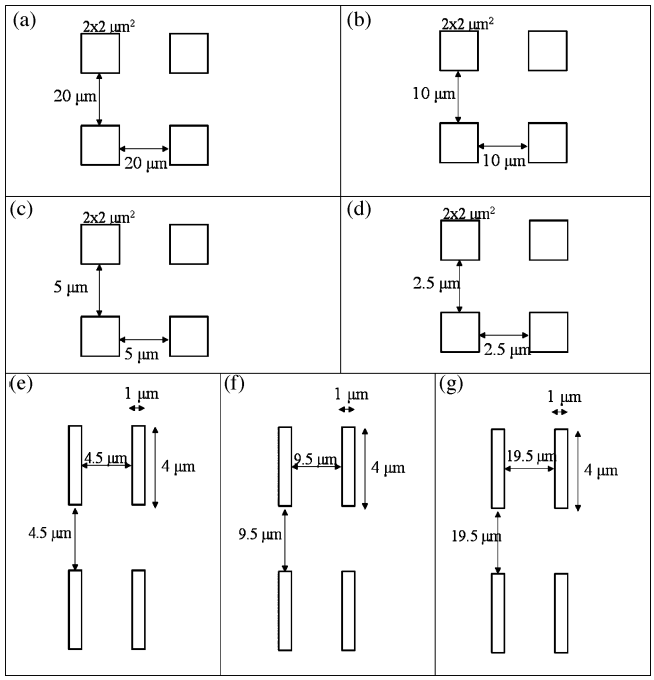

Fig. 2. Mask design to study the effects of Si chip coverage and geometry of oxide openings.

Each chip pair (A and G, B and F, and C and E) has one chip with quadratic openings (2×2 μm^2) and one chip with rectangular openings (1×4 μm^2). Processing of these wafers was done at a total pressure of 20 torr with partial pressure of 60 mtorr for SiH_2Cl_2, 20 mtorr for HCl, and 0.9 mtorr for GeH_4. Thickness and Ge content results on these chips are summarized in Table I. In Table I, chips with similar Si coverage show the same Ge content and thickness regardless of geometry.

The incorporation of B into SiGe is believed to be controlled by strain (Ge content) and epitaxial growth rate [11]. Previous report shows that B concentration is maximized by decreasing the growth rate and increasing the Ge content of the layer. In this study, if the SiGe layers are doped with boron, the amount of incorporated B in SiGe should correlate to Si coverage. Values for substitutional B concentration were obtained from the shift of the rocking curve layer peak position of intrinsic and doped layers in X-ray results. The results from wafers with B-doping are summarized in Table II. As predicted, chip pairs with the same exposed Si area show the same Ge%, growth rate, and B concentration.

The other factor from gas depletion theory that impacts SiGe growth is the diffusion term. This term is related to how the gas flows and forms boundaries over the wafer and the number of molecules available over the chip that is not derived exactly from the partial pressure in the chamber. These factors are determined by growth pressure during epitaxy.

To examine the impact of diffusion, three samples were processed using a mask design that creates nine chips on a wafer (5×5 mm^2), where each chip contains only one size Si opening. The openings in the chips are either 1×1, 2×2, 4×4, 8×8, 10×10, 20×20, 40×40, 80×80, or 160×160 μm^2 and openings within each chip are spaced 100 μm

TABLE I
DEPENDENCY OF THE LAYER PROFILE OF INTRINSIC SiGe ON CHIP COVERAGE

Chip	Geometry	Coverage (%)	Composition (%)	Growth rate (Å/min)
A	2×2 μm^2-20 μm	0.83	26.08	95
G	1×4 μm^2-19.5 μm		26.16	96
B	2×2 μm^2-10 μm	2.8	24.33	60
F	1×4 μm^2-9.5 μm		24.32	63
C	2×2 μm^2-5 μm	8.2	22.23	33
E	1×4 μm^2-4.5 μm		22.2	32

All of the chips are on the same wafer.

TABLE II
DEPENDENCY OF THE LAYER PROFILE OF DOPED SiGe ON CHIP COVERAGE

Chip	Geometry	Coverage (%)	Composition (%)	Growth rate (Å/min)	Active B conc.(cm^{-3})
A	2×2 μm^2-20 μm	0.83	22.5	144	2.38×10^{20}
G	1×4 μm^2-19.5 μm		22.5	144	2.42×10^{20}
B	2×2 μm^2-10 μm	2.8	21	102	2.2×10^{20}
F	1×4 μm^2-9.5 μm		21	102	2.2×10^{20}
C	2×2 μm^2-5 μm	8.2	19.4	73	1.88×10^{20}
E	1×4 μm^2-4.5 μm		19.3	73	1.92×10^{20}

All of the chips are on the same wafer.

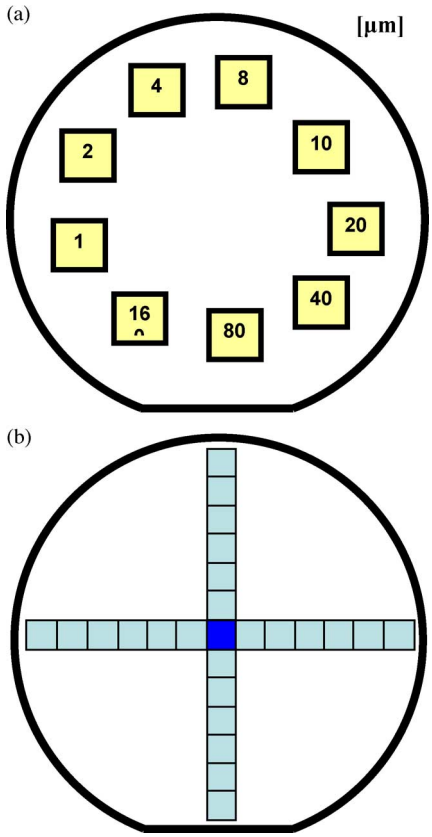

Fig. 3. Wafer pattern designs used in this study.

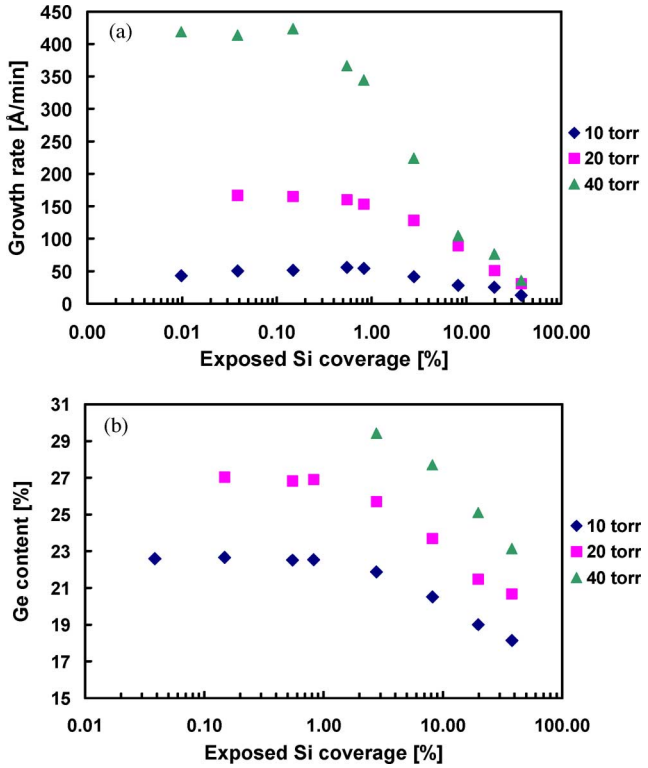

Fig. 4. (a) Growth rate. (b) Ge content of intrinsic SiGe selective epitaxy at 650 °C versus the Si coverage for different total growth pressures but similar precursor partial pressures (the applied P_{DCS}, P_{HCl}, and P_{GeH4} are 60, 20, and 0.9 mtorr, respectively).

apart [mask in Fig. 3(a)]. This mask design creates a wide range of Si chip coverages that vary between 0.01% and 37.95%. In this test, total pressure was varied from 10 to 40 torr and SiGe layers were deposited with the same dichlorosilane (SiH_2Cl_2) and germane (GeH_4) partial pressures on all wafers. This was performed by compensating the flux of precursors for each total pressure where the carrier gas flow (H_2) was kept constant. Both the Ge content and the growth rate were measured and compared, as shown in Fig. 4(a) and (b). There are some missing data in Fig. 4(b) for the sample grown at 40 torr due to strain relaxation.

The three curves in Fig. 4(a) demonstrate that the growth rate increases with increasing growth pressure. For example, for the chip with 1% Si coverage (containing opening sizes of 10 × 10 μm^2), growth rate values of 50, 160, and 350 Å/min were measured at 10, 20, and 40 torr, respectively. Lower pressures

led to slower growth because of the relationship between pressure and gas velocity, depletion volume, and the number of molecules diffusing to the wafer surface. By decreasing the growth pressure, the velocity of the gas is increased, the formed gas boundary moves closer to the substrate, the depletion volume becomes smaller, and the number of diffusing molecules is decreased.

The curves in Fig. 4(a) and 4(b) have two distinguishable regions: a linear region where growth rate and Ge content increase with decreasing Si coverage and a saturation region. The saturation region occurs at smaller values of Si coverage when growth pressure is increased. At 20 torr, saturation occurs at Si coverages below 1% while saturation occurs below 0.65% Si coverage when the pressure is 40 torr. Depicted saturation region is due to very small gas consumption (small as compared to the gas flow).

C. Local Pattern Dependency: Interaction Among the Chips in a Mask

Testing to this point has revolved around the idealized situation where chips are isolated from one another. In practice, a patterned wafer contains many close-packed chips, and the depletion volume of a chip may overlap and interact with neighboring chips.

A test was performed to estimate the interaction radius around a chip versus its Si coverage. For this study, a wafer was processed with a 5×5 mm^2 chip in the center of the wafer. This center chip had 20% Si coverage and was considered the "trap chip" that depletes reactants from the depletion volume. The center chip was surrounded by test chips on four sides extending toward the wafer edge. The surrounding chips had 0.83% Si coverage [mask in Fig. 3(b)]. Fig. 5(a) and (b) shows the impact of the center trap chip on growth rate and Ge content in the surrounding chips. Growth rate was determined with AFM, and Ge content was defined with HRXRD data. In Fig. 5(b), there are no data recorded for Ge content at 40 torr due to strain relaxation.

The curves in Fig. 5 reveal three distinct regions. Within 12 mm of the trap chip, there is a linear increase in growth rate and Ge content as the distance from the trap chip increases. From 12 to 40 mm, the growth rate is saturated and does not vary with distance. Finally, toward the wafer edge, growth rate decreases as the distance from the wafer center increases.

The first region involves openings that are impacted by the depletion volume of the trap chip. In this volume, a significant part of the gas molecules is consumed by the trap chip and the molecules available for surrounding chips are reduced. When the openings are far enough away from the trap chip, they are not influenced by the trap; this corresponds to the second region in this figure. Finally, as the edge of the patterned wafer is approached, the susceptor has a chance to deplete reactants. The uniformity of the deposition over a blanket wafer was checked and nonuniformity was less than 5%. The distribution of layer profile over this wafer reveals a unique picture of the growth and an understanding of pattern dependency of SEG.

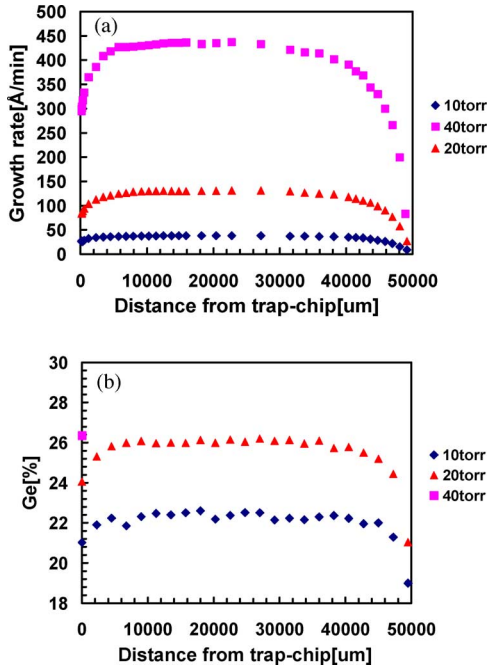

Fig. 5. Illustration. (a) Growth rate. (b) Composition variation through chips with 20% Si coverage trap chip in the middle and 2×2 μm^2 openings with 20 μm distance in the surrounding chips for different growth pressures.

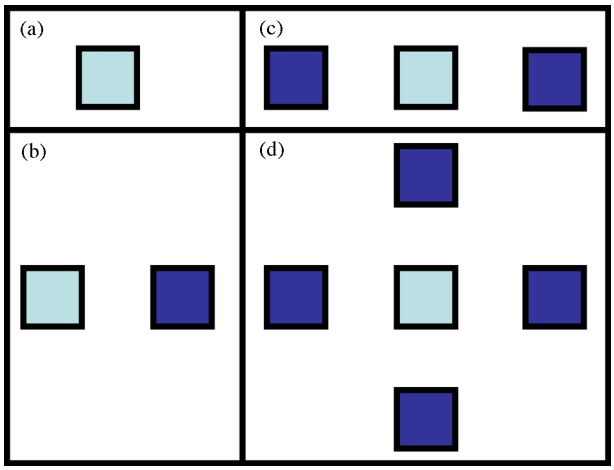

Fig. 6. Mask design to study the interaction among the chips in a wafer. Surrounding gray chips (Si coverage of 37.85% or 19.75%) are located at 5 mm distance from the central white chip (0.83% Si coverage).

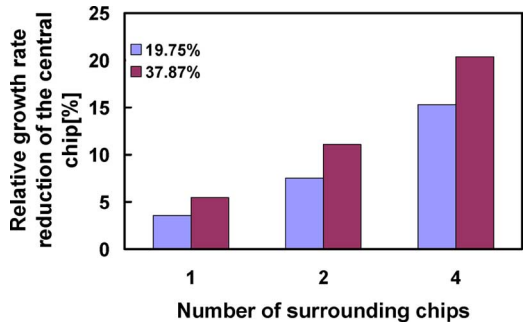

Fig. 7. Illustration of growth rate reduction compared to reference opening on the wafer caused by different numbers of surrounding chips (the applied P_{DCS}, P_{HCl}, and P_{GeH4} are 60, 20, and 0.9 mtorr, respectively).

TABLE III
DEPENDENCY OF THE LAYER PROFILE OF DOPED SiGe ON CHIP COVERAGE WAS INVESTIGATED ON TWO WAFERS WITH SIMILAR GLOBAL AND LOCAL COVERAGES

Chip No.	Geometry	Coverage	Composition (%)	Growth rate (Å/min)
1	2×2 μm^2-20 μm	0.83	25.46	112
2	1×4 μm^2-19.5 μm		25.36	118
3	2×2 μm^2-10 μm	2.8	24.22	94
4	1×4 μm^2-9.5 μm		24.16	97
5	2×2 μm^2-5 μm	8.2	22	46
6	1×4 μm^2-4.5 μm		22.2	49

Chips with odd and even numbers are located on different wafers.

Fig. 5(a) indicates that the shape of the growth rate curves does not change with decreasing growth pressure, but the width of the linear portion (which determines the radius of depletion volume) becomes smaller. An observation on data points in Fig. 5 provides a rough estimation for depletion volume radius. This was performed when the relative variation of the growth rate is less than 5% of the saturation value. The extracted radii are approximately 10, 12, and 14 mm for 10, 20, and 40 torr, respectively. These results indicate that the growth kinetics of the gas flux over the chips has been changed, and as a result, the depletion volume has decreased. HRXRD results in Fig. 5(b) illustrate similar features to Fig. 5(a). Note that the data for Ge content are a mean value over an entire chip. In Fig. 5(b), the layers grown at 40 torr were partially relaxed due to growth above the critical thickness and were omitted.

In follow-up studies, more complicated cases were tested in which a chip can be impacted by two or more surrounding chips. On the mask for this study, the Si coverages of the surrounding chips (19.75% and 37.85% Si coverage) were larger than the central chip (0.83% Si coverage). Four cases were studied, as demonstrated in Fig. 6.

A wafer was patterned such that four independent tests could be conducted simultaneously. Each test pattern was more than 15 mm from the wafer edge and the other test patterns so that results of each pattern can be investigated separately. A reference chip is included [see Fig. 6(a)] to determine SiGe growth when there is no interaction with other features. In all cases, the growth rate and Ge content in the central chip were measured. The change of the growth rate in the central chip relative to the reference chip is shown in Fig. 7. These results reveal that the effect of any chip is additive to the impact of other chips on the central chip. This means that by knowing the impact of one chip, it is possible to estimate the growth rate in a central chip for any number of surrounding chips.

The aforementioned results suggest methods of designing chips with a more uniform layer profile. One approach would be to introduce dummy features or chips to maintain the same coverage over the entire wafer. Secondary ion mass spectrometry (SIMS) squares (160×160 μm^2) would be able to deplete all small openings over the chip and lead to more uniform chips over the whole wafer. A second approach would be to calibrate the layer profile by using a calibration sample that contains chips with various Si coverages [similar to Fig. 4(a) and (b)]. Data from these calibration samples would enable the development of a strategy for chips with complicated layouts (different opening sizes). Each chip can be divided into subregions where the Si coverage is kept constant by modifying the density of the openings. This strategy has to be repeated for all the chips of the wafer.

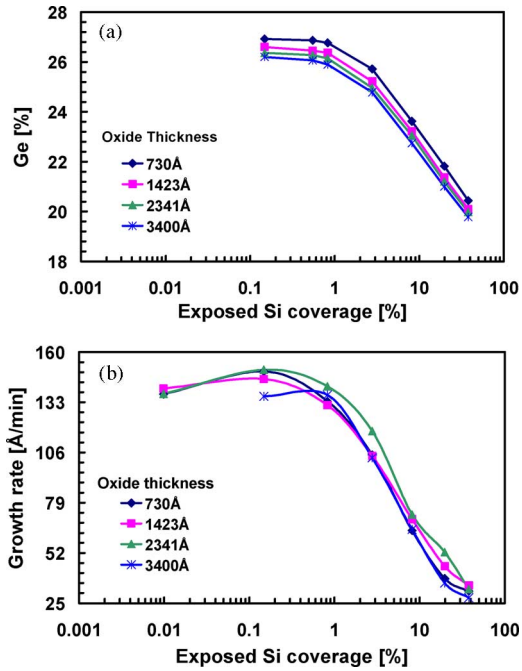

Fig. 8. (a) and (b) Illustration of Ge content and growth rate variation versus Si coverage in four different wafers with different oxide thicknesses (the applied P_{DCS}, P_{HCl}, and P_{GeH4} are 60, 20, and 0.9 mtorr, respectively).

D. Global Pattern Dependency

Previous tests involved work on individual wafers. To examine wafer-to-wafer variation, two different wafers were processed. The chips on each wafer had the same chip Si coverage, but the layout was different on each wafer. Both patterned Si wafers had an oxide thickness of 0.18 μm, and all chips were positioned to avoid being impacted by other chips and the susceptor. The results are illustrated in Table III. In Table III, chips 1, 3, and 5 were located on one wafer while chips 2, 4, and 6 were located on a second wafer. The layer profile is unchanged for all chip pairs with the same Si coverage. Itmeans that our results demonstrate a way to control the global pattern dependency by choosing the same chip Si coverage.

The architecture of the samples was studied by evaluating patterned Si wafers with oxide thicknesses of 73, 140, 235, and 340 nm. The variation of the layer profile over different Si coverages and oxide thicknesses is illustrated in Fig. 8(a) and

(b). Fig. 8 can be considered as an illustration of global versus local emissivity. Ge content decreases with increasing the oxide thickness while the growth rate shows a minor fluctuation. The reason for variation of Ge content for different oxide thicknesses is not known yet; however, it may relates to the properties of oxide surface.

IV. Conclusion

Selective epitaxy growth suffers from a pattern dependency that leads to a variation of Ge content and growth rate for chips with different Si coverages. Pattern dependency was saturated in these studies for chips with Si coverage of less than 1%. The interaction between chips on a patterned wafer originates from the amount of gas consumed by the chips and the distance of the chips from each other (radius of gas depletion). An estimation of the radius of gas depletion for the chips in this study is 8 mm at 10 torr and 15 mm at 40 torr. The interaction of chips on neighboring chips is additive for all chips located within the radius of gas depletion. Using thicker oxide in the pattern led to lower Ge content but had no significant influence on the growth rate. The impact of oxide thickness originates from less heat conduction for thicker oxides that impacts the kinetics of gases over the chip.

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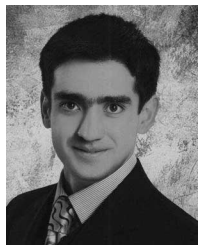

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