A study on the decimation stage of a $\Delta-\Sigma$ ADC with noise-shaping loop between the stages

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**Abstract**
The filter complexity in the multi-stage decimation system of a Δ-Σ ADC increases progressively as one moves to higher stages of decimation due to the fact that the input word length of the higher stages also increases progressively. The main motivation for this thesis comes from the idea of investigating a way to reduce the input word length in the later filter stages of the decimation system which could reduce the filter complexity. To achieve this, we use a noise-shaping loop between the first and later stages so that the input word length for the later stages remains smaller than in the case where we do not use the noise-shaping loop. However, the performance (SNR/Noise-level) level should remain the same in both cases. This thesis aims at analyzing the implications of using a noise-shaping loop in between the decimation stages of a Δ-Σ ADC and also finding the appropriate decimation filter types that could be used in such a decimation system. This thesis also tries to compare the complexity introduced by using the noise-shaping loop with the reduction achieved in the later decimation stages in terms of the input word length. Filter required in the system will also be optimized using minimax optimization technique.

**Keywords**
Oversampling ratio, Noise-shaping, Δ-Σ ADC, Filter Optimization, FIR filter, CIC filter, Decimation
Abstract

The filter complexity in the multi-stage decimation system of a $\Delta$-$\Sigma$ ADC increases progressively as one moves to higher stages of decimation due to the fact that the input word length of the higher stages also increases progressively. The main motivation for this thesis comes from the idea of investigating a way, to reduce the input word-length in the later filter stages of the decimation system which could reduce the filter complexity. To achieve this, we use a noise-shaping loop between the first and later stages so that the input wordlength for the later stages remains smaller than in the case where we do not use the noise-shaping loop. However, the performance (SNR/Noise-level) level should remain the same in both cases. This thesis aims at analyzing the implications of using a noise-shaping loop in between the decimation stages of a $\Delta$-$\Sigma$ ADC and also finding the appropriate decimation filter types that could be used in such a decimation system. This thesis also tries to compare the complexity introduced by using the noise-shaping loop with the reduction achieved in the later decimation stages in terms of the input wordlength. Filter required in the system will also be optimized using minimax optimization technique.
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Chapter 1

Theory

In this chapter, all the theoretical concepts used in the thesis are explained. These explanations are sufficient to understand the work done in the thesis.

1.1 Principles of Δ-Σ Modulation and its applications

1.1.1 Basic Concepts

The two main concepts used in this modulation technique are: Oversampling and Noise-shaping.

1.1.1.1 Oversampling

Sampling the signal at a higher rate than the Nyquist rate is called Oversampling. i.e.,

\[ f_s > 2f_b \] (1.1)

where,

\[ f_b \rightarrow \text{Bandwidth of the baseband signal.} \]

The term quantization noise is important to understand and to know the purpose of oversampling. It is defined as the error that is introduced when a discrete-time signal (with infinite allowable signal levels) is converted to a digital signal (with finite allowable signal levels). Figure 1.1 shows the transfer curve and error function of the quantizer. It can be seen that the quantization error lies between \(-\frac{\Delta}{2}\) and \(\frac{\Delta}{2}\), if the quantizer input is within the signal range i.e., if the quantizer is not overloaded. Here, \(\Delta\) is the distance between any two successive quantization levels (quantization step size). The
Figure 1.1: a) Transfer curve and the b) Quantization error function of the quantizer.

The total number of allowable quantization levels for an $N$-bit quantizer is $2^N$. The quantization step size is

$$\Delta = \frac{2M}{2^N}. \quad (1.2)$$

where,
- $2M \rightarrow$ Full-scale range of the quantizer.
- $N \rightarrow$ Number of bits of quantizer.

In a probabilistic sense, the quantization error can be considered as random white Gaussian noise whose power spectral density (PSD) is given by,

$$R_e(f) = \frac{\Delta^2}{12f_s}. \quad (1.3)$$

where,
- $\Delta \rightarrow$ Quantization step size.
- $f_s \rightarrow$ Sampling frequency.

Due to oversampling, the quantization noise is spread over a wider frequency range as shown in Figure 1.2. The total in-band $(0-f_b)$ noise power will be reduced by a factor of $OSR$ (Oversampling ratio) which is given by,

$$OSR = \frac{f_s}{2f_b} \quad (1.4)$$
where,
\( f_s \rightarrow \) Sampling frequency.
\( f_b \rightarrow \) Bandwidth of the baseband signal.

1.1.1.2 Noise shaping

The process of moving the quantization noise out of the signal-band is called \textit{Noise-shaping}. While the noise is shaped, the input signal remains unchanged in \( \Delta-\Sigma \) modulation. The concept of noise-shaping is showed in Figure 1.3. The PSD of the shaped-quantization noise is given by,

\[
R_q(f) = |NTF|^2 R_e(f)
\]  

\( \text{Figure 1.3: One-sided PSD of quantization noise before and after noise-shaping.} \)
NTF → Noise Transfer Function (to be explained shortly).

\[ R_e(f) \rightarrow \text{PSD of the quantization noise after oversampling.} \]

In Δ-Σ modulation, the NTF is usually given by

\[ NTF = (1 - z^{-1})^L. \]  

(1.6)

where,

L → Order of the noise-shaping loop used.

### 1.1.2 Δ-Σ Modulation

The Δ-Σ modulation technique is used to convert a higher resolution signal to a lower resolution signal while maintaining adequate performance. This type of modulation can be applied to Data-converters and is explained in the following section.

#### 1.1.2.1 Δ-Σ ADC

In this section, a general description of a Δ-Σ ADC system is presented. Figure 1.4 shows the block-level description of a Δ-Σ ADC. In a Δ-Σ ADC,

\[ e_1(n) \]

\[ x(t) \rightarrow \Delta-\Sigma \quad \text{Modulator} \]

\[ y(n) \]

\[ \text{Decimation Filter} \]

\[ y_d(n) \]

Figure 1.4: Δ-Σ ADC system.

the analog input signal (resolution \(\rightarrow\) ∞) is converted to a digital signal (with finite allowable signal levels) of low resolution (usually 1–8 bits). The sample rate of the output signal is then reduced by using a decimation stage. This reduction is necessary as it enables the later signal-processing stages to work at lower data rates. Further discussion on the decimation stage is given in section 1.3.

#### 1.1.2.2 Digital Δ-Σ noise-shaping loop in DACs

A higher resolution digital signal (input) can be converted to a lower resolution digital signal (output) with adequate performance using a Digital Δ-Σ
noise-shaping loop (NL). This loop can be used in the implementation of oversampled DACs. The block-level description of a DAC system using this loop is shown in Figure 1.5. Here, $P$ is usually between 1 and 8 bits ($N > P$).

![Figure 1.5: ∆-Σ DAC system.](image)

In this case, the error introduced is not the quantization noise as is the case in a ∆-Σ ADC. The error introduced here is the round-off noise. As the round-off noise has similar properties as that of the quantization noise, the analysis remains the same in both the applications. Using the noise-shaping loop, the requirements on the DAC can be reduced to a large extent.

1.2 Mathematical Analysis of a ∆-Σ modulator

The block-level description of a ∆-Σ modulator (that uses a single-quantizer) is shown in Figure 1.6. Here,

![Figure 1.6: Block-level description of a ∆-Σ modulator.](image)

$L_0 \rightarrow$ Transfer function of the signal path from $U$ to $Y$.
$L_1 \rightarrow$ Transfer function of the signal path from $V$ to $Y$.

Two terms $NTF$ and $STF$ are introduced.
Here,

\[ \text{NTF} \rightarrow \text{Noise Tranfer Function (Transfer function of the signal path from } E \text{ to } V). \]

\[ \text{STF} \rightarrow (\text{Input}) \text{ Signal Transfer Function (Transfer function of the signal path from } U \text{ to } V). \]

The significance of NTF and STF is that, it describes how the input signal applied to the modulator and the quantization noise added in the quantizer are changed by the modulator. From the Figure,

\[ Y(z) = L_1(z)V(z) + L_0(z)U(z). \quad (1.7) \]

Here, we assume the quantizer (modulator) to be linear. Assuming a linear model means that the quantization error can be considered as additive random white Gaussian noise which can be added to the input of the quantizer to get the output. i.e.,

\[ V(z) = Y(z) + E(z) \quad (1.8) \]

Therefore,

\[ V(z) = \left( \frac{L_1(z)}{1 - L_0(z)} \right) V(z) + \left( \frac{1}{1 - L_0(z)} \right) E(z). \quad (1.9) \]

In the above equation,

\[ \text{STF} = \left( \frac{L_1(z)}{1 - L_0(z)} \right) \quad (1.10) \]

\[ \text{NTF} = \left( \frac{1}{1 - L_0(z)} \right). \quad (1.11) \]

As given in [1], for an \( L^{th}-\text{order} \) \( \Delta-\Sigma \) modulator (\( L^{th}-\text{order} \) loop filter), the NTF is generally given by,

\[ \text{NTF} = (1 - z^{-1})^L \quad (1.12) \]

\[ \text{STF} = z^{-L}. \quad (1.13) \]

As seen before, the PSD of the input quantization noise introduced by an \( N \)-bit quantizer is given by,

\[ R_e(f) = \frac{\Delta^2}{12f_s}. \quad (1.14) \]
From [1], the \textit{rms noise power} is given by
\[
    e_{\text{rms}}^2 = \frac{\Delta^2}{12}. \tag{1.15}
\]
If we assume the PSD to be one-sided, then
\[
    R_e(f) = \frac{\Delta^2}{6f_s}. \tag{1.16}
\]
The quantization noise at the output of the Δ-Σ modulator is given by
\[
    Q(z) = (1 - z^{-1})^L E(z). \tag{1.17}
\]
Therefore, the corresponding PSD is given by
\[
    R_q(f) = |NTF|^2 R_e(z). \tag{1.18}
\]
From [1], the in-band (0–\(f_{\text{b}}\)) quantization noise power at the output of the Δ-Σ modulator is given by
\[
    q_{\text{rms}}^2 = \frac{\pi^2 L e_{\text{rms}}^2}{(2L + 1)(OSR)^{2L+1}}. \tag{1.19}
\]
where,
\[
    \text{OSR} \rightarrow \text{Oversampling ratio} \left(\frac{f_s}{2f_{\text{b}}}\right).
\]
This equation gives the maximum theoretical estimate of the in-band noise at the output of the modulator. If we assume that a full-scale sinusoidal signal of peak amplitude \(M\) is applied to the modulator, then, as
\[
    |STF(z)| = 1, \tag{1.20}
\]
the output signal power is given by
\[
    u_{\text{rms}}^2 = \frac{M^2}{2}. \tag{1.21}
\]
From [1], the \textit{Signal-to-Quantization Noise Ratio (SQNR)} can be given as
\[
    SQNR = \frac{u_{\text{rms}}^2}{q_{\text{rms}}^2}. \tag{1.22}
\]
Here, we assumed that a full-scale input can be applied to the modulator. However, for higher-order modulators, due to stability problems, the allowable input signal range is less than the full-scale range of the quantizer.
1.3 Decimation and its Application in $\Delta$-$\Sigma$ ADC

1.3.1 Decimation

Decimation is a process of reducing the sampling rate of a digital signal. Decimation is a two-stage process, where the first stage consists of a decimation filter. This filter is also called Anti-aliasing filter as it band-limits the signal before the downsampling process to avoid aliasing. The second step called downsampling actually reduces the sampling rate, by a factor called the decimation factor. The Decimation factor is usually a power of 2. Figure 1.7 shows the block-level description of the decimation process. In the figure, the output signal is given by

$$y(n) = x_1(nM). \quad (1.23)$$

![Figure 1.7: Block-level description of the Decimation process.](image)

Mathematically, the output signal $y(n)$ in frequency domain is given by

$$Y(e^{j\omega T}) = \frac{1}{M} \sum_{k=0}^{M-1} X_1 e^{j(\omega T_1 - \frac{2\pi k}{M})}. \quad (1.24)$$

where,

$$T = MT_1. \quad (1.25)$$

The decimation process is explained by using the frequency spectrum of signals at various points of the system in Figure 1.8.

1.3.1.1 Decimation process in $\Delta$-$\Sigma$ ADC

The block-level diagram of a $\Delta$-$\Sigma$ ADC system is shown in Figure 1.9. As stated before, the purpose of using a decimation stage at the output of the $\Delta$-$\Sigma$ ADC is to reduce the sample rate, so that the later signal-processing stages in the system (e.g. a telecommunication system) work at lower sample rates.
The sample rate is usually reduced in stages. To preserve the properties of the output of the Δ-Σ ADC, linear phase filters are preferred. Most used filter types for the decimation in a Δ-Σ ADC are FIR filters and Sinc$^N$/CIC filters [1, 4, 6]. Even though CIC filters contain a feedback loop, they exhibit finite impulse response. The reason for this behaviour is that the output of the feedback portion (accumulator) is allowed to grow (i.e., it is not rounded).

CIC filters are preferred in the starting stages of decimation process (i.e., at higher sample rates), as they are simple and need fewer computations per second. They also preserve the noise-shaping in the signal band. Figure 1.10 explains this in detail. On the other hand, FIR filters are used in the final stages of decimation to achieve higher attenuation near the signal band, so that the amount of out-of-band noise folded into the signal band (due to aliasing) after the downsampling, is minimum. It is also used for
Figure 1.9: Block-level description of a \( \Delta-\Sigma \) ADC system.

droop-compensation. Figure 1.11 explains this in detail. The disadvantage of a CIC filter is that the passband gain is not constant. Gain response in the passband is tilted as shown in Figure 1.10. The FIR filter can be used to compensate for this droop in the passband and thus improve the SQNR (see Fig. 1.11 for details). As an example, the block-level description of a typical \( \Delta-\Sigma \) ADC system with multi-stage decimation is shown in Figure 1.12. Here, \( T_1 = N_1 T \) and \( T_2 = N_2 T_1 = N_1 N_2 T \).

Also,

\[
y_1(n) = y(nN_1) \tag{1.26}
\]

\[
y_2(p) = y_1(pN_2) = y(pN_1 N_2) \tag{1.27}
\]

\[
H_1(z) = \left( \frac{1}{N_1} \frac{1 - z^{-N_1}}{1 - z^{-1}} \right)^{L+1}. \tag{1.28}
\]

where,

\( L \rightarrow \) Order of the \( \Delta-\Sigma \) modulator.

Usually, \( L + 1^{th}\)-order CIC filter is sufficient for an \( L^{th}\)-order \( \Delta-\Sigma \) modulator [1].

The transfer function of \( N^{th}\)-order FIR filter is given by

\[
H_2(z) = \sum_{n=0}^{N} h(n) z^{-n}. \tag{1.29}
\]

where,

\( h(n) \rightarrow \) Impulse response of the filter.

A typical pole-zero plot of a non-recursive low-pass FIR filter is shown in Figure 1.13. In a typical \( \Delta-\Sigma \) ADC system, the final FIR stage decimates by a factor 4 [6].
1.4 Optimization

1.4.1 Optimization of NTF

As stated before, the NTF of an $L$th-order $\Delta$-Σ modulator is given by

$$NTF = (1 - z^{-1})^L$$  \hspace{1cm} (1.30)

A more general NTF can be used for applying optimization on poles and zeros. The above mentioned NTF has $N$-zeros at $z = 1$ i.e., at $f = 0$ and $N$-poles at $z = 0$ i.e., at $f = -\infty$. The zeros of the NTF can be optimized by moving them from the origin ($f = 0$) and placing them in the signal-band such that the in-band noise power is minimized. This would improve the SQNR. The poles of the NTF can be optimized by moving them from $z = 0$ nearer to the zeros. This would reduce the out-of-band NTF gain which, in turn, results in improved stability. Refer to [1, 6] for more details.
|\text{Out-of-band noise that will be folded into the signal band after final decimation.}|
|---|---|
|\text{Tilt-compensation in the signal band.}|

\begin{align*}
|H_2(\omega T_1)|^2 & = \text{Tilt-compensation in the signal band.} \\
|H_2(\omega T_1)|^2 R_d(\omega T_1) & = \text{Out-of-band noise that will be folded into the signal band after final decimation. (Here, Decimation factor = 4)}
\end{align*}

\text{Figure 1.11: Filtering process of FIR filter. a) Squared magnitude response of FIR filter. Noise spectrum at b) the output and c) input of final decimation stage FIR filter.}

\section*{1.4.2 Optimization of the decimation filter}

In general, FIR filters are the most commonly used form of filters, in the decimation process of a $\Delta$-$\Sigma$ ADC system. These are usually designed using McClellan, Parks and Rabiner Optimization algorithm which gives an equiripple solution for the filter magnitude response. This response may not give the peak SQNR. Thus, other optimization techniques using quadratic programming can be used to achieve the peak SQNR. Using minimax optimization algorithm with in-band noise power as the objective function and constraints being the maximum allowable deviation in the pass band ripple allows to use non-linear equations as constraints.
1.5 Effect of the stability of \( \Delta-\Sigma \) modulator on maximum achievable SQNR

As stated in [1, 2, 3, 6] the input signal range that is allowed to ensure stable modulator operation (stable input range) is always less than the full-scale range of the quantizer (ADC). Hence, the maximum achievable SQNR is limited by the stability condition of the \( \Delta-\Sigma \) modulator. While estimating the SQNR, a sinusoidal input signal within this stable input range is considered instead of a full-scale sinusoid. However, the analysis type chosen in the thesis is stochastic in nature and hence the stability of the modulator cannot be dealt in terms of the input signal range.
Chapter 2

System-Flow and Strategy

In this chapter, a detailed description of the Δ-Σ ADC system (model) that is considered for the thesis work and a detailed mathematical analysis of the system is presented. In addition, the strategy that will be followed during the work, is also described.

2.1 System-flow

Here, the term system-flow refers to the procedure followed to describe the flow of the system, starting from the Δ-Σ ADC and ending with the final decimation stage. The analysis type used here is Stochastic in nature, where the quantization error is modelled as an additive random white Gaussian noise. The influence of each block on the quantization noise is described in Figure 2.1, where

![Figure 2.1: Block-level description of the Δ-Σ ADC system with a detailed description of the decimation stage.](image-url)
\( NL \rightarrow \) Digital \( \Delta-\Sigma \) Noise-shaping loop.
\( e_1(n) \rightarrow \) Quantization noise introduced by the quantizer of \( \Delta-\Sigma \) ADC.
\( e_2(n) \rightarrow \) Round-off noise introduced in the NL.
\( q_1(n) \rightarrow \) Shaped-quantization noise of \( \Delta-\Sigma \) ADC.
\( f_1(n) \rightarrow \) Noise at the output of Stage-1 decimation filter.
\( f_2(n) \rightarrow \) Noise after stage-1 downsampling (by a factor \( N_1 \)).
\( q_2(n) \rightarrow \) Noise at the output of the NL, which is the sum of the input noise and the round-off noise introduced in the NL.
\( g_1(n) \rightarrow \) Noise at the output of Stage-2 decimation filter.
\( g_2(n) \rightarrow \) Noise after stage-2 downsampling (by a factor \( N_2 \)).

As shown in the figure, multi-stage decimation is implemented. The total number of decimation stages vary depending on the results obtained during the actual work. In the figure,

\[
\begin{align*}
\omega T_2 &= \frac{\omega T_1}{N_1} \tag{2.1} \\
\omega T_3 &= \frac{\omega T_2}{N_2} = \frac{\omega T_1}{N_1 N_2} \tag{2.2}
\end{align*}
\]

2.1.1 Assumptions of the analysis

- The \( \Delta-\Sigma \) blocks (\( \Delta-\Sigma \) ADC and NL) are assumed to be linear so that the quantization noise (introduced in the \( \Delta-\Sigma \) ADC) and the round-off noise (introduced in the NL) can be assumed as random and independent of the input signal being applied to the system. In this way, one can describe each of these blocks with two transfer functions—one that describes the effect of the system on the input signal (STF) and the other that describes the effect of the system on the noise (NTF). One can apply the principle of superposition to get the final output of each block.

- Only two error sources are assumed in the entire system—the quantization noise from the \( \Delta-\Sigma \) ADC block and the round-off noise from the NL block.

2.1.2 Mathematical analysis

Using [1, 7], the following analysis is done.
The PSD of $e_1(n)$ is given by

$$R_{e_1}(\omega T_1) = \frac{\Delta^2}{12},$$

(2.3)

where,

$\Delta \rightarrow$ Quantizer step size.

If we assume PSD to be one-sided, then

$$R_{e_1}(\omega T_1) = \frac{\Delta^2}{6}.$$  

(2.4)

Here,

$$\Delta = \frac{2A}{2^N},$$

(2.5)

where,

$2A \rightarrow$ Full-scale range of the quantizer.

$N \rightarrow$ Number of bits of quantizer.

As the $\Delta$-Σ ADC is assumed to be linear, the PSD of $q_1(n)$ is given by

$$R_{q_1}(\omega T_1) = |NTF_1(\omega T_1)|^2 R_{e_1}(\omega T_1).$$

(2.6)

The in-band noise power at this point in the system, can be calculated by integrating the PSD between 0 and $\frac{2\pi f_b}{f_s}$, $f_b$ being the bandwidth of the baseband signal. The noise $q_1(n)$ is later filtered (stage-1) to get the noise $f_1(n)$. The PSD of $f_1(n)$ is given by

$$R_{f_1}(\omega T_1) = |H_1(\omega T_1)|^2 R_{q_1}(\omega T_1).$$

(2.7)

The noise $f_1(n)$ is then decimated by a factor $N_1$ to get the noise $f_2(n)$. The PSD of $f_2(n)$ is given by

$$R_{f_2}(\omega T_2) = \frac{1}{N_1} \sum_{k=0}^{N_1-1} R_{f_1}(\omega T_1 - \frac{2\pi k}{N_1}).$$

(2.8)

The round-off noise $e_2(n)$ is added in the NL. The one-sided PSD of $e_2(n)$ is given by

$$R_{e_2}(\omega T_2) = \frac{(\Delta')^2}{6}.$$  

(2.9)

Here,

$$\Delta' = \frac{2A}{2^{N'}}$$

(2.10)
where,
\(2A\) \(\rightarrow\) Signal range of the NL.
\(N'\) \(\rightarrow\) wordlength at the output of the NL (= Full-scale of ADC).

The PSD of noise at the output of the NL \(q_2(n)\) is given by
\[
R_{q_2}(\omega T_2) = |NTF_2(\omega T_2)|^2R_{e_2}(\omega T_2) + R_{f_2}(\omega T_2). \tag{2.11}
\]

This noise \(q_2(n)\) is later filtered (stage-2) to get the noise \(g_1(n)\). The PSD of \(g_1(n)\) is given by
\[
R_{g_1}(\omega T_2) = |H_2(\omega T_2)|^2R_{q_2}(\omega T_2). \tag{2.12}
\]

This noise \((g_1(n))\) is then decimated by a factor \(N_2\) to get the noise \(g_2(n)\). The PSD of \(g_2(n)\) is given by
\[
R_{g_2}(\omega T_3) = \frac{1}{N_2} \sum_{i=0}^{N_2-1} R_{g_1}(\omega T_2 - \frac{2\pi i}{N_2}). \tag{2.13}
\]

The in-band noise power at various points of the system can be calculated to design the system that satisfies the performance requirement that is set initially.

2.2 Strategy used

The main aim of the thesis is to investigate a way to get cost savings in terms of input wordlength of the decimation filters, to reduce the complexity of these filters. In this work, a noise-shaping loop (NL) is used in between the decimation stages. Figure 2.2 describes the procedure to be followed in the work, in the form of a flow diagram. Different steps in the flow diagram are explained briefly:

- Step-1 starts with setting up a \textit{Count} variable to zero. This variable is used to limit the number of iterations in the analysis (this point will be discussed in the end).

- Step-2 starts with setting up an \textit{SQNR} requirement for which the \(\Delta-\Sigma\) ADC should be designed.

- Step-3 deals with the design of the ADC for the required SQNR. In this step, there are many options to choose for the ADC design in terms of order and quantizer size. So, one such design is chosen.
• Step-4 deals with the design of the decimation stage for both the cases—with and without NL. This is done to compare (later) the filter complexities in both the cases and analyze the effect of using a NL, on the system. Just as in step-3, one of the possible designs is chosen.

• Step-5 deals with the calculation of filter complexities in each of the two cases.

• In Step-6, a check is made if all possible NL designs are taken up and analyzed or not. If yes, the next step is taken; else, step-4 is taken where the next possible NL design is taken and analyzed.

• In Step-7, a check is made if all possible ADC designs that satisfy the SQNR requirement, are analyzed or not. If yes, the next step is taken; else, step-3 is taken, where the next possible ADC design is analyzed.

• In Step-8, the Count variable is incremented.

• In Step-9, a check is made if the value of the Count variable equals N or not. If yes, the analysis is stopped; else, step-2 is taken, where the SQNR requirement is changed and the system is analyzed. The value of N is set as per the time in hand (i.e., to limit the time spent on the thesis).

In general, for every iteration of this process, a few things are to be kept in mind. Initially, the decimation filter design and the loop filter design (in ∆-Σ blocks) would involve no optimization and the system is designed to satisfy the SQNR requirement. Later on, optimization techniques should be applied to further reduce the filter complexity. Decimation filter types are restricted to CIC and FIR filters.

2.3 Tools to be used

1. MATLAB™ for simulating the system.
   • Delta-Sigma toolbox.
   • Signal processing toolbox.

2. LATEX, TeXnicCenter and Xfig for documentation.
Start

Count = 0

Set SQNR to be achieved by Delta-Σ ADC.

Design the Δ-Σ ADC for the SQNR requirement.

Design the decimation system with and without using the NL to satisfy the SQNR in both the cases.

Calculate the filter complexities in each of the two cases.

Check if all possible NL designs are finished.

Is Count N?

Count = Count + 1

Check if all possible Δ-Σ ADC designs are finished. (i.e., whether the required SQNR can be obtained by changing the order/quantizer size).

Yes

No

Yes

No

Stop

Figure 2.2: Flow diagram describing the strategy to be followed in the thesis.
Chapter 3

Quantitative Analyses

3.1 Analysis done for a Pessimistic Estimate of Word Length

For the analysis, two decimation systems are considered—one without the noise-shaping loop (Case 1) and the other with noise-shaping loop between the stages (Case 2). Figures 3.1 and 3.2 show the above mentioned systems.

\[
\begin{align*}
    e_1(n) &\xrightarrow{\Delta-\Sigma\ ADC} \xrightarrow{\text{CIC filter}} \xrightarrow{\downarrow N_1} \xrightarrow{\text{FIR filter}} \xrightarrow{\downarrow N_2} \\
    NTF_{ADC}(\omega T_1) &\quad TF_{CIC}(\omega T_1) &\quad TF_{FIR}(\omega T_2) \\
    L &\quad (L + 1) \log_2 N_1 + N_{ADC} &\quad N_1 \quad \text{FIRord} \quad N_2
\end{align*}
\]

Figure 3.1: Block-Diagram of the $\Delta-\Sigma$ ADC System using case 1 decimation system. Here, the various parameters of the system are also shown.

The total in-band noise power in case 1 is calculated as

\[
P_{\text{noise}} = \frac{1}{2\pi} \int_0^{2\pi} R_{e_1}(\omega T) |NTF_{ADC}(\omega T)TF_{CIC}(\omega T)TF_{FIR}(\omega T)|^2 d\omega T.
\]  

(3.1)

The total in-band noise power in case 2 is calculated as

\[
P_{\text{noise}} = \frac{1}{2\pi} \int_0^{2\pi} R_{e_1}(\omega T) |NTF_{ADC}(\omega T)TF_{CIC}(\omega T)TF_{FIR}(\omega T)|^2 d\omega T \\
+ \frac{1}{2\pi} \int_0^{2\pi} R_{e_2}(\omega T) |NTF_{NL}(\omega T)TF_{FIR}(\omega T)|^2 d\omega T.
\]  

(3.2)
From [1], the required word length at the output of CIC stage can be estimated as
\[ W_{NL_{input}} = (L + 1) \log_2 N_1 + N_{ADC}. \] (3.3)
where,
- \( L \rightarrow \) Order of \( \Delta-\Sigma \) ADC.
- \( N_1 \rightarrow \) Decimation factor of Stage 1.
- \( N_{ADC} \rightarrow \) Quantizer size.

Comparing the two systems for a common in-band noise power requirement that is to be obtained at the output, helps to compare the filter complexity in each case. Various conditions are considered depending on different parameter values. The parameters in the above mentioned systems are listed as follows:

- \( N_{ADC} \rightarrow \) Quantizer size of the \( \Delta-\Sigma \) ADC.
- \( L \rightarrow \) Order of the \( \Delta-\Sigma \) ADC.
- \( OSR \rightarrow \) Oversampling ratio.
- \( N_1 \rightarrow \) Decimation factor of Stage 1.
- \( N_2 \rightarrow \) Decimation factor of Stage 2.
- \( M \rightarrow \) Order of the NL.
- \( NLbits \rightarrow \) Output word length of the NL.
- \( FIR_{ord} \rightarrow \) Order of Stage 2 FIR filter in case 1.
- \( FIR_{ordNL} \rightarrow \) Order of Stage 2 FIR filter in case 2.
The two systems are modelled using MATLAB. Here, a single-quantizer second order 1-bit \( \Delta-\Sigma \) ADC is used. The in-band noise power requirement of the entire system is set by estimating the theoretical maximum in-band noise power at the output of the \( \Delta-\Sigma \) ADC block. This theoretical maximum value depends on three parameters—the order of the \( \Delta-\Sigma \) ADC, the quantizer size \( (N_{ADC}) \) and the oversampling ratio (OSR). Here, the OSR will be considered as a variable while the other two parameters remain constant. The plot in Figure 3.3 shows the variation of the in-band noise power at the output of the \( \Delta-\Sigma \) ADC block with OSR. To study the two decimation systems stated earlier, the in-band noise power requirement of the entire system is set as \(-103dB\) with OSR set at 128. The decimation system in case 1 that satisfies this requirement is designed for \( N_1 = 32 \) and \( N_2 = 4 \). The required FIR filter order is obtained from Figure 3.4. The decimation system using NL (Case 2) can be designed for this requirement by controlling various parameters of the system. Figures 3.5 and 3.6 show the PSD of noise at various points in the system (Case 2). For case 1 (with no NL), the Cost function is given by the equation 3.4,

\[
CF_1 = \frac{FIRord \times ((L + 1) \log_2 N_1 + 1)}{N_2}.
\]  

(3.4)

For case 2 (with NL), the Cost function is given by the equation 3.5

\[
CF_2 = \frac{FIRordNL \times NLbits}{N_2} + M \times (((L + 1) \log_2 N_1 + 1) - NLbits).
\]  

(3.5)

Plotting the in-band noise power for various parameters could serve as a reference for choosing the optimum decimation filter that satisfies the total

Figure 3.3: In-band noise spectrum vs OSR.
in-band noise power requirement. For Δ-Σ ADC chosen above, Figure 3.7 shows the variation of in-band noise power with the parameters—OSR, $N_1$, $N_2$, $M$, NLbits, FIRord, FIRordNL. Here, $M$ is varied from $1 \rightarrow 5$, NLbits is varied from $1 \rightarrow (L + 1) \log_2 N_1$, FIRordNL is varied ±20 around the reference value (=FIRord) and OSR is varied from $16 \rightarrow 128$ in powers of 2. For each OSR value, $N_1$ and $N_2$ are chosen such that $N_1 \geq N_2$ as is the case in a decimation system for efficient implementation.

The parameter values that satisfy the in-band noise power requirement (= −103dB) can be obtained from Figure 3.7. The corresponding filter complexity in each case is calculated and tabulated in Table 3.1.
From the above table, $CF_2 < CF_1$ which proves that the use of a noise-shaping loop reduces the filter complexity in the decimation system. Further reduction in the in-band noise power can be achieved by using minimax optimization algorithm on the magnitude response of the stage 2 FIR filter. The in-band noise power is used as the objective function for optimization, with constraints being the allowable pass band deviation. Figure 3.8 shows the optimized magnitude response of the filter for case 2.

### 3.2 Analysis done for a more Practical Estimate of Word Length using Quantization

In the previous section, a pessimistic estimate of the output word length of the CIC stage (Stage 1) is used to estimate the savings in terms of the filter complexity, that can be obtained by using the noise-shaping loop (NL). This estimate is obtained so as to avoid overflow at the output of the first deci-
Figure 3.7: Variation in the in-band noise power with parameters—\textit{NLbits}, \textit{M} and \textit{FIRordNL}.

In this section, a more practical estimate of the output word length of the CIC stage is used for the analysis. This estimate can be obtained by simply quantizing the output of the CIC filter. Figure 3.9 shows the Δ-Σ ADC system corresponding to this case (Case 3). The filter complexity obtained using this case is compared with that obtained in case 2 (that uses NL). The parameters in the above mentioned systems (Case 2 and Case 3) are listed as follows:

- \( N_{\text{ADC}} \) → Quantizer size of the Δ-Σ ADC.
- \( L \) → Order of the Δ-Σ ADC.
- \( \text{OSR} \) → Oversampling ratio.
- \( N_1 \) → Decimation factor of Stage 1.
- \( N_2 \) → Decimation factor of Stage 2.
Table 3.1: Parameter sets which satisfy the in-band noise power \(= -103dB\). Here, \(FIRord = 102\) and \(W_{NLinput} = 16\).

<table>
<thead>
<tr>
<th>OSR</th>
<th>(N_1)</th>
<th>(N_2)</th>
<th>(M)</th>
<th>(NLbits)</th>
<th>(FIRordNL)</th>
<th>(CF_1)</th>
<th>(CF_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>32</td>
<td>4</td>
<td>2</td>
<td>14</td>
<td>102</td>
<td>408</td>
<td>361</td>
</tr>
<tr>
<td>128</td>
<td>32</td>
<td>4</td>
<td>2</td>
<td>14</td>
<td>82</td>
<td>408</td>
<td>291</td>
</tr>
<tr>
<td>128</td>
<td>32</td>
<td>4</td>
<td>4</td>
<td>13</td>
<td>122</td>
<td>408</td>
<td>412</td>
</tr>
</tbody>
</table>

Figure 3.8: Magnitude reponse of the stage 2 FIR filter after optimization.

- \(M\) \(\rightarrow\) Order of the NL.
- \(CICopbits\) \(\rightarrow\) Pessimistic estimate of the output word length of the CIC stage.
- \(Qbits\) \(\rightarrow\) Output word length of the Quantizer (at Stage 1 output).
- \(NLbits\) \(\rightarrow\) Output word length of the NL.
- \(FIRordQ\) \(\rightarrow\) Order of Stage 2 FIR filter in Case 3.
- \(FIRordNL\) \(\rightarrow\) Order of Stage 2 FIR filter in Case 2.

For the analysis, a single-quantizer second order 1-bit \(\Delta-\Sigma\) ADC is used as in the previous section \((L = 2\) and \(N_{ADC} = 1\)). To study the impact of parameters \(OSR\), \(N_1\) and \(N_2\) on filter complexity in both cases (Case 2 and Case 3), typical values of these parameters are chosen. Table 3.2 shows these chosen values.

The aim of this analysis is to know if the use of NL actually reduces the filter complexity when a practical estimate (obtained by quantization) of
Figure 3.9: Block-Diagram of the ∆-Σ ADC System using case 3 decimation system.

Table 3.2: Typical parameter values chosen for the analysis

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSR</td>
<td>N&lt;sub&gt;1&lt;/sub&gt;</td>
</tr>
<tr>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

the output word length of CIC stage (Stage 1) is used. To achieve this, the in-band noise power at the output of the decimation system is plotted for varying values of parameters Qbits, NLbits, FIRordQ and FIRordNL. The limits of these parameters are chosen as shown in Table 3.3.

Table 3.3: Limits of the parameters chosen for the analysis

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qbits</td>
<td>CIC&lt;sub&gt;CIC&lt;/sub&gt;bits → CIC&lt;sub&gt;CIC&lt;/sub&gt;bits</td>
</tr>
<tr>
<td>NLbits</td>
<td>CIC&lt;sub&gt;CIC&lt;/sub&gt;bits → CIC&lt;sub&gt;CIC&lt;/sub&gt;bits</td>
</tr>
<tr>
<td>FIRordQ</td>
<td>FIRordQ&lt;sub&gt;A&lt;sub&gt;stop&lt;/sub&gt;=A&lt;sub&gt;stop&lt;/sub&gt;_req+8&lt;/sub&gt; → FIRordQ&lt;sub&gt;A&lt;sub&gt;stop&lt;/sub&gt;=A&lt;sub&gt;stop&lt;/sub&gt;_req+24&lt;/sub&gt;</td>
</tr>
<tr>
<td>FIRordNL</td>
<td>FIRordNL&lt;sub&gt;A&lt;sub&gt;stop&lt;/sub&gt;=A&lt;sub&gt;stop&lt;/sub&gt;_req+8&lt;/sub&gt; → FIRordNL&lt;sub&gt;A&lt;sub&gt;stop&lt;/sub&gt;=A&lt;sub&gt;stop&lt;/sub&gt;_req+24&lt;/sub&gt;</td>
</tr>
</tbody>
</table>

The initial value of FIRordQ and FIRordNL is chosen based on the stop-band attenuation required for the FIR filter (Stage 2) to fulfill the minimum attainable in-band noise power (obtained when a brickwall filter is used at the output of the ADC block) requirement at the output of the decimation system when Qbits/NLbits = CIC<sub>CIC</sub>bits (i.e., when no quantization/noise-shaping is used). This stop-band attenuation value of the FIR filter is denoted as A<sub>stop</sub>_req. The minimum attainable in-band noise power requirement (P<sub>attainable</sub>) for typical values of parameters chosen for analysis as shown in Table 3.4.
In Table 3.4, there is a slight difference in the attainable in-band noise power for the same OSR but for different $N_1$ and $N_2$. This is due to the additional in-band attenuation caused by the droop of the CIC filter.

![Images of plots](a) $N_1 = 64, N_2 = 2$  
(b) $N_1 = 16, N_2 = 8$  
(c) $N_1 = 8, N_2 = 2$  
(d) $N_1 = 4, N_2 = 4$

Figure 3.10: Inband noise power—$NL_{bits}$ plots obtained in the analysis for parameters $N_1$, $N_2$ and different stop-band attenuation values (Case 3).

<table>
<thead>
<tr>
<th>OSR</th>
<th>$N_1$</th>
<th>$N_2$</th>
<th>$P_{attainable}(dB)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>64</td>
<td>2</td>
<td>-105</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
<td>2</td>
<td>-103</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
<td>2</td>
<td>-60</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>2</td>
<td>-58</td>
</tr>
</tbody>
</table>

From Figures 3.10–3.14, the values of the various parameters that are required for estimating the filter complexity that satisfies the in-band noise power requirement as given in Table 3.4 for Case 2 and Case 3 are listed in Tables 3.5–3.9. The filter complexities are also listed (CF2 and CF3).

From Tables 3.5–3.9, it can be concluded that, for large values of the parameters, OSR and $N_2$, the savings achieved by using NL dominates that
Figure 3.11: Inband noise power—$NLbits$ plots obtained in the analysis for parameters $N_1$, $N_2$, $M$ and different stop-band attenuation values (Case 2). Here, $M = 2$.

achieved by simple quantization. It can also be concluded that, for $M = L$, the savings that can be achieved using the NL is maximum. In short, the following conclusions are obtained from these results:

- For high values of OSR, irrespective of the value of $N_2$, $M = L$ gives maximum savings.
- For low values of OSR and $N_2$, $M = L$ or $M$ slightly greater than $L$ ($\approx L + 1$) gives maximum savings.

On the whole, from this section, the parameters that account for the suitability of using NL in the decimation system are explored to be: OSR, $N_2$ and $M$. The higher the values of the parameters OSR and $N_2$, the higher the efficiency of filter implementation using NL in the decimation system. In almost all the cases, for $M = L$, the savings achieved are maximum.
Table 3.5: Parameter values with calculated filter complexities (Case 2).
Here, $OSR = 128$, $N_1 = 16$, $N_2 = 8$, $P_{\text{attainable}} = -103dB$, $CICopbits = 18$, $A_{\text{stop req}} = 42dB$.

<table>
<thead>
<tr>
<th>$M$</th>
<th>FIRordNL</th>
<th>NLbits</th>
<th>$CF_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>301</td>
<td>14</td>
<td>531</td>
</tr>
<tr>
<td>2</td>
<td>288</td>
<td>12</td>
<td>444</td>
</tr>
<tr>
<td>3</td>
<td>356</td>
<td>10</td>
<td>469</td>
</tr>
<tr>
<td>4</td>
<td>380</td>
<td>9</td>
<td>463</td>
</tr>
</tbody>
</table>

Table 3.6: Parameter values with calculated filter complexities (Case 3).

<table>
<thead>
<tr>
<th>OSR</th>
<th>$N_1$</th>
<th>$N_2$</th>
<th>$P_{\text{att.}}$</th>
<th>CICopbits</th>
<th>$A_{\text{stop req}}$</th>
<th>FIRordQ</th>
<th>Qbits</th>
<th>$CF_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>128</td>
<td>64</td>
<td>2</td>
<td>-105</td>
<td>21</td>
<td>18</td>
<td>45</td>
<td>18</td>
<td>405</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
<td>2</td>
<td>-103</td>
<td>18</td>
<td>42</td>
<td>288</td>
<td>16</td>
<td>576</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
<td>2</td>
<td>-60</td>
<td>12</td>
<td>18</td>
<td>63</td>
<td>10</td>
<td>315</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>2</td>
<td>-58</td>
<td>9</td>
<td>28</td>
<td>110</td>
<td>9</td>
<td>247</td>
</tr>
</tbody>
</table>

3.3 Analysis for the Relationship between the Order of the Noise-shaping loop ($M$) and the FIR filter order (FIRordNL).

The two systems considered for this analysis are shown in Figures 3.15 and 3.16. These systems are the final decimation stage of the decimation systems considered in the previous analysis. A full bandwidth signal is assumed to be applied to the systems. The two systems are compared for a given signal and noise attenuation requirements.

The analysis starts with the design of decimation system shown in Figure 3.15 (Case 4). A full bandwidth signal is applied to this system. The quantizer size is set to 10 bits. For a given signal and noise attenuation requirement say $60dB$ which is the stop band attenuation requirement of the filter used in the system, the filter order is determined. Here, an $L^{th}$-band filter is used where the decimation factor considered in the analysis is 4 (i.e., $L = 4$). The total noise-power is calculated as a cumulative of two components: the inband noise power component ($P_{\text{inbandQ}}$) and the out-of-band noise power component ($P_{\text{outbandQ}}$). The equations used to calculate there noise power components are given below:

$$P_{\text{inbandQ}} = \frac{1}{\pi} \int_{0}^{\frac{\pi}{N_1}} Re(\omega T)|TF_{HBFQ}(\omega T)|^2 d\omega T$$

(3.6)
Table 3.7: Parameter values with calculated filter complexities (Case 2). Here, \( OSR = 128, N_1 = 64, N_2 = 2, P_{\text{attainable}} = -105\, dB, CICopbits = 21, A_{\text{stop req}} = 18dB. \)

\[
\begin{array}{cccc}
M & FIRordNL & NLbits & CF_2 \\
1 & 68 & 17 & 582 \\
2 & 44 & 18 & 402 \\
3 & 44 & 18 & 405 \\
4 & 48 & 18 & 444 \\
\end{array}
\]

Table 3.8: Parameter values with calculated filter complexities (Case 2). Here, \( OSR = 16, N_1 = 8, N_2 = 2, P_{\text{attainable}} = -60\, dB, CICopbits = 12, A_{\text{stop req}} = 18dB. \)

\[
\begin{array}{cccc}
M & FIRordNL & NLbits & CF_2 \\
1 & 49 & 10 & 247 \\
2 & 52 & 10 & 264 \\
3 & 48 & 10 & 246 \\
4 & 45 & 11 & 251 \\
\end{array}
\]

\[
P_{\text{outbandQ}} = \frac{1}{\pi} \int_{\frac{-\pi}{N_1}}^{0} R_e(\omega T) |TF_{HBFQ}(\omega T)|^2 \, d\omega T + \frac{1}{\pi} \int_{\frac{\pi}{N_1}}^{0} R_{\text{sig}}(\omega T) |TF_{HBFQ}(\omega T)|^2 \, d\omega T
\]  

(3.7)

An interesting fact that can be noticed in the equation used to calculate the out-of-band noise power component is that it consists of two terms: the first term is contributed by the quantization noise while the second term is contributed by the portion of the signal outside the band of interest which will be folded back into the band of interest after decimation.

Using these two noise component values as references, the decimation system shown in Figure 3.16 (Case 5) will be designed. The equations used to calculate the two noise components for this system are given below:

\[
P_{\text{inbandNL}} = \frac{1}{\pi} \int_{0}^{\frac{\pi}{N_1}} R_e(\omega T) |TF_{NL}(\omega T)TF_{HBFNL}(\omega T)|^2 \, d\omega T
\]  

(3.8)

\[
P_{\text{outbandNL}} = \frac{1}{\pi} \int_{\frac{-\pi}{N_1}}^{\pi} R_e(\omega T) |TF_{NL}(\omega T)TF_{HBFNL}(\omega T)|^2 \, d\omega T + \frac{1}{\pi} \int_{\frac{\pi}{N_1}}^{\pi} R_{\text{sig}}(\omega T) |TF_{HBFNL}(\omega T)|^2 \, d\omega T
\]  

(3.9)
First, the output word length of the noise-shaping loop (NL) used in the system is set equal to the quantizer size used in the previous system (Case 4) i.e., 10 bits. The order of the NL is calculated such that the condition $P_{\text{inbandNL}} = P_{\text{inbandQ}}$ is satisfied. Having obtained the required order of NL, the filter order required to satisfy the condition $P_{\text{outbandNL}} = P_{\text{outbandQ}}$ is determined. This is repeated for decreasing values of output word length of NL. The obtained order of NL and the filter order in each case are plotted in Figure 3.17.

From these plots, it can be concluded that the relationship between the order of NL and the filter order required is linear and that for a bit saving in output word length of NL, the order of the NL and the filter order required are to be increased on an average by 1.5 and 50 respectively. Also, from Fig. 3.19 which shows the filter complexity of the modulator, FIR filter and the aggregate of the two, it can be concluded that the optimum FIR filter order is to be chosen (from the plot) first and then the corresponding..
output wordlength of the noise-shaper is selected for that filter order. This would result in the system with least filter complexity. Figure 3.19 shows the frequency spectra at various points in the two systems considered in this analysis.
Figure 3.14: Inband noise power—\(NLbits\) plots obtained in the analysis for parameters \(N_1\), \(N_2\), \(M\) and different stop-band attenuation values (Case 2). Here, \(M = 4\).

Table 3.9: Parameter values with calculated filter complexities (Case 2). Here, \(OSR = 16\), \(N_1 = 4\), \(N_2 = 4\), \(P_{\text{attainable}} = -58dB\), \(CICopbits = 9\), \(A_{\text{stop req}} = 28dB\).

<table>
<thead>
<tr>
<th>(M)</th>
<th>(FIRordNL)</th>
<th>(NLbits)</th>
<th>(CF_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>105</td>
<td>8</td>
<td>211</td>
</tr>
<tr>
<td>2</td>
<td>110</td>
<td>7</td>
<td>196</td>
</tr>
<tr>
<td>3</td>
<td>128</td>
<td>6</td>
<td>201</td>
</tr>
<tr>
<td>4</td>
<td>131</td>
<td>6</td>
<td>208</td>
</tr>
</tbody>
</table>

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Figure 3.15: Block-Diagram of the decimation system (Case 4) used for the analysis.

Figure 3.16: Block-Diagram of the decimation system (Case 5) used for the analysis.
Figure 3.17: Plots obtained in the analysis for determining the relationship between the parameters $M$ and $HB\text{fordNL}$. 
Figure 3.18: Plot showing the required filter complexities for different output wordlengths of the noise-shaping loop.
Figure 3.19: a) Frequency spectrum showing the signal and quantization noise at the input and output of NL in Case 5 decimation system. b) Magnitude response of the filter. c) Frequency spectra at the output of the Case 5 decimation system.
Chapter 4

Conclusion

- The proposed technique of using a noise-shaping loop in the decimation system helps in reducing the filter complexity in later stages of decimation.

- The savings achieved using the noise-shaping loop is more than that achieved using pure quantization.

- The parameters \( \text{OSR} \), \( N_2 \) and \( M \) determine the suitability of the proposed technique.

- For Order of Delta-Sigma ADC \( M = \) Order of the Noise-shaping loop \( L \), maximum savings are achieved in almost all cases.

- There exists a linear relationship between the order of the Noise-shaping loop and the FIR filter order.
Chapter 5

Future work

- Further study on the design complexity introduced in the system in terms of stability due to the noise-shaping loop can be done.
- Architectures that suit this implementation can be evaluated.
- This technique can further be designed physically and evaluated to verify if the savings obtained in the system-level can actually be obtained in the hardware.
Bibliography


