Thermal Stability and Dopant Segregation for Schottky Diodes With Ultrathin Epitaxial NiSi$_{(2\text{-}y)}$

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Thermal Stability and Dopant Segregation for Schottky Diodes with Ultrathin Epitaxial $NiSi_{2-y}$

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***Abstract*—The Schottky barrier height (SBH) of an ultrathin epitaxial $NiSi_{2-y}$ film grown on Si(100) is significantly modified by means of dopant segregation (DS). The DS process begins with the $NiSi_{2-y}$ formation and is followed by dopant implantation and drive-in annealing. The rapid lattice restoration and superior morphological stability upon heat treatment up to 800 °C allows the epitaxial $NiSi_{2-y}$ film to take full advantage of the DS process. For drive-in annealing below 750 °C, the effective SBH is altered to ~0.9-1.0 eV for both electrons and holes by B- and As-DS, respectively, without deteriorating the integrity of the $NiSi_{2-y}$ film.**

***Index Terms*—Ultrathin, epitaxy, $NiSi_2$, Schottky barrier height, dopant segregation, morphological stability**

I. INTRODUCTION

An ultrathin silicide film below 10 nm in thickness is projected to be necessary for contact formation in CMOS technologies beyond the 22-nm node [1]. For these technology nodes, Ni-based silicide will most likely continue its dominance in the source/drain contact formation. Recent publications show that a $NiSi_{2-y}$ film grows epitaxially on Si(100) if the initial thickness of Ni-Pt alloys is less than 4 nm and the Pt addition is restricted below 10% [2]-[5]. Polycrystalline $Ni_{1-x}Pt_xSi$ films will form for other thickness and/or composition combinations. In contrast to low-temperature agglomeration of poly-$Ni_{1-x}Pt_xSi$ films, epitaxial $Ni(Pt)Si_{2-y}$ remains morphologically intact upon annealing up to 800 °C. The latest advancements in formation of ultrathin Ni-based silicide films have led to a reproducible growth of such epitaxial $NiSi_{2-y}$ films in a very simple manner [6],[7]. There is, therefore, a need to investigate if the Schottky barrier height (SBH) of such epitaxial $NiSi_{2-y}$ films can be tuned to improve carrier injection for metallic source/drain MOSFETs as an example [8]-[10]. In the present study, Schottky diodes with an epitaxial $NiSi_{2-y}$ film for contact formation are fabricated. Dopant segregation (DS) is then used to achieve the desired modification of effective SBH for the $NiSi_{2-y}$/Si contact. Alternative approaches for SBH modification not studied here include surface passivation [11] and alloying [12,13].

II. EXPERIMENTAL PROCEDURE

To fabricate the Schottky diodes, both *n*- and *p*-type epitaxy Si(100) wafers were used as the starting substrate material. The wafers have a heavily doped substrate to avoid adverse effects of series resistance during electrical characterization [14]-[16]. The lightly doped epitaxial layers were 8.1-9.9 μm thick with a resistivity of 17-25 Ω·cm for the *n*-type wafers, and 5.8-7.2 μm thick with a resistivity of 11-15 Ω·cm for the *p*-type ones. With a conventional LOCOS isolation to define circular diodes of 400 μm in diameter, a 3-nm-thick Ni was deposited in a sputter deposition chamber. Silicidation was carried out in a rapid thermal processing (RTP) chamber at 500 or 750 °C for 30 s, in N_2 atmosphere. The resultant epitaxial $NiSi_{2-y}$ films were about 8 nm in thickness [2]. The wafers were then immersed in an H_2SO_4:H_2O_2 (4:1) solution at 120 °C for 10 min to strip the unreacted Ni from the SiO_2 surface. For the wafers with the silicide formation at 500 °C, B or As was ion implanted (I/I) to a dose of $1 \cdot 10^{15}$ cm^{-2} into the preformed epitaxial $NiSi_{2-y}$ films; B to the $NiSi_{2-y}$ formed on the *n*-type substrate at 2 keV with a tilted angle of 45 degrees and As to the $NiSi_{2-y}$ formed on the *p*-type substrate at 3 keV with a tilted angle of 7 degrees. Monte Carlo simulation [17] indicated that the implanted ions were mostly confined in the ultrathin $NiSi_{2-y}$ films. Subsequently, isochronal drive-in anneals at 500 to 800 °C at a 50-°C interval, each anneal for 30 s, were performed. This process for DS, also known as SADS (silicide as diffusion source), has been successfully employed by several research groups [15],[16],[18]-[21]. The effective SBH, to electrons (ϕ_{bn}) and to holes (ϕ_{bp}), of the epitaxial $NiSi_{2-y}$ films was extracted through characterizing the diodes by means of capacitance-voltage (*C-V*) measurements on an HP4284A precision *LCR* meter at 100 kHz, following the procedure described in [15]. For sheet resistance monitoring as well as physical analyses using secondary ion mass spectroscopy (SIMS) and cross-sectional transmission electron microscopy (XTEM), blanket samples on Si(100) were also prepared following the same procedure described above.

III. RESULTS AND DISCUSSION

Interaction of the 3-nm thick Ni film with Si(100) at 500 °C leads to epitaxial growth of $NiSi_{2-y}$, according to extensive XTEM, diffraction, pole-figure, resistance, and Raman analyses [2]-[5]. After B and As I/I, the resistance of the silicide films is rather high around 150 Ω/□ as shown in Fig. 1. Upon subsequent drive-in annealing, the resistance for both B- and As-implanted $NiSi_{2-y}$ films keeps decreasing until it approaches the value for an as-formed $NiSi_{2-y}$ film at 700-750 °C. The B or As I/I is anticipated to generate damage in the silicide film. As

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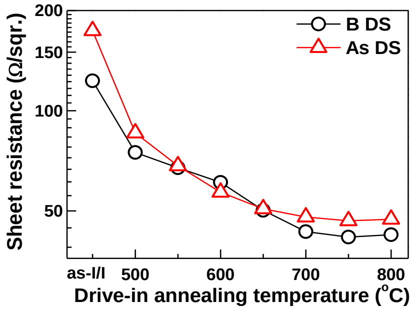

Fig. 1. Sheet resistance of epitaxial $NiSi_{2-y}$ films first ion-implanted with B or As and then followed by drive-in annealing at different temperatures.

seen in Fig. 2(a) for a high-resolution XTEM image, the near-surface region of the silicide films is indeed severely damaged by B I/I. The annealing has apparently caused structural recovery and lattice restoration of the epitaxial $NiSi_{2-y}$ film, cf. Fig. 2(b), and thereby led to the successive resistance decrease below 750 °C. For comparison, the high-resolution XTEM image in Fig. 2(c) shows a defect-free structure for the epitaxial $NiSi_{2-y}$ film formed at 750 °C. Moreover, the I/I and subsequent drive-in annealing have led to no observable loss of $NiSi_{2-y}$ since all the films in Fig. 2 retain their 8-nm thickness. It is worth noting that the temperature behavior in Fig. 1 is identical to that for the $NiSi_{2-y}$ formation at different silicidation temperatures [2],[5]. For comparison, poly-$Ni_{1-x}Pt_xSi$ films of comparable thickness tend to agglomerate with a sharp resistance increase below 600 °C [2],[3]. Hence, the observed morphological stability as well as the ability of rapid lattice restoration is significant for implementation of the DS process for the epitaxial $NiSi_{2-y}$ films.

The extracted effective SBH values for both *p*- and *n*-type Schottky diodes are summarized in Table I for the samples prepared with two silicidation temperatures. For the Schottky diodes formed at 500 °C, the SBH extraction failed due to a large leakage current. The leakage could be due to some imperfections at the interface of the ultrathin epitaxial $NiSi_{2-y}$ film formed at 500 °C [2],[5]. For the $NiSi_{2-y}$ films formed at 750 °C with a much improved interfacial morphology in Fig. 2(c) [2],[5], ϕ_{bn}=0.81 eV was obtained while it remained to be challenging to extract the low ϕ_{bp} due to large leakage. This ϕ_{bn} value is almost identical to that extracted for type-*B* $NiSi_2$ epitaxially grown on Si(111), *i.e.*, 0.79 eV [22]. However, it departs significantly from ϕ_{bn}=0.4 eV obtained for epitaxial $NiSi_2$ on Si(100) [23]. The mysterious difference in ϕ_b between type-*B* $NiSi_2$ on Si(111) and $NiSi_2$ on Si(100) was accounted for by invoking inhomogeneities at the $NiSi_2$/Si(100) interface [22]. It remains unclear if the $NiSi_{2-y}$/Si interface obtained in the present study is more homogeneous than produced 20 years ago, but subtle details of the interfacial structure have been shown to play a critical role in determining SBH [24],[25].

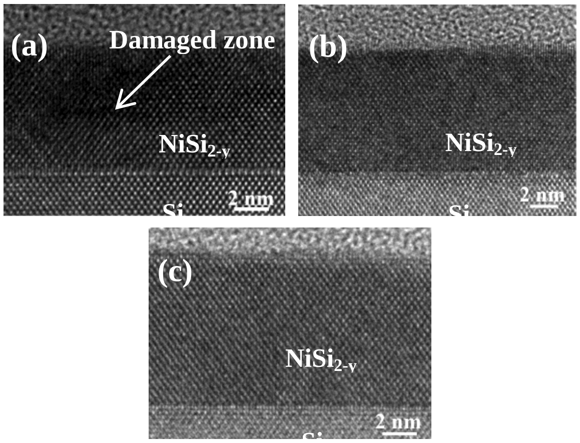

Fig. 2. High-resolution XTEM images for $NiSi_{2-y}$ films formed at 500 °C and then (a) I/I with B and (b) after subsequent drive-in annealing at 750 °C. For comparison, an epitaxial $NiSi_{2-y}$ film formed at 750 °C is depicted in (c).

TABLE I

EXTRACTED SBH VALUES AT TWO SILICIDATION TEMPERATURES AND DIFFERENT DRIVE-IN ANNEALING TEMPERATURES. FOR THE LATTER, B I/I INTO $NiSi_{2-y}$ ON *n*-TYPE Si FOR EXTRACTION OF ϕ_{bn} WHILE As I/I INTO $NiSi_{2-y}$ ON *p*-TYPE Si FOR EXTRACTION OF ϕ_{bp}.

Silicidation temperature (°C)	ϕ_{bn} (eV)	ϕ_{bp} (eV)
500	-	-
750	0.81	-
Drive-in annealing temperature (°C)	ϕ_{bn} (eV)	ϕ_{bp} (eV)
500	0.99	-
550	0.96	-
600	0.99	-
650	1.0	0.86
700	1.0	0.92
750	0.96	0.93

With DS, the effective SBHs, which are also shown in Table I, can be modified to ~0.9-1.0 eV for both polarities after an appropriate drive-in annealing between 500 and 750 °C. Dopant diffusion in the epitaxial $NiSi_{2-y}$ films leading to dopant accumulation at the silicide/Si interface at 650 and 750 °C is evident for both B, Fig. 3(a), and As, Fig. 3(b). For comparison, depth profiling of the dopants in the as-implanted samples are also depicted. The peak broadening at the $NiSi_{2-y}$/Si interface as well as the long B and As tails are attributed to SIMS artifacts, because (i) no I/I damage occurred to the Si substrate and intrinsic diffusion should be negligible below 750 °C [16],[26]; (ii) the longer As tail than the B one would suggest a more rapid As diffusion, contradicting the commonly accepted picture of the opposite [26]; and (iii) diffusion at different temperatures would yield B tails in the Si substrate with distinct slopes, so the parallel B tails are indicative of an artifact. Hence, despite distinct differences in crystallographic phase and crystallinity, the effect of DS on effective SBHs of the epitaxial $NiSi_{2-y}$ films found here are consistent with our previous results with

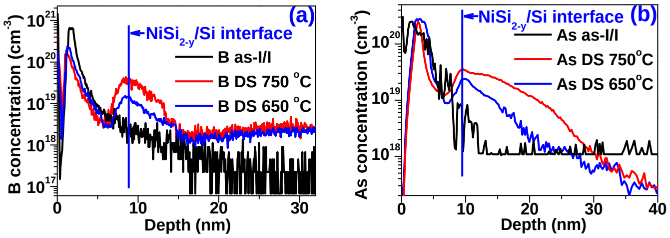

Fig. 3. Dopant depth profiling by means of SIMS showing accumulation of (a) B and (b) As at the $NiSi_{2-y}$/Si interface upon drive-in annealing at 650 and 750 °C. Results for the as-implanted samples are included for comparison.

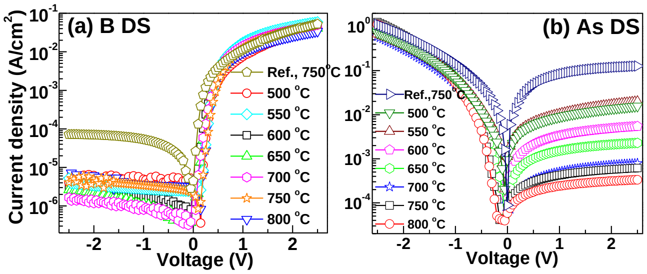

Fig. 4. *I-V* characteristics of $NiSi_{2-y}$/Si diodes on (a) *n*-type Si substrate with B-DS and (b) *p*-type substrate with As-DS, at different drive-in annealing temperatures. Results without DS are included for comparison.

poly-NiSi and PtSi films [15],[16]. This observation further confirms the robustness of the SADS process for DS.

According to the relationship $\phi_{bn}+\phi_{bp}=E_g$, ϕ_{bn} and ϕ_{bp} of ~0.1-0.2 eV have thus been realized for the Schottky diodes with $NiSi_{2-y}$ through As- and B-DS, respectively. The SBH modulation by DS is also confirmed by current-voltage (*I-V*) characterization of the Schottky diodes. In Fig. 4, the *I-V* characteristics show a consistent trend for both types of diodes with a decreasing leakage current density, J_r, at reverse bias with increasing drive-in annealing temperature. The smaller variations in J_r for the *n*-type diodes (*i.e.*, on *n*-type substrate) faithfully reflect the smaller changes in ϕ_{bn} reported in Table I. For the *p*-type diodes, the very small starting ϕ_{bp} requires higher drive-in annealing temperatures, *i.e.*, ≥650 °C, to suppress J_r for a reliable extraction of ϕ_{bp}. The excellent morphological stability of the epitaxial $NiSi_{2-y}$ films practically allows such high-temperature processing so as to attain the desired low ϕ_{bn} and ϕ_{bp} without deteriorating the integrity of the silicide films.

IV. CONCLUSIONS

This work demonstrates a successful implementation of SADS for DS in Schottky diodes with an 8-nm thick epitaxial $NiSi_{2-y}$ film as the metal contact. The excellent morphological stability of the epitaxial $NiSi_{2-y}$ film allows annealing at temperatures up to 800 °C for damage repair and dopant diffusion after ion implantation of B and As into the silicide films. Initially damaged, the $NiSi_{2-y}$ film restores its defect-free crystallographic structure with low resistivity and sharp interface to the underlying Si substrate. Finally, the effective SBH is reduced from 0.3 to 0.1 eV for *p*-type diodes and from 0.8 to 0.2 eV for *n*-type diodes.

REFERENCES

[1] International Technology Roadmap for Semiconductors, 2009 update, http://public.itrs.net.

[2] J. Luo, Z.-J. Qiu, C. L. Zha, Z. Zhang, D. P. Wu, J. Lu, J. Åkerman, M. Östling, L. Hultman, and S.-L. Zhang, "Surface-energy triggered phase formation and epitaxy in nanometer-thick $Ni_{1-x}Pt_x$ silicide films," *Appl. Phys. Lett.*, vol. 96, no. 3, pp. 031911/1-3, Jan. 2010.

[3] Z. Zhang, S.-L. Zhang, B. Yang, Y. Zhu, S.M. Rossnagel, S. Gaudet, A.J. Kellock, J. Jordan-Sweet, and C. Lavoie, "Specific resistivity and morphological stability of sub-10 nm silicide films of $Ni_{1-x}Pt_x$ on Si substrate," *Appl. Phys. Lett.*, vol. 96, no. 7, pp. 071915/1-3, Feb. 2010.

[4] K. De Keyser, C. Van Bockstael, R. L. Van Meirhaeghe, C. Detavernier, E. Verleysen, H. Bender, W. Vandervorst, J. Jordan-Sweet, and C. Lavoie, "Phase formation and thermal stability of ultrathin nickel-silicides on Si(100)," *Appl. Phys. Lett.*, vol. 96, no. 17, pp. 173503/1-3, Apr. 2010.

[5] J. Lu, J. Luo, S.-L. Zhang, M. Östling, and L. Hultman, "On epitaxy of ultrathin $Ni_{1-x}Pt_x$-silicide films on Si(001)," *Electrochem. Solid-State Lett.*, vol. 13, pp. H360-H362, Oct. 2010.

[6] Z. Zhang, B. Yang, Y. Zhu, S. Gaudet, S.M. Rossnagel, A. J. Kellock, A. Ozcan, C. Murray, P. Desjardins, S.-L. Zhang, J. Jordan-Sweet, and C. Lavoie, "Exploitation of a self-limiting process for reproducible formation of ultrathin $Ni_{1-x}Pt_x$ silicide films," *Appl. Phys. Lett.*, vol. 97, no. 25, pp. 252108/1-3, Dec. 2010**.**

[7] X. Gao, J. Andersson, T. Kubart, T. Nyberg, U. Smith, J. Lu, L. Hultman, A.J. Kellock, Z. Zhang, C. Lavoie, and S.-L. Zhang, "Ultrathin epitaxial $NiSi_2$ films with predetermined thickness," *Electrochem. Solid-State Lett.*, vol. 14, no. 7, pp. H268-H270, July 2011.

[8] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048-1058, May 2006.

[9] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T. J. King, and C. Hu, "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime," in *IEDM Tech. Dig.*, 2000, pp. 57-60.

[10] J. Luo, Z.-J. Qiu, Z. Zhang, M. Östling, and S.-L. Zhang, "Interaction of NiSi with dopants for metallic source/drain applications," *J. Vac. Sci. Technol. B*, vol. 28, no. 1, pp. C1I1-C1I11, Jan. 2010.

[11] Q. T. Zhao, U. Breuer, E. Rije, St. Lenk, and S. Mantl, "Tuning of NiSi/Si Schottky barrier heights by sulfur segregation during Ni silicidation," *Appl. Phys. Lett.*, vol. 86, no. 6, pp. 062108/1-3, Feb. 2005.

[12] L. E. Terry and J. Saltich, "Schottky barrier heights of nickel-platnum silicide contacts on *n*-type Si," *Appl. Phys. Lett.*, vol. 28, no. 4, pp. 229-231, Feb. 1976.

[13] R. T. P. Lee, T.-Y. Liow, K.-M. Tan, A. E.-J. Lim, H.-S. Wong, P.-C. Lim, D.M. Y. Lai, G.-Q. Lo, C.-H. Tung, G. Samudra, D.-Z. Chi, and Y.-C. Yeo, "Novel nickel-alloy silicides for source/drain contact resistance reduction in n-channel multiple-gate transistors with sub-35nm gate length," in *Int. Electron Dev. Meet. Tech. Dig.*, 2006, pp. 851-854.

[14] D. Connelly and P. Clifton, "Comments on 'Effective modulation of Ni silicide Schottky barrier height using chlorine ion implantation and segregation'," *IEEE Electron Device Lett.*, vol. 31, pp. 417-418, May 2010.

[15] Z. Zhang, Z.-J. Qiu, R. Liu, M. Östling and S.-L. Zhang, "Schottky-barrier height tuning by means of ion implantation into preformed silicide films followed by drive-in annealing," *IEEE Electron Device Lett.*, vol. 28, no. 7, pp. 565-568, Jul. 2007.

[16] Z.-J. Qiu, Z. Zhang, M. Östling and S.-L. Zhang, "A comparative study of two different schemes to dopant segregation at NiSi/Si and PtSi/Si interfaces for Schottky barrier height lowering," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 396-403, Jan. 2008.

[17] J. F. Ziegler, "SRIM-2010 computer program", available at http://www.srim.org/.

[18] A. Kinoshita, Y. Tsuchiya, A. Yagishita, K. Uchida, and J. Koga, "Solution for high performance Schottky-source/drain MOSFETs: Schottky barrier height engineering with dopant segregation technique," in *VLSI Symp. Tech. Dig.*, 2004, pp. 168-169.

[19] A. Kinoshita, C. Tanaka, K. Uchida, and J. Koga, "High-performance 50-nm-gate-length Schottky-source/drain MOSFETs with dopant segregation junctions," in *VLSI Symp. Tech. Dig.*, 2005, pp. 158-159.

[20] M. Zhang, J. Knoch, Q.T. Zhao, St. Lenk, U. Breuer, and S. Mantl, "Schottky barrier height modulation using dopant segregation in Schottky-barrier SOI-MOSFETs," *Proc. ESSDERC*, 2005, pp. 457-460.

[21] M. Sinha, E. F. Chor, and Y.-C. Yeo, "Tuning the Schottky barrier height of nickel silicide on p-silicon by aluminum segregation," *Appl. Phys. Lett.*, vol. 92, no. 22, pp. 222114/1-3, June. 2008**.**

[22] R. T. Tung, "Schottky-barrier formation at single-crystal metal-semiconductor interfaces," *Phys. Rev. Lett.*, vol. 52, pp. 461–464, Feb. 1984.

[23] R. T. Tung, A. F. J. Levi, J. P. Sullivan, and F. Schrey, "Schottky-barrier inhomogeneity at epitaxial $NiSi_2$ interfaces on Si(100)," *Phys. Rev. Lett.*, vol. 66, pp. 72–75, Jan. 1991.

[24] M. Liehr, P. E. Schmid, F. K. LeGoues, and P. S. Ho, "Correlation of Schottky-barrier height and microstructure in the epitaxial Ni silicides on Si (111)," *Phys. Rev. Lett.*, vol. 54, no. 19, pp. 2139-2142, May 1985.

[25] R. T. Tung, "Recent advances in Schottky barrier concepts," *Mater. Sci. Eng. R*, vol. 35, pp. 1-138, 2001.

[26] J. D. Plummer, M. D. Deal, and P. B. Griffin, *Silicon VLSI Technology, Fundamentals, Practice and Modeling*, Prentice Hall, Inc. Upper Saddle River, New Jersey, 2000, pp. 486-497 and related references therein.