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MUHAMMAD ABBAS and Oscar Gustafsson, Switching Activity Estimation of CIC Filter Integrators, 2010, Asia Pacific Conf. on Postgraduate Research in Microelectronics and Electronics, Shanghai, China.

<http://dx.doi.org/10.1109/PRIMEASIA.2010.5604971>

Postprint available at: Linköping University Electronic Press

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-70452>

Switching Activity Estimation of CIC Filter Integrators

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Abstract—In this work, a method for estimation of the switching activity in integrators is presented. To achieve low power, it is always necessary to develop accurate and efficient methods to estimate the switching activity. The switching activities are then used to estimate the power consumption. In our work, the switching activity is first estimated for the general purpose integrators and then it is extended for the estimation of switching activity in cascaded integrators in CIC filters.

I. INTRODUCTION

Low power design is always a desirable criteria in integrated circuit designs. To accomplish this, it is necessary to find accurate and efficient ways and approaches that can be used to estimate the power consumption and the important factors that are contributing to it. The switching activity is one such factor that needs to be considered to make sure that a low power design is feasible. Therefore it is necessary to develop accurate models at the algorithm level that can be used to estimate the switching activity. An algorithm can be modified at the higher level to achieve low power design goals. The power consumption is generally considered to be proportional to the switching activity, which is defined as the average number of transitions between two logic levels in one clock cycle. In many low power designs, the power factor that is of interest is the average power, since it affects the battery life time that is important for hand held and portable devices [1], [2].

The average dynamic power consumption can be approximated by [3]

$$P_{dyn} = \frac{1}{2}\alpha f_c C_L V_{DD}^2, \quad (1)$$

where α is the switching activity, f_c is the clock frequency, C_L is the load capacitance and V_{DD} is the supply voltage.

The glitches i.e., unwanted transitions, are considered to be the major source that increase the switching activity as they propagate to subsequent stages [4]. Latches may be used to reduce the power consumption by eliminating glitch propagation [5]–[7].

There are various papers [8], [9] which have power models for the estimation of the dynamic power consumption in digital filter structures. The elements considered in the power models are full adders and registers or flip-flops. The basic inherent assumption made in these models is that all full adders in the digital filter structures have comparable switching activity. To further improve the accuracy of these power models, it is important to consider accurate estimated values of switching

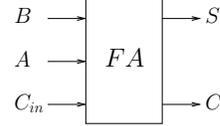


Fig. 1. Full adder.

activities for each structure. Specifically, in this paper we are concerned with estimation of the switching activity of CIC integrators structure. The accurate estimation of switching activity is important because it is one of the important factors that is contributing to dynamic power consumption.

II. GENERAL INTEGRATORS

A. One's Probability

The one's probability is the statistical probability that the signal value is one at the end of a clock cycle. For a signal, X , the one's probability is denoted P_X . Consider a full adder as shown in Fig. 1. The one's probability of the sum output, P_S , and the carry output, P_C , can be written as

$$P_S = P_A + P_B + P_{C_{in}} + 4P_A P_B P_{C_{in}} - 2P_A P_B - 2P_A P_{C_{in}} - 2P_B P_{C_{in}}, \quad (2)$$

and

$$P_C = P_A P_B + P_A P_{C_{in}} + P_B P_{C_{in}} - 2P_A P_B P_{C_{in}}, \quad (3)$$

respectively.

Now, if the full adder is used in an integrator, as shown in Fig. 2, the one's probability of one input, in this case B , will be the same as the one's probability of the sum output. Hence, when inserting $P_B = P_S$ in (2) we get

$$P_S = \frac{P_A + P_{C_{in}} - 2P_A P_{C_{in}}}{2P_A + 2P_{C_{in}} - 4P_A P_{C_{in}}} = \frac{1}{2}. \quad (4)$$

This gives that the one's probability of the sum output is independent of the one's probability of the A and C_{in} inputs when used in an integrator. For the carry output we have, assuming that $P_B = P_S = \frac{1}{2}$,

$$P_C = \frac{P_A}{2} + \frac{P_{C_{in}}}{2}. \quad (5)$$

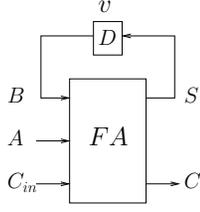


Fig. 2. Full adder with register used in integrator.

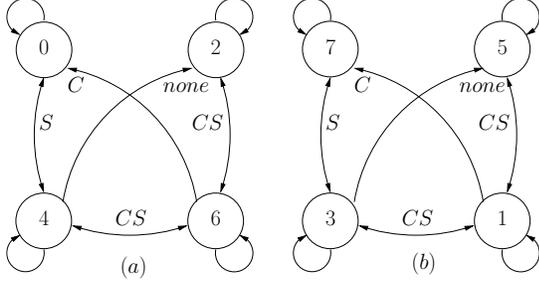


Fig. 3. State transition diagram of an integrator with states representing the input values and cases (a) and (b) for carry input of zero and one respectively.

B. Switching Activity

The computation of the switching activity of general purpose integrators is done by computing the transition probability of all possible transitions for each full adder involved. A state transition graph is shown in the Fig. 3, where a state value represents the input values. A certain type of switching at the output occurs as a result of the transition between two states as shown by branch symbols. We know that for a full adder, when at least one of the three inputs is changed, the outputs may perform a transition. The switching of the sum, carry, or both of the full adder outputs are considered.

A model for estimation of the power consumption as a result of switching activity in a full adder cell was proposed in [10]. The symbols used in this model to represent the three possible types of transitions are S , C , and CS representing the switching of the sum, carry, and both of the sum and carry outputs at the same time, respectively. The difference in our model is that we have a feedback path from the sum output to one of the inputs of the full adder cell that is used as an integrator as shown in Fig. 2.

We first assume that the value of the state variable v is the same as the value of the B input of the integrator that is B , as it is feedback to the input. We showed earlier in (4) that the one's probability of the sum output S as well as the B input is $\frac{1}{2}$. Therefore the one's probability of the state variable is also considered to be $\frac{1}{2}$. However, the switching activity of the state variable v denoted by $\alpha(v)$ differs from what the sum output has. The reason behind this is that the sum output may switch a number of times during one clock cycle depending the values of the carry input as well as of the other input A of the integrator. However, the state variable may only switch at the start of the clock cycle depending its initial value and the value of the S output. Hence, it may switch only once per

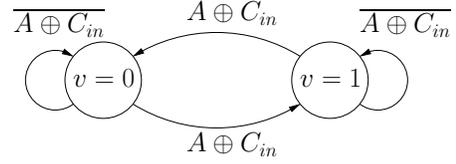


Fig. 4. State transition diagram.

clock cycle. Its transition activity is computed with the help of the state transition graph shown in Fig. 4.

The transition activity of the state variable v as a function of P_{A_k} and $P_{C_{k-1}}$ is given by

$$\alpha_{v_k} = P_{A_k} + P_{C_{k-1}} - 2P_{A_k}P_{C_{k-1}}, \quad (6)$$

where P_{A_k} and $P_{C_{k-1}}$ represents the one's probability of the input A and carry input C_{k-1} respectively. Here k is the full adder index.

For our case, where the transition activity of one input is the same as that of the state variable, v , that represents the feedback of the sum output S to the B input, the switching activity of the carry output as a function of $\alpha(S)$, $\alpha(C)$, and $\alpha(CS)$ that represents the transition activities of the carry, sum, and both of the outputs turns out to be as follows

$$\alpha_{C_k} = \begin{cases} 0, & k < 0, \\ \alpha(C_k) + \alpha(CS_k), & k \geq 0, \end{cases} \quad (7)$$

and for the sum output it is written as

$$\alpha_{S_k} = \alpha(S_k) + \alpha(CS_k). \quad (8)$$

The transition activities $\alpha(S)$, $\alpha(C)$ and $\alpha(CS)$ for a full adder stage in an integrator are

$$\alpha(C_k) = \frac{1}{2}\alpha_{A_k}\alpha_{v_k} + (\alpha_{A_k} + \frac{1}{2}\alpha_{v_k} - 2\alpha_{A_k}\alpha_{v_k})\alpha_{C_{in}}, \quad (9)$$

$$\alpha(S_k) = \frac{1}{2}(\alpha_{A_k} + (1 - 2\alpha_{A_k}\alpha_{v_k})\alpha_{C_{in}} - 2\alpha(C_k) + \alpha_{C_{k-1}}), \quad (10)$$

$$\alpha(CS_k) = \alpha(S_k) + \alpha_{v_k}(1 - \alpha_{A_k} - (1 - 2\alpha_{A_k})\alpha_{C_{in}}), \quad (11)$$

where, $\alpha_{C_{in}} = 0$ for $k > 0$.

If we assume that the carry input C_{in} and also the switching activity of the carry input $\alpha_{C_{in}}$ of first full adder is zero, then by substituting $\alpha_{C_{in}} = 0$ and making use of (6), the general equations used for the computation of the transition activities of each full adder stage in the CIC integrator case can be simplified as

$$\begin{cases} \alpha(C_k) = \frac{1}{2}\alpha_{A_k}\alpha_{v_k}, \\ \alpha(S_k) = \frac{1}{2}(\alpha_{A_k} - 2\alpha(C_k) + \alpha_{C_{k-1}}), \\ \alpha(CS_k) = \alpha(S_k) + \alpha_{v_k}(1 - \alpha_{A_k}). \end{cases} \quad (12)$$

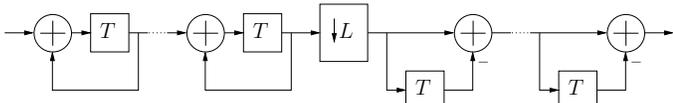


Fig. 5. CIC filter structure as a cascade of integrators and differentiators.

III. CIC FILTER INTEGRATORS

A CIC filter is a multiplierless decimation filter and is very efficient in terms of computational complexity as compared to other decimation filter implementations. It has a lowpass magnitude response. As the name suggests, it is a cascade of integrators and comb filters as shown in the Fig. 5. Its filtering characteristics are improved with the increase of these stages. Since the decimation block is in-between the integrator section and the comb section, the integrator section operates at higher sample rate in comparison to the comb section. The advantage in terms of computational complexity is mainly because of its regular multiplierless implementation which makes it suitable for sample rate applications and furthermore no memory is required for the storage of filter coefficients [11], [12].

The gain of the CIC filter, $(RM)^N$, determines the integrator registers size in the integrator section. R is the decimation factor of the filter, M is the differential delay in the comb section, and N is the number of stages in the CIC filter. If the wordlength of the integrator registers is not sufficient, the filter can be unstable because of overflow. If the output wordlength follows [11]

$$B_{out} = B_{in} + N \lceil \log_2(RM) \rceil, \quad (13)$$

where, B_{out} is the output and B_{in} is the input wordlength of the CIC filter, then the integrators will not overflow.

A. One's Probability

Let us consider an integrator using N bits, where the input to the integrator is W bits. Let us also denote the carry input to the k :th full adder, $1 \leq k \leq N$, as C_k and the output carry bit similarly as C_{k+1} . Now, for the W input bits we assume $P_A = 1/2$ and for the remaining $N - W$ full adders¹ $P_A = 0$. Furthermore, for the first full adder we have $C_0 = 0$. This gives the following one's probability for the carry output

$$P_{C_k} = \begin{cases} \frac{P_{C_{k-1}}}{2} + \frac{1}{4}, & 1 \leq k \leq W, \\ \frac{P_{C_{k-1}}}{2}, & W + 1 \leq k \leq N. \end{cases} \quad (14)$$

The one's probability for a 40-bit integrator in CIC filter with different values of W is shown in Fig. 6.

B. Switching Activity

We consider two cases here while taking into account the one's probability of A for the LSB's and the MSB's of the integrator and then compute the transition activities based on the equation given above.

¹These can in practice be implemented as half adders since the third full adder input is always zero.

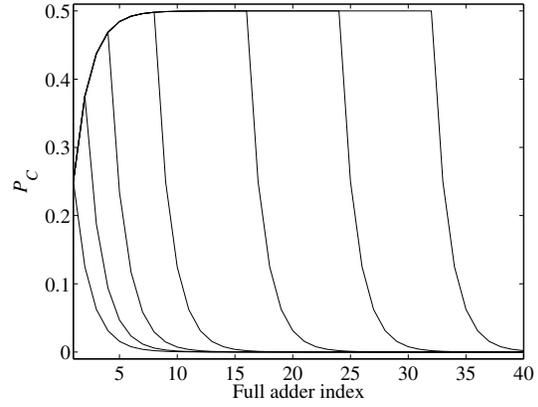


Fig. 6. One's probability for the carry output bit in a 40-bit integrator with various input wordlengths, $W = \{1, 2, 4, 8, 16, 24, 32\}$.

As we know from (6), the transition activity of the state variable v is a function of the one's probability of the A input. So its values for the MSB's and the LSB's of the integrator are given by,

$$\alpha_{v_k} = \begin{cases} \frac{1}{2}, & 1 \leq k \leq W, \\ P_{C_{k-1}}, & W + 1 \leq k \leq N. \end{cases} \quad (15)$$

From the transition activity values of v as given in (15), the carry transition activity for the k -th adder stage is given by

$$\alpha(C_k) = \begin{cases} \frac{1}{4}\alpha_{A_k}, & 1 \leq k \leq W, \\ 0, & W + 1 \leq k \leq N. \end{cases} \quad (16)$$

For the sum output, the transition activity is

$$\alpha(S_k) = \begin{cases} \frac{1}{4}(\alpha_{A_k} + 2\alpha_{C_{k-1}}), & 1 \leq k \leq W, \\ \frac{1}{2}\alpha_{C_{k-1}}, & W + 1 \leq k \leq N. \end{cases} \quad (17)$$

and finally, the CS transition activity for both cases, i.e., $P_{A_k} = \frac{1}{2}$ and $P_{A_k} = 0$, is given by

$$\alpha(CS_k) = \begin{cases} \frac{1}{4}(2 - \alpha_{A_k} + 2\alpha_{C_{k-1}}), & 1 \leq k \leq W, \\ \frac{1}{2}\alpha_{C_{k-1}} + P_{C_{k-1}}, & W + 1 \leq k \leq N. \end{cases} \quad (18)$$

IV. RESULTS

To show the viability of the derived equations for the estimation of switching activity in CIC digital integrators, a VHDL model was developed for a 20-bits length three stage integrator. The input is applied at the first stage of CIC integrator section and the outputs to the next stage integrator are fed after the shifts to reduce the propagation of glitches. The model results for an input wordlength of 8 bits are shown in Fig. 7. The remaining inputs of the first stage integrator are assumed to be zero in this case. As it can be seen from Fig. 7, the carry and sum switching activities of the first integrator stage are of only interest. These two values of switching activities are somehow comparable for all full adder indexes of the later integrator stages. The derived model equations are also verified for the first stage of integrator section with different input

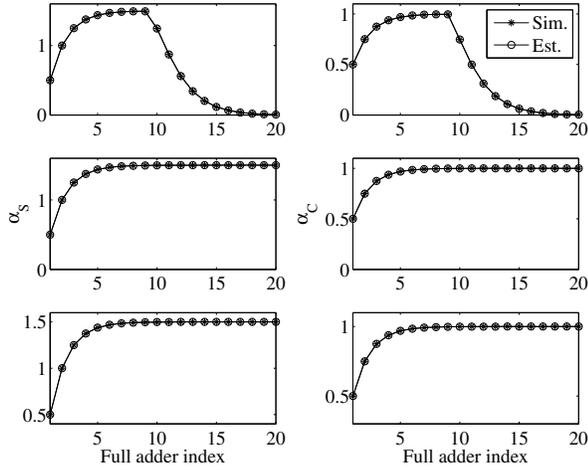


Fig. 7. Switching activity of sum and carry outputs for a three stage integrator section in CIC (Sim. and Est. are the simulated and the estimated values respectively for an input wordlength of 8-bits. The estimated values are based on our proposed model).

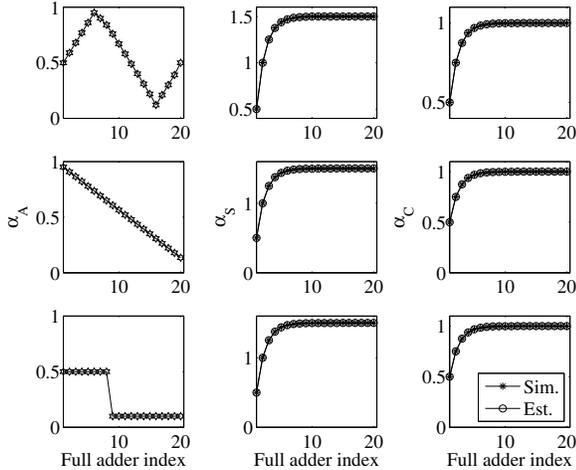


Fig. 8. Switching activities of sum and carry outputs for three different A inputs applied at each full adder in the first stage of the integrator section.

wordlengths and also with inputs having different switching activities patterns as shown in Fig. 8. The model is also tested for single input wordlength and simulated and estimated results are shown in the Fig. 9 for the first stage. The results clearly show the close correspondence between the simulated and theoretical result based on the equations (12) to (18) that are specifically derived for the CIC case. As can be seen from Figs. 7 and 9, switching activities of LSB's for the first stage are relatively higher than that for the MSB's. However, switching activities are somehow comparable for later stages. This model is then helpful for the computation of the power consumption as a result of switching activity estimation.

V. CONCLUSIONS

To achieve low power, it is always important to develop accurate and efficient methods to estimate the switching activity. In this work, a method for estimation of the switching activity

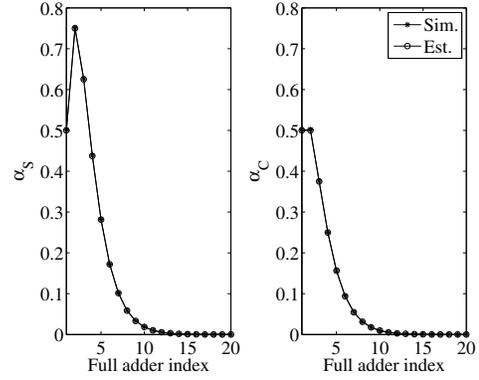


Fig. 9. Switching activity of sum and carry outputs for the first stage of integrator section in CIC (Sim. and Est. are the simulated and the estimated values respectively for a single bit input wordlength. The estimated values are based on our proposed model).

in integrators was presented. The switching activities are then used to estimate the power consumption. We first estimated the switching activity for the general purpose integrators and then specifically for the cascaded integrators in CIC filters. The results for the CIC case clearly show a close correspondence between the theoretical and the simulated ones.

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