Ultra-Low Noise and Highly Linear Two-Stage Low Noise Amplifier (LNA)

Master Thesis Performed in
Electronic Devices Division
By
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LiTH-ISY-EX--11/4496--SE

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Abstract

An ultra-low noise two-stage LNA design for cellular basestations using CMOS is proposed in this thesis work. This thesis is divided into three parts. First, a literature survey which intends to bring an idea on the types of LNAs available and their respective outcomes in performances, thereby analyze how each design provides different results and is used for different applications. In the second part, technology comparison for 0.12µm, 0.18µm, and 0.25µm technologies transistors using the IBM foundry PDKs are made to analyze which device has the best noise performance. Finally, in the third phase bipolar and CMOS-based two-stage LNAs are designed using IBM 0.12µm technology node, decided from the technology comparison. In this thesis a two-stage architecture is used to obtain low noise figure, high linearity, high gain, and stability for the LNA. For the bipolar design, noise figure of 0.6dB, OIP3 of 40.3dBm and gain of 26.8dB were obtained. For the CMOS design, noise figure of 0.25dB, OIP3 of 46dBm and gain of 26dB were obtained. Thus, the purpose of this thesis is to analyze the LNA circuit in terms of design, performance, application and various other parameters. Both designs were able to fulfill the design goals of noise figure < 1 dB, OIP3 > 40 dBm, and gain >18 dB.

Keywords:
Low Noise figure LNA, highly linear, basestation LNA, two stage, CMOS, narrowband LNA.
ABSTRACT

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1. INTRODUCTION

A low noise amplifier (LNA) is used in various aspects of wireless communications, including wireless LANs, cellular communications, and satellite communications. The RF amplifier in Figure 1.1, usually an LNA receives the RF signal, amplifies it and feeds the amplified RF signal to a filter or generally a mixer.

![Block diagram of a basic superheterodyne radio receiver](image)

Figure 1.1. Block diagram of a basic superheterodyne radio receiver

A critical building block in a radio receiver is the LNA with respect to the Friis’s formula as the noise figure of the first block dominates the noise figure of the entire receiver block [1]. So noise optimization plays a big role in the LNA circuit implementation and also the gain of each block as the gain is in the denominator of the Friis’s formula. Thus a lower noise figure with a good gain yields a low noise figure of the LNA, implicating the same for the whole receiver. The LNA amplifies the received signal and boosts its power above the noise level produced by subsequent circuits. In a radio frequency (RF) signal receiving device such as a cellular phone and a base station of a wireless communication system, a received signal has very weak intensity and includes considerable noise mixed therein. As such, the performance of the LNA greatly affects the sensitivity of the radio receiver. The LNA is capable of decreasing most of the incoming noise and amplifying a desired signal within a certain frequency range to increase the signal to noise ratio (SNR) of the communication system and improve the quality of received signal as well.

Additionally, since the stage before the LNA is an antenna or a filter, a specific input impedance (mostly 50 ohm) to guarantee the maximum power transference is needed. In this way, depending upon the application, the LNA design should have enough gain, low noise figure, good matching, high linearity, and/or low power [2]. In the previous years, several number of LNA circuits in RF CMOS has been presented, however, few accurate design methodologies towards very low noise figure have been proposed. The reason is that the linearity is given more importance than noise figure in many applications and due to the trade-off between the noise figure and linearity, noise figure is sacrificed a bit. But having both good noise performance and linearity is possible and will be discussed later in this report. Since the LNA dominates the global noise figure of a receiver, almost all the methods are based on the optimization of the noise performance with predefined gain and power dissipation. In the meantime the other parameters are adapted to the specifications of the various purposes they are used with the help of simulations and interactive procedures [2]. The linearity performance as a direct objective of design is important for broadband LNAs.
used in multi-standard systems and for their applications. Finally, as the technology is scaling down, the LNA design is becoming complicated but still survives with great performances in recent trend using mainly HEMT or SiGe, but not yet CMOS completely.
2. PERFORMANCE METRICS AND RF FUNDAMENTALS

The metrics that are needed to design an LNA are explained below. The understanding of these parameters are so important, since it ensures how much a parameter should be considered and also the consequences of the variation of each of these metrics can be understood.

2.1 PERFORMANCE METRICS

2.1.1 FIGURE OF MERIT (FOM)

One LNA circuit may have a larger BW, while another may have a larger gain, making comparison between different LNAs difficult. To enable such a comparison, designers typically map the multitude of circuit specifications into a single scalar figure-of-merit (FOM). For the case of the wide-band LNA the FOM is defined as [2]:

\[ \text{FOM} = \frac{S_{21} \times \text{BW}}{\text{NF} \times P_{dc}} \]  

(2.1)

It takes into account the power gain \(S_{21}\), bandwidth (BW), noise figure (NF) and power consumed \(P_{dc}\). It is inspired by expression for FOM for narrow-band LNAs, but includes the BW term as this report focuses on wide-band LNAs [2]. Thus, the FOM can be used to compare between different circuits, a higher FOM means a better circuit.

2.1.2 NOISE FIGURE (NF)

The noise figure (NF) is a measure of the amount of noise injected in our desired signal, as in a receiver, as expressed in equation 2.2. At the antenna end, the signal that is available is so week due to the internal and external factors in the communication channel [3]. Noise factor is a measure of how the signal to noise ratio is degraded by a device:

\[ F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \]  

(2.2)

Where \(F\) is the noise factor, \(S_{in}\) is the signal level at the input, \(N_{in}\) is the noise level at the input, \(S_{out}\) is the signal level at the output, and \(N_{out}\) is the noise level at the output.

The noise factor of a device is specified with noise from a noise source at room temperature \(N_{in} = kT\), where \(k\) is Boltzman's constant and \(T\) is the room temperature in Kelvin; \(kT\) is around -174 dBm/Hz. Depending on where devices are positioned in an amplification chain, the individual noise factors will have different effects on the overall noise, according to Friis.

Noise figure is the noise factor, expressed in decibels:

\[ \text{NF (decibels) = noise figure =} 10 \times \log(F) \]  

(2.3)

Noise figure is more often used in microwave engineering, but noise calculations use the noise factor, according to the Friis formula [4],
where, $F_{sys}$ is the total noise of the system, $F_1, F_2$ until $F_{n-1}$ and $G_1, G_2$ until $G_{n-1}$ are the noise factors and the gains respectively of the stages of the system. The noise figure plays a very important role as this has its significance over several factors as explained below.

### 2.1.3 Linearity

The linearity is also an important factor because the LNA must do more than simply amplifying the signal without adding much noise. The LNA, when receiving a weak signal, should maintain the linearity in the presence of strong interferer, otherwise a variety of pathologies may result. The consequences of intermodulation distortion (any order) include desensitization (also known as blocking) and cross modulation. Blocking occurs when the intermodulation products caused by the strong interferer swamp out the desired weak signal, whereas cross-modulation results when nonlinear interaction transfers the modulation of one signal to the carrier of another [5].

There are many measures of linearity, the most commonly used are the third-order intercept (IP3) and the 1-dB compression point (P-1dB). In case of direct conversion homodyne receiver, the second-order intercept (IP2) is more important [5].

#### 2.1.3.1 IP3 (third order intercept point)

When comparing receivers, spectrum analyzers and RF amplifiers, the third order intercept point, which is a measure of the linearity, is an important factor. The third order intercept point (IP3) is the point at which the extrapolated third order intermodulation level (IM3) is equal to the signal levels in the output of a two-tone test when the extrapolation is made from a point below which the third order intermodulation follows the third order law. IP3 may be given as the input level or as the output level for that point and which one has to be specified. One uses the terms input intercept point IIP3 and output intercept point OIP3.

![Figure 2.1. IP3 characteristics graph.](image)
The third-order intercept point relates nonlinear products caused by the third-order nonlinear term to the linearly amplified signal, in contrast to the second-order intercept point that uses second order terms. The intermodulation products are shown as in Figure 2.2. Intermodulation products increase at rates that are multiples of the fundamentals. If not for the output power saturating limit, intermodulation products would overtake the fundamentals as shown in Figure 2.2. IP3 is the point where 3rd order products would overtake fundamentals in output power.

![Figure 2.2. Intermodulation products with frequencies.](image)

Alternatively IP3 is a figure of merit that characterizes a receiver's tolerance to several signals that are present simultaneously outside the desired passband. IP3 is a power level, typically given in dBm, and it is closely related to the 1 dB compression point [6],

$$IP_{3,\text{system}} = \frac{1}{G_1} \frac{G_1 G_2 G_3}{IP_{3,2}} + \frac{1}{G_3} \frac{G_1 G_2 G_3}{IP_{3,4}}$$

(2.5)

where, the $IP_{3,\text{system}}$ is the IP3 value of the entire system, which can be a multistage amplifier, multistage mixer or also the entire receiver system. The $G_1$, $G_2$ and $G_3$ are the gain of three stages in this case and the $IP_{3,2}$, $IP_{3,4}$ are the IP3 values of the respective stages.

### 2.1.4 Receiver Sensitivity

The noise in the original input $N_i$ can be taken to be $kT$B, where $k$ is the Boltzmann constant ($1.38 \times 10^{-23}$), T is the temperature (conventionally taken to be 290 K) and B is the bandwidth. All we need to know is the noise bandwidth of the filters, and we can calculate the total signal-to-noise ratio at the output of the receiver for any level of input signal. The smallest value of input signal which provides a certain minimum output signal to noise ratio is known as the sensitivity of the receiver. Unfortunately, there is not a single definition of sensitivity, since the radio receiver designer often does not know what level of output signal
to noise ratio will be required for the whole system. A common solution is to define the sensitivity of a receiver in terms of the minimum detectable signal (MDS). This is the input signal level that results in a signal-to-noise ratio at the output of 0 dB (in other words, the same signal power and noise power).

2.1.5 S-Parameters

An n-port microwave network has n number of paths into which power can be fed and from which power can be taken. In general, power can get from any arm (as input) to any other arm (as output). There are thus n incoming waves and n outgoing waves. We also observe that power can be reflected by a port, so the input power to a single port can partition between all the ports of the network to form outgoing waves.

Associated with each port is the notion of a "reference plane" at which the wave amplitude and phase is defined. Usually the reference plane associated with a certain port is at the same place with respect to incoming and outgoing waves.

The n incoming wave complex amplitudes are usually designated by the n complex quantities and the n outgoing wave complex quantities are designated by the n complex quantities bn. The incoming wave quantities are assembled into an n-vector A and the outgoing wave quantities into an n-vector B. The outgoing waves are expressed in terms of the incoming waves by the matrix equation $B = SA$ where $S$ is an n by n square matrix of complex numbers called the "scattering matrix". It completely determines the behavior of the network. In general, the elements of this matrix, which are termed "s-parameters", are all frequency-dependent [7].

![Figure 2.3. two port network](image)

For example, the matrix equations for a 2-port as in Figure 2.3 are

$$b_1 = S_{11}a_1 + S_{12}a_2$$  \hspace{1cm} (2.6)

$$b_2 = S_{21}a_1 + S_{22}a_2$$  \hspace{1cm} (2.7)
The S-parameter matrix for the 2-port network is probably the most commonly used and serves as the basic building block for generating the higher order matrices for larger networks. In this case the relationship between the reflected, incident power waves and the S-parameter matrix is given by:

\[
\begin{pmatrix}
  b_1 \\
  b_2
\end{pmatrix} =
\begin{pmatrix}
  S_{11} & S_{12} \\
  S_{21} & S_{22}
\end{pmatrix}
\begin{pmatrix}
  a_1 \\
  a_2
\end{pmatrix}
\]  \hspace{1cm} (2.8)

Each of above equation gives the relationship between the reflected and incident power waves at each of the network ports, 1 and 2, in terms of the network’s individual S-parameters, \( S_{11} \), \( S_{12} \), \( S_{21} \) and \( S_{22} \). If one considers an incident power wave at port 1 \( (a_1) \) there may result from it waves exiting from either port 1 itself \( (b_1) \) or port 2 \( (b_2) \). However if, according to the definition of S-parameters, port 2 is terminated in a load identical to the system impedance \( (Z_0) \) then, by the maximum power transfer theorem, \( b_2 \) will be totally absorbed making \( a_2 \) equal to zero. Therefore,

\[
S_{11} = \frac{b_1}{a_1} = \frac{V_{-1}}{V_{+1}} \quad \text{and} \quad S_{21} = \frac{b_2}{a_1} = \frac{V_{-2}}{V_{+1}} \hspace{1cm} (2.9)
\]

Similarly, if port 1 is terminated in the system impedance then \( a_1 \) becomes zero, giving

\[
S_{12} = \frac{b_1}{a_2} = \frac{V_{-1}}{V_{+2}} \quad \text{and} \quad S_{22} = \frac{b_2}{a_2} = \frac{V_{-2}}{V_{+2}} \hspace{1cm} (2.10)
\]

Each 2-port S-parameter has the following generic descriptions,

- \( S_{11} \) is the input port voltage reflection coefficient
- \( S_{12} \) is the reverse voltage gain
- \( S_{21} \) is the forward voltage gain
- \( S_{22} \) is the output port voltage reflection coefficient

An amplifier operating under linear (small signal) conditions is a good example of a non-reciprocal network and a matched attenuator is an example of a reciprocal network. In the following cases we will assume that the input and output connections are ports 1 and 2 respectively which is the most common convention.

**SCALAR LINEAR GAIN:**

The scalar linear gain (or linear gain magnitude) is given by

\[
|G| = |S_{21}|. \hspace{1cm} (2.11)
\]

That is simply the scalar voltage gain as a linear ratio of the output voltage and the input voltage. As this is a scalar quantity, the phase is not relevant in this case.

**Scalar logarithmic gain**

The scalar logarithmic (decibel or dB) expression for gain \( (g) \) is

\[
g = 20 \log|S_{21}| \quad \text{dB}. \hspace{1cm} (2.12)
\]
This is more commonly used than scalar linear gain and a positive quantity is normally understood as simply a gain. Negative quantity can be expressed as a 'negative gain' or more usually as a 'loss' equivalent to its magnitude in dB. For example, a 10 m length of cable may have a gain of -1 dB at 100 MHz or a loss of 1 dB at 100 MHz.

**Transducer Power Gain**

Transducer power gain, \( G_T \), is defined as the ratio between the power delivered to the load and the power available from the source.

\[
G_T = \frac{1 - |\Gamma_s|^2}{1 - |S_{11}|^2} \frac{|S_{21}|^2}{1 - \left|\Gamma_{out}\right|^2} \frac{1 - |\Gamma_L|^2}{1 - \left|\Gamma_{out}\right|^2}
\]

(2.13)

\[
G_T = |S_{21}|^2
\]

(2.14)

**Operating Power Gain**

Operating power gain, \( G_P \), is defined as the ratio between the power delivered to the load and the power input to the network.

\[
G_P = \frac{1}{1 - |S_{11}|^2} |S_{21}|^2
\]

(2.15)

**Available Power Gain**

Available power gain, \( G_A \), is defined as the ratio between the power available from the network and the power available from the source as shown in equation 2.16.

\[
G_A = |S_{21}|^2 \frac{1}{1 - |S_{22}|^2}
\]

(2.16)

Since the power available from the source is greater than the power input to the LNA network, \( G_P > G_T \). The closer the two gains are, the better the input matching is. Similarly, because the power available from the LNA network is greater than the power delivered to the load, \( G_A > G_T \). The closer the two gains are, the better is the output matching.

**Voltage standing wave ratio**

The voltage standing wave ratio (VSWR) at a port, is a similar measure of port match to return loss but is a scalar linear quantity, the ratio of the standing wave maximum voltage to the standing wave minimum voltage. It therefore relates to the magnitude of the voltage reflection coefficient and hence to the magnitude of either \( S_{11} \) for the input port or \( S_{22} \) for the output port.

At the input port, the VSWR (\( S_{in} \)) is given by

\[
S_{in} = \frac{1 + |S_{11}|}{1 - |S_{11}|}
\]

(2.17)
At the output port, the VSWR ($S_{\text{out}}$) is given by

$$S_{\text{out}} = \frac{1 + |S_{22}|}{1 - |S_{22}|}$$  \hspace{1cm} (2.18)

### 2.1.6 Stability

If a 1-port network has reflection gain, its S-parameter has size or modulus greater than unity. More power is reflected than is incident. Suppose the reflection gain from our 1-port is $S_{11}$, having modulus bigger than unity and if the 1-port is connected to a transmission line with a load impedance having reflection coefficient $g_1$, then oscillations may well occur if $g_1^* S_{11}$ is bigger than unity. The round trip gain must be unity or greater at an integer number of $2\pi$ radians phase shift along the path. This is called the "Barkhausen criterion" for oscillations. Clearly if we have a source matched to a matched transmission line, no oscillations will occur because $g_1$ will be zero.

If an amplifier has either $S_{11}$ or $S_{22}$ greater than unity then it is quite likely to oscillate or go unstable for some values of source or load impedance. If an amplifier (large $S_{21}$) has $S_{12}$ which is not negligibly small, and if the output and input are mismatched, round trip gain may be greater than unity giving rise to oscillation. If the input line has a generator mismatch with reflection coefficient $g_1$, and the load impedance on port 2 is mismatched with reflection coefficient $g_2$, potential instability happens if $g_1 g_2^* S_{12} S_{21}$ is greater than unity.

Also, in the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations, and perhaps at unexpectedly high or low frequencies.

The Stern stability factor characterizes circuit stability as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}| |S_{12}|}$$  \hspace{1cm} (2.19)

where,

$$\Delta = S_{11} S_{22} - S_{12} S_{21}.$$  \hspace{1cm} (2.20)

When $K > 1$ and $\Delta < 1$, the circuit is unconditionally stable. That is, the circuit does not oscillate with any combination of source and load impedances. A designer should perform the stability evaluation for the S parameters over a wide frequency range to ensure that $K$ remains greater than one at all frequencies. As the coupling ($S_{12}$) decreases, i.e. as reverse isolation increases, stability improves. Techniques such as resistive loading and neutralization can be used to improve stability for an LNA [8].
Aside from the two metrics $K$ and $\Delta$, the source and load stability circles can also be used to check for LNA stability.

- The input stability circle draws the circle $|\Gamma_{out}| = 1$ on the Smith chart of $\Gamma_S$.
- The output stability circle draws the circle $|\Gamma_{in}| = 1$ on the Smith chart of $\Gamma_L$.

The non-stable regions of the two circles should be far away from the center of the Smith chart. In fact the non-stable regions are better located outside the Smith chart circles.
3. TYPES OF IMPLEMENTATION

The LNA can be implemented in various topologies depending on the required specification and the purpose they are being used. In this way they can be divided mainly in two broad categories, narrowband LNA and wideband LNA. In each particular band, the circuit type varies into several categories as will be explained below.

3.1 Narrowband and Wideband Low noise amplifiers

This category is the primary difference in the LNA types, where the bandwidth determines the amplifier type.

3.1.1 Narrowband LNA

Narrowband designs benefit significantly from the resonant input circuit and loads to achieve high gain, low noise figure, and impedance matching. A wideband LNA must provide high gain, low noise figure and also acceptable input matching over many octaves [9]. In some applications a broadband is not required and therefore it is desirable to reduce power consumption and increase gain by using narrowband techniques. A cascade narrowband LNA is the best structure for a good trade-off between low noise, high gain, and stability.

The merit of narrow band communication is to realize stable long-range communication. In addition, the carrier purity of transmission spectrum is very good, therefore it is possible to manage an operation of many radio devices within same frequency bandwidth at same time. In other words, it leads the high efficiency of radio wave use within same frequency band. Narrow band communication is the optimal in the site where several radio-control equipments are used, such as a construction site or an industrial plant.

Since the receiver bandwidth is narrow, it is difficult for high-speed data communication. Of course, as a frequency standard, temperature compensation is also necessary for crystal oscillation in a narrowband circuit.

3.1.2 Wideband LNA

The wideband LNA are those where the ratio between the bandwidth and the center frequency can be as large as two. The wideband receivers can replace several LC-tuned LNAs typically used in multiband and multimode narrow-band receivers. A wideband LNA saves chip area and also is used for flexible radios with much signal processing [11].

Conventional wideband amplifiers are either distributed or use resistive feedback. The distributed approach often suffers from high power consumption and low gain whereas the noise of the resistive feedback amplifiers is usually quite high [9]. The wideband LNAs built of MOSFETs have difficulties in achieving high sensitivity, low noise figure, gain and also to avoid pass-band ripple and stop-band attenuation.
The above equation shows the importance of the bandwidth (BW), signal to noise ratio (SNR) and the noise factor (F) [1].

Thus stacking several front-ends for the reception of various standards is one of the design trends to realize the wideband receivers. A single front-end wideband LNA to accommodate all standards to reduce the front-end area is expected.

The wideband LNA can be better since most of the narrowband LNAs are typically LC tuned and integrated inductors are the most area consuming on-chip components, a large amount of chip area is required. This increased area implies high cost. On the other hand, the option of using a wideband LNA allows some hardware sharing and has smaller area, hence cost advantage.

3.2 Single-ended and Differential LNA

3.2.1 Single-ended LNAs

A single-ended amplifier has only one input and output, and all voltages are measured in reference to signal common. With this amplifier, Vout is equal to Vin multiplied by the gain of the amplifier. A feature of single-ended amplifiers is that only one measurement point is needed for the input and the output terminal for a single port network [12]. The following Figure 3.1 represents a single-ended amplifier.

![Figure 3.1. Single Ended amplifier.](Image)

3.2.2 Boon and Bane of Single-ended LNAs

One of the main drawbacks of this amplifier type is the fact that in a multi-channel system, signal common (defined as the common point supplying power for the analog circuitry) can be common to all channels. Another disadvantage is that it is susceptible to noise (internal or external interference in the form of unpredictable voltages) on the input.
Additionally, single-ended inputs can suffer from noise injection. Noise can be injected into signals because the wire that carries the signals can act as an aerial and thus pick up all manner of electrical background noise. Once this noise has been introduced into the signal this way there is no way to remove it [13].

Good for measurements between any point and chassis ground. Susceptible to noisy environment. Same signal common reference for multiple channels. Cannot be used for "above ground" measurements [12].

### 3.2.3 Differential LNAs

A differential amplifier has two inputs and amplifies the difference between them. The voltage at both inputs is measured with respect to signal common as seen in the Figure 3.2.

![Figure 3.2. Fully differential amplifier](image)

Calculating the gain for a differential is more complex than a single-ended one. There are two gains associated with a differential amplifier, differential gain (Gd) and common gain (Gc). The output of a differential amplifier is described by the following:

\[
V_{\text{OUT}} = V_{\text{OUT}}^+ - V_{\text{OUT}}^- \quad (3.2)
\]

\[
V_{\text{IN}} = V_{\text{IN}}^+ - V_{\text{IN}}^- \quad (3.3)
\]

Thus the \( V_{\text{OUT}} \) can be expressed as

\[
V_{\text{OUT}} = V_{\text{IN}} \times G_d . \quad (3.4)
\]

In an ideal differential amplifier \( G_c \) (common mode gain) would be zero, and the output of the amplifier would simply be the amplified difference between \( V_{\text{IN}} \) and \( V_{\text{OUT}} \). Unfortunately, ideal differential amplifiers do not exist in practice, therefore \( G_c \) should be as small as possible [12]. The ratio of the differential gain to the common gain becomes important since the goal is to make the second term in the above gain equation negligible. This is referred to as the Common Mode Rejection Ratio (CMRR) and leads to the Common Mode Rejection (CMR) specification that is usually used. The CMR specification is defined as follows:

\[
\text{CMR}=20\log(\text{CMRR})=20\log(G_d/G_c) . \quad (3.5)
\]
The goal when designing such an amplifier is to make the CMR as high as possible. A higher CMR indicates a differential amplifier that is less susceptible to voltages common to both inputs (noise). Another benefit of a high CMR is the ability to accurately measure a small voltage difference between two points that are both at a higher voltage potential. Since CMR decreases as the frequency of a signal increases, it is usually specified at a particular frequency [12].

3.2.4. Boon and Banes of Differential LNAs

Differential amplifiers are not quite common, since they do not have the advantage of single-ended amplifiers. They are useful for "above ground" measurements, as long as the CMV (Common Mode Voltage) of the amplifier is not exceeded. They are also useful in environments where there is potential noise. One of the drawbacks of the standard differential amplifier is that in a multi-channel system, signal ground is often the same for all channels. An obvious disadvantage of differential inputs is that you need twice as many wires, so you can connect only half the number of signals, compared to single-ended inputs.

The differential amplifiers are mainly used as they would provide different matching levels and also better linearity. Differential inputs reduce noise and allow for potentially longer cabling. They can be short circuited to be used as single ended inputs if required. Differential inputs can be used for floating signals, but in such cases a reference should be provided to the instrumentation.

Less susceptible to noisy environment (CMR). Can be used for "above ground" measurements up to the CMV. Some signal common reference for multiple channels. Possible crosstalk with wide voltage differences between channels.

3.3 Feedback and Feedforward LNAs

3.3.1 Feedback Amplifiers

The amplifiers can also be classified in terms of the feedback being used. The feedback is the most commonly known terminology, which is in the amplifier, a fraction of the output of which is combined with the input so that a negative feedback opposes the original signal as shown in Figure 3.3, which is a resistive feedback LNA. The applied negative feedback improves performance (gain stability, linearity, frequency response, step response) and reduces sensitivity to parameter variations due to manufacturing or environment. Because of these advantages, negative feedback is used in this way in many amplifiers and control systems.

A feedback amplifier is a system of three elements, mainly an amplifier with gain \( A_{OL} \), an attenuating feedback network with a constant \( \beta < 1 \), and a summing circuit [14]. The voltage gain of the amplifier with feedback, the closed-loop gain \( A_{fb} \), is derived in terms of the gain of the amplifier without feedback, the open-loop gain \( A_{OL} \) and the feedback factor \( \beta \), which governs how much of the output signal is applied to the input. The open-loop gain \( A_{OL} \) in
general may be a function of both frequency and voltage, the feedback parameter $\beta$ is determined by the feedback network that is connected around the amplifier.

$$A_{fb} = \frac{V_{out}}{V_{in}} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}} \quad (3.6)$$

If $A_{OL} \gg 1$, then $A_{fb} \approx 1 / \beta$ and the effective amplification (or closed-loop gain) $A_{fb}$ is set by the feedback constant $\beta$, and hence set by the feedback network, usually a simple reproducible network, thus making linearizing and stabilizing the amplification characteristics straightforward. Note also that if there are conditions where $\beta A_{OL} = -1$, the amplifier has infinite amplification and it has become an oscillator, and the system is unstable. The combination $L = \beta A_{OL}$ appears commonly in feedback analysis and is called the loop gain. The combination $(1 + \beta A_{OL})$ also appears commonly and is variously named as the de-sensitivity factor or the improvement factor. Feedback can be used to extend the bandwidth of an amplifier (speed it up) at the cost of lowering the amplifier gain

### 3.3.2 Feedforward Amplifiers

Feedforward type amplifiers are those where the noise cancellation techniques can be easily facilitated with less effect on the stability concern. The feedforward technique is free of global feedback, so instability risks are relaxed. In this a path to the output is split into two paths, one with the original signal and the other one with active components, say an amplifier. The function of this type can be understood from the Figure 3.4 shown below. The inversion of the signal is taken and added to the signal at node Y and hence the noise signals get cancelled and the desired signals are retrieved.

![Figure 3.3. Basic feedback amplifier structure.](image)

![Figure 3.4. A LNA with feedforward structure.](image)
The advantage of this feedforward structure is its ability of distortion cancellation, but the usage of this feedforward path amplifier is not significant due to the complexity of the LNA, and there are concerns over the area it consumes [1].

3.4 Single band and Multi band type LNAs

The next category dealt here is the band selectivity part of the LNA. The single band LNAs have a specific operation frequency and the multiband LNAs select a particular operating frequency between several received frequencies. Multiband LNAs are suitable for wideband applications and may be tunable linear amplifiers are needed, thereby trade-off between the linearity and gain.

The implementation of these can be done like multiband antenna leading to a single wideband LNA, or multiple antennas with a dedicated narrowband LNA for them as shown below in Figure 3.5 and Figure 3.6, respectively [15].

![Figure 3.5. Multiband antenna with single wideband LNA.](image1)

![Figure 3.6. Multiband receiver with several narrowband LNA.](image2)

The usage of single band range LNA are still dominating due to their small area, low cost implementation and also most devices or base-stations are still working on a particular range of frequencies. For multi band range LNAs, the complexity of the mixer is of great concern.
and also its linearity. Thus to avoid all complexity issues, instead the optimization can be done for the required range in more effective way, compared to single band amplifiers.

### 3.5 SIDO and DISO LNAs

The final category is the Single Input Differential Output (SIDO) and Differential Input and Single Output (DISO). These two share the features of both a single-ended LNA and also the differential-ended LNA. The usage of these two depends on the blocks preceding and following the LNA, an example of each shown in Figure 3.7 and Figure 3.8 showing SIDO and DISO respectively.

The differential architecture has advantages like direct connection to the double-balanced mixer and the rejection against the common mode noises from the power supply and the substrate. Also the differential architecture has ability to reduce the second intermodulation (IM2) effect. This SIDO can also be used to avoid an external balun. The SIDO implementation can be performed using a trifilar transformer (a transformer which has three windings in an accurate 1:1:1 ratio) [16]. An AC voltage across any winding will also be present on the others [17].

![Figure 3.7. SIDO architecture.](image-url)

![Figure 3.8. DISO architecture.](image-url)
The performance of these two topologies, like the linearity, noise optimization, and the gain depends on the type of application they are being used. Now in SIDO as briefed out above, when a transformer is used to convert a single signal into a differential signal, there will be some losses and hence noise may be at high risk. Also, the area that these circuits occupy is usually large compared to normal differential amplifiers. Thus these types of LNAs are not seen being used in many applications in the current trend of RF systems.
4. Comparison and analysis of various LNAs

In this part we will be comparing the current work with previous literatures on LNA and state the difference, advancement and further improvement that can be done.

4.1 Research Paper Comparison

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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[19]</td>
<td>0.6</td>
<td>-5/17</td>
<td>22</td>
<td>NG</td>
<td>0.435</td>
<td>10</td>
<td>2.5</td>
<td>0.35µ/CMOS</td>
<td>0.812</td>
</tr>
<tr>
<td>[22]</td>
<td>0.75</td>
<td>10/36</td>
<td>34</td>
<td>-18/-7</td>
<td>0.9</td>
<td>190</td>
<td>1.8/3*</td>
<td>0.25µ/SiGe</td>
<td>1.43</td>
</tr>
<tr>
<td>[18]</td>
<td>0.9</td>
<td>14.1/30</td>
<td>16</td>
<td>-11/-12.7</td>
<td>0.9</td>
<td>11</td>
<td>2.8</td>
<td>0.35µ/SiGe</td>
<td>NG</td>
</tr>
<tr>
<td>[27]</td>
<td>0.9</td>
<td>7.1/15.9</td>
<td>8.8</td>
<td>-38.1/NG</td>
<td>0.8</td>
<td>7.5</td>
<td>2</td>
<td>0.24µ/CMOS</td>
<td>0.19</td>
</tr>
<tr>
<td>[21]</td>
<td>0.9</td>
<td>-3.1/18.4</td>
<td>21.5</td>
<td>&lt;-10/-10</td>
<td>NG</td>
<td>36.5</td>
<td>2.5</td>
<td>0.25µ/SiGe</td>
<td>0.59</td>
</tr>
<tr>
<td>[23]</td>
<td>1.1</td>
<td>NG</td>
<td>18</td>
<td>&lt;-5/-7</td>
<td>0.1-1.7</td>
<td>NG</td>
<td>NG</td>
<td>NG/CMOS</td>
<td>0.8</td>
</tr>
<tr>
<td>[24]</td>
<td>1.3</td>
<td>-2/15</td>
<td>17</td>
<td>&lt;-18/-25</td>
<td>1.8</td>
<td>12</td>
<td>2.7</td>
<td>NG/SiGe</td>
<td>0.25</td>
</tr>
<tr>
<td>[26]</td>
<td>1.4</td>
<td>-1.5/18.5</td>
<td>20</td>
<td>&lt;-10/-13</td>
<td>0.002-1.1</td>
<td>18</td>
<td>1.8</td>
<td>90n/CMOS</td>
<td>0.06</td>
</tr>
<tr>
<td>[20]</td>
<td>1.7</td>
<td>0/11</td>
<td>10</td>
<td>-35/-15</td>
<td>1.9</td>
<td>12</td>
<td>1</td>
<td>0.5µ/CMOS</td>
<td>NG</td>
</tr>
<tr>
<td>[11]</td>
<td>&lt;2</td>
<td>0/13.7</td>
<td>13.7</td>
<td>&lt;-8/-12</td>
<td>0.250-1.1</td>
<td>35</td>
<td>2.5</td>
<td>0.25µ/CMOS</td>
<td>0.075</td>
</tr>
</tbody>
</table>

Table 4.1. Performance comparison of LNAs from the literature.

* two-stage LNA voltage: stage 1/stage2 voltage supply.

NG- Not given.

4.2 Datasheets Comparison

In this section the various LNA products available in the market provided by various companies are displayed. The products selected are mostly those related to base station applications.
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CFS0303-SB</td>
<td>pHEMT</td>
<td>0.3</td>
<td>0.1-10</td>
<td>14.6</td>
<td>O: 23</td>
<td>O:17</td>
<td>3</td>
<td>560</td>
</tr>
<tr>
<td>MGA-633P8</td>
<td>pHEMT</td>
<td>0.37</td>
<td>0.9</td>
<td>18</td>
<td>O:37</td>
<td>O:22</td>
<td>5</td>
<td>495</td>
</tr>
<tr>
<td>HMC617LP3</td>
<td>pHEMT</td>
<td>0.5</td>
<td>0.55-1.2</td>
<td>16</td>
<td>O: 37</td>
<td>O:20</td>
<td>5</td>
<td>NG</td>
</tr>
<tr>
<td>MGA-631P8</td>
<td>pHEMT</td>
<td>0.53</td>
<td>0.9</td>
<td>17.5</td>
<td>O:32.6</td>
<td>O:18</td>
<td>4</td>
<td>550</td>
</tr>
<tr>
<td>SKY65037-360LF</td>
<td>pHEMT</td>
<td>0.6</td>
<td>0.9</td>
<td>15-25</td>
<td>O:34</td>
<td>O:18</td>
<td>5</td>
<td>240</td>
</tr>
<tr>
<td>SKY65040-360LF</td>
<td>pHEMT</td>
<td>0.6</td>
<td>2.5</td>
<td>22</td>
<td>O:34</td>
<td>O:18</td>
<td>5</td>
<td>193</td>
</tr>
<tr>
<td>MGA-13216</td>
<td>pHEMT</td>
<td>0.61</td>
<td>1.5-2.5</td>
<td>35.8</td>
<td>O : 40.5</td>
<td>O:23</td>
<td>5</td>
<td>1110</td>
</tr>
<tr>
<td>ALM-11036</td>
<td>pHEMT</td>
<td>0.78</td>
<td>0.85</td>
<td>15.6</td>
<td>I:23.3</td>
<td>I:4</td>
<td>5</td>
<td>715</td>
</tr>
<tr>
<td>BGU7003</td>
<td>SiGe</td>
<td>0.8</td>
<td>0.04-6</td>
<td>18.3</td>
<td>I: -0.2</td>
<td>I: -20</td>
<td>2.5</td>
<td>70</td>
</tr>
<tr>
<td>TQP3M9005</td>
<td>pHEMT</td>
<td>0.8</td>
<td>1.9</td>
<td>15.3</td>
<td>O:34</td>
<td>O:22</td>
<td>5</td>
<td>340</td>
</tr>
<tr>
<td>ADL5523</td>
<td>pHEMT</td>
<td>0.8</td>
<td>0.9</td>
<td>21.5</td>
<td>O:34</td>
<td>O:21</td>
<td>5</td>
<td>500</td>
</tr>
<tr>
<td>MBC13917</td>
<td>SiGe</td>
<td>0.95</td>
<td>0.1-2.5</td>
<td>27</td>
<td>O:9.5</td>
<td>O:1</td>
<td>2.7</td>
<td>100</td>
</tr>
<tr>
<td>ALM-1612</td>
<td>pHEMT</td>
<td>0.95</td>
<td>1.575</td>
<td>18.2</td>
<td>I : 2</td>
<td>I: 8</td>
<td>2.7</td>
<td>54</td>
</tr>
<tr>
<td>HMC356LP3</td>
<td>pHEMT</td>
<td>&lt;1</td>
<td>0.35-0.55</td>
<td>17</td>
<td>O:38</td>
<td>O:21</td>
<td>5</td>
<td>NG</td>
</tr>
</tbody>
</table>

Table 4.2. Performance comparison of various LNA products by different companies.

* I/O: Input or Output values

NG: Not given

Observations and comments:

- It can be noted that in most of the research papers, the LNAs are designed using either SiGe (BiCMOS) or CMOS transistor. But, most of the commercial LNAs are designed using the GaAs-pHEMT. Also, there are not too many commercial LNAs having noise figure less than 0.5 dB.

- The silicon process has higher integration solution than other types of transistors process. Until, recently the GaAs-HEMT and other BiCMOS (SiGe mostly) process has been dominating the RF field due to their better performances. But now the CMOS process is starting to show up.

- The trade-off between the noise figure, linearity and gain and power can be observed. A low noise figure with a good linearity is a possible design with some trade-off over power, gain and few other parameters.

- The requirements of an LNA design are dependent on the purpose or the application it is being used. Generally base-stations look out for low NF with good linearity whereas WLAN, Bluetooth, GPS and few other applications look out for more on linearity with quite an acceptable noise figure.
The presence of inductor has significance on the LNA performance depending on, if it’s on-chip or off chip. The presence of inductors in a circuit has shown a good low noise figure in most cases, but power consumption is a bit higher.

The LNA for narrowband applications has better noise figure than the wideband types, since the optimization to be done is quite in smaller range.
5. **Device Comparison**

This part of the report provides information regarding the devices that are in use, their characteristics and performances in various technologies available in recent trend. The major transistor device types that are in use for LNA applications are the GaAs-HEMT, SiGe BiCMOS and CMOS. Till few years back and even now, there are many LNAs using the GaAs type of devices due to their low noise and high operational frequencies for RF applications in spite of being expensive. The research progresses towards the rapid development of silicon (mainly CMOS) based transistor which provides better integration. The products with higher performance requirements, as needed in base-stations, the SiGe is providing good support and also lower cost for RF field. But the CMOS is used in low performance applications like GPS systems, sensors and few others. As a part of this thesis, we will compare mainly the CMOS transistor’s and the bipolar transistor’s (partially BiCMOS) details and performances.

5.1 **Devices performance Comparison**

As a part of the thesis, I would consider only the bipolar (maybe part of a BiCMOS technology) and the MOSFET devices in more depth than other types of devices. When an LNA is designed, in most cases the major noise contributor is the input transistor. So, having noise as the main concern we will initially look and compare the device’s noise characteristics.

5.1.1 **Noise performance**

The noise figure is one of the major concern for a RF circuit design, mainly for an LNA. The origin of noise can be in many categories. We will consider the origin and the types of noise in a BJT and MOSFET.

**ORIGIN:**

**Bipolar Transistor:**

In a general BJT, the base resistance is directly related to the noise figure and also the resistance between the base and emitter plays quite a significant role. When the width of the emitter is increased the resistance across them will also increase respectively and hence due to that, when a voltage is applied across that terminal, the noise due to the resistance $R_{be}$, varies.

Similarly is the base resistance $R_{bb}$ a main component, since most amplifiers have the RF input given to the Base (gate) of the transistor and thus, the first impact of noise is on the $R_{bb}$ and the total noise is dependent mainly on the same. Also the resistances and capacitances across each terminal of a transistor have their part in the noise contribution.
The base connection resistance is inversely proportional to the doping level of the base itself. Consider the thermal noise due to base as shown below,

$$I_{n,b}^2 = 1/ R_{bb},$$

where the $R_{bb}$ is the base connection resistance and $I_{n,b}^2$ is noise source due to current source.

Generally for high current gain, the doping level should be low, but at the same time $R_{bb}$ will be high and consequently strong noise contribution is involved. This is a common trade off and generally compromised by the designer as per the requirements.

**MOSFET:**

The gate resistance does not contribute much of the noise, as in case of BJT, instead it is the channel resistance which has impact on the noise.

When we consider the substrate resistance and capacitance, depending on the bias conditions and also on the magnitude of the effective substrate resistance and size of the back-gate transconductance the noise generated may exceed the thermal noise contribution of the ordinary channel charge.

**Types of Noise:**

The most common types of noise are the thermal noise, shot noise and the flicker noise. The other kinds of noises are the burst noise, avalanche noise, which will not be explained in this work.

**Thermal Noise:**

The thermal noise is mainly generated due to the series resistors at the terminals of the transistors. The random fluctuation of the velocity of the charge particles forms the thermal noise.
This noise is also directly proportional to the absolute temperature and the noise bandwidth over which the measurement is done. For this noise, the spectral density is a constant and is independent of the frequency.

The random thermal agitation of charges in the conductor is the reason for this noise and hence to reduce the noise generated of a given resistance, the temperature should be kept as low as possible and the bandwidth limited to a minimum useful value.

**Shot noise:**

This is originated mainly due to the random motion of the charge carriers. For shot noise to occur, there must a direct current flow and also a potential barrier over which the charge carriers flows.

For a common emitter circuit configuration:

\[ I_{nb}^2 = 2 \times q \times I_b \times \Delta f, \]  \hspace{1cm} (5.1)

where \( I_{nb} \) is the current noise source due to base, \( I_b \) is the base DC current, \( \Delta f \) is the frequency bandwidth, \( q \) is elementary charge. A similar expression can be written for the \( I_{nc}^2 \) where instead \( I_b \) should be replaced by current noise source due to collector terminal, \( I_c \).

The \( I_{nb} \) and the \( I_{nc} \) are correlated as both are influenced by the emitter current since they are proportional to the \( I_b \) and \( I_c \).

\[ I_E = I_b + I_c. \]  \hspace{1cm} (5.2)

Low noise is achieved at a low DC value, but at the same time, low DC bias decreases the \( g_m \) and gain. Thus the shot noise is associated with each terminal current.

**Flicker noise:**

The flicker noise also often noted as \( 1/f \) noise is mostly significant in the lower frequency range. This is mainly related to the DC current and also crystal lattice. The BJT has a smaller flicker noise than the FETs, hence the flicker corner frequency (\( f_c \)) of the BJT is lower than the FET.

The figure below shows the types of noise and their significance for a SiGe transistor. As seen, in case of the SiGe the shot noise due to collector current has the major influence of all, followed by the thermal noise of the base resistance and followed by other types depending on the frequency.
Figure 5.2. Noise contribution of the equivalent circuit noise source of SiGe HBT[25].

Figure 5.3 shows why the GaAs-HEMT has been dominating the RF design due to its very low minimum noise figure compared to other technologies. This is just a comparison and not the exact values for the current trend since the SiGe and the MOS are also having low minimum noise figures, in the range of 0.1-0.5 dB approximately, but the GaAs still have lower than these as the technology goes down. SiGe has started to come up now for extremely good performances like low noise figure and also high linearity and few other major metrics based on applications. And for unbalanced applications like either low noise figure or high linearity, the CMOS is taking significance in recent years.

Figure 5.3. Minimum noise figure of different devices [25].

Tuned noise parameter measurements deliver noise parameters for each device. However for the design of low-noise LNAs, accurate high-frequency equivalent circuits are a prerequisite which can also be used for the noise modelling. The measured minimum noise figures for the three different devices are shown in Figure 5.3 in the frequency range from 2 GHz to 20
GHz. As expected the HEMT is superior to the silicon counterparts in the whole frequency range and the SiGe HBT is superior to the MOSFET. While Fmin for CMOS tends to be the same or a bit lower than that for bipolar and hence achieving the comparable noise performance can be difficult, due to imperfect impedance matching for noise in the CMOS. The noise resistance of a device \( R_n \propto 1/gm \) and also \( R_{\text{N MOS}} > R_{\text{N BIPOLAR}} \) which means any noise mismatch is amplified for the CMOS process.

5.1.2 General Comparison between BJT and FET

The BJT has traditionally been the analog designer's transistor of choice, due largely to its higher transconductance and its higher output impedance (drain-voltage independence) in the switching region.

The MOSFET's advantages in digital circuits does not translate into supremacy in all analog circuits. The two types of circuits (analog and digital) draw upon different features of transistor behaviour. Digital circuits switch, spending most of their time outside the switching region, while analog circuits depend on MOSFET behaviour held precisely in the switching region of operation.

Nevertheless, MOSFETs are widely used in many types of analog circuits because of certain advantages. The characteristics and performance of many analog circuits can be designed by changing the sizes (length and width) of the MOSFETs used. By comparison, in most bipolar transistors the size of the device does not significantly affect the performance. MOSFET’s ideal characteristics regarding gate current (zero) and drain-source offset voltage (zero) also make them nearly ideal switch elements, and also make switched capacitor analog circuits practical. In their linear region, MOSFETs can be used as precision resistors, which can have a much higher controlled resistance than BJTs. In high power circuits, MOSFETs have the advantage of not suffering from thermal runaway as BJTs do.

The main advantage of BJTs versus MOSFETs in the analog design process is the ability of BJTs to handle a larger current in a smaller space. Fabrication processes exists that incorporate BJTs and MOSFETs into a single device. Mixed-transistor technologies are called Bi-FETs (Bipolar-FETs) if they contain just one BJT-FET and BiCMOS (bipolar-CMOS) if they contain complementary BJT-FETs. Such devices have the advantages of both insulated gates and higher current density [28].

- BJT has a low input resistance \( r_{\text{in}} \). But as MOSFET's gate is insulated from the channel (\( r_{\text{in}} > 10^{11} \) ohm), it draws virtually no input current and therefore its input resistance is infinity in theory (at DC only).
- BJT is current (\( I_b \) or \( I_e \)) controlled, but MOSFET is voltage (\( V_{gs} \)) controlled. Consequently, the power consumption of MOSFETs is lower than BJTs.
- MOSFETs are easy to fabricate in large scale and have higher element density than BJTs.
- MOSFETs have thin insulation layer which is more prone to statics and requires special protection.
- MOSFETs have higher cut-off frequency and higher maximum current than BJTs.
- MOSFETs are much more widely used (especially in computers and digital systems) than BJTs [29].

There are many differences between CMOS and bipolar devices which impact the RF circuits. One difference to note is the transconductance-to-current ratio (gm/I) of the devices. Whereas bipolar devices have roughly a constant gm/I, equal to one over the thermal voltage, MOS devices have a lower gm/I, which can be shown to be inversely proportional to the gate overdrive voltage (VGS-VT) in saturation. This is valid at both long-channel and short-channel limits, with gm/I taking a value of 2/VGT in long-channel and 1/VGT in extreme short-channel, where VGT is (VGS-VT). As a result, a FETs gm/I decline as current increases as displayed in Figure 5.4. To increase the output signal current, one can then either increase the FETs input voltage swing (shifting the burden to previous stages), the device size (moving to weaker inversion, i.e., lower gate-overdrive), or the bias current. In the CMOS designs, the reduced gm/I noticeably affects the divider, LO buffers, and mixer switches.

![Figure 5.4. Current versus gm/I characteristics of general CMOS transistor.](image)

The MOS devices are more sensitive to substrate resistance than bipolar devices due to bulk transconductance and parasitic capacitance at the source and drain as referred in Figure 5.5. Bipolar devices only interact with the substrate through the collector. To illustrate this, simulations were run on LNAs when sweeping the substrate resistance in the transistor model. In this simulation, the SiGe LNAs NF is virtually independent of substrate resistance, whereas the CMOS LNAs NF varies up to 0.5 dB. To get good model-to-hardware correlation in CMOS, the substrate has to be accurately modelled. Towards this end, the RF-CMOS technology includes “RF-FET” layout cells in which the substrate and gate connections are fixed and included in the model.

Thus, after this comparison, it might appear that the bipolar is better than the CMOS, but the linearity is better in the CMOS than the bipolar and the noise figure can be improved with a very good matching in the CMOS transistors.
Figure 5.5. CMOS simulation metrics versus R_sub.
6. Technology dependence and performance of Bipolar (BiCMOS) and CMOS transistors

In this section, we will simulate the noise performance of both the bipolar transistor and the CMOS transistor in various technology nodes (120nm, 180nm and 250nm). Simulations were performed in each of these technologies using a single transistor device and the minimum noise figure was obtained. The design was done in cadence environment with IBM PDK together with the Agilent Technologies' GoldenGate simulator. The STM PDK was also used in the 120nm and 180nm to compare with IBM PDK.

The testbench was setup as a two-port network operating at the frequency of interest, 2 GHz with voltage supplies as Vdd and Vgs for the CMOS. The testbench looks as in Figure 6.1. Similarly setup is used for the bipolar transistor with voltage supplies Vcc and Vbe, testbench shown in Figure 6.2.

6.1 Bipolar transistor

In IBM 6WL (250nm) process, the 7WL (180nm) process and the 8WL (120nm), the most significant noise source was the resistance at the input terminal. After that the noise due to the base-emitter junction is significant and also the shot noise. The other terminal noise has less significance compared to that of the base terminal. All these conclusions were made from the NCT analysis, available in the GoldenGate simulator, which displays the percentage of noises (thermal noise, shot noise, and so on) in each component used in the design, like the transistors, resistors, and so on. The simulation results are shown in the Table 6.1 and variation of the noise figure minimum (NFmin) with respect to frequency, VCC and VBE are shown in Figure 6.2-6.4.
<table>
<thead>
<tr>
<th>Technology node [nm]</th>
<th>Vcc [V]</th>
<th>Vbe [V]</th>
<th>Emitter width [µm]</th>
<th>Emitter length[nm]</th>
<th>Noise Figure minimum [dB]</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>1.8</td>
<td>0.6</td>
<td>0.24</td>
<td>10</td>
<td>0.21</td>
<td>High Ft</td>
</tr>
<tr>
<td>120</td>
<td>1.8</td>
<td>0.6</td>
<td>0.24</td>
<td>10</td>
<td>0.3</td>
<td>High breakdown</td>
</tr>
<tr>
<td>180</td>
<td>2.5</td>
<td>0.8</td>
<td>0.24</td>
<td>10</td>
<td>0.58</td>
<td>High FT</td>
</tr>
<tr>
<td>180</td>
<td>2.5</td>
<td>0.8</td>
<td>0.24</td>
<td>10</td>
<td>0.75</td>
<td>High Breakdown</td>
</tr>
<tr>
<td>250</td>
<td>3.3</td>
<td>0.8</td>
<td>0.24</td>
<td>10</td>
<td>0.53</td>
<td>High FT</td>
</tr>
<tr>
<td>250</td>
<td>3.3</td>
<td>0.8</td>
<td>0.24</td>
<td>10</td>
<td>0.54</td>
<td>High breakdown</td>
</tr>
</tbody>
</table>

Table 6.1. Technology comparison. Simulation results of bipolar transistor.

Figure 6.2. Plot of frequency versus NFmin in different technologies for bipolar transistor.
Figure 6.3. Plot of Vcc versus NFmin in different technologies for bipolar transistor.

Figure 6.4. Plot of Vbe versus NFmin in different technologies for bipolar transistor.
6.2 CMOS transistor

Figure 6.5. Simulation testbench for technology comparison - CMOS type

For the CMOS transistor, the thermal noise is simply the primary and dominant noise, after which comes the flicker noise for (lower frequencies mainly) and then the shot noise. Similar to the bipolar transistor part the NCT analysis was used to conclude with these results.

As stated before the simulations were done for a single common emitter (common source) transistor and no other transistors or RLC components were placed. So hence the series resistance of the terminals (mainly base or gate) is the dominant noise component of the circuit. The simulation results are shown in Table 6.2. In this Table 6.2, the Dgnfet device type has very low noise figure minimum (0.04dB). The noise modelling for this device type is not known properly to explain the reason for so low noise figure. The NFmin versus frequency, VDD and VGS are shown in the Figure 6.6-6.8.

<table>
<thead>
<tr>
<th>Technology node [nm]</th>
<th>Vdd [V]</th>
<th>Vgs [V]</th>
<th>width [um]</th>
<th>length[nm]</th>
<th>Noise Figure minimum [dB]</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>120</td>
<td>1.5</td>
<td>0.6</td>
<td>10</td>
<td>120</td>
<td>0.18</td>
<td>Nfet_rf</td>
</tr>
<tr>
<td>120</td>
<td>2.5</td>
<td>0.7</td>
<td>10</td>
<td>240</td>
<td>0.04</td>
<td>Dgnfet</td>
</tr>
<tr>
<td>180</td>
<td>2.5</td>
<td>0.7</td>
<td>40</td>
<td>180</td>
<td>0.22</td>
<td>Nfet_rx</td>
</tr>
<tr>
<td>180</td>
<td>2.5</td>
<td>0.8</td>
<td>20</td>
<td>320</td>
<td>0.24</td>
<td>Nfet25_rf</td>
</tr>
<tr>
<td>180</td>
<td>3.3</td>
<td>1.6</td>
<td>20</td>
<td>400</td>
<td>0.44</td>
<td>Nfet_33x</td>
</tr>
<tr>
<td>250</td>
<td>3.3</td>
<td>0.9</td>
<td>20</td>
<td>240</td>
<td>0.33</td>
<td>Nfet_rf</td>
</tr>
<tr>
<td>250</td>
<td>3.3</td>
<td>0.9</td>
<td>20</td>
<td>400</td>
<td>0.24</td>
<td>Nfet33_rf</td>
</tr>
</tbody>
</table>

Table 6.2. Technology comparison. Simulation results of CMOS transistor.
The simulations were done for the bipolar devices as well as the CMOS devices for various processes in the IBM PDK kit, the noise figure minimum was calculated and the NCT analysis was also reviewed, which will display the percentage of noise contributed by the various devices used, only one transistor in this case.

![Figure 6.6](image1)

Figure 6.6. Plot of frequency versus NFmin in different technologies for CMOS.

![Figure 6.7](image2)

Figure 6.7. Plot of Vdd versus NFmin in different technologies for CMOS.
Figure 6.8. Plot of Vgs versus NFmin in different technologies for CMOS.

6.3 Conclusions

For the bipolar and the CMOS transistors the minimum noise figure NFmin increases with the increase in frequency and decreases with the increase in voltage supply. When comparing the NFmin with the Vbe and Vgs, it is lowest at a particular voltage and gets higher before and after that voltage.

Thus from the above simulation results and graphs, the suitable transistors in particular technology node required for our application, the one having the lowest noise figure minimum is selected. The selected transistor will be used for designing the LNA circuit which will be described in the following sections. We are choosing the 120nm technology bipolar and CMOS transistors for our design as the lowest noise figure was obtained and also the lower supply voltage can be used, hence lower power consumption as discussed in chapter 7.
7. Design and implementation of LNA

After comparing the technology and characteristics of the bipolar (BiCMOS) and CMOS transistors, the 120nm technology was used for the LNA design. The goal is to design a low noise amplifier with low noise figure, a high IP3, good gain mainly. Other metrics such as stability, 1dB compression point and so on are also taken into consideration. The BiCMOS transistor is used for designing at first to observe its performance and then the CMOS transistor is used for designing the LNA since CMOS has better performance, cost, functionality and manufacturability for digital and analog integrated circuits. The CMOS has higher $F_T$ than other types and hence provides freedom for high speed analog circuit and also CMOS has better bias and gain control.

The preliminary specification are low noise figure, less than 1dB, gain around 18-20dB and OIP3> 40 dBm. For this purpose, I will be using a reference paper by Domine Leenaerts, NXP Semiconductors, which implemented a Base Station LNA, with 0.5dB noise figure and 36 dBm OIP3 using a SiGe transistor (discrete device) in a 250nm BiCMOS technology [22]. In the paper, a two-stage LNA is used which completely fits to the specification required in this work. Since the reference paper uses a SiGe transistor the integration density will be high and also the entire components are integrated on-chip. The measured results of their LNA has a noise figure of 0.75 dB and OIP3 of 36dBm as stated above, which is needed parameter values for a base station application, in particular macro base station where sensitivity is more important. If we suppose the same performance can be obtained using a CMOS process it will be even better as the product markets tends towards CMOS for most applications. Thus the LNA designing in CMOS and meeting the specifications will be a part of this thesis.

7.1 Reason for this design

As mentioned in the previous parts, the current trend for the LNA with very low noise prefers the SiGe transistors since higher integration level is possible with the use of silicon. But, the main purpose of the work is to verify the simulated performance of the MOS transistor towards low noise figure and high linearity.

When designing a single stage LNA with either bipolar transistors or CMOS transistors, we may get a low noise figure with better IP3, but not with a reasonable gain and stability. Due to the trade-offs between each of the parameters it is quite difficult to have a low noise figure, high IP3, good gain and stability and also optimized values of the components used. Now, these drawbacks can be overcome with the use of a two stages LNA and hence goes the design of the same in the following sections. These can be understood more clearly by the Friis' formula for noise and linearity as stated in equation 2.4 and 2.5.

From the equation 2.4 and 2.5 it can be understood that, the noise figure for the first stage with high gain and the IP3 of the later stages with less gain can yield a good performance with low noise figure and high linearity, thus the entire receiver sensitivity can be controlled.
In the following sections, the design and implementation of the bipolar transistor two-stage LNA, similar to Leenaerts [22] will be designed and after understanding of the implementation of this design a new circuit similar to this bipolar design but in CMOS will be implemented, thereby, the difference in characteristics and further improvements will be performed in the CMOS process.

7.2 Bipolar (BiCMOS)

The bipolar is also stated as BiCMOS, the intent is to have the characteristics of a SiGe transistor in the design, but since this work will not go into the layout in this thesis just a LNA schematic using a BJT which was mentioned as bipolar transistor all over will be done. The design of the LNA in this case is done by designing the two stages individually and connect them together to complete the two-stage design. The IBM 8WL, means 120nm technology node with transistors pre-defined with dimensions and parasitics and the term WL stands for applications in wireless and low power purposes. And the transistor type that is chosen for this purpose is modelled for RF applications. The reason for such selections is to ensure that, even after layout and fabrication of the design there will not be too large variation compared to the results obtained during the simulations before the layout.

7.2.1 First Stage

The schematic of the first stage is shown in Figure 7.1, constituting a single transistor with passive components to vary the impedances, gain, noise and other metrics. The width of the transistor is first fixed to 10µm and checked for results like, NF, optimal impedance Z_{opt}, and gain. The main aim of the design work was to have the lowest noise figure possible along with a good linearity and then a better gain. Since the input port resistance is 50Ω, we need to bring the optimal impedance to a close range to have the noise figure (NF) close to the noise figure minimum (NFmin).

Initially, the optimal impedance Z_{opt} was around 824+j1152Ω. Now to bring it near 50Ω, the multiplicity of the transistor was increased to 17, which brought the Re\{Z_{opt}\} to near 50Ω with some positive imaginary part. To eliminate this imaginary part, an inductor equal to the reactance part of the Z_{opt} was added. The Z_{opt} is the optimal impedance of the device, which when matched to the source impedance Z_s provides a good noise match. This can be explained by the formula below. When the match is done the second value tends to zero and hence F=F_{min}. This is the approach employed here.

\[
F = F_{MIN} + \frac{\Delta R}{R_s} \left| Z_s - Z_{opt} \right|^2
\]

(7.1)

Let Z_{opt} = R + X.

Now X is positive and hence \(X_L = 2\pi F L\).

Where, F= frequency of interest, 2 GHz in this case.

\[L = \text{inductance equivalent to } X_L.\]
Thus from this, the L can be obtained and placed in series with the gate as shown in the Figure 7.1 as Lin. After inserting the Lin, the NF ≈ NFmin= 0.49 dB.

![Figure 7.1. Schematic of first stage of LNA using bipolar transistor.](image)

The components I28 (DC block) and I26 (DC pass), as seen in Figure 7.1, are used to block the DC and feed the DC current respectively. And now the Lout is inserted. This is to control the gain, as the gain is dependent on the load and to control the output impedance. Since the output impedance is high, over 50Ω and there is a need to reduce the output impedance Zout since this will allow to have a larger transistor width for the second stage and hence a higher IP3 values can be obtained. For this reason, tapping of the inductor as shown in the figure worked out well and reduced the Re{Zopt} ≈ 13Ω.

The degeneration inductor (Ldegen) is used to reduce the gain a bit and to control the Zopt and Zin (input impedance), which also translates to better S_{11} values and hence has better input isolation. Finally the C1 capacitor is to control the stability of the system, mainly it varies the Zin and Zopt values in large variation. The C1 also helps to vary the gain and IP3 values. Thus the insertion of C1 brings flexibility to the design which changes few parameters drastically. This concludes the circuit setup with the values used as displayed below.

<table>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>0.81</td>
<td>2.3</td>
<td>2.5n</td>
<td>0.8</td>
<td>1.7</td>
<td>0.12</td>
<td>10</td>
<td>16</td>
</tr>
</tbody>
</table>

Table 7.1. Component values in the first stage of the bipolar transistor LNA.
7.2.2 Stage 1 Simulation results

With the above circuit design and component values, the simulations were run to obtain the metrics desired and is obtained using the SP and IP analysis. Using these analysis several simulations were run sweeping each of the variable to see its impact over the results. From the SP analysis available in the GoldenGate results window, the NF, NFmin, Z parameters, S parameters, gains, stability variables and few more parameters can be obtained. The IP analysis is for obtaining the IIP3 and the OIP3 values. After the simulations, the values obtained are listed in the Table 7.2 below.

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</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.49</td>
<td>0.49</td>
<td>15</td>
<td>25.5</td>
<td>10.6</td>
<td>-10.8</td>
<td>-3</td>
<td>0.58</td>
</tr>
</tbody>
</table>

Table 7.2. Simulation results of the first stage of the bipolar transistor LNA.

These are the main result variables for the first stage. Every metrics are as expected and also the stability is good since Δ < 1. The Δ is a stability measure defined by equation shown below, when Δ<1 the circuit can be considered to be unconditionally stable. The remaining parameters are shown below.

\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \]  

(7.5)

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>50.9+j0.14</td>
<td>49.6+j59</td>
<td>13.2+j10.7</td>
<td>17.6</td>
<td>14.6</td>
<td>-22.54</td>
<td>14.6</td>
</tr>
</tbody>
</table>

Table 7.3. Remaining Simulation results of the first stage of the bipolar transistor LNA.

From Table 7.3, the Zopt is almost 50 Ω and the Zin close to it, thereby making a good S11 value. I am not any more concerned about the circuit design and parameters as the purpose is to verify and understand, since CMOS design is the goal.

7.2.3 Second Stage

The second stage design is almost similar to what is done in the first stage except for few changes and increase in the emitter length of the transistor used. This is done to have a large IP3 value in the second stage and having a reasonable gain so that when the two stages are added together the final circuit will have good gain and also IP3 values. To have a higher IP3 values, transistors with larger width are used which is directly proportional to the IP3 values and can be understood from the equation 7.6 below,

\[ IP3 = \sqrt{\frac{4G_m}{3G_{m3}}} \]

(7.6)

where, \( G_m \) is the output transconductance of the circuit and \( G_{m3} \) is the 3 order product of nonlinear term in the Taylor series expansion. By having a large transistor the Zin and Zopt will be low, and this is the reason for having a low Zout in the first stage so that there will not
be much interstage matching problems. The schematic of this stage is shown below in Figure 7.2.

As seen in the schematic, there is not much a difference between the first and second stage, except that instead of the C1, C3 a feedback capacitor is used to get more linearity and also flatten the gain instead of a steep curve. And the Lout is not tapped since we will require an output impedance high enough, equal to around 50Ω. Thus from this circuit, a high linearity with a reasonable gain and a low NF not deviating too much from the NFmin is obtained. The component values are chosen after several simulations and are displayed below in Table 7.4.

<table>
<thead>
<tr>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>0.81</td>
<td>9</td>
<td>0.2</td>
<td>0.2</td>
<td>0.12</td>
<td>20</td>
<td>26</td>
</tr>
</tbody>
</table>

Table 7.4. Component values in the second stage of the bipolar transistor LNA.

![Figure 7.2. Schematic of second stage of LNA using bipolar transistor.](image)

### 7.2.4 Stage 2 Simulation Results

The simulations are similar to what was done in the first stage, using the SP and IP analysis to find the required results. In this simulation, the interesting parameter was the C3 capacitor which works as a feedback tuning the gain and the impedance levels, also not to forget, the IP3 value. The results for this stage is displayed below in Table 7.5.
<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.5</td>
<td>0.59</td>
<td>16.7</td>
<td>36.2</td>
<td>19.5</td>
<td>-7</td>
<td>-7.3</td>
<td>0.7</td>
</tr>
</tbody>
</table>

Table 7.5. Simulation results of the second stage of the bipolar transistor LNA.

The NF is deviated almost 1 dB from the NFmin, otherwise the rest of the values are reasonably OK and also the circuit is stable.

<table>
<thead>
<tr>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>15+j 9.6</td>
<td>0.45-j0.96</td>
<td>12.2+j1.75</td>
<td>13.68</td>
<td>17.26</td>
<td>-18.75</td>
<td>15.77</td>
</tr>
</tbody>
</table>

Table 7.6. Remaining Simulation results of the second stage of the bipolar transistor LNA.

The Zopt is brought close to the Zout of the first stage, and the Zout of this stage is not yet optimized. Also the S12 is not a good value. Something around -30dB can be accepted as a good value, but once the two stages are combined together the value gets really good due to good isolation which will be seen in the next section.

**7.2.5 Two-Stage BiCMOS LNA**

Now the two stages that were designed separately are connected together to form the entire LNA design and the performance can be observed. The setup of the two stages has not been changed and to create a DC block between the two stages, a capacitor is placed, which also has some impact in the performance of the design. The two-stage LNA now looks as Figure 7.3 below.

![Figure 7.3. Schematic of two-stage LNA using bipolar transistor](image-url)
The C2 (80 pF) is the blocking capacitor in between the two stages, and the rest when clubbed together gave a really good performances. All other components values are the same except for the C3 capacitor (400fF).

### 7.2.6 Two-stage LNA simulation results

The simulation for the entire circuit is performed and to find the 1dB compression point, a GoldenGate Gain Compression (GC) analysis was done and the required P-1dB in terms of gain and output and input power was determined. The results are tabulated below in Table 7.7.

<table>
<thead>
<tr>
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<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.5</td>
<td>0.5</td>
<td>32.2</td>
<td>34</td>
<td>1.3</td>
<td>-8</td>
<td>-19</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Table 7.7. Simulation results of the two-stage of the bipolar transistor LNA.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>-8.68</td>
<td>21.84</td>
<td>51+j0.19</td>
<td>6.86-j36.8</td>
<td>15.3-j15.5</td>
<td>31.57</td>
<td>-37.3</td>
<td>31.5</td>
</tr>
</tbody>
</table>

Table 7.8. Remaining Simulation results of the two-stage bipolar transistor LNA.

These are the final main parameter values obtained. Not everything are exactly the same as of the reference I chose, there are few values better, and there are few slightly degraded from what they obtained. One of those issues is the stability, which for this design is unconditionally stable above 1 GHz frequency.

### 7.2.7 Optimized two-stage LNA

Now to go one step further and analyse the circuit, an improvisation of linearity and system stability is required and hence as a result, matching networks are used and optimized towards even a better OIP3.
The components used in the circuit above including the matching networks are tabulated below.

<table>
<thead>
<tr>
<th>Vcc  [V]</th>
<th>Vbe 1 [V]</th>
<th>Vbe 2 [V]</th>
<th>L match 1a [nH]</th>
<th>L match 1b [nH]</th>
<th>L match 2 [nH]</th>
<th>L degen1 [nH]</th>
<th>L degen2 [nH]</th>
<th>L inter-stage [nH]</th>
<th>Lin [nH]</th>
<th>Lout [nH]</th>
<th>Cout [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3</td>
<td>0.81</td>
<td>0.81</td>
<td>4.308</td>
<td>5</td>
<td>10</td>
<td>2n</td>
<td>286.5p</td>
<td>2.477</td>
<td>3.18</td>
<td>3.595</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>2.928</td>
<td>10</td>
<td>20</td>
<td>0.12</td>
<td>0.12</td>
<td>16</td>
<td>40</td>
<td></td>
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</tbody>
</table>

Table 7.9. Component values in the optimized two-stage bipolar transistor LNA.

### 7.2.8 Optimized Simulation Results

The simulation procedure is the same as the one used before the change in the circuit. The use of the inter-stage match has enhanced the isolation a bit and also increased the OIP3 values more than obtained in the previous design. All these are performed for circuit connected to a 50Ω input and output port resistance and the results are shown below.
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</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.55</td>
<td>0.6</td>
<td>26.8</td>
<td>40.3</td>
<td>13.5</td>
<td>-2.6</td>
<td>-2.7</td>
<td>0.68</td>
</tr>
</tbody>
</table>

Table 7.10. Results of the optimized two-stage bipolar transistor LNA.

<table>
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<tr>
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</thead>
<tbody>
<tr>
<td>-1.85</td>
<td>20.48</td>
<td>36.3+j1.01</td>
<td>8.55-j43.8</td>
<td>36.28+j23.78</td>
<td>26.58</td>
<td>-39.5</td>
<td>23.32</td>
</tr>
</tbody>
</table>

Table 7.11. Remaining Results of the optimized two-stage bipolar transistor LNA.

Thus, the two-stage low noise amplifier design using the bipolar transistor in the 120nm technology has been verified and also modified to an optimized performance design. The corresponding plots are displayed below. Though the required operating frequency is 2 GHz the simulations were done from 0.5GHz to 5GHz to observe the characteristics of the circuit before and after the required 2GHz. This would help to analyse the stability, gain performance, and noise variation over this frequency range.

Figure 7.5. Plot of frequency versus nfmin for two-stage bipolar transistor LNA.
Figure 7.6. Plot of frequency versus $S_{21}$ for two-stage bipolar transistor LNA

Figure 7.7. Plot of frequency versus $S_{22}$ and $S_{11}$ for two-stage bipolar transistor LNA
The successful design of the two-stage LNA in the previous section is the motivation for continuing the design using CMOS transistor devices due to few superior advantages over other device types. Mainly, the cost is reduced and also, the linearity of CMOS is higher than other devices as discussed in previous sections, hence trying to maintain a low noise figure is the key for this design, since attaining high linearity is a bit
easier. The noise of a CMOS is very low compared to the bipolar part which is evident in the technology comparison section, and hence the design should be carefully dealt with, to not have more difference between the NF and NFmin. The design is done similarly in two parts, designing the two stages individually and later add them together to get the entire two stage design. Another advantage is that the CMOS transistor used is from the same technology node and is available in the IBM 8WL process too, as a result, the implementation is will be easier. The reason for selecting the 120nm technology is because the NFmin is around 0.18 dB, smallest compared to other technologies and also the supply voltage can be reduced. As a result smaller noise figure and also power dissipation can be obtained.

7.3.1 First stage

Similar to section 7.2.1, a single transistor which is a RF model operating in the 1.5 V supply is placed and simulated. Now similar to the bipolar process, we will calculate the Zopt value first and bring it equal or within the 50Ω source resistance so that the NF and NFmin can be brought as close as possible. Initially, the impedance levels were very high compared to that in the bipolar process, \( \text{Re}(Z_{\text{opt}}) = 2175.24 + j \ 6047.5\Omega \). The impedance is so high due to the device physics of the CMOS transistor which was explained in the previous sections. The impedance value stated above was calculated by using a testbench similar to that in Figure 6.1. So now as a result, higher transistor width is required and hence a transistor of width of 10µm with multiplicity of 50. The circuit schematic of the first stage is shown below in Figure 7.10.

![Figure 7.10. Schematic of the first stage of LNA using CMOS transistor.](image-url)
The Lin is used to cancel out the imaginary part of the Zopt so that the real part is exactly 50Ω. And hence the NF = NFmin. Now, the load impedance is placed for controlling the Zout and the gain. Also for the same purpose, the C1 is inserted and the input impedance can be controlled by varying it. The degeneration inductor is not suited to use in this design as inserting it has reduced the gain badly and also Zopt, so it is not used here. This is the circuit setup and the component values are tabulated below.

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</thead>
<tbody>
<tr>
<td>1.5</td>
<td>0.55</td>
<td>9.85</td>
<td>7</td>
<td>1.2</td>
<td>10</td>
<td>0.12</td>
<td>50</td>
</tr>
</tbody>
</table>

Table 7.12. Component values of first stage CMOS transistor LNA.

### 7.3.2 First stage simulation results:

The simulations are done using SP and IP analysis which yields the parameter metrics that are displayed in the table below. The other characteristics and process are similar to that of bipolar transistor design.

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<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.16</td>
<td>0.16</td>
<td>21.2</td>
<td>29.17</td>
<td>7.98</td>
<td>-1</td>
<td>-0.9</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 7.13. Simulation results of first stage CMOS transistor LNA.

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</thead>
<tbody>
<tr>
<td>50+ j0</td>
<td>15.78+j105</td>
<td>10.75-j12.5</td>
<td>14.2</td>
<td>14.2</td>
<td>-26</td>
<td>14.25</td>
</tr>
</tbody>
</table>

Table 7.14. Remaining Simulation results of first stage CMOS transistor LNA.

As seen above, the NF is as low as 0.16 dB, which is very small compared to that obtained in the bipolar case. And the drain current taken is around, Id ~ 33.46 mA. These are satisfying results. But we must observe how they react when joined with second stage.

### 7.3.3 Second Stage:

The schematic of the second stage will be similar to the second stage of the bipolar design, but we will be omitting the degeneration inductor and also include the shunt capacitor at the drain as there was a need to improve the OIP3, output impedance and to reduce gain a bit. The Cf capacitor is used to improve the linearity and have a feedback to control the gain slope and flatten it. The schematic is shown in the Figure 7.11 below.

The components value of this design is tabulated in Table 7.15. The major difference is that the width of the transistor, which is 89 multiplicity of 10µ width. The rest is similar. And also
the Lin, gate inductor used is a null value as it was used to check performance when the Zopt was exactly 50Ω. But later, it will be seen that exact values are not so critical as we have good performances.

![Schematic of the Second stage of LNA using CMOS transistor.](image)

Table 7.15. Component values of second stage CMOS transistor LNA.

<table>
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<tr>
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</thead>
<tbody>
<tr>
<td>2.5</td>
<td>0.6</td>
<td>8</td>
<td>0.1</td>
<td>10</td>
<td>0.24</td>
<td>80</td>
</tr>
</tbody>
</table>

7.3.4 Second stage simulation results:

The simulation procedure and other procedures are similar to that of the first stage and the results obtained are tabulated.

![Simulation results of second stage CMOS transistor LNA.](image)

Table 7.16. Simulation results of second stage CMOS transistor LNA.

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<tr>
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</thead>
<tbody>
<tr>
<td>2</td>
<td>0.15</td>
<td>1.03</td>
<td>22.6</td>
<td>33.6</td>
<td>11</td>
<td>-0.5</td>
<td>-7</td>
<td>0.44</td>
</tr>
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<td>----------</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>15.8+j66.3</td>
<td>1.63-j9.9</td>
<td>20.27+j0.68</td>
<td>13.57</td>
<td>14.4</td>
<td>-15.8</td>
<td>12.91</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 7.17. Remaining Simulation results of Second stage CMOS transistor LNA.

The drain current is $I_d=15.35$ mA.

The $\text{Re}\{Z_{\text{opt}}\}$ is made close to the $Z_{\text{out}}$ of the first stage to avoid much mismatch between the two stages. In this stage it can be observed that NF is around 1 dB, reason, the OIP3 is given more importance for the second stage than other parameters.

### 7.3.5 Two-stage CMOS LNA design:

Once the two stages are completed the two-stage design can be designed combining both stages we as did in the bipolar design. The schematic of the two-stage CMOS LNA is displayed below in Figure 7.12.

![Figure 7.12](image)

Figure 7.12. Schematic of the two-stage LNA using CMOS transistors.

### 7.3.6 Two-stage LNA Simulation results:

By simulating the two stages together, with using matching networks at the input and output to provide a perfect $50\Omega$ match, NF $\approx N_{\text{Fmin}}$, OIP3 $\approx 36\,\text{dBm}$, gain $\approx 29\,\text{dB}$. But by removing the matching networks, the OIP3 was increased to $48\,\text{dBm}$ and this was possible using the $C_2$ capacitor in the schematic. Now, to have better $S_{11}$, slight matching towards $50\Omega$ was done. To have a high IIP3 the gain was reduced a bit, and hence the circuit now gives values as tabulated in table below.
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</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.25</td>
<td>0.25</td>
<td>26.5</td>
<td>46</td>
<td>19.5</td>
<td>-6.35</td>
<td>-12</td>
<td>0.24</td>
</tr>
</tbody>
</table>

Table 7.18. Simulation results of two stage CMOS transistor LNA.

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>-8.7</td>
<td>15.6</td>
<td>50+j1.023</td>
<td>46.53+j33.4</td>
<td>78.5-j16.63</td>
<td>25.61</td>
<td>-43.8</td>
<td>25.3</td>
</tr>
</tbody>
</table>

Table 7.19. Remaining Simulation results of two stage CMOS transistor LNA.

These are the final results for the CMOS two-stage LNA design. The drain currents are the same for the two stages and the design can be further improved for reducing the drain current and also the stability of the system. This design is unconditionally stable from 800MHz which was estimated from the Δ graph as in Figure 7.17, where the magnitude of Δ is less than 1 above 800MHz. But as a part of the thesis, it is not so important to get the most optimized results. The task is to analyse and understand if a two-stage LNA with lowest noise figure, high OIP3 and a good gain is possible with reasonable stability and other parameters, which is achieved using the above design. Further the various parameters across other frequencies are plotted below.

Figure 7.13. Plot of frequency versus noise figure and noise figure minimum for two-stage CMOS LNA.
Figure 7.14. Plot of frequency versus $S_{21}$ for two-stage CMOS LNA.

Figure 7.15. Plot of frequency versus $S_{11}$ and $S_{22}$ for two-stage CMOS LNA.
Figure 7.16. Plot of frequency versus various gains for two-stage CMOS LNA.

Figure 7.17. Plot of frequency versus stability (delta) for two-stage CMOS LNA.
The above plots describe the performance of the circuit over a range of frequencies. Two main things that are observed is that, the difference between the NF and the NFmin scaling with frequency is not close, and the OIP3 value is almost constant. The rest of the parameters are the stability, S parameters and the different types of gains in the design.

7.4 Comparison between the bipolar and the CMOS design

The results can be compared for the bipolar and CMOS transistor design. For the bipolar circuit design, the values obtained can be found in Table 7.10. The NF is 0.6dB, gain is 27 dB and OIP3 around 40 dBm. Comparing with the reference [22] which has simulated NF around 1 dB for 1.8 GHz, gain 34dB and OIP3 of 36 dBm, the bipolar design of this work has better performance in simulations. The noise is lower and also the IP3 is larger than the reference and the gain in this work is around 27 dB, which lesser compared to the reference, but since the required gain was around 20 dB this is not a problem.

Now the CMOS simulation results are found in Table 7.18 where, the NF is 0.25dB, gain is 26 dB and OIP3 is 46 dBm. Compared to the bipolar design results the CMOS design has better values, this is what the design work is intended. In the simulations the performance of

Thus it can be concluded that the LNA design has the potential to be successful using the CMOS.

7.5 Design Flow Chart

The flow chart below describes the design flow for a LNA used in this thesis and also provides a general path and parameters to be considered while designing a LNA. In the flow chart, each phase of the thesis and the step taken to finish them will be displayed.

Initially the LNA specifications was decided and later to select a suitable technology node to perform the design, technology simulations were performed and later the suitable technology for the required specifications is chosen.

After the technology comparison the LNA design was using the bipolar and the CMOS process. Then the remaining steps like choosing the device sizes, components values and other factors to tune the two-stage LNA to the required frequency and specifications with best optimized values. The iterations of the design were repeated until the required results are obtained. Thus the two-stage LNA can be designed and verified as shown in the design flow chart below.
LNA DESIGN SPECIFICATIONS

Choice of Technology in the IBM PDK. (120nm/180nm/250nm)

Selecting suitable bipolar transistor
Selecting suitable NMOS transistor

Estimate device size and suitable supply & bias voltages

Device Simulations/Testing

Is $NF \approx NF_{min}$
Is $Z_{opt} > 50$
Is gain $> 20$
Add series gate inductor for match
Add degeneration inductor
Place output inductor and check bias voltages

Is $OIP3 > 40$
Is $S11 \approx S_{opt}$
Is $Z_{in} \& Z_{out}$ close to $Z_{out}$
Is design stable
Is $Z_{in} \& Z_{out}$ close to $Z_{out}$
Try shunting at load or make feedback.

Improvise I/O matching network
Vary topology

Check if entire specifications are met.
Optimize and finalize design
8. Conclusion

An ultra-low noise two-stage LNA is designed using the IBM BiCMOS 120nm technology. For bipolar design, noise figure of 0.6dB, OIP3 of 40.3dBm and gain of 26.8dB were obtained. For the CMOS design, noise figure of 0.25dB, OIP3 of 46dBm and gain of 26dB were obtained. The noise for the CMOS design is lower, the linearity is higher with a good gain and hence a satisfactory result of the CMOS LNA design was obtained. Compared to the bipolar transistor results the CMOS design has better simulated performance. Both designs were able to fulfill the design goals of noise figure < 1 dB, OIP3 > 40 dBm, and gain >18 dB. Thus it can be concluded that the LNA design shows good potential using a CMOS circuit design.
9. Future Work

- Optimize the CMOS design for fabrication and evaluate and compare the results. The current work performed has mostly ideal components. These have to be replaced and design a complete schematic of the proposed LNA and then go to the layout to enable fabrication. Finally test and compare with simulation and measurement values and also with current products in the market.

- An LNA for better area efficiency and lower power consumption with similar good performance of this work. As the power consumption is high and also the area of the current work is large, which can be reduced even more and obtain some good performance something similar to what has been achieved in this thesis.

- Try different architecture like differential type of LNA for better matching and can make it easy to combine with a mixer too. Integrate LNA and mixer in a single chip, which saves some area, losses and cost.
10. References:


[6]. http://www.users.york.ac.uk/~dajp1/Introductions/GSW_Noise_and_IP3_in_Receivers.pdf


[15]. Bevin G. Perumana, Jing-Hong C.Zhan, Stewart S. Taylor, Brent R.Carlton, and Joy Laskar, “A 9.2 mW, 4-8GHz Resistive Feedback CMOS LNA with 24.4 dB Gain, 2 dB Noise Figure , and 21.5 dBm Output IP3,” IEEE SiRF, 2008, pp. 34-37.


[21]. http://www.springerlink.com/content/g2t041127042083g/fulltext.pdf

[22]. Domine Leenaerts, Jos Bergervoet, Jan-Willem Lobeek, and Marek Schmidt-Szalowski, “900MHz/1800MHz GSM Base station LNA with sub-1dB Noise Figure and +36dBm OIP3,” IEEE RFIC Symposium, 2010, pp. 513-516.


