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CMOS RF Power Amplifiers for Wireless Communications

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Cover image:
The cover image demonstrates the idea of outphasing.

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Abstract

The wireless market has experienced a remarkable development and growth since the introduction of the first modern mobile phone systems, with a steady increase in the number of subscribers, new application areas, and higher data rates. As mobile phones and wireless connectivity have become consumer mass markets, the prime goal of the IC manufacturers is to provide low-cost solutions.

The power amplifier (PA) is a key building block in all RF transmitters. To lower the costs and allow full integration of a complete radio System-on-Chip (SoC), it is desirable to integrate the entire transceiver and the PA in a single CMOS chip. While digital circuits benefit from the technology scaling, it is becoming harder to meet the stringent requirements on linearity, output power, bandwidth, and efficiency at lower supply voltages in traditional PA architectures. This has recently triggered extensive studies to investigate the impact of different efficiency enhancement and linearization techniques, like polar modulation and outphasing, in nanometer CMOS technologies.

This thesis addresses the potential of integrating linear and power-efficient PAs in nanometer CMOS technologies at GHz frequencies. In total eight amplifiers have been designed - two linear Class-A PAs, two switched Class-E PAs, and four Class-D PAs linearized in outphasing configurations. Based on the outphasing PAs, amplifier models and predistorters have been developed and evaluated for uplink (terminal) and downlink (base station) signals.

The two linear Class-A PAs with LC-based and transformer-based input and interstage matching networks were designed in a 65nm CMOS technology for 2.4GHz 802.11n WLAN. For a 72.2Mbit/s 64-QAM 802.11n OFDM signal with PAPR of 9.1dB, both PAs fulfilled the toughest EVM requirement in the standard at average output power levels of +9.4dBm and +11.6dBm, respectively. The two PAs were among the first PAs implemented in a 65nm CMOS technology.

The two Class-E PAs, intended for DECT and Bluetooth, were designed in 130nm CMOS and operated at low 'digital' supply voltages. The PAs delivered +26.4 and +22.7dBm at 1.5V and 1.0V supply voltages with PAE of 30% and 36%, respectively. The Bluetooth PA was based on thin oxide devices and the performance degradation over time for a high level of oxide stress was evaluated.

The four Class-D outphasing PAs were designed in 65nm, 90nm, and 130nm CMOS technologies. The first outphasing design was based on a Class-D stage utilizing a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5V supply voltage in a 65nm CMOS technology without excessive device voltage stress. Two on-chip transformers combined the outputs of four Class-D stages. At 1.95GHz the PA delivered +29.7dBm with a PAE of 26.6%. The 3dB bandwidth was 1.6GHz, representing state-of-the-art bandwidth for CMOS Class-D RF PAs. After one week of continuous operation, no performance degradation was noticed. The second design was based on the same Class-D stage, but combined eight amplifier stages by four on-chip transformers in 130nm CMOS to achieve a state-of-the-art output power of +32dBm for CMOS Class-D RF PAs. Both designs met the ACLR and modulation requirements without predistortion when amplifying uplink WCDMA and 20MHz LTE signals.

The third outphasing design was based on two low-power Class-D stages in 90nm CMOS featuring a harmonic suppression technique, cancelling the third harmonic in the output spectrum which also improves drain efficiency. The proposed Class-D stage creates a voltage level of $V_{DD}/2$ from a single supply voltage to shape the drain voltage, uses only digital circuits and eliminates the short-circuit current present in inverter-based Class-D stages. A single Class-D stage delivered +5.1dBm at 1.2V supply voltage with a drain efficiency and PAE of 73% and 59%, respectively. Two Class-D stages were connected to a PCB transformer to create an outphasing amplifier, which was linear enough to amplify EDGE and WCDMA signals without the need for predistortion.

The fourth outphasing design was based on two Class-D stages connected to an on-chip transformer with peak power of +10dBm. It was used in the development of a behavioral model structure and model-based phase-only predistortion method suitable for outphasing amplifiers to compensate for both amplitude and phase mismatches. In measurements for EDGE and WCDMA signals, the predistorter improved the margin to the limits of the spectral mask and the ACLR by more than 12dB. Based on a similar approach, an amplifier model and predistortion method were developed and evaluated for the +32dBm Class-D PA design using a downlink WCDMA signal, where the ACLR was improved by 13.5dB. A least-squares phase predistortion method was developed and evaluated for the +30dBm Class-D PA design using WCDMA and LTE uplink signals, where the ACLR was improved by approximately 10dB.

Populärvetenskaplig sammanfattning

Trådlös kommunikation har sedan de första moderna mobiltelefonsystemen introducerades upplevt en enastående utveckling med ett ständigt ökande antal abonnenter, nya användningsområden och högre datahastigheter. Då mobiltelefoner och trådlösa apparater med radiokommunikation har blivit en massmarknad för konsumenter är det ytterst viktigt för tillverkare att ta fram små och billiga lösningar.

Effektförstärkaren är ett mycket viktigt byggblock i alla radiosändare. Effektförstärkaren sitter innan antennen och ser till att signalen blir tillräckligt stark för att sändas allt från ett tiotal meter, t.ex. Bluetooth, till tiotals kilometer, t.ex. GSM. För att minska kostnaden och nå målet med en full integrering av en komplett radio på ett chip (System-on-Chip, SoC) är det önskvärt att integrera hela kombinationen av sändare och mottagare, sändtagaren (transceiver på engelska), tillsammans med effekt-förstärkaren på samma CMOS-chip.

Medan digitala kretsar drar fördel av miniatyriseringen av transistorerna i CMOS blir det allt svårare att nå de tuffa kraven på linjäritet, uteffekt, bandbredd och energieffektivitet i effektförstärkaren då allt lägre spänningar används för att inte skada transistorerna. För att öka datahastigheten i trådlös kommunikation används numer både amplitud- och fasmodulering, vilket leder till dålig energieffektivitet med traditionella förstärkararkitekturer. Detta har lett till att man intresserat sig för att utvärdera nya kretstekniker och designmetoder för att kunna nå den önskade prestandan i effektförstärkare implementerade i CMOS.

Den här avhandlingen utvärderar potentialen i att integrera linjära och högeffektiva effektförstärkare och effektförstärkar-arkitekturer i CMOS-teknologier vid GHz-frekvenser. Totalt sett har åtta förstärkare konstruerats och utvärderats - varav två är linjära klass-A-förstärkare, två switchade klass-E-förstärkare samt fyra klass-D-förstärkare med konstant amplitud på utsignalen. Klass-D-förstärkarna har linjäriserats

genom outphasing-tekniken där två fasmodulerade signaler med konstant amplitud förstärks av två högeffektiva förstärkare, vars utsignaler läggs ihop för att skapa en amplitud-modulerad signal. Förutom förstärkarna, som byggts i 65nm, 90nm och 130nm CMOS-teknologier, har korrigeringsmetoder utvecklats och utvärderats för signaler för både mobiltelefoner och basstationer.

Preface

This Ph.D. thesis presents my research during the period February 2007 through October 2011 at the Electronic Devices group, Department of Electrical Engineering, Linköping University, Sweden. The following papers are included in the thesis:

- **Paper 1 – Jonas Fritzin,** Atila Alvandpour, "A 3.3V 72.2Mbit/s 802.11n WLAN Transformer-Based Power Amplifier in 65nm CMOS," *Journal of Analog Integrated Circuits and Signal Processing* (*Springer*), vol. 64, no. 3, pp. 241-247, August 2010.

- **Paper 2 – Jonas Fritzin,** Ted Johansson, Atila Alvandpour, "Impedance Matching Techniques in 65nm CMOS Power Amplifiers for 2.4GHz 802.11n WLAN," *IEEE European Microwave Conference* (*EuMC*), pp. 1207-1210, Amsterdam, The Netherlands, October 2008.

- **Paper 3 – Jonas Fritzin**, Atila Alvandpour, "Low Voltage Class-E Power Amplifiers for DECT and Bluetooth in 130nm CMOS," *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (*SiRF*), pp. 57-60, San Diego, CA, USA, January 2009.

- **Paper 4 – Jonas Fritzin,** Timmy Sundström, Ted Johansson, Atila Alvandpour, "Reliability Study of a Low-Voltage Class-E Power Amplifier in 130nm CMOS," *IEEE International Symposium on Circuits and Systems* (*ISCAS*), pp. 1907-1910, Paris, France, May 2010.

- **Paper 5 – Jonas Fritzin,** Christer Svensson, Atila Alvandpour, "A Wideband Fully Integrated +30dBm Class-D Outphasing RF PA in 65nm CMOS," *to be presented at IEEE International Symposium on Integrated Circuits* (*ISIC*), Singapore, December 2011. ***Chip Design Competition Finalist.***

- **Paper 6 – Jonas Fritzin**, Christer Svensson, Atila Alvandpour, "A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm for WCDMA/LTE," *IEEE European Solid-State Circuits Conference* (*ESSCIRC*), pp. 127-130, Helsinki, Finland, September 2011.

- **Paper 7 – Jonas Fritzin**, Christer Svensson, Atila Alvandpour, "A Class-D Outphasing RF Amplifier with Harmonic Suppression in 90nm CMOS," *IEEE European Solid-State Circuits Conference* (*ESSCIRC*), pp. 310-313, Seville, Spain, September 2010.

- **Paper 8 – Jonas Fritzin**, Ylva Jung, Per Niklas Landin, Peter Händel, Martin Enqvist, Atila Alvandpour, "Phase Predistortion of a Class-D Outphasing RF Amplifier in 90nm CMOS," *IEEE Transactions on Circuits and Systems–II: Express Briefs*, vol. 58, no. 10, pp. 642-646, October 2011.

- **Paper 9 – Jonas Fritzin**, Christer Svensson, Atila Alvandpour, "Design and Analysis of a Class-D Stage with Harmonic Suppression," *accepted for publication in IEEE Transactions on Circuits and Systems–I: Regular Papers*, 2011.

- **Paper 10 –** Per Niklas Landin, **Jonas Fritzin**, Wendy Van Moer, Magnus Isaksson, Atila Alvandpour, "Modeling and Digital Predistortion of Class-D Outphasing RF Power Amplifiers," *submitted for publication*, 2011.

- **Paper 11 –** Ylva Jung, **Jonas Fritzin**, Martin Enqvist, Atila Alvandpour, "Least-Squares Phase Predistortion of a +30dBm Class-D Outphasing RF PA in 65nm CMOS," *submitted for publication*, 2011.

My research has also included involvement in projects that has generated the following papers falling outside the scope of this thesis:

- **Jonas Fritzin**, Ted Johansson, Atila Alvandpour, "Power Amplifiers for WLAN in 65nm CMOS," *Swedish System-on-Chip Conference* (*SSoCC*), Södertuna Slott, Sweden, May 2008. ***Best Student Presentation Award***.

- **Jonas Fritzin,** Ted Johansson, Atila Alvandpour, "A 72.2Mbit/s LC-Based Power Amplifier in 65nm CMOS for 2.4GHz 802.11n WLAN," *IEEE Mixed Design of Integrated Circuits and Systems* (*MIXDES*) *Conference*, pp. 155-158, Poznan, Poland, June 2008.

- **Jonas Fritzin**, Atila Alvandpour, "A 72.2Mbit/s Transformer-Based Power Amplifier in 65nm CMOS for 2.4GHz 802.11n WLAN," *IEEE NORCHIP Conference,* pp. 53-56, Tallinn, Estonia, November 2008.

- **Jonas Fritzin**, Atila Alvandpour, "Low-Voltage High-Efficiency Class-E Power Amplifiers in 130nm CMOS for Short-Range Wireless Communications," *Swedish System-on-Chip Conference* (*SSoCC*), Arild, Sweden, May 2009.

- Sher Azam, Rolf Jonsson, **Jonas Fritzin**, Atila Alvandpour, Qamar Wahab, "High Power, Single Stage SiGaN HEMT Class E Power Amplifier at GHz Frequencies," *IEEE International Bhurban Conference on Applied Sciences & Technology* (*IBCAST*) *Conference*, Islamabad, Pakistan, January 2010.

- Hashim Raza Khan, Qamar Ul Wahab, **Jonas Fritzin**, Atila Alvandpour, "A 900MHz 26.8dBm Differential Class-E CMOS Power Amplifier," *IEEE German Microwave Conference* (*GeMIC*), pp. 276-269, Berlin, Germany, March 2010.

- **Jonas Fritzin**, Christer Svensson, Atila Alvandpour, "A Digital Linear CMOS RF Amplifier," *Swedish System-on-Chip Conference* (*SSoCC*), Kolmården, Sweden, May 2010.

- Ted Johansson, Noora Solati, **Jonas Fritzin**, "A High-Linearity SiGe RF Power Amplifier for 3G and 4G Small Basestations," *submitted for publication*, 2011.

- **Jonas Fritzin**, Christer Svensson, Atila Alvandpour, "A Fully Integrated High Power CMOS Power Amplifier," *Swedish System-on-Chip Conference* (*SSoCC*), Varberg, Sweden, May 2011.

- Rashad Ramzan, **Jonas Fritzin**, Jerzy Dabrowski, Christer Svensson, "Wideband Low Reflection Transmission Line for Bare Chip on Multilayer PCB," *ETRI* (*Electronic and Telecommunication Research Institute*) *Journal,* vol. 33, no. 3, pp. 335-343, June 2011.

- **Jonas Fritzin**, Behzad Mesgarzadeh, Atila Alvandpour, “A Class-D Stage with Third Harmonic Suppression and DLL-Based Phase Generation,” *submitted for publication*, 2011.

Contributions

The main contributions of this dissertation are as follows:

- Design and implementation of two linear WLAN PAs with LC-based and transformer-based input and interstage matching networks in 65nm CMOS.
- Design and implementation of two low-voltage Class-E RF PA designs in 130nm CMOS, also evaluated from a reliability perspective.
- Design and implementation of a high-voltage Class-D stage used in two fully integrated PA designs in 65nm and 130nm CMOS with output powers larger than +30dBm and with large bandwidths.
- Design, analysis, and implementation of a Class-D stage with 3rd harmonic suppression, short-circuit current elimination, and improvement in drain efficiency.
- Development of Class-D outphasing amplifier behavioral models and predistorters, verified and evaluated in measurements on a low-power outphasing RF amplifier with on-chip transformer in 90nm CMOS and a fully integrated +32dBm PA.
- Development of a phase predistortion method with a least-squares parameter estimator suitable for outphasing PAs. The predistortion method was evaluated on a +30dBm Class-D RF PA.

Abbreviations

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
CF	Crest Factor
DC	Direct Current
DE	Drain Efficiency
DECT	Digital Enhanced Cordless Telecommunications
EDGE	Enhanced Data Rates for GSM Evolution
EVM	Error Vector Magnitude
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	Global System for Mobile communications
HBT	Heterojunction Bipolar Transistor
IC	Integrated Circuit
InP	Indium Phosphide

IEEE	The Institute of Electrical and Electronics Engineers
ITRS	International Technology Roadmap for Semiconductors
LO	Local Oscillator
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MESFET	Metal-Semiconductor Field Effect Transistor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PMOS	P-channel Metal-Oxide-Semiconductor
PAE	Power-Added Efficiency
RF	Radio Frequency
RMS	Root-Mean-Square
WLAN	Wireless Local Area Network
WCDMA	Wideband Code Division Multiple Access

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Jonas Fritzin
Linköping, October 2011

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Part I

Background

Chapter 1

Introduction

1.1 Motivation and Scope of This Thesis

The wireless market has experienced a remarkable development and growth since the introduction of the first modern mobile phone systems, with a steady increase in the number of subscribers, new application areas, and higher data rates. As mobile phones and integration of wireless connectivity have become consumer mass markets, the prime goal of the IC manufacturers is to provide low-cost solutions.

CMOS has for a long time been the choice for digital integrated circuits due to its high level of integration, low-cost, and constant enhancements in performance. The RF circuits have typically been predominantly designed in GaAs [1] and silicon bipolar, due to the better performance at radio frequencies. However, due to the significant scaling of the MOS transistors, the transition frequency has reached over 100GHz. Along with the enhancements in speed, the MOS transistors have become popular to use for RF applications. The digital baseband circuits have successfully been integrated in CMOS, as well as most radio building blocks, and the last part to be efficiently integrated in CMOS is the Power Amplifier (PA). To lower the cost and to achieve full integration of a radio System-on-Chip (SoC), it is desirable to integrate the entire transceiver and the PA in a single CMOS chip. Since the PA often is the most power hungry component in the transmitter, it is important to minimize the power consumption to achieve a highly power-efficient and to extend battery life-time of portable devices. With a high efficiency, the heat dissipation of the devices is reduced, lowering the requirements and cost of the packaging of the IC.

While digital circuits benefit from the technology scaling, it is becoming harder to meet the stringent requirements on linearity, output power, bandwidth, and efficiency at lower supply voltages in traditional PA architectures. This has recently triggered extensive studies to investigate the impact of different efficiency enhancement and linearization techniques, like polar modulation and outphasing, in nanometer CMOS technologies.

This thesis addresses the potential of integrating linear and power-efficient PAs in nanometer CMOS technologies at GHz frequencies. In total eight amplifiers have been designed - two linear Class-A PAs, two switched Class-E PAs, and four Class-D PAs linearized in outphasing configurations. Based on the outphasing PAs, amplifier models and predistorters have been developed and evaluated for uplink (terminal) and downlink (base station) signals.

1.2 Organization of This Thesis

This thesis is organized into two parts:

- Part I - Background
- Part II - Papers

Part I provides the background for the concepts used in the papers.

Chapter 1 discusses the background of RF technology, history of integrated circuits, and future challenges in RF CMOS circuit design with emphasis on PA design.

Chapter 2 treats the operation of the transistor and intrinsic/extrinsic parasitics.

Chapter 3 introduces concepts and definitions used in PAs and describe the fundamental operation of the amplifier classes used in the papers.

Chapter 4 describes the matching techniques for PAs, specifically targeting the PAs in **Paper 1** and **Paper 2**.

Chapter 5 introduces two major linearization and efficiency enhancements techniques for switched amplifiers, i.e. polar modulation and outphasing. Class-D and outphasing RF PA implementations are presented in **Paper 5** - **Paper 9**. This chapter also provides an introduction to the predistortion methods presented in **Paper 8, Paper 10,** and **Paper 11**.

Chapter 6 discusses the major breakdown mechanisms of MOS devices from a circuit designer's perspective. This chapter serves as a background for the PA implementations in **Paper 3** - **Paper 6**.

Chapter 7 concludes the thesis and suggests further areas to be investigated.

In Part II the papers included in this thesis are presented in full.

1.3 Summary of Papers

The two linear PAs, presented in **Paper 1** and **Paper 2**, have been designed in a 65nm CMOS technology, targeting the 2.4GHz 802.11n WLAN standard. The PAs are two-stage amplifiers with LC-based and transformer-based input and interstage matching networks, respectively. For a 72.2Mbit/s 64-QAM 802.11n OFDM signal with PAPR of 9.1dB, both PAs fulfilled the toughest EVM requirement at average output power levels of +9.4dBm and +11.6dBm, respectively. The PAs were among the first PAs implemented in a 65nm CMOS technology.

Two Class-E PAs intended for DECT and Bluetooth, presented in **Paper 3** and **Paper 4**, have been designed in 130nm CMOS and operated at low 'digital' supply voltages. At 1.5V supply voltage and 1.85GHz, the DECT PA delivered +26.4dBm of output power with a drain efficiency (DE) and power-added efficiency (PAE) of 41% and 30%, respectively. At 1.0V supply voltage and 2.45GHz, the Bluetooth PA delivered +22.7dBm of output power with a DE and PAE of 48% and 36%,

respectively. The Bluetooth PA was based on thin oxide devices and the performance degradation over time for a high level of oxide stress was evaluated.

The four Class-D outphasing PAs have been designed in 65nm, 90nm, and 130nm CMOS technologies. The first outphasing design, presented in **Paper 5**, was based on a Class-D stage utilizing a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5V supply voltage in a 65nm CMOS technology without excessive device voltage stress. Two on-chip transformers combined the outputs of four Class-D stages. At 1.95GHz and a 5.5V supply voltage, the output power was +29.7dBm with a DE and PAE of 30.2% and 26.6%, respectively. The 3dB bandwidth was 1.6GHz (1.2-2.8GHz), representing the state-of-the-art bandwidth among published Class-D RF PAs. The PA was operated for 168 hours (1 week) without any performance degradation. The second design, presented in **Paper 6**, was based on the same Class-D stage as the first design, but combined eight amplifier stages by utilizing four on-chip transformers in a 130nm CMOS technology. At 1.85GHz and 5.5V supply voltage, the output power was +32dBm with a DE and PAE of 20.1% and 15.3%, respectively. The peak output power of +32dBm represents the state-of-the-art output power among published Class-D RF PAs. Both designs met the ACLR and modulation requirements without predistortion when amplifying uplink WCDMA and LTE (20MHz, 16-QAM) signals.

The third outphasing design was based on two low-power Class-D stages in 90nm CMOS featuring a harmonic suppression technique, presented in **Paper 7** and analysed in **Paper 9**, cancelling the third harmonic in the output spectrum which also improves drain efficiency. The proposed Class-D stage creates a voltage level of $V_{DD}/2$ from a single supply voltage to shape the drain voltage, uses only digital circuits and eliminates the short-circuit current present in inverter-based Class-D stages. A single Class-D stage delivered +5.1dBm at 1.2V supply voltage with a DE and PAE of 73% and 59%, respectively. Two Class-D stages were connected to a PCB transformer to create an outphasing amplifier, which was linear enough to amplify EDGE and WCDMA signals without the need for predistortion.

The fourth outphasing design, presented in **Paper 8**, is based on two Class-D amplifier stages connected to an on-chip transformer. The peak power of the amplifier was +10dBm and has been used in the development of a behavioral model structure and a model-based phase-only predistortion method suitable for Class-D outphasing RF amplifiers to compensate for both amplitude and phase mismatches. In measurements at 2GHz, the predistorter proved to be successful and improved the margin to the limits of the EDGE spectral mask at 400kHz and the WCDMA ACLR at 5MHz offset by 12.2-12.4dB. Based on a similar approach, presented in **Paper 10**, an amplifier model and predistortion method were developed and evaluated for the +32dBm Class-D PA design using a downlink WCDMA signal, where the ACLR at 5MHz was improved by 13.5dB. In **Paper 11**, a least-squares phase predistortion method was developed and evaluated for the +30dBm Class-D PA design using WCDMA and LTE uplink signals, where the ACLR was improved by approximately 10dB.

1.4 Brief History of RF Technology, Transistors, and Integrated Circuits

This chapter briefly enlightens the main milestones, which have made the electronics and wireless revolution possible. Furthermore, a comparison of semiconductor technologies and their current performance will be discussed along with their potential performance in the future.

The initial step towards solid-state devices was taken in 1874, as Ferdinand Braun discovered the metal-semiconductor contact, but it took another 51 years (1925) until the Field-Effect Transistor (FET) was patented by the physicist Julius Edgar Lilienfeld. In 1947, at Bell Labs in the US, a bipolar transistor device was developed by John Bardeen, Walter Brattain, and William Shockley, who received the Nobel Prize for their invention in 1956. The first integrated circuit (IC) was developed in 1958 by Jack Kilby, working at Texas Instruments, and consisted of a transistor, a capacitor, and resistors on a piece of germanium [2], [3]. Independent from Kilby, in the following year Robert Noyce [4] invented an IC with planar interconnections using photolithography and etching techniques still used today. However, it took another few years until Frank Wanlass in 1963, at Fairchild Semiconductor, developed the Complementary Metal-Oxide-Semiconductor (CMOS) process, which enabled the integration of both NMOS and PMOS transistors on the same chip. The first demonstration circuits were an inverter and a ring-oscillator [5].

In 1965 Gordon Moore, one of Intel's co-founders, predicted that the number of devices would double every twelve months [6]. The prediction was modified in 1975 [7], such that the future rate of increase in complexity would rather double every two years instead of every year and became known as Moore's law. In some people's opinion this prediction became a self-fulfilling prophecy that has emerged as one of the driving principles in the semiconductor industry, as engineers and researchers have been challenged to deliver annual breakthroughs to comply with the "law".

Since the '70s, the progress in several areas has made it feasible to keep up the pace in the electronics development to deliver more reliable, complex, and high-performance integrated circuits. A few years ago, Intel announced the first microprocessor with more than 2 billion transistors on the same die in a 65nm process [8], which would not have been possible without the tremendous scaling of CMOS transistors. However, with the transistor scaling, the issues with leakage become troublesome in traditional planar CMOS transistors, but have been reduced in new transistors like the three-dimensional FinFETs [9].

As mass-consumer products require a low manufacturing cost, silicon have been preferred as semiconductor material, as it has been possible to integrate more and more functionality along with a constant increase of performance. Without the scaling of both transistors and the cost of manufacturing of CMOS transistors, high-technology

products like portable computers and mobile phones would probably not have been mass-consumer markets [10].

The birth of wireless communication is dated to 1895, when Guglielmo Marconi managed to transmit a radio signal for more than a kilometer with a spark-gap transmitter, which was followed up by the first transatlantic radio transmission in 1902. The first analog mobile phone system in Scandinavia, Nordic Mobile Telephone System (NMT), appeared in the early 1980s. The NMT system was succeeded by the GSM system (Global System for Mobile communications; originally Groupe Spécial Mobile) in the '90s, which has been followed by several new standards for long and short distance communications. The evolution from the GSM system in the '90s with raw data rates of some kbps to today's high-speed WLAN and LTE standards with data rates of several 100Mbps has made it feasible to not only transmit voice data, but also transmit and receive pictures and movies. The significant increase in data rates has been viable through several enhancements, not only on the device level, but also through the development of more complex modulation schemes. They have evolved from Gaussian Minimum-Shift Keying (GMSK) modulation used in GSM to amplitude and phase modulations with large Peak-to-Average Power Ratio (PAPR) as in the WLAN and the LTE systems to support higher data rates, requiring highly linear transmitters. The radio architectures have evolved into architectures called transceivers, including both the transmitter and receiver sections. The digital baseband (DB) circuits, the local oscillator (LO), the mixer, the low-noise amplifiers (LNA) [11], the analog-to-digital converters (ADC), and the digital-to-analog converters (DAC) have successfully been implemented in CMOS and BiCMOS technologies [12]. However, one of the most challenging building blocks to efficiently integrate in CMOS is the PA. It has been predominantly designed in other technologies due to the higher efficiency [1], like GaAs HBTs [13] and Metal-Semiconductor Field Effect Transistors (MESFET) [14], Si BJT or SiGe HBT [15] for mobile handsets. One of the first CMOS RF PAs capable of delivering 1W of output power was presented in 1997 and implemented in a 0.8μm technology operating at 824-849MHz [16]. In the following year, a PA in a 0.35μm technology was presented and operated at 2GHz with an output power of 1W [17].

1.5 Future Possibilities and Challenges

Since the early '90s, silicon devices have had good enough performance for transceiver design [18]. By combining the low cost and integration capabilities of CMOS/BiCMOS, these technologies will make them the choice of RF transceivers with fully-integrated PAs, as long as RF and system design goals can be achieved. Figure 1.1 [19] shows an application spectrum and what semiconductors are likely to be used in certain frequency ranges. The application spectrum is currently predicted up to 100GHz, but both Indium Phosphide (InP) High Electron Mobility Transistor (HEMT) and Gallium Arsenide (GaAs) Metamorphic High Electron Mobility Transistor (MHEMT) have shown acceptable performance in the THz regime and can be expected to continuously dominate for extremely high frequency applications.

The main drivers of wireless communications systems today are cost, frequency bands, power consumption, functionality, size, volume of production, and standards. As wireless functionality has been integrated into more and more applications and entered mass-consumer markets, silicon-based technologies have continuously replaced the traditional III-V semiconductors when acceptable RF performance has been met. In PAs, the discussion will regard output power, linearity, efficiency, bandwidth, and integration. Currently, the market of WLAN transceivers is dominated by CMOS, where fully-integrated solutions, including the PA, have been presented [20]-[22]. Silicon-based technologies will be the choice for high volume and cost sensitive markets, but is not expected to be the choice when the key demands are very high gain, very high output power, and extremely low noise.

1.6 Semiconductor Materials

1.6.1 Scaling Trend of CMOS

As shown in Figure 1.1 a number of semiconductor materials exist, which are suitable for RF circuit design. Considering the scaling trend of MOS device in Table 1-1, we can foresee almost a reduction of two of the gate oxide thickness and a reduction of four of the gate length for the thin oxide devices in the next ten years [18], leading to potentially extreme f_T. To meet the high output power requirements in PAs a large supply voltage is desirable. Thus it is likely to use the thick oxide (I/O) devices or a combination of both devices in PA design. The trend for the thick oxide devices is not as extreme as for the thin oxide devices, as they are expected to have an oxide thickness of 2.6nm in ten years, comparable to existing thick oxide devices today.

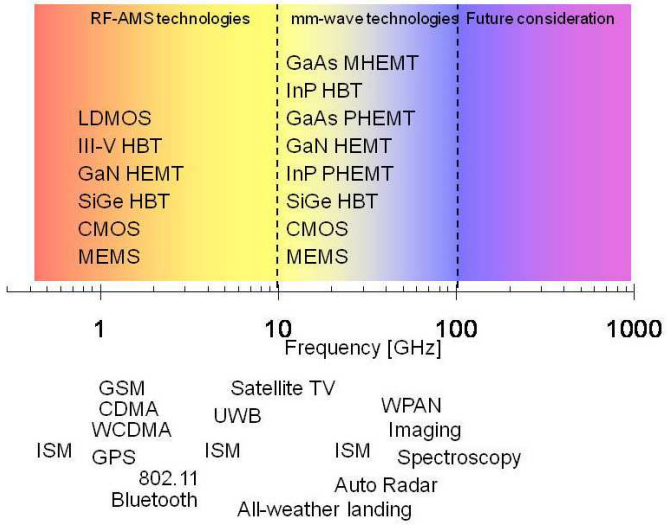

Figure 1.1: Application spectrum and semiconductors likely to be used today [19]

1.6.2 Comparison of Silicon and Other Semiconductors

As GaAs was one of the first semiconductors used in RF design and is still used in most terminal PAs, a short comparison of the specific properties of III-V compounds and silicon is given here. Table 1-2 shows the key characteristics of the basic materials of the most common MMIC technologies.

Considering the carrier velocity and mobility, they are higher for the electrons than for the holes. The difference between electrons and holes is much larger in III-V devices (e.g. GaAs) than for silicon devices [12], but the carrier velocity and mobility of electrons are lower for silicon devices. Due to the large difference in complementary III-V devices and the lower hole carrier velocity and mobility in GaAs, silicon technologies are better suited when it comes to high speed complementary logic. However, for high-speed circuits n-based GaAs devices are advantageous as long as no complementary devices are needed.

Another important parameter when considering complementary logic is the thermal conductivity as listed in Table 1-2. If the parameter is low, it implies issues to dissipate heating. Considering the two billion-transistor processor [8], a good thermal conductivity of the substrate material is necessary in order to make sure that the chip is not overheated. The comparable integration level in GaAs is typically limited to approximately 1000 transistors [12].

A parameter not beneficial in the silicon case is the substrate resistivity, which is

TABLE 1-1: PREDICTED CMOS SCALING BY ITRS [18]

Year of production	2010	2013	2016	2019	2022
Technology node [nm]	45	32	22	16	11
Thin oxide device					
- Nominal V_{DD} [V]	1.0	1.0	0.8	0.8	0.7
- t_{ox} [nm]	1.5	1.2	1.1	1.0	0.8
- Peak f_T [GHz]	280	400	550	730	870
- Peak f_{max} [GHz]	340	510	710	960	1160
- Ids [µA/µm]: min L	8	6	4	3	2
Thick oxide device					
- Nominal VDD [V]	1.8	1.8	1.8	1.5	1.5
- t_{ox} [nm]	3	3	3	2.6	2.6
- Peak f_T [GHz]	50	50	50	70	70
- Peak f_{max} [GHz]	90	90	90	120	120
Passive elements for PAs					
- Inductor Q [1GHz, 5nH]	14	18	18	18	18
- Capacitor Q [1GHz, 10pF]	>100	>100	>100	>100	>100
- RF cap. density [fF/µm^2]	5	7	10	10	12

TABLE 1-2: COMPARISON OF MMIC TECHNOLOGIES [12], [24]

	Silicon	SiC	InP	GaAs	GaN
Electron mobility at 300K [cm^2/Vs]	1500	700	5400	8500	1000-2000
Hole mobility at 300K [cm^2/Vs]	450	n.a	150	400	n.a.
Peak/saturated electron velocity [10^7 cm/s]	1.0/1.0	2.0/2.0	2.0/2.0	2.1/n.a	2.1/1.3
Peak/saturated hole velocity [10^7 cm/s]	1.0/1.0	n.a	n.a	n.a	n.a
Bandgap [eV]	1.1	3.26	1.35	1.42	3.49
Critical breakdown field [MV/cm]	0.3	3.0	0.5	0.4	3.0
Thermal conductivity [W/(cm K)]	1.5	4.5	0.7	0.5	>1.5
Substrate resistivity [Ωcm]	1-20	1-20	>1000	>1000	>1000
Number of transistors in IC	>1 billion	<200	<500	<1000	<50
Transistors	MOSFET, Bipolar, HBT, LDMOS	MESFET, HEMT	MESFET, HEMT, HBT	MESFET, HEMT, HBT	MESFET, HEMT
Costs prototype, mass fabrication	High, low	Very high, n.a.	High, very high	Low, high	Very high, n.a.

relatively low compared to the III-V semiconductors, and degrades the quality factor of integrated passives [23]. In Table 1-1 the predicted quality factors at 1GHz are given for on-chip inductors and capacitors, and as seen in the table, the inductors will continue to be a limiting factor in on-chip matching networks.

A common argument to use silicon and CMOS is cost, as previously discussed, and the relative speed performance between the electron and hole carrier based devices makes silicon a preferable choice for complementary logic. To further reduce the cost, the PA can be integrated with the CMOS transceiver. While BiCMOS solves the integration of the PA and with better RF performance of the bipolar devices compared to the MOSFET devices, it has an approximately 20% higher mask count and therefore also a higher price for the same technology node [1]. Typically, GaAs have lower masks costs since less processing steps are needed, but considering yield aspects and that CMOS processes can use larger wafers, make CMOS processes favorable in mass fabrication [12]. Thus, a major benefit of using CMOS PAs is the possibility of full integration.

The historical trend of CMOS scaling has enabled high-speed CMOS devices, as seen in Table 1-1, and the trend is expected to continue, but at the expense of lower supply voltages. The supply voltage and the associated RF output power of III-V technologies are larger [12], [15]. Therefore these technologies have dominated the market of terminal PAs [25]. For higher output power, SiC, GaN, and also LDMOS have superior performance over the other devices, due to the larger supply voltage and thermal conductivity, but these technologies a lower level of integration.

Even if high-performance CMOS-based GSM/GPRS [26], GSM/EDGE [27], and WCDMA [28] PAs, as well as fully-integrated WLAN CMOS transceivers with integrated front-ends [20]-[22] have been reported, further research is needed in the field of CMOS power amplifiers. Challenges are the limitations on the supply voltage, posing challenges to meet the requirements on linearity, output power, bandwidth, and efficiency.

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Chapter 2

CMOS Device Modeling and Parasitics

2.1 Introduction

While designing digital and analog integrated circuits, it is obviously important to understand the operation of the CMOS device. The DC operation of the device is covered in [1] and not discussed in this chapter. In analog circuit design small-signal models have found widespread use as it describes the linearized operation of the transistor at a specific DC bias point. In this chapter, the small-signal model presented is based on [1], taking into account intrinsic capacitances, and also describes what extrinsic components should be included. However, notice that in PAs, the transistors are operated under large voltage swing, making the devices cross the borders between different operating regions.

2.2 The MOS Device

2.2.1 Structure

In this section the operation of an n-channel MOS (NMOS) device is considered since the main operation principles of the p-channel MOS (PMOS) device are the same. Figure 2.1 shows a simplified structure of an NMOS consisting of two strongly-doped 'n' areas in the substrate called Source (S), and Drain (D). Between the substrate and the Gate (G), there is an insulating layer made of silicon dioxide (SiO_2). The device is located in a p-substrate and is called Bulk (B) or Body, typically connected to the lowest potential in the system in order to keep the source/drain junction diodes reverse-

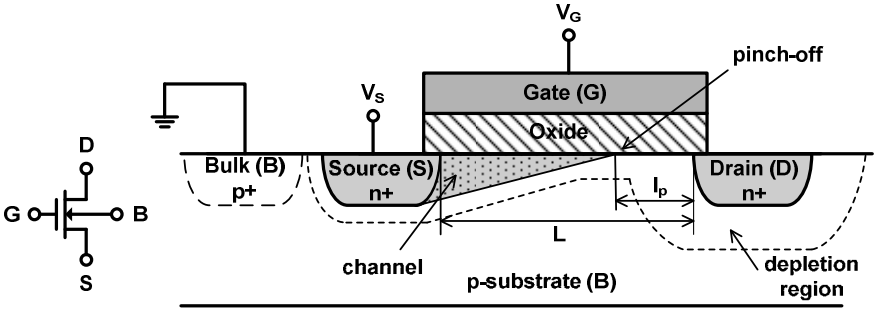

Figure 2.1: Schematic and cross section view of an NMOS transistor

biased. The region located between the drain and source, and beneath the gate, is called the channel, L, even though a channel between the drain and the source only exists under certain biasing conditions at the four terminals. Furthermore, the perpendicular extension of source and drain terminals, relatively the channel, is denoted as the width, W. The thickness of the layer separating the channel and the gate is called t_{ox} and has a physical thickness of ~1.0-5.0nm in submicron CMOS technologies.

2.2.2 Small-Signal Model

2.2.2.1 Intrinsic Model

The intrinsic small-signal model of a MOS transistor, Figure 2.2a, is obtained by independently applying small signal changes at the terminals of the device and identifying the changes in charges and currents in the device. By applying very small changes of the bias voltages at the device terminals, one at a time, and studying the effect on the drain current, an expression for the overall small change on the drain current can be expressed as in (2.1). Note that the intrinsic modeling does not include the extension of the drain and source, as well as the overlay capacitance between the gate, drain, and source shown in Figure 2.3.

In (2.1) the derivatives were replaced by a number of transconductances and the output conductance as defined in (2.2). g_m represents the gate transconductance, usually just called the transconductance. g_{mb} and g_{sd} represents the substrate transconductance and the source-drain conductance, respectively. Depending on how the transistor is biased, the transistor operates in different regions, and consequently the computation of the parameters depends on in what region the transistor operates. Assuming that the transistor operates in the saturation region, the transconductances and the source-drain conductance can be computed according to (2.3)-(2.5). Combining the transconductances and the intrinsic capacitances of the device a small-signal model can be drawn as in Figure 2.2a, where the output conductance is replaced by a resistor [1]. However, regarding the transconductances we can conclude that the substrate conductance, g_{mb}, only come into play as there is a difference in potential between the

$$i_{ds} \approx g_m v_{gs} + g_{mb} v_{bs} + g_{sd} v_{ds} \tag{2.1}$$

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{BS},V_{DS}}, \; g_{mb} = \left.\frac{\partial I_{DS}}{\partial V_{BS}}\right|_{V_{GS},V_{DS}}, \; g_{sd} = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS},V_{BS}} \tag{2.2}$$

$$g_m \approx \frac{2I_{DS}}{V_{GS} - V_{th}} \approx \sqrt{\frac{2\mu C_{ox} W I_{DS}}{L}} \tag{2.3}$$

$$g_{sd} \approx \frac{\mu C_{ox} W}{2L} (V_{GS} - V_{th})^2 \lambda \approx \lambda I_{DS} \tag{2.4}$$

$$g_{mb} \approx \frac{g_m \gamma}{2\sqrt{\phi_0 + V_{SB}}} \tag{2.5}$$

source and the substrate. With increasing V_{DS}, the output conductance degrades [1], leading to higher output impedance. However, further increasing V_{DS}, the depletion region associated with the drain extends further into the substrate and affects the source depletion region. Due to this interaction, the difference in potential between drain and source is lowered, resulting in lower threshold voltage. This effect is called drain-induced barrier lowering (DIBL) [2] and counteracts the impact on the output impedance, due to the channel-length modulation. Further increase of V_{DS} leads to impact ionization, lowering the output impedance [3].

These phenomenons are important in analog circuit design, as the output conductance is directly related to intrinsic voltage gain of the transistor. In a typical power amplifier circuit, the voltage swings are large (especially in the output stage), and therefore this phenomenon has an impact on the output impedance of the device. The same considerations apply to the intrinsic capacitors of the device and have to be taken into account in the transistor model in order to achieve reliable simulation results.

2.2.2.2 Extrinsic Components

Extrinsic capacitances exist between all terminals and model effects like overlay capacitances, C_{ov}, fringing capacitances, C_{fringe}, related to the extension of the drain and source, C_{bottom}, and sidewall capacitances, $C_{sidewall}$, as in Figure 2.3. The capacitances are added in parallel to the intrinsic small-signal model as in Figure 2.2b.

2.2.3 EM-Simulated Parasitics

While there are many transistor parameters and parasitics, which can be included into the transistor model, there are also parasitics that are not directly related to the MOS device itself. If the transistor is used in power amplifier applications, the current flowing through the transistors may reach several hundred milli-amperes or even amperes. Consequently, not only the transistor has to withstand the large currents, but also the interconnections around the device. As the current flows between the drain and source, one solution is to stack several metal layers on top of each other at the drain and

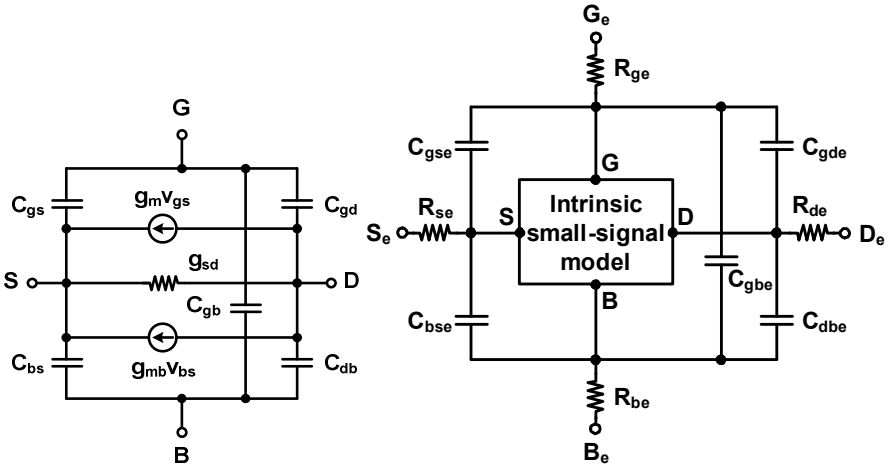

Figure 2.2: (a) Intrinsic small-signal model of MOS transistor [1]
(b) Small-signal model with extrinsic elements added

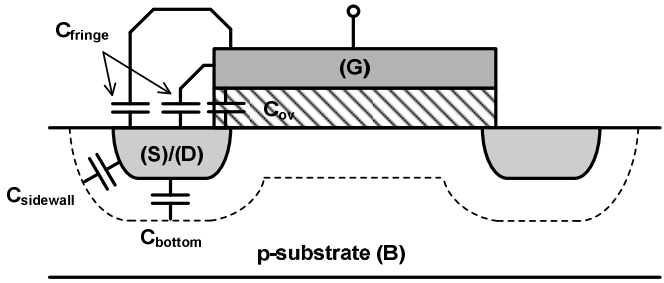

Figure 2.3: Extrinsic capacitances in the MOS transistor

source to meet the current density limitations of the metal traces. This would not only lead to a lower electromigration [4], but also to lower resistive voltage drop across the interconnections and introduce more capacitive coupling between gate, drain, and source as seen in Figure 2.4a. Since not all metal layers are included in the transistor model, the additional capacitances and dielectric losses need to be taken into account and added to the existing transistor model. The layout parasitics can typically be represented as either π or T equivalent circuits [5].

Considering the cascode amplifier stage in Figure 2.4b, used in **Paper 1** and **Paper 2,** it would have layout parasitics associated in a similar way as in Figure 2.4a. However, instead of inserting π or T equivalent circuits between every two nodes in the simulation model of the amplifier, the parasitic connections were approximated with series connections of capacitance and resistance between gate, drain, and source at the

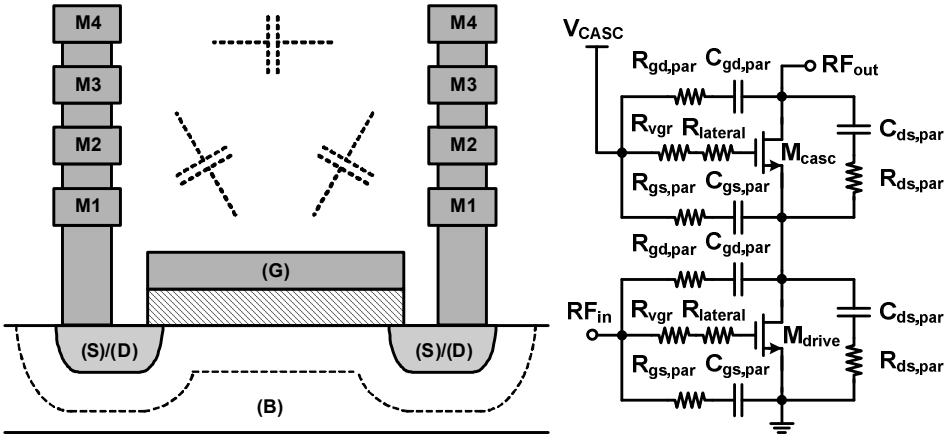

Figure 2.4: (a) Parasitic capacitances between gate, drain, and source (b) Model of cascode stage with parasitics, incl. the vertical gate resistance

frequency of operation. It means that two components, one resistive and one reactive component were used instead of six. The values of the parasitic components were estimated through electromagnetic simulations and depending on how the signals were applied between a pair of terminals, two different extraction formulas, based on the impedance (Z) parameters, were used. Equation (2.6) was used for differential signals and (2.7) for computation of the input impedance at port 1 [6]. In a similar way the signal traces included the series inductance and series resistance, but also the parasitic capacitance to the substrate [7]. To improve the model of the cascode stage, parasitic inductances should be included as well [8]. Considering the accuracy of the estimated parasitic impedances, the single-ended impedance has a very good accuracy since only one terminal is excited with a signal. In the differential case, when varying the amplitudes of the differential signals and the phases, the error in the simulated current between the approximate network and a π or T equivalent circuit representation is kept below 20%. Moreover, the parasitic impedance is placed in parallel with the small input impedance of the large devices, and the error introduced by photo-lithography effects can be as large as 20% in RC extraction from design to fabrication [9].

2.2.4 Gate Resistance

To achieve a "complete" model of the device and to accurately predict power gain, input and output impedance, and phase delay between the current and the gate voltage, a number of resistive components should also be included at the drain, source, gate, and substrate. The resistive components at the drain and source typically depend on the resistivity in the regions and how the regions are contacted. Substrate resistance can be

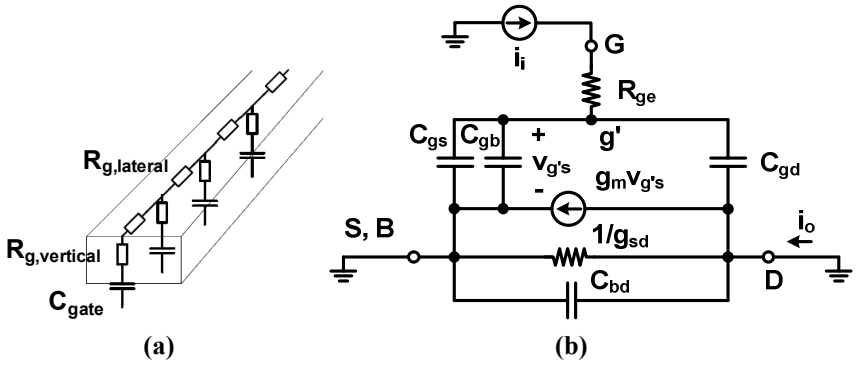

Figure 2.5: (a) Vertical gate resistance
(b) Circuit to estimate ω_T

$$Z_{dd} = Z_{11} - Z_{12} - Z_{21} + Z_{22} \tag{2.6}$$

$$Z_{se} = Z_{11} - Z_{12}Z_{21}/Z_{22} \tag{2.7}$$

$$R_{g,lateral} = \alpha \frac{W}{L} R_{sq} \tag{2.8}$$

$$R_{g,vertical} = \frac{r_C}{WL} \tag{2.9}$$

$$C_g = C_{gs} + C_{gb} + C_{gd} \tag{2.10}$$

$$f_T = \frac{1}{2\pi} \frac{i_o}{i_i}\bigg|_{vds=0} = \frac{1}{2\pi} \frac{g_m}{C_g} = \frac{1}{2\pi} \frac{g_m}{C_{gs} + C_{gb} + C_{gd}} \tag{2.11}$$

$$\omega_{\max} \approx \frac{\omega_T}{\sqrt{4R_{ge}^{'}\left(g_{sd} + \omega_T C_{gd}\right)}}; R_{se} << R_{ge} \tag{2.12}$$

modeled by a single resistor up to frequencies of 10GHz [10] and as a parallel RC circuit for higher frequencies [11].

The gate has been made predominantly by silicided poly-silicon with a resistance up to 10Ω/□ [12], R_{sq}, and the lateral gate resistance, $R_{g,lateral}$, can be computed according to (2.8). If the gate is connected at one side α becomes 1/3, and if connected at both sides, α can be reduced to 1/12 [12]. Another gate resistance component, which has not always been taken into account in the transistor models, is a contact resistance [13] between the silicide and the poly-silicon in the MOS transistor gate, denoted as $R_{g,vertical}$ in Figure 2.5a. Assuming the contact resistivity is r_C, the additional contact resistance can be computed according to (2.9). Since the additional contact resistance may be as large as the resistance in (2.8) and is expected [13] to be the dominant factor for technologies with smaller gate lengths than 0.35μm, it is important to consider the

resistive contribution to accurately predict transistor performance at higher frequencies. Both resistive contributions are usually represented by a single resistor computed as the sum of (2.8) and (2.9) [14], as in the simulation model of the amplifiers in **Paper 1** and **Paper 2**. The gate resistance can be significantly reduced by using silicided gates, multiple contacts, and splitting the device into several parallel devices. The silicided poly-silicon gate has been replaced by metal gates in some recently developed 45nm CMOS processes [15]-[17]. The high-k metal-gate makes it possible to fabricate gates with physically thicker oxides, but still with improved electrical properties. In [17] a reduction in gate leakage of up to >25X has been demonstrated. The improvement in reduced gate leakage is very important, as the leakage power has grown to become a large portion of the total power consumption [18], [19], in microprocessors [20].

Two common figure-of-merits (FoM) of the transistors are the transition frequency, f_T, and maximum oscillation frequency, $f_{\max}$. The transition frequency is defined as the frequency at which the small-signal current gain equals unity as a DC source is connected between drain and a grounded source [1] (while neglecting the small current through C_{gd}). An estimation of f_T (2.11) can be made by using the simplified circuit in Figure 2.5b. The total capacitance seen at the gate to ground is defined as C_g (2.10), including both intrinsic and extrinsic capacitances. $f_{\max}$ is also called unity power gain frequency. When computing $f_{\max}$ it is assumed that the transistor is conjugately matched at the input and output to compute the unilateral power gain [1], [5], and is defined at the frequency as the power gain drops to unity. The relationship [1] between f_T and $f_{\max}$ is then found in (2.12). From (2.12), we can conclude the dependency of the effective gate resistance, R'_{ge}, and how it limits the usefulness of the device. However, as concluded in [10], $f_{\max}$ is a small-signal parameter, presuming a conjugate-matched output, which is not likely the case in the output stage of a power amplifier [21], as discussed in Chapter 4, and can roughly be used in the context of the driver stages where the signal levels are smaller. The gate resistance can be reduced by several layout techniques as previously described. Impedance matching techniques are treated in Chapter 4.

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Chapter 3

The RF Power Amplifier

3.1 Introduction

This chapter provides the fundamental knowledge and aspects of RF power amplifier design. Several performance metrics, like output power, drain efficiency, and power-added efficiency are introduced, which are then followed by a description of PA classes and how they operate. The PA classes covered are the linear amplifiers, like class A, AB, B, (and C), and the switched mode classes D, E, and F.

3.2 Power Amplifier Fundamentals

A typical transmitter includes a Digital Baseband (DB), Digital-to-Analog Converters (DAC), Mixers (X), two phase-shifted LO signals, followed by the PA, and a matching network, including filters. Transmitter configurations are two-step transmitters [1], direct-modulation transmitters, and direct-conversion transmitters as

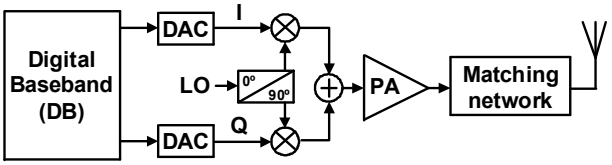

Figure 3.1: Block diagram of a direct-conversion transmitter

$$x_{BB}(t) = I(t) + jQ(t) \tag{3.1}$$

$$x(t) = r(t)\cos(\omega_c t + \varphi(t)) \tag{3.2}$$

$$r(t) = \sqrt{I^2(t) + Q^2(t)} \tag{3.3}$$

$$\varphi(t) = \arctan\left(Q(t)/I(t)\right) \tag{3.4}$$

shown in Figure 3.1. The signal to be transmitted, $x_{BB}(t)$ in (3.1), is initially processed by the DB and split into the in-phase, I, and quadrature, Q, channels, which are upconverted to the RF carrier by the quadrature modulator, usually implemented by two mixers and two LO signals with a phase difference of 90 degrees. Since the power of the output signal, $x(t)$ in (3.2), from the quadrature modulator usually is too low for radio transmission, the signal is amplified by the PA before being fed to the antenna. Ideally, the output of the PA is just an amplified version of the quadrature modulator output. A detailed description of transceiver design will not be covered by this chapter, but has been discussed by a number of authors [2], [3].

3.2.1 Output Power

To define Output Power, P_{out}, we consider the basic circuit in Figure 3.2, which shows a PA with two driver stages connected to a load, R_L. The output power is defined as the active power delivered to the load, i.e. the antenna, at the fundamental frequency. Assuming that the load is purely resistive at the frequencies of interest we can represent the load as a resistor, R_L. The load impedance can be transformed to have both a higher and lower value with an imaginary part by the matching network. This matter will be discussed in the next chapter, but for the moment we assume that the load can be represented by a resistor.

Based on the circuit in Figure 3.2, we can define the instantaneous output power at

$$P_{out,inst} = v_{OUT}(t) i_{OUT}(t) \tag{3.5}$$

$$P_{out,av} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} P_{out,inst}(t)\, dt \tag{3.6}$$

$$P_{out}(A) = \frac{A^2}{2R_L} = \frac{V_{out,\max}^2}{2R_L} = \frac{V_{out,rms}^2}{R_L} \tag{3.7}$$

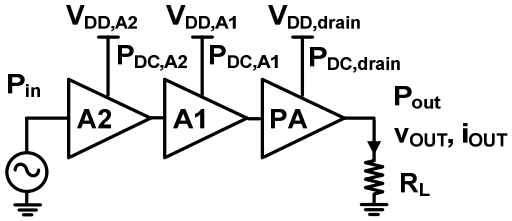

Figure 3.2: Power amplifier (PA) with two driver stages, A1 and A2, connected to an antenna

any particular moment as $P_{out,inst}$ (3.5) with an average power of $P_{out,av}$ (3.6). The PA also generates power at frequencies other than at the intended one, but these are neglected at the moment. We define $V_{out,\max}$ as the sinusoidal amplitude, A, of the signal at the fundamental frequency and $V_{out,rms}$ as the corresponding rms value. The power generated at the fundamental frequency is called P_{out} (3.7).

3.2.2 Gain and Efficiency

Considering the circuit in Figure 3.2 again, we introduce the input RF power, P_{in}, driving the whole amplifier chain. By combining the input power, P_{in}, and the output power, P_{out}, the Gain, G, can be defined as the ratio of the output power and the input power, usually expressed in dB (3.8).

$$G_{dB} = 10 \log_{10}\left(\frac{P_{out}}{P_{in}}\right) \tag{3.8}$$

An important measure of the PA is the efficiency as it directly affects the talk-time in handheld devices and has an impact on the electricity bill in base stations. One of the efficiency measures is the Drain Efficiency, DE (3.9), which is defined as the ratio between the average output power at the fundamental, P_{out}, and the DC power consumption, $P_{DC,drain}$, of the very last stage in the amplifier chain of the PA. It should be noted that the Drain Efficiency is denoted Collector Efficiency for bipolar devices. When considering the input power, P_{in}, needed to drive the amplifier chain, we can define another efficiency metric called Power-Added Efficiency [4], PAE (3.10), as the input power subtracted from the output power, which is then divided by the total DC power consumption, $P_{DC,tot}$. The total DC power consumption includes the DC power consumed at the drain and the total DC power consumed by the amplifier stages A1 and A2.

$$DE = \frac{P_{out}}{P_{DC,drain}} \tag{3.9}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,tot}} = \frac{P_{out} - P_{in}}{P_{DC,drain} + \sum_{k=1}^{n} P_{DC,Ak}} \tag{3.10}$$

3.2.3 Peak Output Power, Crest Factor, and Peak to Average Power Ratio

With the development of modulation schemes utilizing both amplitude and phase modulation we need to introduce new measures called Crest Factor, CF, and Peak-to-Average Power Ratio, $PAPR$. For a signal with envelope profile $A(t)$, the average output power, $P_{out,av}$, and Peak Envelope Power, PEP, can be defined as in (3.11) and (3.12) [5], [6], respectively.

$$P_{out,av} = \frac{A_{rms}^2}{2R_L} \tag{3.11}$$

$$PEP = \frac{A_{\max}^2}{2R_L} \tag{3.12}$$

The *CF* is defined as the ratio of the peak voltage to the rms value (3.13), while *PAPR* refers to the ratio of the average output power and the peak output power (3.14) and is usually expressed in dB.

$$CF = \frac{A_{\max}}{A_{rms}} \tag{3.13}$$

$$PAPR_{dB} = 10\log_{10}\left(CF^2\right) = 20\log_{10}\left(\frac{A_{\max}}{A_{rms}}\right) \tag{3.14}$$

Signals with high *PAPR* are especially troublesome to transmit from an efficiency point of view as the signal requires significant signal headroom such that the peak envelope amplitudes are transmitted without significant distortion. Therefore, in conventional linear amplifiers there is significant power dissipation as the transistor output stage is biased to handle the large power peaks, even though the output power for most of time is relatively low compared to the peak power level.

3.2.4 Power Amplifier Drain Efficiency for Modulated Signals

The efficiency concept can be further explored for modulated signals [4]. In (3.7) we have defined the efficiency for a signal with constant amplitude, A, and therefore the instantaneous drain efficiency can be calculated for a specific output voltage amplitude. Assuming that the amplitude changes over time, $A(t)$, means that the drain efficiency, n_d, will also vary over time as in (3.15). The average efficiency over time can be calculated as in (3.16). The average efficiency can also be based on the envelope probability density function, $p(A)$, which does not require any information about the time behavior of the envelope signal (3.17) [4], [7].

Consider an ideal Class-A amplifier [8], [9], as in section 3.3.1, with an output RF voltage amplitude of A, with a constant DC power, $P_{DC,drain}$, consumed by the output stage. The drain efficiency can be computed for a given ratio of the output amplitude and the supply voltage, V_{DD}, as in (3.18). The curve has a quadratic behavior dependent on the output amplitude with a maximum efficiency of 50%. Furthermore, considering a

$$n_d\left(A(t)\right) = \frac{P_{out}\left(A(t)\right)}{P_{DC,drain}\left(A(t)\right)} \tag{3.15}$$

$$n_d = \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{T/2} n_d\left(A(t)\right)dt \tag{3.16}$$

$$n_d = \int_0^{A_{\max}} n_d(A)p(A)\,dA \tag{3.17}$$

transmission of a signal with a *PAPR* of 10dB, the average efficiency would drop to 5% in the ideal case [10]. This simple example shows the need for power efficient PAs transmitting signal with high demands on linearity and high efficiency during power back-off.

$$DE(A) = \frac{P_{out}(A)}{P_{DC,drain}(A)} = \frac{A^2/2R_L}{V_{DD}I_{DC}} = \frac{A^2/2R_L}{V_{DD}(V_{DD}/R_L)} = \frac{1}{2}\left(\frac{A}{V_{DD}}\right)^2 \tag{3.18}$$

3.2.5 Linearity

Several wireless communication standards employ modulation schemes with non-constant envelopes, which need to be amplified by PAs capable of linear amplification. To quantify the level of linearity, or rather, the level of non-linearity, several measures exist. Initially, a number of fundamental non-linearity concepts [1] will be introduced, followed by a number of application-related non-linearity measures like Spectral Mask, Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR).

3.2.5.1 Gain Compression, Harmonics, and Intermodulation

We return to Figure 3.2, but now to investigate the gain characteristics of the PA. The analysis will be limited to memoryless systems, which can be approximated by a polynomial (3.19). The analysis will be made up to the fifth order, neglecting higher order nonlinearities. Let the input signal, $x(t)$, be transmitted by a differential PA, such that the output signal of the PA, $y(t)$, now contains additional components including the input signal to the power of three and five. Recall that even order nonlinearities cancel if the amplifier is fully differential.

Assuming that a sinusoidal signal (3.20) is applied to the non-linear system, the resultant signal (3.21) now not only contains power at the fundamental frequency component. We can see that the first term, the in-band component is distorted by the nonlinearities of the PA, but the phase component is unchanged. This explains why nonlinear PAs can be used for constant amplitude modulation [11]. If the input amplitude (or power) is increased even further, the gain of a PA begins to decline. When the gain is 1dB less than the small-signal gain, we define this compression point

$$y(t) \approx \alpha_1 x(t) + \alpha_3 x^3(t) + \alpha_5 x^5(t) \ldots \tag{3.19}$$

$$x(t) = A\cos\left(\omega t + \phi(t)\right) \tag{3.20}$$

$$\begin{aligned} y(t) &= \left[\alpha_1 A(t) + \frac{3}{4}\alpha_3 A^3(t) + \frac{5}{8}\alpha_5 A^5(t)\right]\cos\left(\omega t + \varphi(t)\right) + \\ &= \left[\frac{1}{4}\alpha_3 A^3(t) + \frac{5}{16}\alpha_5 A^5(t)\right]\cos\left(3\omega t + 3\varphi(t)\right) + \\ &= \left[\frac{1}{16}\alpha_5 A^5(t)\right]\cos\left(5\omega t + 5\varphi(t)\right) \end{aligned} \tag{3.21}$$

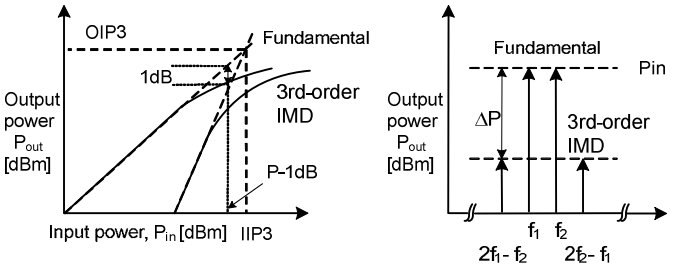

Figure 3.3: (a) Gain compression curve
(b) Intermodulation spectrum of two-tone test

as the 1dB Compression Point (P-1dB) as in Figure 3.3a. When the output power does not further increase due to a higher input power, the PA is said to be saturated and it cannot deliver more power regardless of the input power to PA.

Another source of distortion in amplifiers is intermodulation, which appears when two closely located frequencies are transmitted through the PA at the same time (3.22). This effect can also be evaluated by the polynomial in (3.19), but for simplicity only first, second, and third order nonlinearities are included (3.23). For an input signal (3.22) the generated intermodulation products are found in (3.24) [1], as well as some DC terms and harmonics not shown. Of particular interest are the frequencies generated at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$, as these components show up very closely to the frequency

$$x(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t) \tag{3.22}$$

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)... \tag{3.23}$$

$$\begin{aligned}
&\omega_1 \pm \omega_2 : \alpha_2 A_1 A_2\cos((\omega_1+\omega_2)t) + \alpha_2 A_1 A_2\cos((\omega_1-\omega_2)t)\\
&2\omega_1 \pm \omega_2 : \frac{3\alpha_3 A_1^2 A_2}{4}\cos((2\omega_1+\omega_2)t) + \frac{3\alpha_3 A_1^2 A_2}{4}\cos((2\omega_1-\omega_2)t)\\
&2\omega_2 \pm \omega_1 : \frac{3\alpha_3 A_2^2 A_1}{4}\cos((2\omega_2+\omega_1)t) + \frac{3\alpha_3 A_2^2 A_1}{4}\cos((2\omega_2-\omega_1)t)\\
&\omega_1,\omega_2 : \left(\alpha_1 A_1 + \frac{3\alpha_3 A_1^3}{4} + \frac{3\alpha_3 A_1 A_2^2}{2}\right)\cos(\omega_1 t) +\\
&\qquad \left(\alpha_1 A_2 + \frac{3\alpha_3 A_2^3}{4} + \frac{3\alpha_3 A_2 A_1^2}{2}\right)\cos(\omega_2 t)
\end{aligned} \tag{3.24}$$

$$IIP3\big|_{dBm} = \frac{\Delta P\big|_{dB}}{2} + P_{in}\big|_{dBm} \tag{3.25}$$

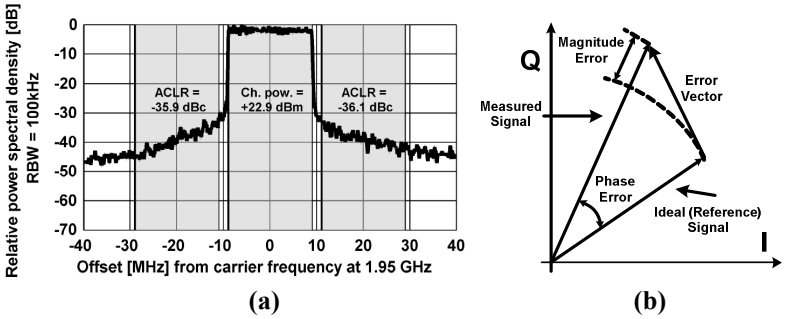

Figure 3.4: (a) ACLR measurement for an LTE signal [13]
(b) Vector definitions in EVM

components of the signal, ω_1 and ω_2, and increase proportionally to A^3 ($A_1 = A_2$). When increasing the input amplitude even further, the lines of the fundamental term and the third-order terms ($2\omega_1$-ω_2 and $2\omega_2$-ω_1) will eventually cross each other as illustrated in Figure 3.3a and Figure 3.3b. This point is called third-order intercept, IP3. Graphically the Input-refered IP3, *IIP3*, can be calculated according to (3.25).

Other measures to describe the nonlinearities of the PA are amplitude modulation to amplitude modulation (AM-AM) and amplitude modulation to phase modulation (AM-PM) distortion. AM-AM is defined as the relationship between the amplitude of the input signal and the output signal, similarly to the relationship between output power and input power to the PA and the gain compression of the system. AM-PM represents the distortion process, as the increase of input power causes an additional phase shift on the output signal [9].

3.2.5.2 Spectral Mask and Adjacent Channel Power Ratio

As the radio transmission has a frequency bandwidth (channel) allocated around the carrier, where the transmission may be conducted, any power falling outside these frequencies will disturb neighboring channels and the transmission therein. The boundaries specifying between what frequencies the transmission should occur is usually specified with a spectral mask, where the power around the carrier is specified in decibel to carrier (dBc) or in exact power levels given in dBm in a specified bandwidth at certain frequency offsets. The Adjacent Channel Power Ratio (ACPR) is defined [12] as the ratio of power in a bandwidth away from the main signal to the power in a bandwidth within the main signal, where the bandwidths and acceptable ratios are determined by the standard being employed. Figure 3.4a shows the measured spectrum and measured Adjacent Channel Leakage Ratio (ACLR), the technical term used in the 3GPP standards but is the same as ACPR, for a 20MHz LTE signal applied to the Class-D outphasing PA in [13].

3.2.5.3 Error Vector Magnitude

Another signal quality measure is the Error Vector Magnitude (EVM), which is computed on I and Q data (or amplitude and phase). In the I versus Q plane (Figure 3.4b) each location encodes a specific data symbol, which has a certain number of bits depending on the complexity of the modulation scheme used. At any point in time the magnitude and phase of the signal can be measured and mapped towards an ideal reference signal based on transmitted data stream, clock timing, filtering parameters, etc. [14], [15]. The difference between the measured signal and the ideal reference signal creates the error vector and is generally defined as the rms value of the error vector over time [16]. Sometimes the peak value is also used. The EVM measure provides the direct measure of the signal quality and the transmitter and receiver/demodulation accuracy, and the result captures several signal impairments like AM-AM distortion, AM-PM distortion, phase noise, and random noise.

3.3 Power Amplifier Classes

As the foundation of efficiency and linearity has been covered in the previous sections, the fundamental PA classes will here be described with the trade-offs between linearity and power efficiency emphasized. Initially, the linear amplifiers are described. These amplifiers use the device as a voltage-controlled current-source, where the input voltage controls the output current. Section 3.3.4-3.3.6 describes the switching amplifiers, utilizing the transistor as a switch to modulate the signal.

3.3.1 Class-A

The Class-A PA, Figure 3.5a, is the most “classical” PA with a transistor biased so that it never turns off. The conduction angle is defined as the portion of the input signal during which the transistor conducts, meaning that a Class-A PA has a conduction angle of 360 degrees. The typical drain voltage and drain current waveforms are shown in Figure 3.5b, which assume a highly linear relationship between the signal drain current and the sinusoidal input voltage, v_{in} (3.26). Due to the non-abrupt drain current, the linearity of the amplifier is certainly high, but suffers from low efficiency due to the same reason. In reality the relationship is not that perfectly linear [9], but the ideal model is used since it is very tractable from an analytical perspective.

The derivation of the efficiency has been done by several authors [8], [9], [17], and a short review will be given here. The basic circuit considered is shown in Figure 3.5a, with a transistor biased at a certain voltage level with a certain bias current, I_{DC}, and the signal component of the drain current, i_{rf} [8]. The drain current can be expressed as in (3.27). The output voltage is the signal current multiplied with the load resistance (3.28). Due to the large supply inductor, only DC current flows through the inductor, and consequently, the signal current is just the signal component of the drain current. The drain voltage is the sum of the signal voltage and DC voltage and as the inductor is short-circuited for DC frequencies, the DC drain voltage is the supply voltage.

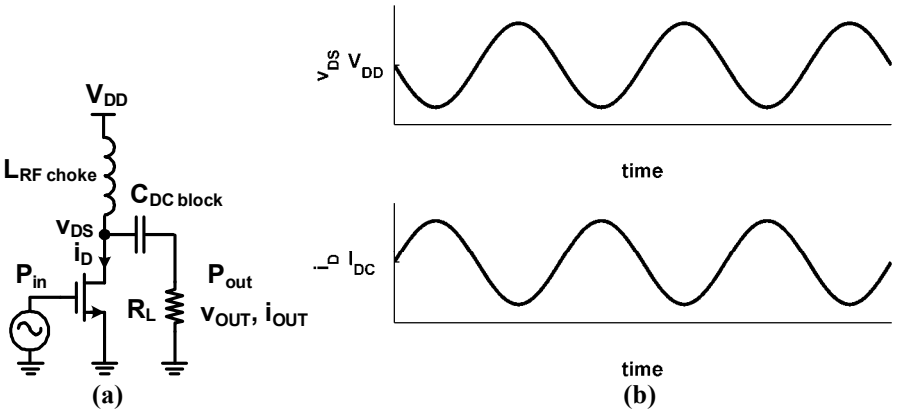

Figure 3.5: (a) Generic single-stage Class-A/B/C power amplifier (b) Drain voltage and current waveforms in an ideal Class-A

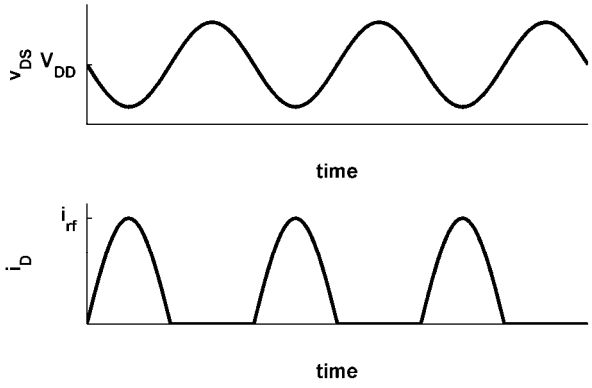

Figure 3.6: Drain voltage and current waveforms in an ideal Class-B

It means that the peak drain voltage is $2V_{DD}$ with a peak drain current of $2V_{DD}/R$. From the assumptions mentioned above, the output power can now be stated according to (3.29) and the dissipated DC power (3.30) – which is independent of the output RF signal. Eventually, the maximum efficiency of 50% can be computed according to (3.31). Assuming a lower output swing (3.32) with amplitude A, the efficiency drops significantly and more power is dissipated across the device. One should also note that the efficiency of 50% in Class-A PAs is the absolute maximum, assuming the full voltage swing is attainable, no losses in matching network, and no amplitude modulation is present.

In **Paper 1** and **Paper 2**, two linear CMOS PAs are designed in a 65nm CMOS technology to operate in the 2.4-2.5GHz band. The PAs utilize thick oxide (5.2nm) transistors, but used different input and interstage matching networks. A 72.2Mbit/s, 64-

QAM 802.11n OFDM signal was applied to both PAs. The measured average output power levels of the two designs were +9.4dBm and +11.6dBm, respectively, while having an EVM of 3.8%.

3.3.2 Class-B and AB

The 'sister' of Class-A PA is Class-B, which has the same type of basic circuitry as Class-A, but is biased differently. In Class-B the bias voltage is adjusted such that the transistor only conducts current half of the RF cycle, i.e. at the threshold voltage, such that the conduction angle is 180 degrees. With the intermittent operation of the transistor, we can expect more distortion on the output voltage and a high-Q tank is needed at the output to get a fairly sinusoidal signal back. Similarly for the Class-B amplifier as for the Class-A amplifier, we can analyze the drain voltage and current waveforms in Figure 3.6, where it is assumed that the drain current is sinusoidal for the part of the period when the transistor is conducting, which is a quite crude approximation as the change is abrupt. The fundamental component of the drain current can be computed according to (3.33), based on Fourier coefficients. As the maximum output voltage is V_{DD}, the maximum value of the signal component of the drain current is $2V_{DD}/R_L$, equal to Class-A amplifiers. As the maximum output voltage is the same as for Class-A amplifiers, the maximum output power is equal to (3.29). The DC supply

$$i_D \propto k\left(v_{in} - V_{th}\right) \tag{3.26}$$

$$i_D = I_{DC} + i_{rf}\sin\omega t \tag{3.27}$$

$$v_{out} = -i_{rf} R \sin\omega t \tag{3.28}$$

$$P_{out} = P_{rf} = \frac{i_{rf}^2 R_L}{2} = \frac{V_{DD}^2}{2R_L} \tag{3.29}$$

$$P_{dc} = V_{DD} I_{DC} = V_{DD} i_{rf} \tag{3.30}$$

$$DE = \frac{P_{rf}}{P_{DC}} = \frac{i_{rf}^2\left(R_L/2\right)}{i_{rf} V_{DD}} = \frac{i_{rf} R_L}{2V_{DD}} = \frac{V_{DD}}{2V_{DD}} = \frac{1}{2} \tag{3.31}$$

$$DE(A) = \frac{P_{out}(A)}{P_{DC,drain}(A)} = \frac{A^2/2R_L}{V_{DD} I_{DC}} = \frac{A^2/2R_L}{V_{DD}\left(V_{DD}/R_L\right)} = \frac{1}{2}\left(\frac{A}{V_{DD}}\right)^2 \tag{3.32}$$

$$i_{D,fund} = \frac{2}{T}\int_0^{T/2} i_{rf}\sin\left(\omega t\right)\sin\left(\omega t\right) dt = \frac{i_{rf}}{2} \tag{3.33}$$

$$\overline{i_D} = \frac{1}{T}\int_0^{T/2} \frac{2V_{DD}}{R_L}\sin\left(\omega t\right) dt = \frac{2V_{DD}}{\pi R_L} \tag{3.34}$$

$$DE = \frac{P_{out,\max}}{P_{DC}} = \frac{V_{DD}^2/2R_L}{2V_{DD}^2/\pi R_L} = \frac{\pi}{4} \approx 0.785 \tag{3.35}$$

current can also be found through Fourier coefficients (3.34). The maximum *DE* of the Class-B amplifier is found as in (3.35).

It is clear that Class-B amplifiers achieve a significantly higher efficiency than Class-A amplifiers, but at the expense of more distortion. Therefore many practical PAs are a mix of Class-A and Class-B with a conduction angle between 180 and 360 degrees to get an acceptable trade-off between linearity and efficiency.

3.3.3 Class-C

Reducing the conduction angle even further, compared to Class-B, leads to a situation when the transistor is more turned off than turned on. Mathematical derivations show an efficiency of 100% as the conduction angle is reduced to 0. But since the gain and output power goes to zero simultaneously, this type of amplifier is not very frequently used in RF applications at GHz frequencies, even though successful implementations at 900MHz do exist [18]. The operation of the transistor can be done in a similar way when it is operated in Class-C mode and a full derivation is given in [8] and [17].

3.3.4 Class-D

The amplifier circuits so far have focused on providing an acceptable trade-off between linearity and efficiency. By taking advantage of the complementary MOS devices, a highly efficient amplifier can be designed by using inverters as in Figure 3.7a. Instead of using the transistors as current-sources, the transistors are now used as switches instead such that the output voltage toggles between two voltage extremes, i.e. ground and V_{DD}. The basic principle behind the high efficiency can be found by looking at its IV characteristics in Figure 3.8, and conclude that the voltage across the transistors is zero as the current flows through the switches (transistors). Similarly, when there is voltage across the switch, the current is zero. However, one drawback with this amplifier class is that there is no linear relationship in amplitude between the input signal and the output signal, but by modulating the duty cycle of the driving signal, the amplitude of the output voltage amplitude can be controlled.

Assuming a driving signal with 50% duty cycle, the output signal would have the same duty cycle. Analyzing the Fourier coefficients of the square output voltage waveform reveals that power will be lost in the harmonics (3.36). A filter, i.e. an inductor and capacitor in series with the load is needed, ideally providing a short at the fundamental frequency and infinite impedance at all other frequencies. This means that all power is forced to the fundamental frequency. Further utilizing (3.36), we can compute the fundamental component of the output voltage across the load resistance and the current through the load, eventually leading to the output power at the fundamental (3.37). The average (DC) current from V_{DD} is the average of the current passing through the PMOS, a half wave sinusoidal signal with amplitude $i_{out,1}$ (3.38). With all relationships established, the *DE* is computed to be 100% according to (3.39). However, such an ideal and lossless filter characteristics does not exist. Therefore, it might be more tractable to consider the power available in the fundamental component, compared to the total power in the square wave as in (3.40). It is clear that a significant

amount of power is wasted in the harmonics, unless we provide an ideal filter, which is not realistic in real implementations. This combined with the charging and discharging of the drain capacitance and the short-circuit power, discussed below, makes the efficiency lower than 100%.

Analyzing the amplifier output stage, the inverter in Figure 3.7b, the power dissipation can be divided into dynamic power and static power. The dynamic power origins from switching power and short-circuit power, while the static power is related to leakage current as previously discussed in Chapter 2. The switching power relates to the charging and discharging of the capacitive load, which includes the drain capacitance of the inverter and may dissipate significant power when large transistors are used. Assuming the input voltage is zero, the PMOS will turn on and start to charge the total load capacitance, C_D, requiring energy of $C_D V_{DD}^2$. When the input toggles to V_{DD}, the PMOS is turned off, and the NMOS is turned on. The charge stored on C_D is then dumped to ground through the NMOS, while no additional energy is pulled from V_{DD}. The switching power can be expressed as in (3.41), where f is the clock frequency of the input signal, and α is the switching activity ratio, which determines how

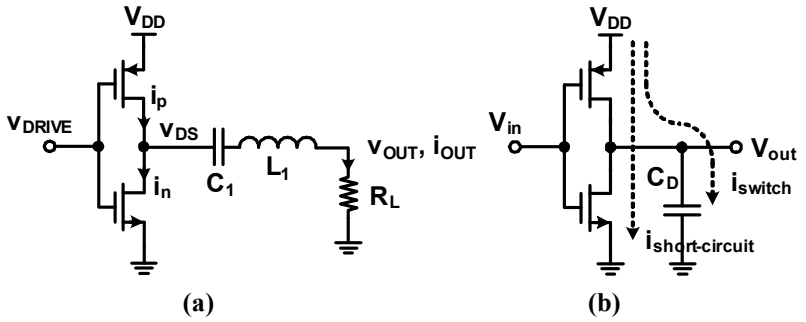

Figure 3.7: (a) Class-D amplifier
(b) Schematic of CMOS inverter including dynamic currents

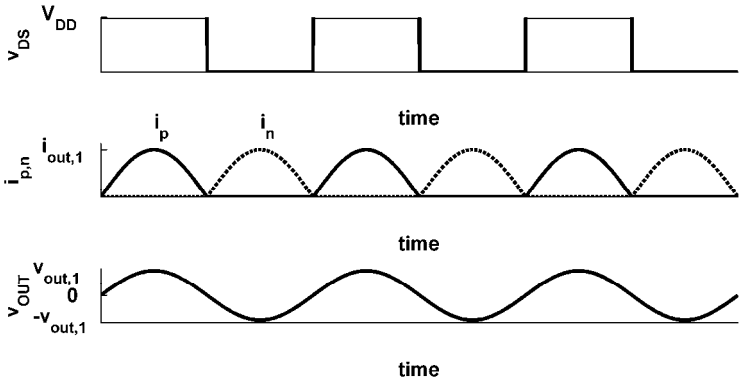

Figure 3.8: Class-D amplifier waveforms

$$b_n = \frac{V_{DD}}{n\pi}\left[1-(-1)^n\right] = v_{out,n} \tag{3.36}$$

$$P_{out,1} = v_{out,1} i_{out,1}/2 = \left(\frac{2V_{DD}}{\pi}\right)\left(\frac{2V_{DD}}{\pi R_L}\right)\Big/2 = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{3.37}$$

$$I_{DC} = \frac{i_{out,1}}{\pi} = \frac{2V_{DD}}{\pi^2 R_L} \tag{3.38}$$

$$DE = \frac{P_{out,1}}{P_{DC}} = \frac{2V_{DD}^2/\pi^2 R_L}{V_{DD} I_{DC}} = \frac{2V_{DD}^2/\pi^2 R_L}{V_{DD}\left(2V_{DD}/\pi^2 R_L\right)} = 1 \tag{3.39}$$

$$\frac{b_1^2}{\sum_{n=1}^{\infty} b_n^2} = \frac{\left(\frac{2V_{DD}}{\pi}\right)^2}{\sum_{n=1}^{\infty}\left(\frac{V_{DD}}{n\pi}\left[1-(-1)^n\right]\right)^2} \approx 0.814 \tag{3.40}$$

$$P_{switching} = \alpha\, f\, C_D\, V_{DD}^2 \tag{3.41}$$

$$P_{short-circuit} = \frac{\beta}{12}\left(V_{DD} - 2V_{th}\right)^3 f\tau \tag{3.42}$$

$$v_{DS}\left(t = t_1\right) = 0 \tag{3.43}$$

$$\left.\frac{\partial v_{DS}}{\partial t}\right|_{t=t_1} = 0 \tag{3.44}$$

frequently the output switches from low-to-high per clock cycle [19]. However, the input signal has a finite rise-time, which for a short moment leads to that both the NMOS and PMOS transistors are turned on causing to a direct path between V_{DD} and ground. The power dissipated, due to the direct path, is denoted as short-circuit power and can be calculated according to (3.42) [20], where β is the gain factor of the transistors and τ is the input rise/fall time. The short-circuit power can be kept below 10% of the switching component in a properly designed circuit [21]. Due to the significant scaling of the MOS transistors, the leakage power has become a major contributor to the overall power dissipation [22]-[24] and comes from various sources like subthreshold leakage current, gate leakage currents, and reversed junction leakage currents [25].

3.3.5 Class-E

The Class-D amplifier showed the potential over "classical" linear amplifiers to achieve higher efficiencies up 100%, by operating the transistors as switches. However, it was also clear that Class-D suffered from loss mechanisms, due to the parasitic capacitance of the output stage. The Class-E topology, Figure 3.9, solves these issues by

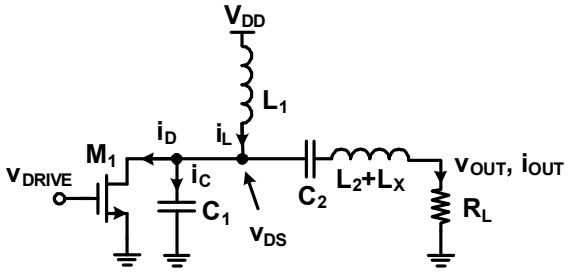

Figure 3.9: Class-E amplifier

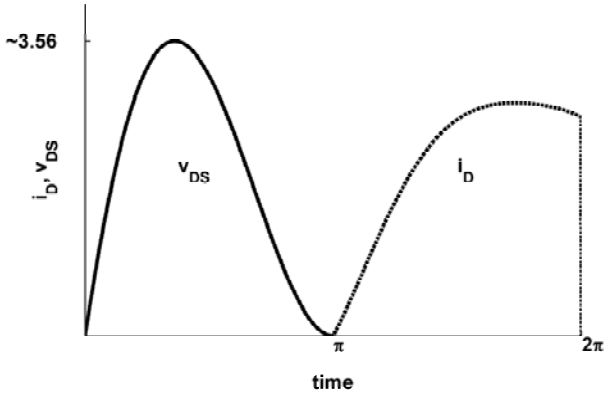

Figure 3.10: Normalized drain voltage and current waveforms in an ideal Class-E [28]

shaping the drain voltage with a reactive load impedance in order to decrease the drain voltage to zero as the switch turns on, t_1 in (3.43) [26], to minimize the charges stored on the drain capacitance, which will be discharged to ground. Thus, the power consumption due to charging/discharging the drain capacitance, as in Class-D, is eliminated. Another condition (3.44), concerns the slope of the drain voltage, which should be zero at turn-on in order to allow for component mismatches without causing significant power loss [27], [28]. The conditions on the drain voltage result in ideal efficiency of 100%, eliminating the losses associated with charging the drain capacitance as in Class-D, reduction of switching losses, and good tolerance of component variation [29]. Ideally, the resulting drain voltage and current waveforms would look like the waveforms in Figure 3.10.

A major drawback in Class-E implementations is the very high peak drain voltage, which are troublesome in nanometer CMOS technologies with thin gate oxides and occurs while the device is turned off, posing reliability issues. To ensure reliable operating at RF, a secure approach is to make sure that safe operation is met even for DC conditions, which translate into never exceeding the critical oxide field of ~1V/nm

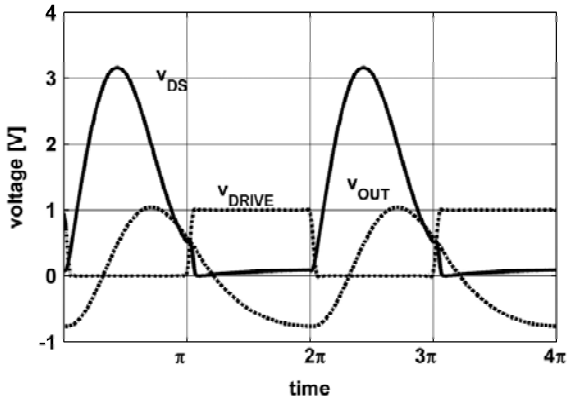

Figure 3.11: Simulation results of drain voltage, v_{DS}, driver signal, v_{DRIVE}, and output voltage, v_{OUT}

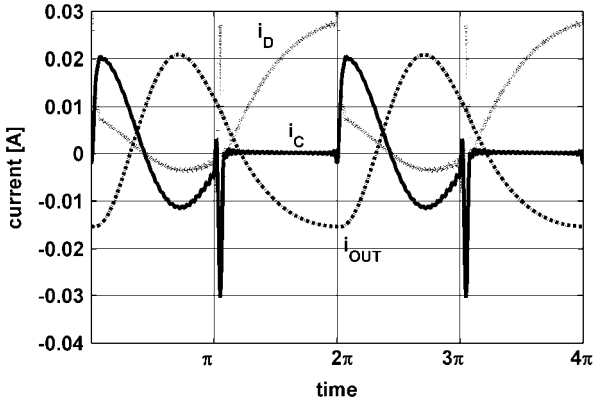

Figure 3.12: Simulation current waveforms: drain current, i_D, current through shunt capacitance, i_C, output current, i_{OUT}

gate oxide at the drain of the transistor [30]. However, as discussed in Chapter 6, this is a quite safe approach not necessarily exploiting the maximum capability of the device at RF operation.

At first sight, the conditions in (3.43) and (3.44) may seem to be trivial to solve analytically, but soon one realize the complex dependencies between all circuit components. A number of authors [17], [31], [32], have already derived the design equations so this will not be repeated here. Instead a more intuitive approach of the idealized operation of the Class-E amplifier in Figure 3.9 is described. Similarly to Class-D amplifiers, Class-E amplifiers do not inherently feature linear amplification,

but is a good candidate to be used in polar-modulated amplifiers [33], [34], pulse-width modulation [35], and outphasing with combiners with isolation.

The device, M_1 is assumed to be driven by a square wave with 50% duty cycle [31]. The RF choke, L_1, is assumed to only carry DC current. The Q of the series-tuned circuit, L_2 and C_2, is high enough so the output can be assumed to be a sinusoidal signal, and the reactance $j\omega L_X$ applies only at the fundamental. For all other frequencies the reactance is assumed to be infinitely large. The switching operation of the device is lossless, except for any charges stored in C_1, which are discharged to ground at device turn on and the transition of the device is assumed to be instantaneous. Moreover, the device is assumed to have zero on-resistance and an infinitely large off-resistance.

When the switch is closed, the DC current through inductor L_1, flows through the switch. As the switch opens, the sinusoidal output current subtracted from the DC current will charge the capacitor C_1 and the parasitic capacitors of the device for a non-negligible amount of the period time. Simultaneously, the voltage across the device increases and eventually rises to a peak voltage level of ~$3.56V_{DD}$ [28] and the charges stored in the capacitors are dumped to the load. The utilization of the capacitor C_1 is a major benefit of Class-E compared to Class-D, where the parasitic drain capacitance always discharges to ground. Beneficially, this capacitor can be made up entirely by the parasitic drain capacitance of the device, eliminating the need for an additional capacitor, while also reducing the on-resistance for more output power.

A simulation of a Class-E amplifier in a 130nm CMOS process is performed with the parameters and performance as given in Table 3-1. All components are ideal, except for the transistor, and its on-resistance. The voltage and current waveforms are plotted in Figure 3.11 and Figure 3.12, respectively, and are defined as in Figure 3.9. The current through inductor L_1 is not perfect DC, but is always positive, and therefore it is not plotted. Considering the voltage waveforms, the peak of the v_{DS} do not reach $3.56V_{DD}$, and as the transistor turns on by v_{DRIVE}, v_{DS} is not zero. Due to the nonzero v_{DS}, we can clearly see from the current waveforms how the charges stored on C_1 are dumped to ground through the transistor at $t_1 = \pi$. As long as the transistor is turned on (between π and 2π), the current, i_D, through the transistor increases. At transistor turn off, the current through the capacitor increases rapidly, due to the current, i_L, through L_1 and the reversed output current, i_{OUT}. After some time, the output current becomes positive and shortly the capacitors are discharged. At the time the currents through the capacitors are zero, v_{DS} reaches its highest peak.

As previously stated, the dependencies between the component values are not trivial from an analytical point of view. In [27] the effect of various component values is

TABLE 3-1: SIMULATION PARAMETERS

Width [μm]	C_1 [pF]	C_2 [pF]	L_1 [nH]	L_2 [nH]	L_x [nH]	R_L [Ω]	V_{DD} [V]	DE [%]	P_{out} [dBm]	f [GHz]
230	0.431	6	35.5	1.05	5.27	50	1	88	9	2

$$DE \approx 1/\left(1 + 1.4 r_{on} / R_L\right) \tag{3.45}$$

$$P_{out} = 0.577 \frac{V_{DD}^2}{R_L} \tag{3.46}$$

$$Z_{load} = Z_0 \frac{R_L + jZ_0 \tan\left(2\pi l/\lambda\right)}{Z_0 + jR_L \tan\left(2\pi l/\lambda\right)} \tag{3.47}$$

elaborated and it is found that variations of the shunt susceptance ($B = \omega C$) still results in high efficiency over a large range of values. However, for small values C_1 will experience both high and low voltage peaks. For large values, the rise-time of v_{DS} will be long, and thus, the peak voltage is reduced.

One important component is obviously the transistor itself and intuitively we can pull more current trough a larger device when it is turned on, than for a smaller device, since the on-resistance is smaller. As derived in [36], the drain efficiency, *DE*, could be approximated by (3.45). Due to the continuous scaling of the transistors it becomes increasingly challenging to design Class-E amplifiers, due to the high voltage peaks generated. It forces the design to use a smaller supply voltage, but at the same time the load resistance decreases rapidly (3.46).

In **Paper 3** two Class-E CMOS PAs in 130nm CMOS are operated at low supply voltages. The first PA is intended for DECT, while the second is intended for Bluetooth. Both are using inverters as driver stages. At 1.5V supply voltage, the DECT PA delivered +26.4dBm of output power with a DE and PAE of 41% and 30%, respectively. The Bluetooth PA delivered an output power of +22.7dBm at 1.0V with a DE, and PAE of 48% and 36%, respectively. The Bluetooth PA was based on thin oxide devices and the performance degradation over time for a high level of oxide stress was evaluated in **Paper 4.**

3.3.6 Class-F

Similar to Class-E, the Class-F amplifier employs drain voltage waveform shaping to achieve a high efficiency. Figure 3.13 shows a Class-F amplifier with a transmission line at the drain [8] and a high-*Q* tank in parallel with the load resistor. The length of the transmission line is λ/4 at the fundamental frequency and the *Q* is considered high enough to short circuit all frequencies outside the desired bandwidth. Due to the transmission line, the load impedance seen at the drain can be computed through (3.47).

From (3.47), we can conclude that the load impedance, Z_{load}, seen at the drain is Z_0^2/R_L at the fundamental. At all even harmonics, the impedance seen is R_L, which is zero at all harmonics. Moreover, at all odd harmonics, the transmission line shows an infinitely large impedance as the equivalent R_L is equal to zero. Furthermore, assuming a square drive voltage with 50% duty cycle only containing odd harmonics, consequently the square wave would also appear at the drain and the load current is purely sinusoidal at the fundamental frequency. Figure 3.14 also reveals that the Class-F amplifier ideally is capable of providing 100% efficiency (recall the Class-D

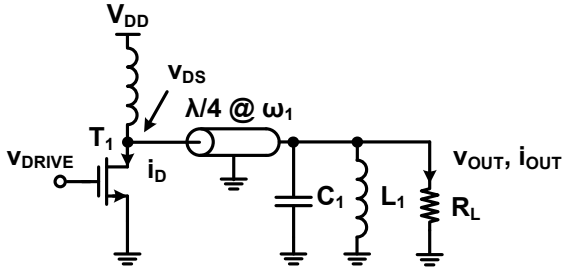

Figure 3.13: Class-F amplifier

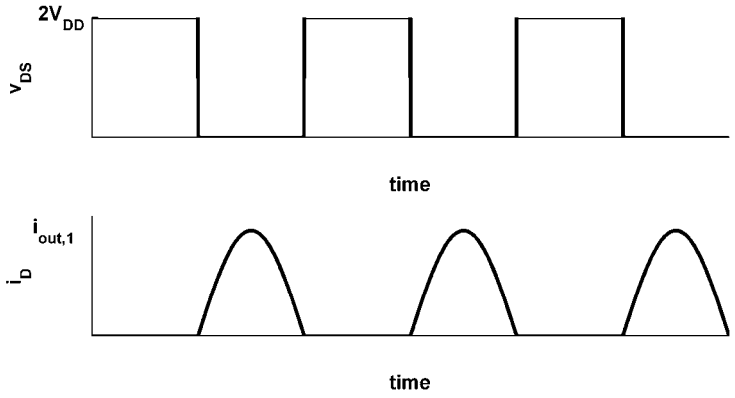

Figure 3.14: Class-F amplifier waveforms

waveforms) and from the basic topology presented, different circuit combinations with the same characteristics have been presented as inverse Class-F and Class-E/F amplifiers [37].

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Chapter 4

Matching Techniques

4.1 Introduction

In the previous chapter it was assumed that the load connected to the PA could represent any desired value. However, assuming an antenna impedance of 50Ω, it has to be transformed to a different (usually lower) value to achieve a sufficiently high output power. Assuming an available voltage swing of 1V would only generate as little as 10mW across a 50Ω load, which is not sufficient for many applications. This simple example demonstrates the necessity of using load impedance matching networks. In the previous chapter a great portion of the material dealt with the efficiency of the different classes, but no energy was spent on investigating the load itself. In this chapter we will see how the design of the matching network has a significant impact on the overall efficiency of the matching network and consequently also on the total efficiency of the transmitter. Moreover, the input and interstage matching in a multi-stage amplifier is discussed.

4.2 Conjugate and Power Match

Figure 4.1a shows a current generator which could represent the output current generator of a transistor with internal output impedance comprised by a parallel resistor (assuming the drain capacitance has been tuned out) [1]. Considering the maximum power theorem [2], we would choose a load resistor, R_L, equivalent to the real part of the generator's impedance [3] to achieve maximum output power. However, 50% of the

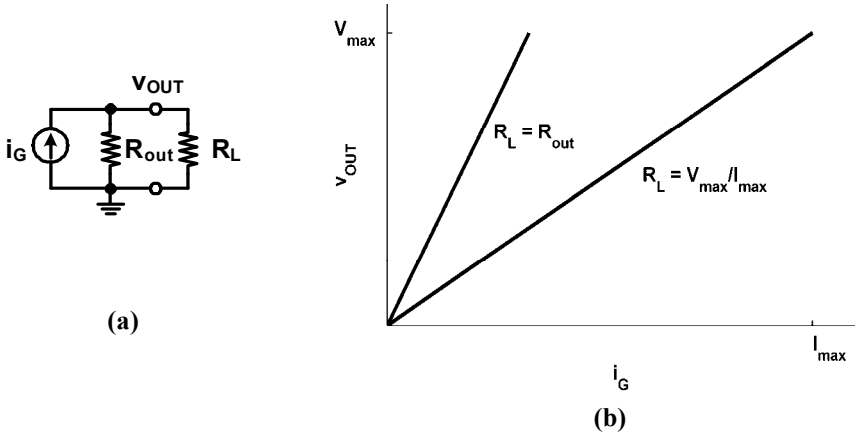

Figure 4.1: (a) Current generator with output resistance, R_{out}, and load, R_L, (b) Conjugate match, $R_L = R_{out}$, and loadline match, $R_L = V_{max}/I_{max}$; $R_{out} >> R_L$

power would be lost in the internal resistance, making this choice of load resistor unattractive [1], [4]. Moreover, the maximum power theorem does not pay attention to physical limitations such as maximum allowed drain voltage before gate oxide breakdown or the current capability of the device if the current generator would represent the output current generator of a transistor. As seen in Figure 4.1b, ideally the maximum allowed drain voltage is quickly reached as the load resistor, R_L, is chosen equivalent to the internal output resistance, R_{out}, while the current is significantly lower than the physical maximum I_{max}. Choosing another load resistor to an approximate value of V_{max}/I_{max} as in (4.1) (assuming $R_{out} >> R_L$) indicates a more suitable load resistor to utilize the transistor in a better way.

$$\frac{R_{out}R_L}{R_{out}+R_L} = \frac{V_{max}}{I_{max}} \tag{4.1}$$

Consequently, another choice of load resistor than R_{out}, leads to higher output power, higher efficiency, and improved utilization of the transistor. It means that the maximum power theorem is not useful when designing the output matching in a PA as we are matching for optimum power characteristics to squeeze out the maximum power available from the transistor.

4.3 Load-pull

The effect of using a loadline match instead of conjugate is also evident in Figure 4.2a, where a Class-A amplifier has been matched in two different ways. The solid line represents the power characteristics in a conjugate match for low input drive levels, while the dashed line represents a power match (loadline). The figure shows that the

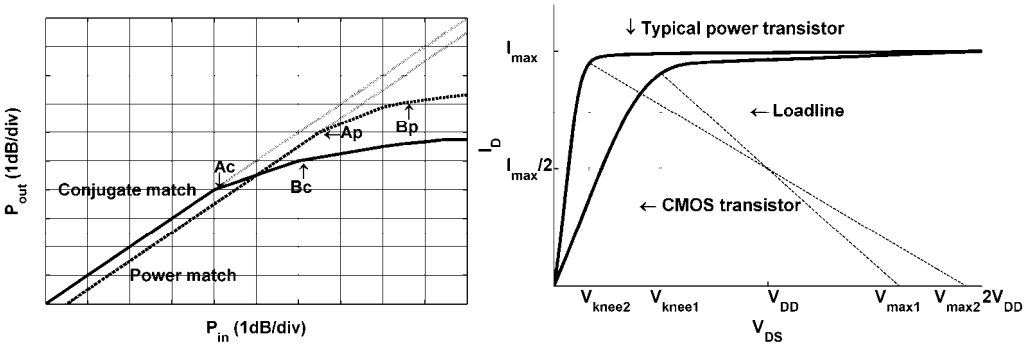

Figure 4.2: (a) Compression characteristics for conjugate (c) and power match (p) with markers at maximum linear points (Ac, Ap), and at the 1dB compression points (Bc, Bp) (b) Loadline for a typical power transistor and a CMOS transistor in Class-A biasing

conjugate matched amplifier has a higher gain at low input drive levels than the power matched amplifier. However, the conjugate matched amplifier has a lower 1dB compression point and lower saturated output power than the power matched amplifier. In linear amplifier design, the 1dB compression point is a key parameter to evaluate the linear performance of a PA and a slightly lower gain is usually acceptable if a higher 1dB compression point can be high achieved. Typically, a power-matched amplifier can push the compression parameters to 1-2dB higher levels [1], [3].

Obviously, the IV characteristic of the transistors in Figure 4.1 was very ideal. A more realistic characteristic is shown in Figure 4.2b for an MOS device, where also the characteristic of a typical power device (e.g. GaAs) is drawn. The loadline concept works better for the power device, than for the MOS device which has a relatively soft transition from the linear to the saturation region. For the power transistor, a suitable choice of load resistor would be as in (4.2) [3].

$$R_L = \frac{(V_{\max} - V_{knee})}{I_{\max}} \tag{4.2}$$

The characteristic is very profound in deep-submicron CMOS technologies, where the voltage knee may be as high as 50% of the supply voltage [3], when the same knee voltage in typical power transistors is about 10-15% of the supply voltage. Due to the high voltage knee, the loadline concept may not be very useful when determining the optimum load resistor for the MOS device as the capability of the transistor would not be fully utilized. A better approach is to use load-pull technique to determine the optimum load impedance. In the load-pull technique, a calibrated load capable of covering the Smith chart is varied at the output of the PA. In the absence of calibrated mechanical tuners [1] or in an early design stage, software packages can perform virtual load-pull simulations with an accuracy mainly determined by factors like transistor

models, layout parasitics, and packaging. The output from load-pull simulations is power contours representing the boundaries between specific output power levels. Typically, the maximum power level, the 1dB, and 2dB power contours are of interest, as the compression points are directly related to the linearity in an amplifier providing linear amplification. From the power contours, an optimum or suitable load impedance can be chosen in order to allow for component mismatches. Due to the large-signal variations in PAs and the varying output impedance, the motive for using load-pull simulations is further strengthened.

4.4 Matching Network Design

Until now, the load impedance has been considered to be purely resistive, but when using load-pull simulations, the load impedance may contain imaginary parts. It was also clear from the introduction of this chapter that the resistive portion of the load impedance maybe significantly smaller than 50Ω in order to achieve sufficient output power. To provide a down-transformation of the 50Ω load impedance, an L-match network is often used.

4.4.1 L-Match

In the L-match the load, R_L, is transformed to a lower value to get the desired output power. The L-match consists of a series inductor, L, and a parallel combination of a capacitor, C, with the load impedance, R_L, as in Figure 4.3. In an ideal matching network without any losses, all the power will be dissipated in the load, R_L. Real components have finite Q and results in losses, lowering the output power and reducing the efficiency of the impedance transformation.

The Power Enhancement Ratio, E, in (4.3) is defined as the ratio of the RF power delivered to the load with a transformation network in place to the power delivered to the load for the same sinusoidal input voltage source when it drives the load directly and

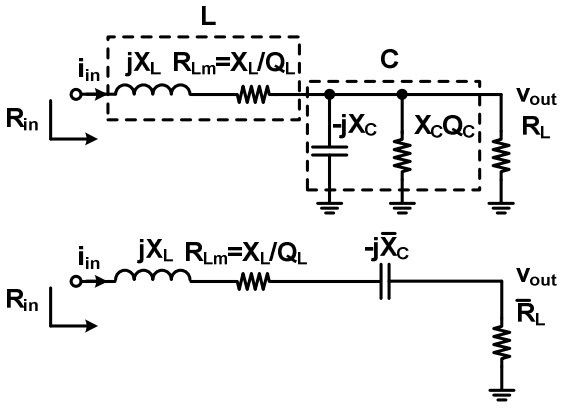

Figure 4.3: L-matching network

$$E = \frac{P_{out}\ with\ matching\ network}{P_{out}\ without\ matching\ network} = (r)(IL) = (r)(IL_1 IL_2) \tag{4.3}$$

$$IL = \frac{Power\ received\ by\ load}{Power\ received\ by\ load + Power\ loss} \tag{4.4}$$

$$Q_m = \left(\frac{R_L \,//\, X_C Q_C}{X_C}\right) = \frac{R_L Q_C}{R_L + X_C Q_C} \tag{4.5}$$

$$\overline{X_C} = X_C\left(\frac{Q_m^2}{1+Q_m^2}\right) \tag{4.6}$$

$$\overline{R_L} = \left(\frac{1}{1+Q_m^2}\right)\left(\frac{X_C R_L Q_C}{R_L + X_C Q_C}\right) = \frac{X_C Q_m}{1+Q_m^2} \tag{4.7}$$

$$IL_1 = \frac{i_{in}^2 \overline{R_L}}{i_{in}^2\left(\overline{R_L} + \frac{X_L}{Q_L}\right)} = \frac{1}{1+\frac{Q_m}{Q_L}} \tag{4.8}$$

$$IL_2 = \frac{V_o^2/(2R_L)}{V_o^2/(2(R_L \,//\, X_C Q_C))} = \frac{X_C Q_C}{X_C Q_C + R_L} = 1 - \frac{Q_m}{Q_C} \tag{4.9}$$

$$E = \frac{V_{\max}^2/(2R_{in})IL}{V_{\max}^2/(2R_L)} = \frac{R_L}{R_{in}} IL = (r)(IL_1 IL_2) \tag{4.10}$$

$$R_{in} = \overline{R_L} + \frac{X_L}{Q_L} = \frac{R_L}{1+Q_m^2}\left(1-\frac{Q_m}{Q_C}\right)\left(1+\frac{Q_m}{Q_L}\right) \tag{4.11}$$

$$IL = IL_1 IL_2 = \frac{1 - Q_m/Q_C}{1 + Q_m/Q_L} \tag{4.12}$$

$$E = \frac{1+Q_m^2}{\left(1+\frac{Q_m}{Q_L}\right)^2} \tag{4.13}$$

can be computed for any matching network [5]. This performance measure not only includes the ideal impedance transformation ratio, $r = R_L/R_{in}$, but also accounts for the Insertion Losses, *IL* (4.4) [6], in the passive components, which has significant impact when implementing the passive components on-chip in silicon technologies. The Insertion Loss, *IL* in (4.3), can be divided into two parts, one part for the inductor loss, IL_1 (4.8), and one part for the capacitor, IL_2 (4.9).

The parallel combination of the capacitor, *C*, and the load impedance, R_L, creates a virtual series resistance, $\overline{R_L}$, and negative reactance, $-j\overline{X_C}$, with a quality factor of Q_m (4.5). In order to compensate for the negative reactance, an inductor is located in series

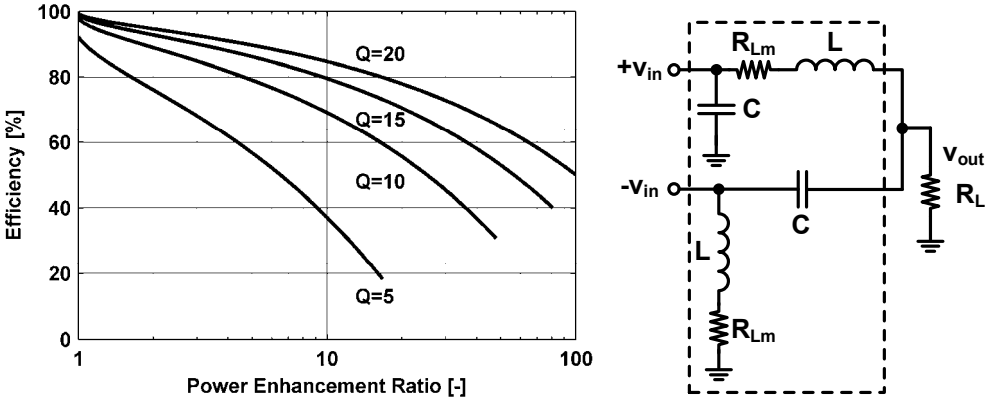

Figure 4.4: (a) Efficiency [9] of L-matching network for inductor quality factor, $Q_L = Q$, and Power Enhancement Ratio, E (b) Lattice-type balun inside the box with dashed lines driven by a differential signal, $+v_{in}$ and $-v_{in}$

with the parallel combination as seen in Figure 4.3. Denote the maximum voltage across the load to V_{max}, while not using any matching network at all. Taking into account the two separate insertion losses, IL_1 and IL_2 in (4.8) and (4.9), the E can be rewritten (4.10) as a function of the ideal impedance transformation and the insertion losses and eventually as a function of quality factors. The E for a lossless matching network, $Q_L = Q_C = \infty$, is then just $1+Q_m^2$ or the ratio of the load resistance, R_L, and the ideal input resistance, R_{in}. Consequently, if the quality factors and the desired output power are known, the efficiency can be calculated by solving the equations in a given order. Determining the E from (4.3) and assuming that Q_L is known, leads to the computation of Q_m in (4.13), so that X_C can be computed from (4.5). Assuming the inductor will cancel the reactance created by the capacitor, X_L must be equal to X_C in (4.6). Moreover, the input resistance, R_{in}, and the total insertion loss, IL, can be evaluated from (4.11) and (4.12) [7].

When implementing the matching networks on PCBs, the quality factors can be quite high. When on-chip matching networks are used, they tend to be quite lossy, due to the low Q of the inductors. To evaluate the performance of on-chip L-match network, the derived equations can be used. As the Q of the on-chip capacitors are much higher than the inductors, Q_C is assumed to be infinitely large in the equations (4.5)-(4.13). In Figure 4.4a, the desired E is swept for a variety of inductor quality factors, $Q_L = Q$, where the impact of a low inductor quality factor is apparent. This is especially troublesome in low-voltage CMOS technologies, where significant enhancement ratios are needed to achieve sufficient output power. One should also recall that the efficiency plotted only corresponds to the L-matching network itself - losses associated with the

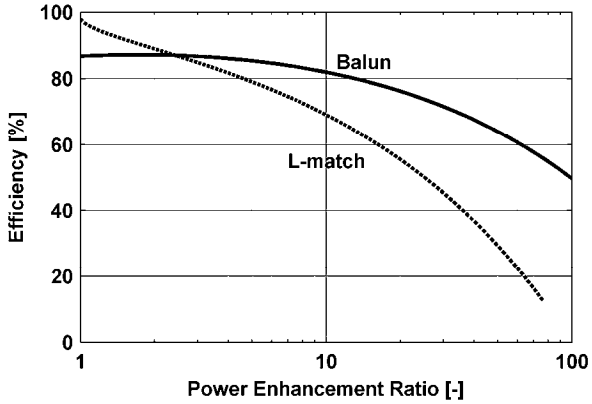

Figure 4.5: Efficiency of L-match and balun for $Q_L = 10$

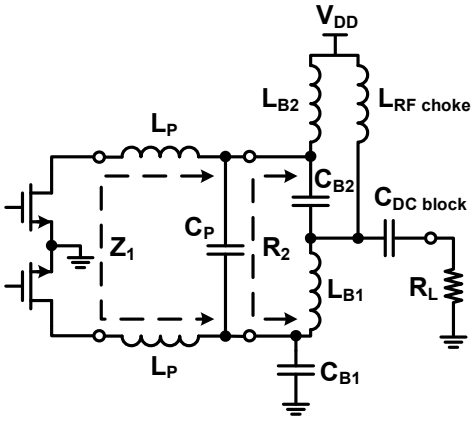

Figure 4.6: Simplified schematic of output matching network, where PCB transmission lines are omitted

amplifier are not included and therefore the efficiency of a complete transmitter is lower than the efficiencies plotted in Figure 4.4a.

4.4.2 Balun

From Figure 4.4a it was clear that the efficiency of the L-match network dropped significantly for large power enhancement ratios. Therefore, in order to obtain a higher efficiency, two amplifiers could be operated in parallel and combine the output power from each amplifier. A convenient way of combining the power from two amplifiers is to use a balun [1], [8] as in Figure 4.4b. By operating the amplifiers differentially, the double voltage swing is available, which means that the differential impedance the overall amplifier has to drive is four times larger than if a single-ended amplifier would

have been used. As each amplifier can see a higher impedance than if a single L-match would have been used, each amplifier can then utilize a lower power enhancement ratio with a higher efficiency and bandwidth. Investigating and applying nodal analysis for the differential amplifier connected to a balun in Figure 4.4b, the input impedance of the balun can be found as in (4.14) (neglecting the parasitic resistances in the inductors).

If the input impedance is supposed to be resistive (4.15), the component values can be calculated according to (4.16). As for the L-matching network we assume the capacitors are lossless. The nodal analysis shows that the output voltage across the load can be written as in (4.17) [9] and makes it possible to calculate the currents through the inductors and the corresponding losses such that an overall efficiency can be computed. In a similar way as for the L-match network, the power enhancement ratio is swept and the efficiency can be evaluated. Figure 4.5 shows the efficiency of an L-match and a balun for different power enhancement ratios. For enhancement ratios larger than two, the balun outperforms the L-match, and as the ratio is approaching one, the matching network can be left out completely.

Due to the properties of the balun it was used in the implemented amplifiers presented in **Paper 1 - Paper 4**, but using off-chip components. The quality factors of the off-chip matching networks are significantly higher, but show the same trends as in Figure 4.4 and Figure 4.5. Since the balun cannot be directly connected to output of the

$$Z_{in} = \frac{4\frac{L}{C}R_L + \left(\omega L - \frac{1}{\omega C}\right)^2 R_L + j\left(2R_L^2 - 2\frac{L}{C}\right)\left(\omega L - \frac{1}{\omega C}\right)}{4R_L^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{4.14}$$

$$Z_{in} = \left\{\omega L = \frac{1}{\omega C}\right\} = \frac{L}{R_L C} \tag{4.15}$$

$$\sqrt{Z_{in}R_L} = \omega L = \frac{1}{\omega C} \tag{4.16}$$

$$v_{out} = v_{in}\frac{R_L\left(1 + \omega^2 CL - j\omega CR_{Lm}\right)}{R_L + R_{Lm} - \omega^2 R_L CL + j\omega R_L CR_{Lm} + j\omega L} \tag{4.17}$$

$$C_P = \frac{2L_P\omega - \mathrm{Im}\{Z_1\}}{\omega\left(\mathrm{Re}\{Z_1\}^2 + 4L_P^2\omega^2 - 4L_P\omega\,\mathrm{Im}\{Z_1\} + \mathrm{Im}\{Z_1\}^2\right)} \tag{4.18}$$

$$R_2 = \frac{\mathrm{Re}\{Z_1\}^2 + 4L_P^2\omega^2 - 4L_P\omega\,\mathrm{Im}\{Z_1\} + \mathrm{Im}\{Z_1\}^2}{\mathrm{Re}\{Z_1\}} \tag{4.19}$$

$$\sqrt{R_2R_L} = \omega L_{B1} = \omega L_{B2} = \frac{1}{\omega C_{B1}} = \frac{1}{\omega C_{B2}} \tag{4.20}$$

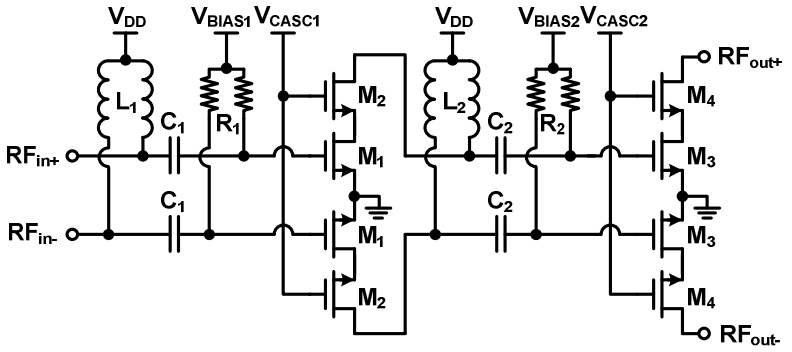

Figure 4.7: Power amplifier with LC-based matching networks in Paper 2 [11]

transistors, bondwires and transmission lines were used at the immediate output of the differential amplifier as in Figure 4.6. For simplicity we assume that the bondwire inductance and the interconnections from the PA to the balun can be represented by L_P, and that the balun makes an impedance transformation from a resistive value R_2 to a resistive R_L. A pre-matching capacitor, C_P, was used before the balun to compensate for the bondwire inductance and interconnection lines from the PA to the balun [10] and transforms the optimum load impedance, $\mathrm{Re}\{Z_1\}$, to a higher level R_2. Analyzing the matching network in Figure 4.6, the relationships between the parasitic inductance, L_P, the virtual resistance R_2 of the balun, the balun components, L_{Bx} and C_{Bx}, and the pre-matching capacitor are found in (4.18)-(4.20).

4.5 Input and Interstage Matching

4.5.1 LC-Based Matching Network

The matching issues discussed so far mainly targets the last stage of the power amplifier. However, typically the amplifier consists of more than a single stage to achieve sufficient gain. One of the amplifiers in **Paper 2** [11], Figure 4.7, uses input and interstage matching networks based on inductors and capacitors. As the power amplifier targeted a high level of linearity, it means that a high level of linearity must be maintained through the amplifier chain to the output stage. A simplified schematic of the interstage matching between the first and second stage is shown in Figure 4.8 and Figure 4.9. For simplicity M_1 and M_2 is assumed to have an output impedance comprising a parallel resistor, R_{out}, and drain capacitance, C_D. Further, C_D is assumed to be much smaller than the equivalent input capacitance, C_{in}', as defined in (4.22). R_{out} is assumed to be sufficiently large to be neglected.

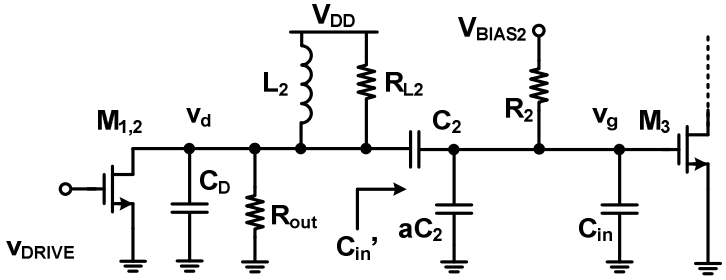

Figure 4.8: Interstage matching between first and second stage

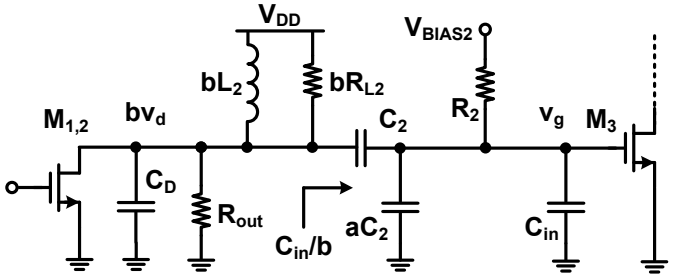

Figure 4.9: Capacitive division

$$\omega_0 = \frac{1}{\sqrt{L_2 C_{in}'}} \tag{4.21}$$

$$C_{in}' = \frac{C_2(aC_2 + C_{in})}{C_2 + aC_2 + C_{in}} = \frac{k(ka+1)}{k+ka+1} C_{in} = \frac{1}{b} C_{in} \tag{4.22}$$

$$v_g = v_d \frac{C_2}{C_2 + aC_2 + C_{in}} = v_d \frac{k}{k+ak+1} \tag{4.23}$$

The inductor, L_2, is used to tune out the equivalent capacitance, C_{in}', of C_2 ($C_2 = k\,C_{in}$) and C_{in}, the gate capacitance, according to (4.21) at the operating frequency ω_0. The parallel capacitor aC_2 of C_{in} represents the parasitic capacitance to the substrate of C_2. The combination of C_2 and C_{in} creates a voltage divider leaving a signal swing at the gate of M_3 as in (4.23).

To maximize the voltage swing at the gate of M_3, the capacitor C_2 should ideally be infinitely large. However, the parasitic capacitance to the substrate and the large gate capacitance would require unreasonable small inductance values. Considering (4.22), C_{in} can be reduced by a factor b [7]. Thus, if the effective input capacitance is lowered by a factor b, the inductance and its parallel resistor can be increased by a factor of b (assuming constant Q). Additionally, the voltage gain is a factor of b larger at v_d. By knowing the maximum available voltage swing at v_d, and the needed drive signal at M_3,

the ratio between C_2 and C_{in} can be determined. C_2 also separates the drain of $M_{1,2}$ and the gate of M_3, which makes it possible to bias M_3 via a large resistor, R_2.

4.5.2 Transformer-Based Matching Network

Integrated transformers have received a lot of attention [12]-[16] as they have proven to give satisfactory performance over a wide range of frequencies, and due to their capability of signal combining and impedance transformation. The basic principle is shown in Figure 4.10 [12]. A current passes through the primary inductor, L_P. The magnetic flux created by current in the primary winding, i_1, induces a current, i_2, in the secondary winding, L_S, which produces a voltage, v_2, across the load, Z_S, connected between the secondary terminals. The impedance seen at the primary side of the transformer is Z_P and the transformation of the voltages and currents in an ideal transformer are related to the turns ratio as in equation (4.24). The strength of the

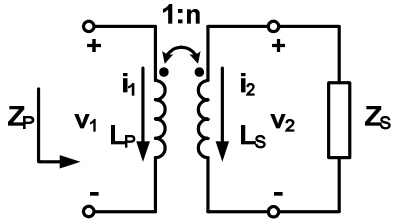

Figure 4.10: Ideal transformer [12]

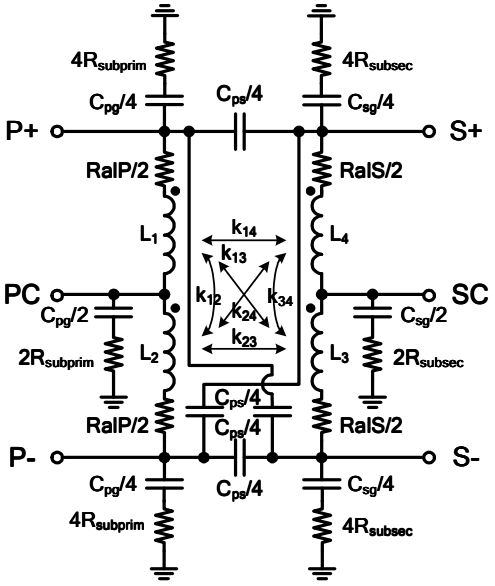

Figure 4.11: Lumped transformer model

$$n = \frac{v_2}{v_1} = \frac{i_1}{i_2} = \sqrt{\frac{L_S}{L_P}} = \sqrt{\frac{Z_S}{Z_P}} \tag{4.24}$$

$$k = \frac{M}{\sqrt{L_P L_S}} \tag{4.25}$$

$$G_{\max} = \left|\frac{S_{21}}{S_{12}}\right|\left(k_s - \sqrt{k_s^2 - 1}\right) \tag{4.26}$$

$$k_s = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} \tag{4.27}$$

$$\eta = \frac{1}{1 + 2\sqrt{\left(1 + \frac{1}{Q_P Q_S k^2}\right)\frac{1}{Q_P Q_S k^2}} + \frac{2}{Q_P Q_S k^2}} \tag{4.28}$$

magnetic coupling between the two windings is defined as the magnetic coupling coefficient, k (=1 for an ideal transformer), by equation (4.25) where M is the mutual inductance between the two windings.

The integrated transformers are in CMOS technologies implemented as coupled integrated inductors, which means that resistance reduction in the windings can be accomplished by using several metal layers on top of each other to reduce the losses in the transformer. The magnetic coupling between the windings is mainly determined by the width and spacing of the metal traces [12], [17]. The magnetic coupling between the windings can be maximized by letting two adjacent conductors belong to two different windings, as the mutual inductance increases. Two conductors of the same winding contribute to the self-inductance and lower the coupling coefficient (4.25). The coupling factor is increased [12] for smaller metal trace widths than for larger widths, but simultaneously the winding resistance increases, as well as the losses, leading to a compromise between coupling and loss.

To evaluate the performance of a transformer, a full 3D electromagnetic simulation would be preferable, but due to the time-consuming simulations, lumped models representing the physical operation of the transformer are tractable in the early design phase. The planar square transformers used in the amplifier in **Paper 1** [18] were based on a lumped transformer model described in [19], where the circuit component values were computed using FastHenry [20] and FastCap [21]. Figure 4.11 shows the lumped model, which includes coupling to the substrate, inductances, the coupling between the primary and secondary windings, capacitive coupling, and the series resistance in the windings. As the quality factor is important for the integrated inductors, so are the quality factors of the primary and secondary windings of the integrated transformer, as well as the coupling factor. Consequently, when a suitable transformer has been found using the lumped transformer models, an electromagnetic simulation should be performed in order to improve the simulation model of the amplifier. A common figure-

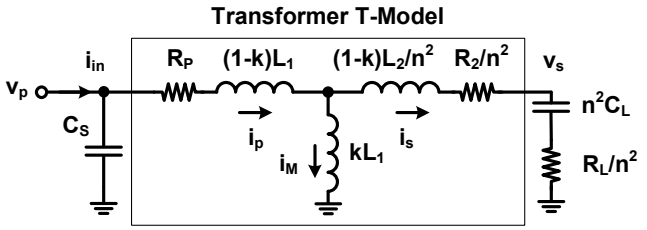

Figure 4.12: Transformer T-model

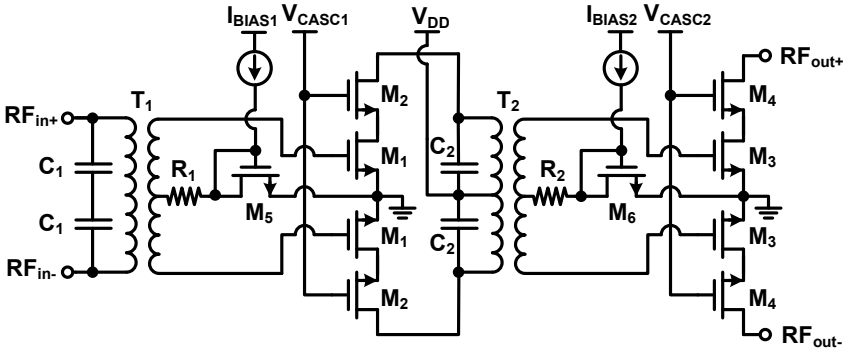

Figure 4.13: Power amplifier with transformer-based input and interstage matching networks in Paper 1 [18]

of-merit used to characterize transformers has been the maximum available gain, $G_{\max}$ [22]-[24], defined in terms of S-parameters [6] for any termination impedances as in equation (4.26) and (4.27). The maximum available gain, $G_{\max}$, is a measure of the gain of the system when the source and load reflections coefficients are conjugately matched to S_{11} and S_{22} [22] and puts a number on how efficient the transformer can be when transferring power from the input to the output during optimal conditions.

The T-model [6] can be used in the evaluation of the transformer [24]. For the T-model shown in Figure 4.12 [5], the efficiency, η, was derived as in (4.28), while using tuning capacitors and optimum choice of L_P. In (4.28), Q_P and Q_S are the quality factors of the primary and secondary windings, respectively. This model was further used in the development of a fully-integrated GSM/GPRS PA [25]. From (4.28), we can see that the efficiency can be maximized by using a coupling factor as close as possible to unity and making the Q of the primary and secondary windings, as large as possible. However, the number of turns and the inductances are limited by the parasitic capacitances from the traces to the substrate and limits the usable frequency range, as well as layout constraints of the process chosen, making it challenging to find an optimum transformer design. Moreover, in PA design the inductances of the

transformers are limited by the large capacitances of the transistors when the transformers are used for interstage matching as in [18].

Figure 4.13 shows the amplifier in [18], using integrated transformers for the input and interstage matching. At the primary windings of both transformers, T_1 and T_2, tuning capacitors, C_1 and C_2, are located in order to reduce the losses [12], while the gate capacitance is put in series with the secondary windings (and its inductance) of the transformer. Since the primary and secondary windings of the implemented transformers are galvanically isolated, the center taps can be used for either biasing of the amplifying transistor, as in the first stage, or power supply of the amplification stage, as in the second stage. The input tuning capacitors, C_1, at the input of the first stage were replaced by a single off-chip component. The input power to the amplifiers was applied differentially with an external 50-to-100Ω balun connected to the signal source. The input impedance of the PAs was designed to present 100Ω differentially.

4.5.3 Cascode Stage

The amplifiers, presented in **Paper 1** and **Paper 2** [11], [18], utilize a cascode configuration in the amplifier stages, which is a combination of a common-gate and a common-source stage. One reason is that in linear PAs with an RF-choke, the drain voltage may reach levels approaching $2V_{DD}$, and therefore cause destructive oxide breakdown and hot electrons. To prevent oxide breakdown to occur, usually a thick gate oxide transistor is put as cascode transistor, M_2 and M_4 in Figure 4.13, in order to protect the input transistors, M_1 and M_3, and distribute the voltage stress during operation. To provide highest protection for the transistors, the gates of the cascode transistors should be biased at V_{DD}, but a lower bias level can provide better performance [13], as it reduces the smallest drain-source voltage for which the cascode transistor operates in the saturation region.

The cascode stage is also used to enable higher output impedance and higher supply voltage than if a single common-source stage would have been used [26]. Though, one has to make sure that the width of the cascode transistor is large enough to not degrade the linearity, but at the same time not too large to have a significant impact on the interstage matching (C_D in Figure 4.8) [27] or the output matching [1]. The input transistors were also chosen as thick oxide transistors to ensure reliable operation. Consequently, to achieve sufficient gain, large transistors were chosen, but results in low input impedance of the device. To improve the RF performance, thin oxide devices should be used, but may require a reduction in supply voltage.

4.6 References

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Chapter 5

Linearization and Efficiency Enhancement Techniques for Power Amplifiers

5.1 Introduction

To meet the increasing demand for higher data rates, wireless systems target higher bandwidth efficiency and increased number of frequency bands. Higher bandwidth efficiency is achieved through more advanced modulation schemes, such as M-QAM and OFDM, which pose challenges to achieve the required linearity in the transmitter circuits in order to comply with spectral and modulation requirements. In addition, to reduce the number of transmitters, a single transmitter covering several frequency bands with maintained RF performance is desirable, which is typically not achieved with the tuned linear Class-A/AB/B PAs. Power consumption is a central issue in all radio transmitters, requiring RF PAs with high efficiency. In traditional linear PA design, this is hard to combine with the requirements on linearity and the high PAPR, which characterizes advanced modulation schemes. CMOS processes are excellent for digital circuits and benefit from the scaling of the technology feature size. Therefore it is therefore a natural step to move functionality from the analog domain to the digital domain, whenever possible. Two major linearization techniques, where highly efficient non-linear PA topologies can be used in order to achieve an overall efficient and linear PA are Polar Modulation and Outphasing.

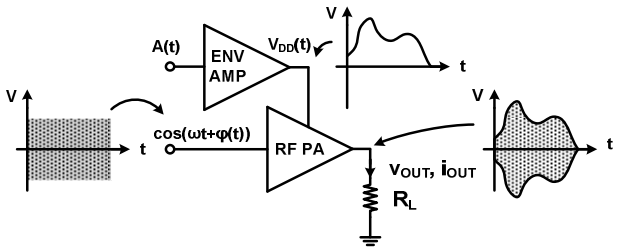


Figure 5.1: Polar Modulation

$$v_{out}(t) = \alpha V_{DD}(t)\cos\left(\omega t + \varphi(t)\right) \tag{5.1}$$

$$V_{DD}(t) = \beta A(t) \tag{5.2}$$

$$\begin{aligned} v_{out}(t) &= \alpha\beta A(t)\cos\left(\omega t + \varphi(t)\right) \\ &\sim A(t)\cos\left(\omega t + \varphi(t)\right) \end{aligned} \tag{5.3}$$

5.2 Polar Modulation

The basic principle in Polar Modulation, Figure 5.1, is to combine a highly efficient non-linear RF PA with a highly efficient envelope amplifier (ENV AMP) to achieve a highly efficient linear PA. The idea of Polar Modulation originates from the Envelope Elimination and Restoration (EER) technique developed by Kahn in 1952 [1], and therefore it is also denoted as the Kahn Technique Transmitter. Suitable RF PAs to be used are switched mode PAs, such as Class-D/E PAs.

Figure 5.1 demonstrates the concept of Polar Modulation, where $\varphi(t)$ and $A(t)$ contains the phase and amplitude information of the RF signal, respectively. The RF output signal is proportional to the supply voltage as in (5.1), where α represents the ratio of the output amplitude to the supply voltage. Furthermore, the supply voltage is modulated according to the amplitude signal, $A(t)$, as in (5.2), where β represents the ratio of the supply voltage to the amplitude signal. The modulated RF output signal can then be expressed as in (5.3) and it is clear that it contains both amplitude and phase modulation.

5.3 Outphasing

5.3.1 Outphasing Background

The basic principle of the outphasing concept, Figure 5.2, is that an amplitude- and phase-modulated signal, $s(t)$ in (5.4), is decomposed into two constant amplitude signals, $s_1(t)$ and $s_2(t)$ as in (5.5) [2], [3], containing the original signal and the quadrature signal, $e(t)$ (5.6).

The two constant amplitude signals are separately amplified by two switching (and preferably highly efficient) PAs and then recombined. In the combiner, the quadrature signals cancel each other and the output signal is an amplified version of the amplitude and phase-modulated signal. Considering the combiner (the plus sign) in Figure 5.2, it can be concluded that the original signal is restored and amplified as long as the combiner is linear and the two amplifier paths are well-balanced. Common ways to combine the PA outputs are:

(1) Using a matched combiner with isolation [4], which suffers from low efficiency unless the power is recycled [5].

(2) Using on-chip [6], [7] or off-chip [8]-[11] λ/4 transmission lines as in Figure 5.3a. The amplifier stages are assumed to be Class-D, here modeled as ideal voltage sources [12].

(3) To eliminate the area-consuming and bandwidth-limiting λ/4 transmission lines [9], a more straightforward method could be to connect the load between the two amplifier outputs, making the transformers suitable from an implementation perspective. This is demonstrated in Figure 5.3b.

The λ/4 transmission lines convert the voltage signals, $V_i e^{\pm j\varphi}$, to current signals, which flow to a common load, R_L, to generate the output voltage, v_{out}, in (5.7) at the fundamental frequency [12]. The output voltage is proportional to $cos(\varphi)$ and the instantaneous amplitude of the amplitude- and phase-modulated signal, $s(t)$. $4/\pi$ is the coefficient of the fundamental component of a square-wave and Z_0 is the characteristic impedance of the λ/4 transmission line.

Similarly, the transformers combine the voltage signals induced from primary turns and apply them on a common load. The transformers are assumed to have a turns ratio

$$s(t) = r(t)e^{j\theta(t)} = r_{\max}\cos\left(\varphi(t)\right)e^{j\theta(t)};\ 0 \le r(t) \le r_{\max} \tag{5.4}$$

$$\begin{aligned} s_1(t) &= s(t) + e(t) = r_{\max}e^{j\theta(t)}e^{j\varphi(t)} \\ s_2(t) &= s(t) - e(t) = r_{\max}e^{j\theta(t)}e^{-j\varphi(t)} \end{aligned} \tag{5.5}$$

$$e(t) = js(t)\sqrt{\frac{r_{\max}^2}{r^2(t)} - 1} \tag{5.6}$$

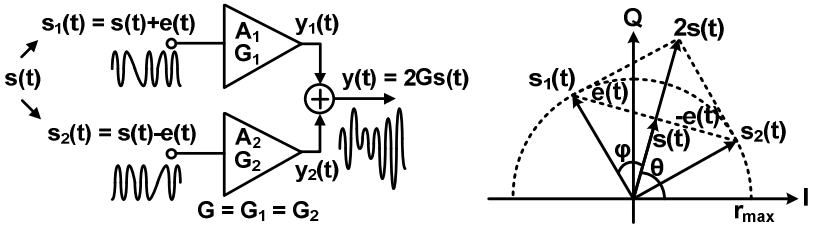
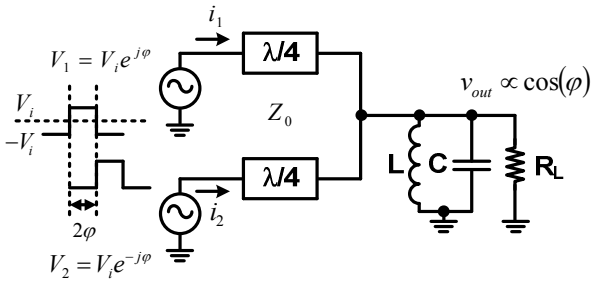
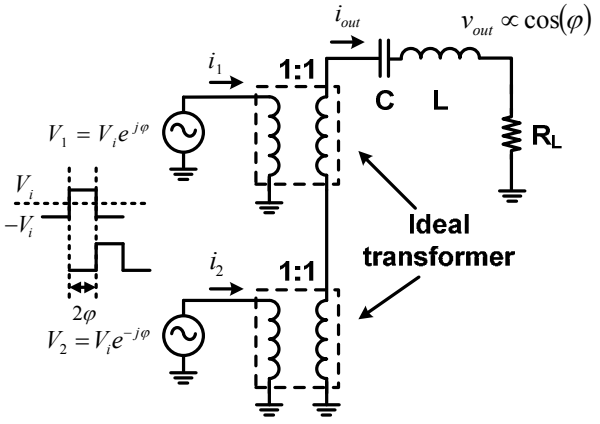


Figure 5.2: Outphasing



(a)



(b)

Figure 5.3: (a) Transmission line combiner [12]
(b) Transformer combiner [12]

$$v_{out}(\varphi) = -j\frac{4}{\pi}\frac{2R_L V_i \cos(\varphi)}{Z_0} \propto \cos(\varphi) \tag{5.7}$$

$$v_{out}(\varphi) = \frac{4}{\pi}\frac{2V_i \cos(\varphi)}{R_L} \propto \cos(\varphi) \tag{5.8}$$

of 1:1 and perfect mutual coupling. As for the transmission line case, the output voltage at the fundamental frequency is proportional to $cos(\varphi)$ (5.8) and the instantaneous amplitude of $s(t)$.

5.3.2 Chireix Combiner and Comparison of PA Types

When using a combiner (a load) with no isolation as in Figure 5.4, each PA, modeled as ideal voltage sources denoted V_1 (5.9) and V_2 (5.10), sees a time-varying load impedance [9], [13], which depends on the outphasing angle as in (5.11) and (5.12). Notice that in (5.9)-(5.15) α is used instead of φ. If the PA would be a Class-B,

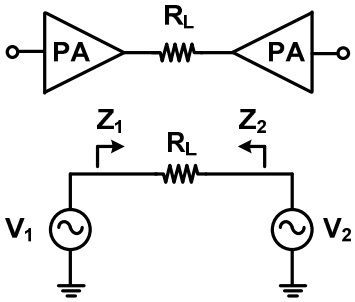


Figure 5.4: Combining with no isolation

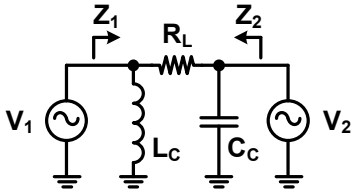


Figure 5.5: Combining with Chireix compensation elements

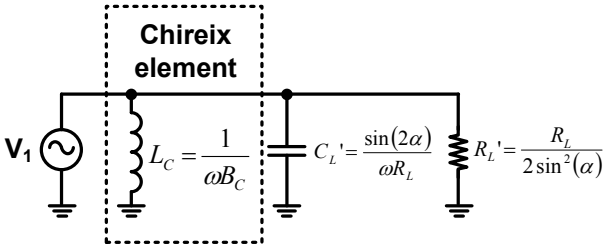


Figure 5.6: Load impedance compensation for V_1 [9]

the output voltage depends on the load impedance, thus degrading linearity and efficiency due to the varying impedances [14]. As the maximum efficiency occurs when the seen load impedance is purely resistive, the basic idea of the Chireix [2] combiner is to add parallel reactive elements, C_C and L_C in Figure 5.5 and Figure 5.6, in order to cancel the reactive part of the load at a certain predefined phase offset value to improve the efficiency at back-off. The efficiency is found as in (5.13) [9], optimal for (5.14), with a back-off from peak power according to (5.15). The efficiency versus power back-off is shown in Figure 5.7 demonstrating that a high efficiency can be achieved at a large back-off when using compensation elements.

In order to analyze the use of reactive elements the load impedance Z_1 can be written in a parallel expression form. In Figure 5.6, the new Z_1 constitutes a resistive part R_L' and a capacitive part C_L'. At a certain phase offset, the capacitive part can be

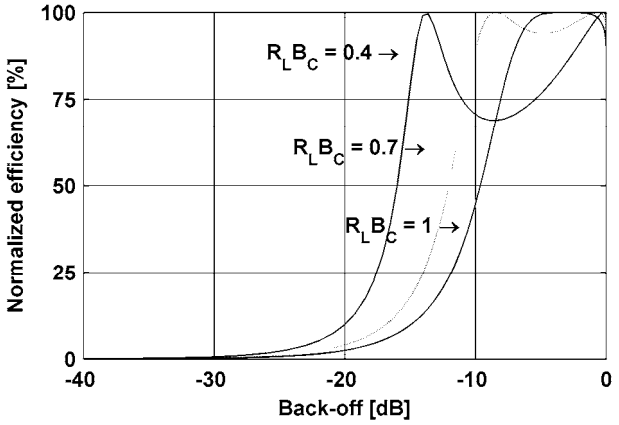


Figure 5.7: Efficiency at power back-off with Chireix compensation elements

$$V_1 = V_0\left(\cos\alpha + j\sin\alpha\right) \tag{5.9}$$

$$V_2 = V_0\left(\cos\alpha - j\sin\alpha\right) \tag{5.10}$$

$$Z_1 = R_L\frac{V_1}{V_1 - V_2} = \frac{R_L}{2}\left(1 - j\cot\alpha\right) \tag{5.11}$$

$$Z_2 = R_L\frac{V_2}{V_2 - V_1} = \frac{R_L}{2}\left(1 + j\cot\alpha\right) \tag{5.12}$$

$$\eta = \frac{1}{\sqrt{1 + \frac{1}{4}\left(\frac{\sin 2\alpha - R_L B_C}{\sin^2\alpha}\right)^2}} \tag{5.13}$$

$$\begin{aligned} \alpha &= \frac{1}{2}\arcsin\left(R_L B_C\right) \\ \alpha &= \frac{\pi}{2} - \arcsin\left(R_L B_C\right),\ 0 \le \alpha \le \frac{\pi}{2} \end{aligned} \tag{5.14}$$

$$BO = 20\log\left(\sin\alpha\right) \tag{5.15}$$

compensated with a parallel inductive element, L_C. Similarly for Z_2, the inductive part can be compensated by a capacitive element, C_C.

It should be noted that the compensation elements are chosen for a specific outphasing angle and frequency, making it less attractive for PAs covering multiple frequency bands. If the used PAs would behave as ideal voltage sources the DC power would scale according to the load impedance and the efficiency would be high regardless of outphasing angle [9]. As discussed for the Class-B PA case, most PAs do

not behave as ideal voltage sources and cannot accept a variable load without distorting the signal. Therefore, such a solution either needs modulation-controlled reactive components in parallel to each PA to compensate for the varying load [13] or use predistortion. Using an inverter-based Class-D PAs mitigates this issue, since the output of an inverter-based Class-D amplifier can be considered as an ideal voltage source, whose output voltage is independent of the load impedance [15]. Therefore, no compensation of the varying load is needed to maintain the linearity. For combiners with no isolation, matching network losses can be reduced at power back-off, improving the efficiency [12].

Another candidate for outphasing is the Class-E amplifier, which absorbs the drain capacitance into the matching network to achieve high efficiency. But in Class-E amplifiers, the zero-voltage switching characteristic depends on the load impedance and is sensitive to load variations [5], [14]-[16], generally making Class-E unsuitable for combiners with no isolation [5]. Thus, to avoid distortion, a combiner with isolation such as a Wilkinson combiner is needed, which isolates the two amplifiers and provides a fixed load impedance to each amplifier [5], [6]. However, a Wilkinson combiner achieves 100% efficiency only at maximum output power [5]. At back-off, power is dissipated in the isolation resistor of the combiner [5]. Class-E amplifiers have, nonetheless, demonstrated good efficiency at power back-off power for combiners with no isolation [17], [18], but may require predistortion to become linear [17].

The Class-D outphasing PA presented in **Paper 5** [19] was based on a Class-D stage utilizing a cascode configuration, driven by an AC-coupled low-voltage driver, to allow 5.5V supply in a 65nm CMOS technology without excessive device voltage stress. The outputs of four Class-D stages were combined by utilizing two on-chip transformers. At 1.95GHz and a 5.5V supply, the output power was +29.7dBm with DE and PAE of 30.2% and 26.6%, respectively. The 3dB bandwidth was 1.6GHz (1.2-2.8GHz). The PA was operated for 168 hours (1 week) without any performance degradation.

The PA design, presented in **Paper 6** [20], was based on the same Class-D stage as the first design, but combined eight amplifier stages by utilizing four on-chip transformers in a 130nm CMOS technology. At 1.85GHz and a 5.5V supply, the output power was +32dBm with a DE and PAE of 20.1% and 15.3%, respectively. Both designs met the ACLR and modulation requirements without predistortion when amplifying uplink WCDMA and LTE (20MHz, 16-QAM) signals.

5.4 Comparison of State-of-the-Art PAs

The performance of the PAs in **Paper 5** [19] and **Paper 6** [20] are compared with published fully integrated Class-D and outphasing PAs in Table 5-1, and the fully integrated polar modulated PAs and linear (Class-AB) PAs listed in Table 5-2 and Table 5-3. The PAs are sorted with regard to output power. The linear PAs have reached higher output powers, partly explained by the lower fundamental tone in Class-D PAs compared to linear PAs. However, it should be noticed that Class-D PAs recently have

gained increased research interest and that +30dBm Class-D PAs have just been targeted and demonstrated as late as this year (2011) [19], [20], [28].

Comparing the PAE of the published PAs at GHz frequencies, the best PAE of +30dBm Class-D PAs is almost 30%, while the PAE of most linear PAs is around 35-40%. Note that the PA in [42] is a PA module, where the transformers are put on a separate high-resistivity Si substrate. Comparing the peak PAE of the polar modulated PAs with output power around +30dBm to +32dBm, the efficiency is in the same order as for the linear PAs.

For many applications the peak PAE is not of interest due to the various modulation schemes including amplitude modulation. Therefore, in the tables a column is included indicating the PAE given a specific back-off in dB. Recent Class-D PAs [24], [26], [28] demonstrate efficiency enhancement schemes making them achieve an efficiency of ~15% at ~7dB back-off, which is comparable to most of the linear PAs. As the Class-D PA in **Paper 5** [19] used a large supply voltage of 5.5V, it is suitable for polar modulation by modulating the supply voltage. At +22.7dBm and +19.7dBm (7dB and 10dB of back-off) when the supply voltage is reduced, the PAE is still as high as 20%

TABLE 5-1: COMPARISON OF STATE-OF-THE-ART FULLY INTEGRATED CLASS-D AND OUTPHASING RF PAS

Ref., Year	Peak P_{out} [dBm]	V_{DD} [V]	DE [%]	PAE [%]	PAE [%], BO [dB][c]	f [GHz]	Tech. [nm]	BW [GHz]
[21] Nam, 2010	+21.6	1.9	64.0	52.0	21, 7	1.92	130	0.30[a]
[22] Chowdhury, 2010	+21.8	1.0	-	44.2	18, 7	2.25	65	1.00[a]
[23] Palaskas, 2010	+25.1	2.0	-	40.6	18, 7	2.40	32	1.00[a]
[24] Yoo, 2011	+25.2	2.5	-	55.2	32, 7	2.25	90	1.00[b]
[25] Xu, 2011	+25.3	2.0	-	35.0	22, 5.7	2.40	32	1.00[a]
[26] Yoo, 2011	+27.0	-	-	26.0	15, 7	2.4	90	>0.7[b]
[7][d] Xu, 2009	+28.1	2.4	-	19.7	8, 7	2.25	45	0.60[b]
[27][e] Walling, 2009	+28.6	2.5	-	28.5	12, 6	2.2	65	-
[19] Fritzin, 2011	+29.7 +30.5	5.5 6.0	30.2 29.7	26.6 26.5	8, 6.6	1.95 1.95	65	1.60[b] 1.60[b]
[28][f] Tai, 2011	+31.5	2.4	-	27.0	12, 6.5 16, 6.7	2.40	45	1.70[b]
[20] Fritzin, 2011	+32.0	5.5	20.1	15.3	4, 7	1.85	130	0.90[b]

(a) 1dB bandwidth
(b) 3dB bandwidth
(c) PAE for a given back-off (BO) in dB from Peak Pout. Values are explicitly written or extracted from graphs
(d) Utilize predistortion
(e) Class-E PA
(f) Utilizing the dynamic power control (DPC)

TABLE 5-2: COMPARISON OF STATE-OF-THE-ART FULLY INTEGRATED POLAR MODULATED RF PAS

Ref., Year	Peak P_{out} [dBm]	V_{DD} [V]	DE [%]	PAE [%]	PAE [%], BO [dB][c]	f [GHz]	Tech. [nm]	BW [GHz]
[22] Chowdhury, 2011	+21.8	1.0	-	44.0	18, 8	2.25	65	0.8[a]
[24][d] Yoo, 2011	+25.3	2.5	-	55.2	32.1, 6	2.20	90	1.0[b]
[29][e] Reynaert, 2005	+27.0	3.3	-	34.0	22, 3	1.75	180	-
[19][d,e] Fritzin, 2011	+29.7	5.5	30.2	26.6	20, 7 17, 10	1.95	65	1.60[b]
[30][e] Brama, 2008	+30.5	2.5	55.0	48.0	20, 10	1.60	130	0.2[a]
[31][e] Lee, 2010	+30.7	3.3	-	45.6	10, 10	1.60	180	>0.5
[32][e] Park, 2007	+32.0	3.3	-	40.0	30, 6	1.90	180	-
[33][e] Lee, 2008	+32.2	3.3	39.0	35.6	32, 6	1.88	180	-
[34][e] Kim, 2007	+33.5	3.3	-	41.0	-	1.90	180	-

(a) 1dB bandwidth
(b) 3dB bandwidth
(c) PAE at back-off (BO) in dB from Peak P_{out}. Explicitly written or extracted from graphs
(d) Class-D PA
(e) The supply voltage is lowered. Efficiency numbers do not include amplitude modulator

and 17%, respectively. These efficiency numbers are competitive compared to the PAs listed in Table 5-2 and Table 5-3, even if an amplitude modulator would lower the efficiency. It should be noticed that some of the linear PAs utilize predistortion [40], [43], to be able to operate the PA closer to their compression point with higher efficiency.

Major benefits of Class-D PAs are the load impedance insensitivity and the bandwidth. While linear PAs use tuned amplifier stages limiting the bandwidth, the bandwidth of Class-D PAs is maintained through the amplification chain to the load, where transformers with high bandwidth can be used for impedance transformation [19], [20] (even though tuning capacitors are usually used to reduce the losses between the primary and secondary windings). Comparing the bandwidth of Class-D PAs [19], [20], [28], they have about twice the bandwidth of the linear PAs and polar modulated PAs. This is a beneficial property for Class-D PAs as cellular terminal PAs are desired to cover a large number of frequency bands, to reduce the total number of PAs required to cover all frequency bands from 700MHz to 2.6GHz in LTE and WCDMA [44], [45] (neglecting band 42 and 43 at 3.4GHz and 3.6GHz in LTE). To optimize the performance in a specific frequency band and output power, tunable matching networks may be necessary [46]. Moreover, Class-D PAs has benefited from the scaling of

TABLE 5-3: COMPARISON OF STATE-OF-THE-ART FULLY INTEGRATED LINEAR RF PAS

Ref., Year	Peak P_{out} [dBm]	V_{DD} [V]	DE [%]	PAE [%]	PAE [%], BO [dB] [c]	f [GHz]	Tech. [nm]	BW [GHz]
[35] Liu, 2008	+27.0	1.2	32.0	-	15, 6	2.40	130	-
[36] Tan, 2011	+28.0	1.8	-	31.9	15, 6	2.75	32	0.45[b]
[37] Chowdhury, 2009	+30.1	3.3	36.6	33.0	12.4, 7	2.30	90	0.70[b]
[38] Kim, 2011	+31.0	3.3	-	34.8	23, 5 15, 8.7	2.50	180	-
[39] An, 2008	+31.2	3.3	-	41.0	-	1.80	180	-
[40][e] Afsahi, 2010	+31.5	3.3	-	25.0	14, 7	2.45	65	0.80[b]
[39] An, 2008	+32.0	3.3	-	30.0	-	1.80	180	-
[41] Degani, 2009	+32.0	3.3	-	48.0	25, 7	2.50	90	>1.4[b]
[42][d] Kim, 2011	+32.5	3.5	-	48.0	18, 7	1.80	180	-
[43][e] Afsahi, 2010	+33.5	3.3	44.2	37.6	22, 7	2.40	65	0.40[b]

(a) 1dB bandwidth
(b) 3dB bandwidth
(c) PAE at back-off (BO) in dB from Peak P_{out}. Explicitly written or extracted from graphs
(d) The PA in [42] is a PA module, where the transformers are put on a separate high-resistivity Si substrate
(e) Utilize predistortion

CMOS with higher switching speeds, making Class-D PAs suitable for nanometer CMOS technologies.

As Class-D output stages operate as inverters, the drain voltage is tied to either V_{DD} or *GND*, and therefore they are insensitive to load variations (also seen in simulations) compared to the Class-A/AB/B PAs. Of course the output power depends on the load, but no voltage peaks would occur at the drain, potentially destroying the device. In Class-A/AB/B PAs, where the drain voltage depends on the load, a stacked-cascode output stage may be necessary to handle load mismatch conditions [47], [48].

The drawback of utilizing Class-D amplifiers is that significant power will be lost in the harmonics, contaminating the frequency spectrum, and also result in short-circuit power dissipation. If the Class-D stage behaves as an ideal voltage source, but with eliminated, or at least smaller harmonics, the amplifier stage can also be used for outphasing. A Class-D stage with suppression of the 3rd harmonic and short-circuit current elimination is described in **Paper 7** [49] and analyzed in **Paper 9** [50].

5.5 Predistortion of Class-D Outphasing Amplifiers

Introducing a gain mismatch, ΔG, and phase mismatch, $\Delta\phi$, in the path of $s_1(t)$ in Figure 5.2, it is clear from (5.16) [14] that besides the amplified signal a part of the quadrature signal remains. The quadrature signal has a larger bandwidth than the original signal, $s(t)$, due to the non-linear operation to create it. Figure 5.8 shows the power spectral densities of $s(t)$, $s_1(t)$, and $e(t)$ for an uplink WCDMA signal. The spectrum of the quadrature signal extends far into the adjacent and alternate channels [51] and degrades system performance measures like ACLR and margins to the spectral mask unless the quadrature signal is cancelled in the power combiner. Therefore a low level of phase and gain mismatch is required between the two signal paths and is difficult to achieve without a feedback system. Besides a distorted spectrum, the mismatch between the two stages will limit the dynamic range in the output stage [52]-[56].

Previous predistortion methods of RF PAs include model-based predistorters using model structures such as Volterra series [57], parallel Hammerstein structures [58], or look-up tables [59], which also can be made adaptive [60]. With the increased interest in linearized switched amplifiers, like the outphasing amplifier, suitable amplifier models and predistortion methods are necessary. Phase-predistortion was evaluated for Chireix combiners in simulations and by using signal generators in measurements (no PA was used) [55]. A gain/phase imbalance minimization technique was verified in measurements in [61], and predistortion was used for high power devices in [62]. In

$$\begin{aligned} s(t) &= s_1(t) + s_2(t) = (1+\Delta G)e^{j\Delta\phi}\left[s(t)+e(t)\right] + \left[s(t)-e(t)\right] = \\ &= \left[1+(1+\Delta G)e^{j\Delta\phi}\right]s(t) + \left[(1+\Delta G)e^{j\Delta\phi}-1\right]e(t) \end{aligned} \tag{5.16}$$

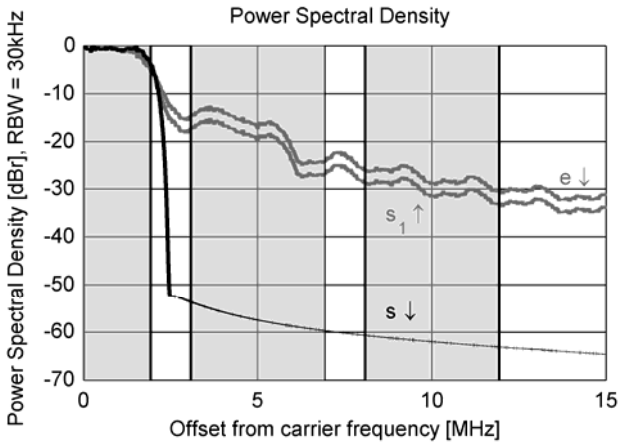


Figure 5.8: Power spectral density of $s(t)$, $s_1(t)$, and $e(t)$ for an uplink WCDMA signal

[62], the predistorter separately compensated for gain and phase imbalances, where the gain imbalance is eliminated by changing the amplitudes of the input outphasing signals. The gain imbalance can also be eliminated by adjusting the voltage supplies in the output stage [9], [13].

Paper 8 [63] presents a behavioural model structure and a model-based phase-only predistortion method suitable for outphasing RF amplifiers. The predistorter proposed in this paper compensates for both amplitude and phase distortion by changing only the phases of the two input outphasing signals. The proposed predistortion method has been used for EDGE and WCDMA signals applied to a Class-D outphasing RF amplifier with an on-chip transformer used for power combining in 90nm CMOS. The predistortion method was applied at the baseband level and has not been implemented in hardware. Based on a similar approach presented in **Paper 10**, an amplifier model and predistortion methods were developed and evaluated using a downlink WCDMA signal, where the ACLR was improved by more than 10dB. In **Paper 11**, a least-squares phase predistortion method was developed and evaluated for the +30dBm Class-D PA design [19] using WCDMA and LTE uplink signals, where the ACLR was improved by approximately 10dB.

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Chapter 6

CMOS Device Reliability

6.1 Introduction

With the tremendous scaling of MOS devices and reduction in fabrication cost, by utilizing a high level of integration of functionality, CMOS-based electronics is a mass-consumer market. Another key factor behind the success of CMOS devices is the reliable operation of the devices. However, the reliable operation is only achieved at low supply voltages and within specified voltage ranges across the device terminals. This increases the design challenges in circuits with large voltage swings, like PAs [1], to achieve the desired output power while still having an acceptable lifetime.

The PAs has predominantly been designed in other processes with faster and high-breakdown voltage transistors, like GaAs HBT [2]-[4], LDMOS [5], [6], and silicon bipolar [7], [8]. However, while most low-voltage and I/O transistors in CMOS operate with a 1-3.3V supply, the output power of PAs for cellular standards is in the order of +30dBm and higher, representing a peak-to-peak voltage swing of 20V. This demonstrates the need for power combining structures and amplifier stages, which can handle a high supply voltage (and voltage stress) to lower the losses in the matching network and achieve a large bandwidth [9], while delivering the desired output power and providing "sufficient" reliability. In this chapter, the main degradation mechanisms of MOS devices are briefly discussed from a circuit designer's perspective.

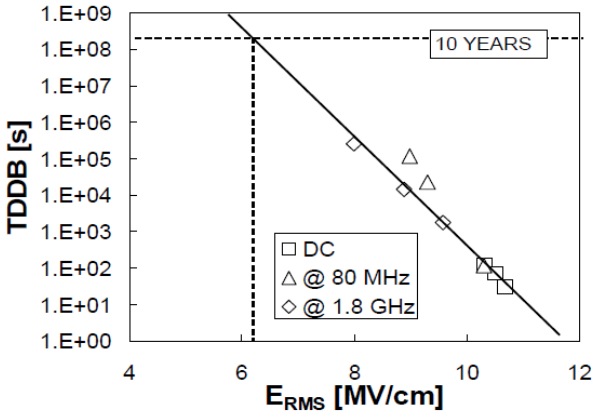

Figure 6.1: Time-Dependent Dielectric Breakdown (TDDB) plotted versus oxide rms field value measured at DC, 80MHz and 1.8GHz [14]

6.1.1 Gate oxide breakdown

Transistor scaling is ideally performed by keeping the electric field strength constant inside the transistor, while scaling the physical dimensions of the MOS device. Thus, with the shrinking thickness of the gate oxide (e.g. 1.2nm in a 65nm process) and the shorter channel lengths, the supply voltage has to be reduced. Gate oxide breakdown results in permanent damage to the device and is caused by tunneling currents through the oxide due to high electric fields across the oxide and result in oxide defects. When the breakdown occurs, it may appear as an ohmic connection (a short) between the gate and the silicon substrate.

The voltage stress across the oxide varies, depending on how the device is utilized in the circuit. Considering Class-E amplifiers discussed in Chapter 3, the drain voltage approaches $3.56V_{DD}$ when the device is in its off-state, i.e. the gate is tied to *GND*. Thus, the maximum field appears at the oxide edge between the gate and the drain. A common practice has been to keep the maximum voltage drops across the devices below $2V_{DD,nominal}$. In that way, the field across the oxide never exceeds the breakdown field of ~1V/nm gate oxide [10], [11]. However, considering Class-E PAs, the gate-drain voltage swings often do exceed these recommendations during RF operation. As discussed in [12], [13], the impact of RF stress is not as damaging as DC stress. During RF operation, the Time-Dependent Dielectric Breakdown (TDDB) is proportional to the root mean square (rms) value of the electric field applied to the gate oxide [10], [14], as shown in Figure 6.1. In [14], the transistors had similar time-to-failure when rms RF and DC stress experiments were compared.

In **Paper 5** [15] and **Paper 6** [16] a Class-D stage, shown in Figure 6.2, with a 5.5V supply was proposed, where the rms electric fields between gate-drain, gate-source, and gate-bulk were <0.7 V/nm gate oxide. This is expected to result in a lifetime of more

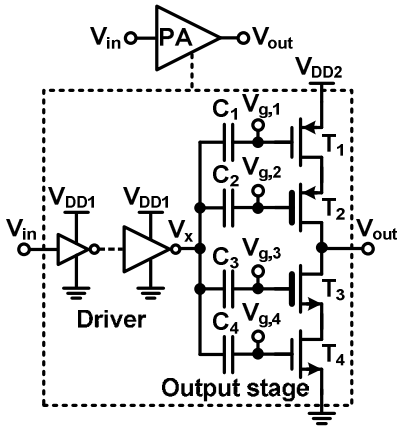

Figure 6.2: Class-D stage proposed in Paper 5 [15] and Paper 6 [16]

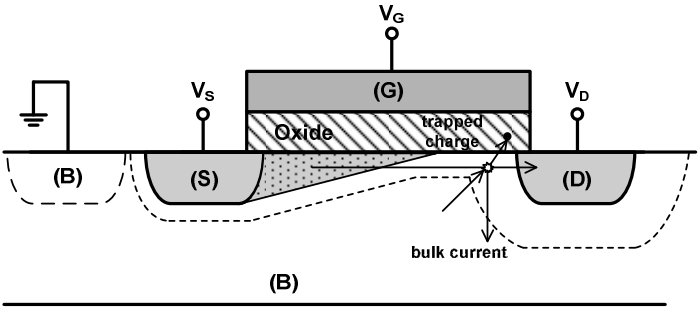

Figure 6.3: Hot carrier stress

than 10 years [17]. If only the thin oxide devices, T_1 and T_4, were driven in the output stage in [16], the output power would is reduced and the rms electric fields between gate and drain of T_1 and T_4 do increase. This would require either a lower V_{DD2} or fixed bias levels $>V_{DD2}/2+V_{DD1}/2$ for T_2 (or $<V_{DD2}/2-V_{DD1}/2$ for T_3), further reducing the output power. The PA in [15] was operated for 168 hours without any sign of performance degradation.

6.1.2 Hot carrier degradation

Hot Carrier (HC) stress occurs when carriers are accelerated in the channel because of a high field between the drain and the source [10], [17]. Due to high electric field, some of the hot carriers can collide with the silicon lattice and cause impact ionization as illustrated in Figure 6.3. The accelerated carriers may also result in avalanche multiplication and surface defects, causing reduced carrier mobility in the channel. The threshold voltage may also shift, caused by trapped charges in the oxide, degrading the PA performance over time.

For HC stress to occur, the device must conduct a sufficient current, while having a large V_{DS}. For devices with channel length >100nm [10], [18], HC stress typically occurs when the drain-source voltage is larger than maximum rated V_{DS} while V_{GS} is around half the drain-source voltage. For devices with channel length shorter than 100nm, maximum HC stress occurs for $V_{GS} = V_{DS}$ and for V_{DS} greater than the maximum rated V_{DS}. Considering switching amplifiers, like Class-D/E, there is only a small voltage drop across the transistor when it conducts current. This can be compared to linear Class-A PAs, which have a significant voltage across the device while conducting current. Thus, switching amplifiers are less disposed to suffer from HC stress compared to linear PAs.

6.1.3 Punch-trough and drain-bulk breakdown

While large transistor terminal voltages may damage the oxide, large voltages may also cause other effects like punch-through and drain-bulk breakdown. When the gate bias of a transistor is absent, the current flowing between the drain and source is very low as the drain-bulk/source-bulk diodes are connected back-to-back with different polarities. Increasing the drain voltage will cause the drain-bulk depletion region to extend to accommodate the voltage drop. Continuously increasing the drain voltage will make the depletion regions approach each other, as illustrated in Figure 6.4, and increase the current between the drain and the source even without substantial gate bias. Compared to gate oxide breakdown and HC stress, punch-through is not directly a destructive phenomenon. However, a larger current and large voltage drop across the device may result in thermal issues and also generate hot carriers.

While ensuring that V_{DS} and the electric field across the oxide are sufficiently small, the drain-bulk diode can experience a significant voltage if V_D is continuously increased. As the bulk, in a standard CMOS process, is connected to a fixed electric potential (often *GND*), the diode reverse bias voltage is directly proportional to the drain voltage. However, compared to the above-mentioned stress phenomena, the drain-bulk diode breakdown occurs at high rather voltage levels around 10V in nanometer technologies [16]. As the Class-D output stage in Figure 6.2 operates as an inverter, the drain voltage is tied to either V_{DD2} or *GND* and therefore it is less sensitive to load variations (seen in simulations) compared to Class-A/AB/B PAs. Naturally the output power would vary depending on the load, but no voltage peaks would occur at the drain potentially destroying the device. In Class-A/AB/B PAs, where the drain voltage depends on the load, stacked-cascode output stage may be necessary to handle load mismatch conditions [19], [20].

6.1.4 Required time of operation

As concluded in this chapter, the lifetime of the devices strongly depends on the voltages applied on the device terminals. A natural question to ask is what is a reasonable lifetime of a PA? While digital circuits usually are designed with a low supply voltage and low device voltage stress for low power operation with an expected lifetime of at least 10 years, terminal PAs may have a significantly lower required lifetime when considering the time the PA is actually operated. In [10], a test time of

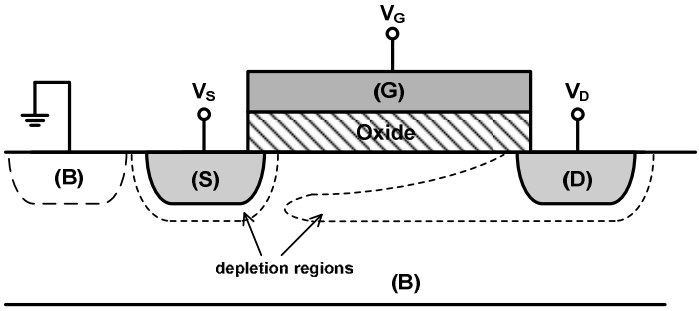

Figure 6.4: Punch-through

168 hours (1 week) at elevated supply voltage is considered to cover more than five years of product reliability for WLAN. Assuming a 2G GSM phone with a 12.5% duty cycle (1 out of 8 time slots), four hours of talk time per day for 1.5 years (estimated lifetime of handset PA) [21], represents only ~275 hours of continuous PA operation.

These examples show that the required lifetime during operation is significantly lower than years and can be measured in terms of weeks. However, we should keep in mind that these calculations are only relevant for terminal/user equipment, whereas the required lifetime in base station PAs is significantly longer.

This chapter has briefly described the major breakdown mechanisms in CMOS devices. While the transistor degradation is important to consider in order to maintain the functionality of the circuits, it has been discussed and shown that the transistor voltage stress can be used as a design parameter in PAs to maximize performance and to ensure sufficient lifetime.

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Chapter 7

Conclusions and Future Work

7.1 Summary

The power amplifier (PA) is a key building block in all RF transmitters. To lower the costs and allow full integration of a complete radio System-on-Chip (SoC), it is desirable to integrate the entire transceiver and the PA in a single CMOS chip. While digital circuits benefit from the technology scaling, it is becoming harder to meet the stringent requirements on linearity, output power, bandwidth, and efficiency at lower supply voltages in traditional PA architectures, such as the Class-A PAs in **Paper 1** and **Paper 2**. This has recently triggered extensive studies to investigate the impact of different efficiency enhancement and linearization techniques, like polar modulation and outphasing with Class-E, **Paper 3** and **Paper 4,** and Class-D PAs, **Paper 5 - Paper 8**, in nanometer CMOS technologies. While the reduced dimensions of the transistors in nanometer CMOS technologies require lower supply voltages, it is desirable to operate the PAs with a supply voltage as high as possible to maximize output power and efficiency. This raises reliability concerns in PAs with large voltage swings, such as the Class-E PA in **Paper 4**. Therefore, it is necessary to evaluate the impact of the large voltage swings on the reliability to ensure an acceptable lifetime of the PA.

This thesis has addressed the potential of integrating highly linear and power-efficient PAs in nanometer CMOS technologies at GHz frequencies. In total eight amplifiers have been designed - two linear Class-A PAs, **Paper 1** and **Paper 2,** two low-voltage switched Class-E PAs, **Paper 3** and **Paper 4**, and four Class-D PAs, **Paper 5 - Paper 8**, linearized in outphasing configurations. Based on the outphasing PAs, amplifier models and predistorters have been developed and evaluated for uplink

(terminal) and downlink (base station) signals as presented in **Paper 8, Paper 10,** and **Paper 11**.

As the output of a Class-D stage switches between V_{DD} and *GND*, it becomes robust against load impedance variations, which are common in handheld devices [1], [2]. However, to overcome the lower output power of Class-D PAs compared to Class-A/AB/B PAs, given the same supply voltage and load resistance, a Class-D stage operating at a 5.5V supply voltage without excessive device voltage stress has been presented in **Paper 5** and **Paper 6**. The Class-D stage has been used in two PAs designs, among the first Class-D RF PAs reaching +30dBm, in 65nm and 130nm CMOS technologies. The PAs demonstrate a state-of-the-art output power of +32dBm, **Paper 6,** and state-of-the-art 3dB bandwidth of 1.6GHz, **Paper 5,** for Class-D PAs. Comparing the 3dB bandwidth with the bandwidth of linear PAs it is twice as large as for most of the state-of-the-art linear (Class-A/AB/B) PAs with similar output power. The large bandwidth is useful in cellular applications as it potentially could reduce the number of PAs required to cover all frequency bands from a few hundred MHz to some GHz.

A Class-D stage, presented in **Paper 7** and analysed in **Paper 9**, cancelling the third harmonic in the output spectrum and improving drain efficiency is a solution for amplifiers to reduce the harmonic distortion over a large frequency range. The Class-D stage has demonstrated to be useful in outphasing applications as well.

In theory two switched PAs linearized in an outphasing configuration results in a perfectly linear and power efficient PA. However, in real implementations the individual amplifier stages experience gain and phase mismatches, distorting the spectrum. Based on Class-D outphasing PA implementations, amplifier models and phase-only predistorters have been proposed to compensate for amplitude and phase mismatches within the dynamic range of the PA as presented in **Paper 8, Paper 10**, and **Paper 11**. As shown by measurements, the spectral performance of a Class-D PA can be significantly improved by only adjusting the phases of the input signals for an outphasing PA with limited dynamic range.

7.2 Conclusions and Future Work

While the switched Class-D/E PAs have the potential of higher efficiency compared to traditional PA architectures, it is more challenging to reach the required dynamic range for some standards than if a linear PA would have been used. Thus, to achieve a large dynamic range, power combining methods [3] or mixed-mode PAs [4] are necessary to make the switched PAs a viable solution for applications requiring a large transmit power control.

Comparing the peak and 7dB back-off (PAPR in LTE and WLAN) PAE of the fully integrated Class-D PAs with an output power between +25dBm and +30dBm, the PAE has until recently [3], [5], [6], been lower compared to linear and polar modulated PAs with a comparable output power. As Class-D PAs now reach the same output power

levels as other types of RF PAs by using Class-D stages with high supply voltages as in **Paper 5** and **Paper 6**, potential research directions are to further investigate and develop efficiency enhancements methods for Class-D PAs as in [3], [5]. Due to the large bandwidth in Class-D, an improved version of the amplifier stage in **Paper 7** lacking the third harmonic but designed for higher output power could be a step towards a wideband PA with low harmonic distortion and improved drain efficiency.

In general, the Class-D outphasing designs have demonstrated sufficient linearity without the need for predistortion, but for PAs with limited dynamic range and matching between the amplifier stages, a phase-only predistorter is a viable way to go to improve linearity as shown in **Paper 8, Paper 10,** and **Paper 11**. Compared to **Paper 8** and **Paper 10, Paper 11** presents a least-squares predistortion method where no iterations are needed.

In applications with lower output power requirements than cellular applications, like WLAN, the PA has successfully been integrated in CMOS and replaced the external PA. While traditional PA topologies are becoming challenging to design in nanometer CMOS technologies, switched and highly efficient PA architectures have gained research interest. However, while these PA architectures are attractive from an implementation point of view, they also have their own specific challenges and limitations when used in linearization schemes. Together the requirements on output power, efficiency, dynamic range, linearity, reliability, noise levels, and cost will be the key aspects determining whether the PA will be integrated together with the transceiver in CMOS for cellular applications.

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