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# Low-voltage ambipolar polyelectrolyte-gated organic thin film transistors

Abdellah Malti, Magnus Berggren, and Xavier Crispin<sup>a)</sup>

*Organic Electronics, ITN, Linköping University, SE-601 74 Norrköping, Sweden*

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Organic transistors that use polyelectrolytes as gate insulators can be driven at very low voltages ( $< 1V$ ). The low operating voltage is possible thanks to the formation of electric double layers upon polarization which generates large electric fields at the critical interfaces in the device structure. In this work, we use a semiconducting blend (of a high electron affinity polymer and a low ionization potential one) in conjunction with a solid polyelectrolyte insulator to fabricate low-voltage ambipolar organic transistors. For both n- and p-channel operation, we use a polycation with readily mobile - yet large enough to limit bulk doping of the semiconductor - counterions.

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Organic electronics offers the promise of large area, easily-processable and low-cost electronics.<sup>1,2</sup> Various ambipolar organic transistor routes have been explored: Multilayered,<sup>3</sup> evaporated small molecules,<sup>4,5</sup> as well as from single polymer systems,<sup>6,7</sup> and polymer blends.<sup>8</sup> The dielectrics needed to gate the semiconductor channel in organic thin film transistors [OTFTs] have also received considerable attention from the scientific community.<sup>9</sup> However, the coarse printing (or coating) techniques, and desired low-voltage operation, that make organic electronics technology so attractive are often incompatible with the traditional dielectrics (oxides, high-k dielectrics, etc.) commonly used in the silicon-based electronics industry. Polyelectrolytes, composed of charged polymer chains and mobile counterions, offer a good compromise as they allow the generation of a very large electric field at the semiconductor-dielectric interface at film thicknesses ranging from 100 nm to 1  $\mu\text{m}$  (i.e., at thicknesses that can easily be manufactured using common printing or coating tools).<sup>10</sup> Complementary circuits, with p- and n-type devices, play a pivotal role in electronics as they offer low static power consumption and high noise immunity.<sup>11,12</sup> Polyelectrolyte gated complementary circuits have been demonstrated, but these devices necessitate a sophisticated patterning process.<sup>13</sup>

In this work, we present a similar low voltage concept that does away with the patterning step as it utilizes a blend of air-stable n- and p-type semiconducting polymers.<sup>8</sup> This semiconductor layer is gated with a polycation that contains relatively large mobile ethylsulfate ions. These devices are stable in air and operate in the hole or the electron transporting regime (in addition to the ambipolar regime in which both charges run along the channel simultaneously).

To fabricate these devices, source and drain electrodes are patterned with wet lithography from a 5 nm chromium (for adhesion) and 50 nm gold layers on glass (see figure 1a). These electrodes are interdigitated to decrease gate leakage.<sup>13</sup> Regioregular

poly(3-hexylthiophene) [P3HT] (average  $M_n$  between 15,000 and 45,000) obtained from Sigma-Aldrich and poly[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5'-(2,2'-bithiophene) [P(NDI2OD-T2)]<sub>n</sub> (ActivInk<sup>TM</sup> N2200 by Polyera®) are dissolved separately in dichlorobenzene at concentrations of 3mg/ml and 5mg/ml respectively (see figure 1b for the chemical structures).<sup>14</sup> Both solutions are filtrated using a PTFE filter with 0.45  $\mu\text{m}$  pores. The solutions are then blended together with a magnetic stirrer for 30 min, then immersed into an ultrasonic bath at 50 °C for 30 min. The semiconductor layer is deposited on the source and drain electrodes by spin-coating the P3HT/[P(NDI2OD-T2)]<sub>n</sub> blend at 3000 rpm. The film is then vacuum-annealed at 90 °C for 30 s. The polyelectrolyte layer is composed of ([Poly(vinylpyrrolidone-co-dimethyl-ethyl-amoniomethylmethacrylate)]<sup>n+</sup> [ethylsulfate]<sup>n-</sup>) [P(VP-EDMAEMAES)] provided by BASF. This polycation is dissolved at 20% weight ratio in a 1:1 solution of 1-propanol and water. The solution is then spin-coated on top of the semiconductor at 3000 rpm and vacuum-annealed at 90 °C for 90 s. The device structure, along with the frontier molecular energy levels of the active materials with respect to the workfunction of gold, are shown in figure 1. The injection of holes from a gold electrode to the Highest Occupied Molecular Orbital (HOMO) of P3HT is ohmic<sup>15</sup>, whereas electrons have to overcome an injection barrier of around 0.9 eV from the gold electrode to the Lowest Unoccupied Molecular Orbital (LUMO) of [P(NDI2OD-T2)]<sub>n</sub>.<sup>16,17</sup> For the energy levels quoted above, we assume that the gold electrodes are atomically clean. However, it has been demonstrated that under similar manufacturing conditions, the workfunction of gold electrodes is typically found between 4.4 and 4.6 eV.<sup>18</sup> This brings down the actual electron injection barrier to only 0.2-0.4 eV.

Upon polarizing a polyelectrolyte, an electric double layer [EDL] (also known as a Helmholtz layer) is formed. This EDL is due to the reorganization of mobile ions upon biasing the device.<sup>11,19</sup> The electric field generated at the interface is generally on the order of  $10^9 \text{ Vm}^{-1}$ .<sup>20</sup>

<sup>a)</sup>Electronic mail: xavier.crispin@liu.se

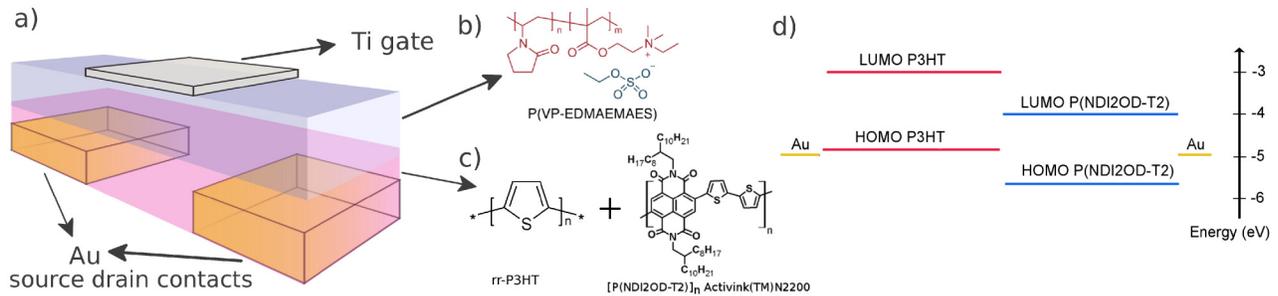


FIG. 1. (Color online) (a) Device schematic of the transistor. (b) Chemical structure of the polyelectrolyte. (c) Chemical structure of the semiconductors. (d) Energy levels of the active materials with respect to the workfunction of (atomically clean) gold.

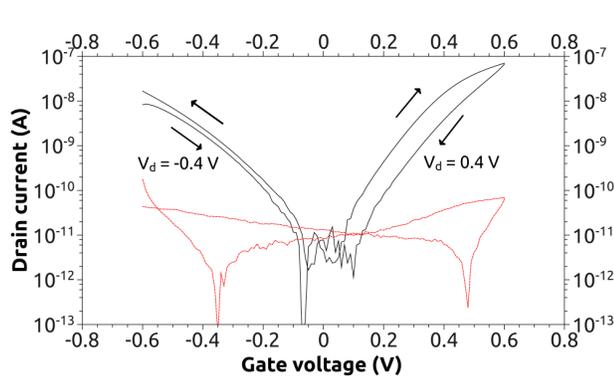


FIG. 2. (Color online) Transfer characteristics of the drain current versus gate voltage at a drain voltage of 0.4 V for positive  $V_g$ , and -0.4 V for negative  $V_g$ .  $W/L = 1000/3$ . Scan speed: 0.12 V/s.

The choice of this particular polyelectrolyte can be motivated by its relatively fast rate of polarization (the EDLs are formed at a rate of 10 KHz), a capacitance per area in excess of  $10 \mu\text{F}/\text{cm}^2$ , and the molecular nature of its ethylsulfate counterions.<sup>15</sup> The latter is expected to slow down the penetration of the anion into the semiconductor, thus minimizing electrochemical reactions at the semiconductor-electrolyte interface.

The transfer curve (see figure 2) shows that the transistor functions as n-type (positive  $V_g$  and  $V_d$ ) as well as p-type (negative  $V_g$  and  $V_d$ ), and with substantial symmetry that can be attributed to a rather similar electron and hole injection barriers. The arrows show the direction of the sweep, and the hysteresis suggests that some minor electrochemical doping might occur. This OTFT exhibits an on-off ratio of around  $10^4$ . All the measurements were conducted in ambient atmosphere and at room temperature. The mobility in the linear regime was calculated from the following equation  $\frac{\partial I_d}{\partial V_g} = \frac{W}{L} C_i \mu V_d$ , and yields  $0.008 \text{ cm}^2/\text{Vs}$  for the n-type and  $0.015 \text{ cm}^2/\text{Vs}$  for the p-type. These mobility values are much lower than those reported in devices with thin oxide dielectrics.<sup>21</sup> The difference in mobility can be tentatively attributed to

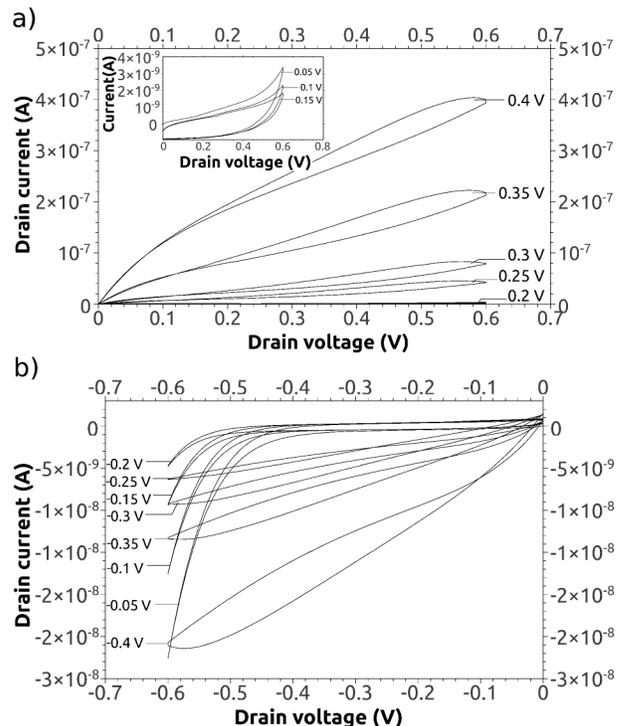


FIG. 3. (a) n-type output characteristics showing the drain current versus drain voltage for gate voltages between 0.05 V and 0.4 V (Inset presents a zoom for gate voltages between 0.05 V and 0.15 V). (b) p-type output characteristics showing the drain current versus drain voltage for gate voltages between -0.05 V and -0.4 V. Scan speed: 0.12 V/s

charge trapping along the semiconductor-polyelectrolyte due to the presence of ions.<sup>9,10</sup>

The n-type output curve in the first quadrant is shown in figure 3a. The superlinear behavior exhibited at low gate-source voltages (between 0 V and 0.15 V) in the inset demonstrates ambipolar behavior.<sup>16</sup> Figure 3b shows the output curve in the third quadrant (p-type mode of operation). The superlinearity of the drain current at low voltages (between 0V and -0.2 V) is strong evidence

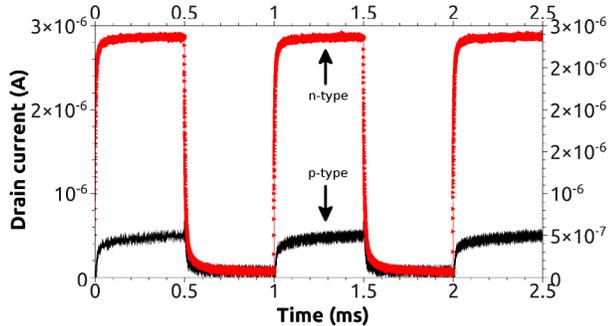


FIG. 4. (Color online) Transient measurements that show the drain current's response to a 1 KHz square-shaped pulse of (+/-)1 V on the gate and (+/-)0.4 V drain-source voltage. The line with symbols (red) represents the n-type response  $V_d = 0.4$  V and  $V_g = 1$  V. The line without symbols (black) represents the p-type response - i.e:  $V_d = -0.4$  V and  $V_g = -1$  V.

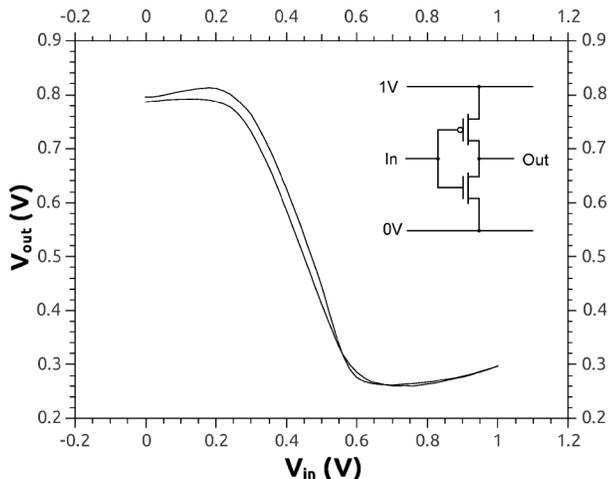


FIG. 5. Electrical characteristics of a complementary-like inverter. The channel length of the transistors is  $3 \mu\text{m}$ . The channel width of the pull-up transistor and the pull-down transistor are 15 and 3 nm respectively.

that both holes and electrons coexist simultaneously in the channel.<sup>8</sup>

The dynamic response of these ambipolar transistors was studied by applying a 1KHz square-shaped (+/-)1 V pulse to the gate while the output drain current was measured as a voltage drop over a  $10 \text{ k}\Omega$  resistance connected in series with the drain electrode. In these measurements, we subtract the capacitance peak according to a procedure previously reported.<sup>19</sup> Figure 4 shows the transient curves for both the p- and n-channel OTFTs. The transistor channel turns on faster than  $200 \mu\text{s}$ . The width to length ratio  $W/L$  of the n-type transistor is five times that of the p-type transistor.

Finally, in figure 5, we present the electrical character-

istics of a polyelectrolyte-gated complementary-like inverter composed of two ambipolar transistors. The gain of this inverter is approximately 2, and the lack of full rail-to-rail swing makes it rather vulnerable to noise.

In conclusion, we have fabricated low-voltage ambipolar OTFTs from a blend of air-stable polymers. The choice of a polycation with relatively large anions ensures that the transistor channel opens quickly in both n- and p-operation mode.

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