A high-linearity SiGe RF power amplifier for 3G and 4G small basestations

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Abstract

This paper presents the design and evaluation of a linear 3.3 V SiGe power amplifier (PA) for 3G and 4G femtocells with 18 dBm modulated output power at 2140 MHz. Different biasing schemes to achieve high linearity with low standby current were studied. The ACPR linearity performance with WCDMA (3G) and LTE (4G) downlink signals were compared, and differences analysed and explained.

Keywords

Power amplifier, WCDMA, LTE, biasing, linearity, ACPR

1. Introduction

Long Term Evolution (LTE) is becoming a widely used standard for 4G to meet demands for increased data rates of cellular transmissions (Astély, Dahlman, Furuskär, Jading, Lindström and Parkvall 2009). While 3G WCDMA uses fixed 5 MHz channels with transmission bandwidth of 3.84 MHz (bandwidth utilisation of 77 %) (3GPP TS25.104 2010), LTE uses bandwidths between 1.4 MHz and 20 MHz (all but the lowest band with utilisation of 90 %) (3GPP TS36.104 2010), which allows for efficient use of spectrum and high data rates up to 100 Mbit/s in the downlink (DL) and 50 Mbit/s in the uplink (UL).

With the introduction of advanced modulation schemes, such as used in EDGE (2.5G), WCDMA (3G) and OFDMA (4G), the linearity of the power amplifier (PA) has become an important research topic. The air interface of LTE is based on orthogonal frequency division multiple access (OFDMA) in the DL and single carrier frequency division multiple access (SC-FDMA) in the UL direction. The use of SC-FDMA reduces the peak to average power ratio (PAPR) by 2-4 dB, which mitigates the linearity requirement and also helps the design of high efficiency terminal power amplifiers, in contrast to WiMax which uses OFDMA for both DL and UL. However for the DL from the basestation, 3G WCDMA and 4G LTE use high Peak-to-Average Power Ratio (PAPR) of 10-12 dB. This requires a large power back-off from peak power, reducing the efficiency. If using a linear class-A/AB amplifier design for this application, DC-to-RF conversion efficiency plays a minor role, instead heat dissipation from the DC biasing current is a major concern. A linear PA with low DC biasing current therefore becomes essential.

ACPR (Adjacent Channel Power Ratio, also ACLR), which is affected by multi-carrier intermodulation, is a good indication of "wideband linearity" for devices operating with multicarrier signals compared to other linearity measures such as P-1dB compression point, third-order intercept (TOI), or IMD products. The 3GPP standards define limits for ACPR and EVM (Error Vector Magnitude), which both relate to linearity, but as a rule of thumb the ACPR requirements are harder to fulfil.

Commonly, GaAs HBT PAs have been used for linear PA applications at low-to-medium power levels for both handsets (usually in multichip modules (MCM)), and basestations (Franco 2009; Li, Zhu, Prikhodko and Tkachenko 2010). Advances in SiGe BiCMOS technologies, using the SiGe bipolar transistors for the amplifier and with possibility of

higher integration using CMOS parts, make it interesting to evaluate the potential of this technology. As GaAs-based devices generally are regarded to be more linear than Si-based devices, it is especially interesting to investigate the 3G and 4G DL modulation schemes' impact on performance and linearity of Si-based PA designs.

Recent published work has explored SiGe-based devices for terminal UL applications. Li, Lopez, Lie, Chen, Wu and Yang (2010) designed a SiGe cascode differential PA chip and used it in an Envelope-Tracking amplifier measurement setup to achieve high efficiency and high linearity for LTE applications. Krishnamurthy et al. (2010) describe a commercial multi-stage design in SiGe technologies, however focusing on WiMax performance with PAPR of about 6 dB. Good linearity is achieved by dynamically balancing the biasing and generation of harmonics between three amplifier stages. (The idea has similarities with the work by Aoki, Kunihiro, Miyazaki, Hirayama and Hida (2004) where two amplifiers with different gain expansion/compression characteristics are connected in series to cancel harmonics.)

This paper describes a linear SiGe PA design capable of delivering 18 dBm of modulated linear output power in the 2110-2170 MHz DL band using a 3.3 V supply voltage for WCDMA and LTE signals. Target is an output stage for a home basestation (femtocell) for 3G and 4G operation, but could also be a basestation linear predriver amplifier stage.

2. Amplifier Design

2.1 Amplifier core design

The goal of the PA design in this paper was an amplifier for 3GPP basestation (femtocell) downlink Band 1 (2110-2170 MHz) with 18-20 dBm modulated output power, aimed for a home base station. Carrier frequency of 2140 MHz and supply voltage of 3.3 V were used in all simulations and evaluations. As modulated signal power plus PAPR for the signal roughly translates to peak power with linear performance (Cripps 2002), the goal for the P-1dB output power was set to 27 dBm.

IBM 5PAe 0.35 µm SiGe BiCMOS foundry technology was used. The process includes an RF-PA optimized SiGe-bipolar device with high breakdown voltages, BV_{CEO} of 8.3 V, and BV_{CBO} of >20 V, which allows linear PA class-A/AB operation up to 5 V supply voltage with margins for load mismatch and long-term reliability without the need for cascode amplifier topology. The technology is aimed for integrated PA design, with features such as two thick top metal layers, TWV (through-wafer vias), 50 Ohm-cm substrate resistivity, and 0.35 um CMOS. The TWV is especially useful for PA applications since it provides a low-reactance path to ground, and increases the RF gain.

72 transistor elements of 3 x 0.8 x 20 um^2 emitter area were needed to achieve the target output P-1dB output power according to estimations and initial load-pull simulations in Agilent ADS. A single-stage single-ended amplifier topology was used. Seven TWV close to the transistor elements array assured good emitter ground connections to the amplifier.

2.2 Bias circuit design

Besides supporting the PA with a well-defined DC-bias point, the biasing circuit can have a large influence on the linearity of the PA. Fig. 1 shows the schematic of a one-stage PA with a conventional resistive bias. The circuit consists of LC-based input and output matching networks, series capacitors for signal DC blocking (not shown), an RF choke (RFC) to the power supply, a load, R_L (50 Ohm), and a bias resistor, R_{bias}. The biasing may also consist of two resistors arranged as a voltage divider between supply and ground.

The PA core and biasing were simulated using Agilent GoldenGate simulator in the Cadence Virtuoso design environment. Ideal LC input and output matching networks were used to tune the PA to achieve maximum output power while keeping ACPR <-45 dBc for the adjacent channel according to the 3GPP standards for WCMDA (3GPP TS25.104 2010) and LTE (3GPP TS36.104 2010) signals. Fig. 2 shows the bias current dependence on the simulated maximum WCDMA modulated linear output power while maintaining ACPR<-45 dBc for the PA in Fig. 1. The ACPR performance was optimised in each point by tuning matching and input power. The highest modulated power for the resistor-biased amplifier, 20.2 dBm, was achieved using a collector bias current in the 400-450 mA range.

As discussed in Section 1, the efficiency of the studied amplifier is of less importance; instead low DC standby current while maintaining linear operation becomes essential. If we could reduce the biasing current without degrading the linearity, this would be a significant advantage.

The drop in linearity at high output power levels is related to early gain compression caused by V_{be} (base-emitter voltage) DC bias drop at the RF transistor (Yoshimasu, Akagi, Tanba and Hara 1998). Fig. 3a shows the V_{be} characteristics for the PA in Fig. 1 for two bias currents representing weak Class-A (I_c=500 mA) and Class-AB (I_c=300 mA) operation, with similar behaviour for both bias currents.

To avoid the bias drop, what we want is a constant voltage source (and an RF block). In in Fig. 3b the V_{be} characteristics have been added for the circuits in Fig. 4a (biasing using a constant voltage source and an ideal RF block (*Vsource*)), and Fig. 4b (implementation of the constant voltage source biasing using a current mirror (*Current mirror*)). A modified Wilson current mirror (Wilson 1968; Hart and Barker 1976) was used, as it is well known to provide robust and distortion-free constant current or voltage. For simplicity, same 3 x 0.8 x 20 um^2 emitter area transistor elements as used for the amplifier were used for the current mirror design, one element for each transistor in the schematic. A 3 nH on-chip inductor was used as RF block between the bias circuitry and the RF path.

In Fig. 5, the linear P_{out} characteristics is compared for the three different biasing circuits. The improvement by using a voltage source is clearly visible at lower bias currents where an additional 0.5 dBm of modulated power could be obtained using bias currents in the 275-300 mA range (Class-AB) without loss of ACPR. The reduced DC current during maintained linear operation is the real advantage of the improved biasing circuitry.

3. Measurements

A. 3.1 Basic RF evaluation

Several PA design variants were fabricated. Fig. 6 shows a micrograph of a fabricated PA with an additional on-chip input prematch. The chip size of all variants was 715 x 830 μm^2. The chips were directly bonded on the testboard, which was a two-layer 0.2 mm thick PCB with ε_r of 4.7 and tan δ of 0.019. Matching to 50 Ω was achieved by passive SMD components. The testboard was designed in Agilent ADS and from the simulations, starting values for the component values and positions on the PCB were obtained. An external SMD resistor (Rmirror in Fig. 4b) was used during the evaluations to select transistor bias current. RF measurements were done using Rohde & Schwarz SMBV100A Vector Signal Generator and Anritsu 2692 Vector Signal Analyzer.

The PA was matched for highest saturated output power and high gain using a bias current of around 300 mA (class-AB). If higher output power is needed, the PA can be operated 5 V, which will further increase the output power an estimated 2-3 dB. However, with the used PCB with no additional cooling or heatsink, the temperature at 5 V supply became too much elevated to perform any reliable measurements.

Fig. 7 shows a plot of the measured and simulated output power and PAE vs. input power at 3.3 V supply voltage and a frequency of 2140 MHz. The PA delivered 26.4 dBm P-1 saturated power with a maximum collector efficiency of more than 50 %. The small-signal gain was 14 dB. There is a good correlation between the measured and simulated characteristics as can be seen from the plots.

A. 3.2 Linearity performance

In this section, we will evaluate linearity performance using ACPR as defined in the 3GPP standards (3GPP TS25.104 2010; 3GPP TS36.104 2010). We will compare WCDMA signals with LTE signals at the same frequency and try to understand differences in the obtained values.

The 3GPP standards define a number of Test Models for the DL, i.e. predefined signal sets aimed for measuring certain parameters or performance. For WCDMA, Test Model 1 (TM1) should be used for ACPR tests (3GPP TS25.141, 2009). LTE should use E-UTRA test Model 1.2 (E-TM1.2) (3GPP TS36.141, 2010). The ACPR was measured using the same setup as in the previous section and was also simulated with additional parasitics from external components and PCB using Agilent's GoldenGate simulator in Cadence Virtuoso design environment with Test Model signals generated in Agilent Signal Studio as baseband inputs in the simulations.

Fig. 8 shows the measured ACPR performance for a WCDMA TM1-64QAM signal and an LTE E-TM1.2-64QAM signal, with different LTE bandwidths. The WCDMA signal reached the -45 dBc limit at a measured modulated output power of 17.9 dBm. The LTE signals, except for 1.4 MHz bandwidth, reached the limit at slightly lower output power, around 17.0-17.4 dBm, while the 1.4 MHz signal reached the limit at 18.4 dBm. Simulated values for the measurement case (not shown) were similar (18.2, 16.7-17.4, and 18.8 dBm), but lower than expected from section 2 where all parameters (bias, matching component values) were optimized for each point and just a few parasitics included in the simulations.

Interestingly, Fig. 8 shows a clear visual grouping of the measured ACPR curves (simulated curves show same visual grouping), which appears to be characteristic for the different signals. This behaviour can be understood by considering the different bandwidth utilisation of the signals. Higher utilisation results in more signal power closer to the band limit, with a larger part of the "signal tail" going into the next band, which will increase ACPR (Sesia, Toufik, and Baker 2009). All LTE signals, except the 1.4 MHz, have the same utilisation (90 %) and fall into one group. The 1.4 MHz has lower utilisation (77 %) and thus ACPR is higher. Although the 1.4 MHz LTE signal and the WCDMA signal have the same utilisation (77 %), the occupied bandwidth (99 % of the power) is somewhat larger for the WCDMA signal. It was measured to 4.2 MHz or 84 % of the band, and for the LTE signal it was 1.09 MHz or 78 % of the band. This will contribute to an increase in ACPR, which may well explain the observed difference.

To increase the ACPR even further (or more correctly, the output power before ACPR limitation), different approaches are needed. Using an analogue Dynamic Predistorter, Yamanouchi, Aoki, Kunihiro, Hirayama, Miyazaki, and Hida (2007), were able to improve the output power by over 15 dB for WCDMA terminal (UL) signals. But the most commonly used approach today is Digital Pre-Distortion (DPD) (Kim, Stapleton, Kim and Edelman 2005) where algorithms in the baseband are used to correct for the non-linearities of the PA.

4. Conclusions

A 3.3 V linear 18 dBm modulated output power SiGe-based PA have been designed and evaluated for WCDMA and LTE downlink signals. Different biasing schemes for high linearity with low standby current were studied. By using a current mirror instead of a conventional resistor biasing, increased ACPR at lower DC biasing was achieved. Differences in ACPR linearity between WCDMA and LTE signals were observed and explained.

Acknowledgments

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Figure Captions

Figure 1. PA design schematics with conventional resistor biasing.

Figure 2. Simulated maximum WCDMA modulated output power while ACPR<-45 dBc for the PA in Fig.1 with the conventional resistor biasing.

Figure 3a. V_{be} vs. P_{out} for the PA in Fig.1 with the conventional resistor biasing for two biasing currents.

Figure 3b. V_{be} vs. P_{out} for different biasing schemes and biasing currents.

Figure 4a. PA design schematics an ideal voltage source for the biasing.

Figure 4b. PA design schematics an current mirror circuit for the biasing.

Figure 5. Simulated maximum WCDMA modulated output power while ACPR<-45 dBc for PA design schematics with conventional resistor biasing in Fig. 1 (*Resbias*), ideal voltage source in Fig. 4a (*Vsource*), and current mirror circuit in Fig. 4b (*Current mirror*).

Figure 6. Chip photo. Chip size was 715 x 830 μm^2 for all chip variants.

Figure 7. Measured and simulated output power and efficiency vs. input power at 2140 MHz and 3.3 V supply voltage.

Figure 8. Measured ACPR performance for WCDMA and LTE signals.

Figure 1

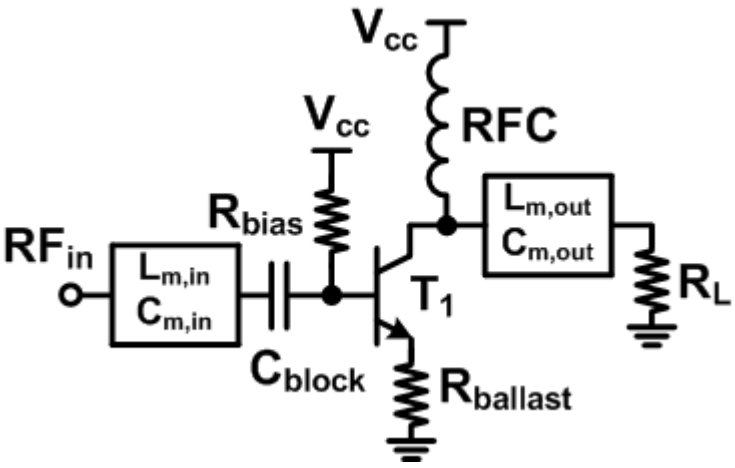

Vcc
Vcc
RFC
Rbias
Lm,out
Cm,out
RFin
Lm,in
Cm,in
T1
RL
Cblock
Rballast

Figure 2

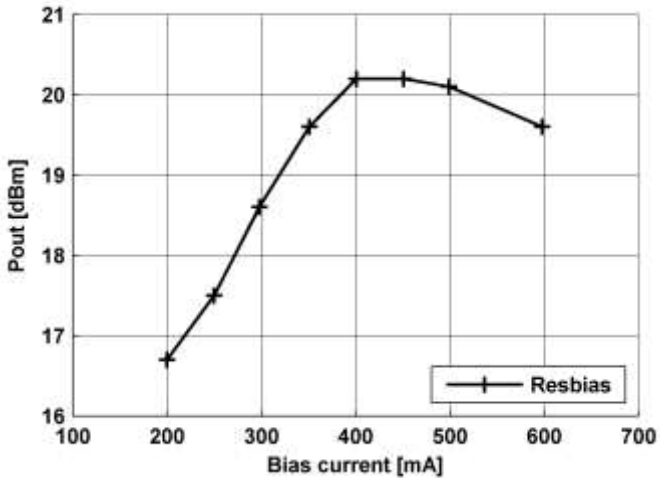

21
20
19
18
17
16
Pout [dBm]
100
200
300
400
500
600
700
Bias current [mA]
Resbias

Figure 3a

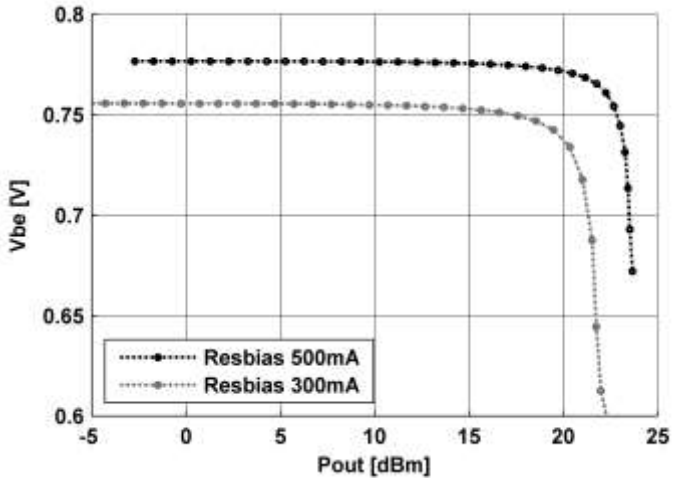

0.8
0.75
0.7
0.65
0.6
Vbe [V]
-5
0
5
10
15
20
25
Pout [dBm]
Resbias 500mA
Resbias 300mA

Figure 3b

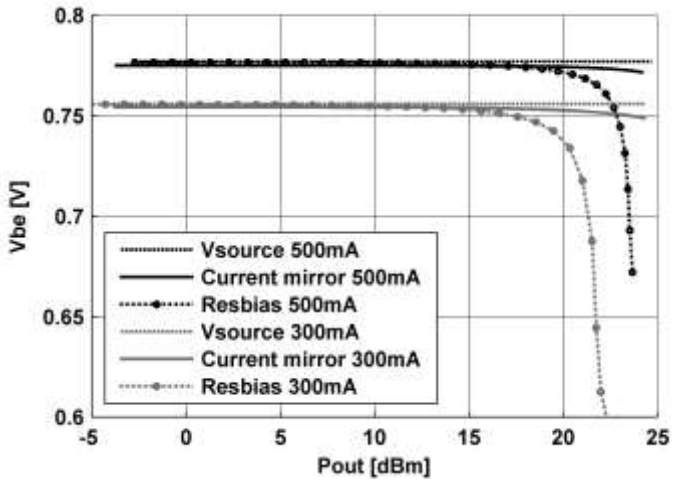

0.8
0.75
0.7
0.65
0.6
Vbe [V]
-5
0
5
10
15
20
25
Pout [dBm]
Vsource 500mA
Current mirror 500mA
Resbias 500mA
Vsource 300mA
Current mirror 300mA
Resbias 300mA

Figure 4a

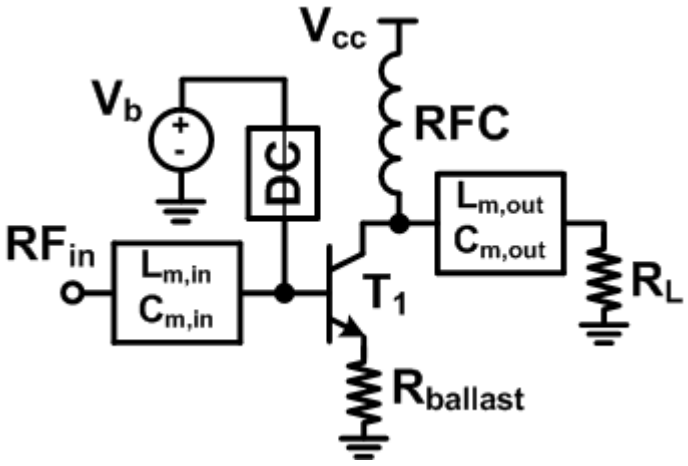


Figure 4b

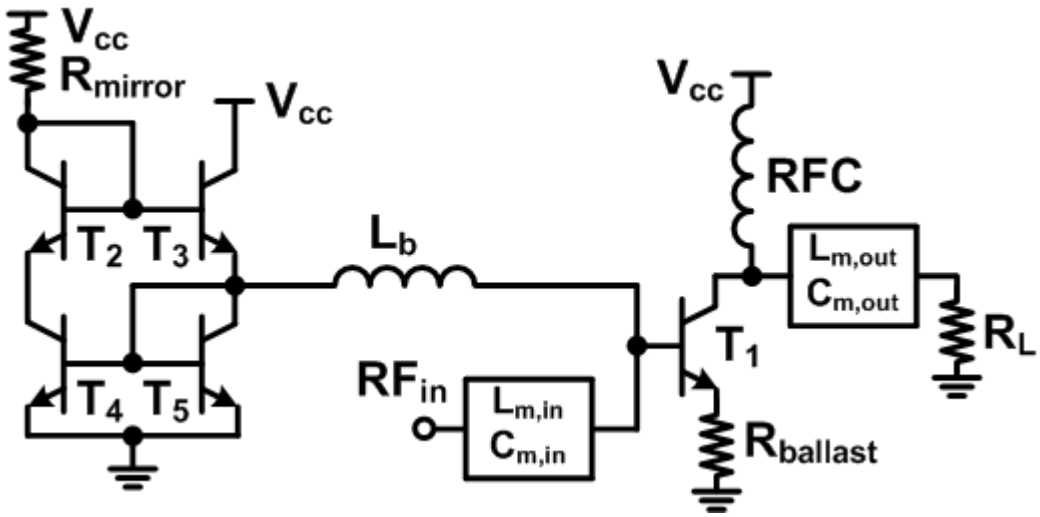

Vcc
Rmirror
Vcc
T2 T3
T4 T5
Lb
RFin
Lm,in
Cm,in
Vcc
RFC
Lm,out
Cm,out
T1
RL
Rballast

Figure 5

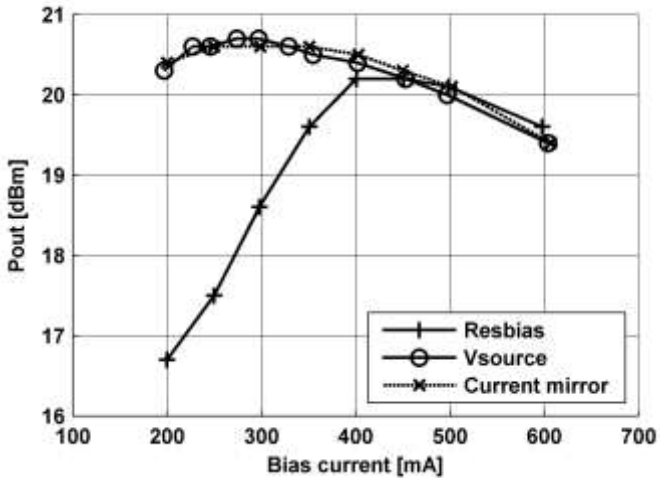

21
20
19
18
17
16
Pout [dBm]
100
200
300
400
500
600
700
Bias current [mA]
Resbias
Vsource
Current mirror

Figure 6

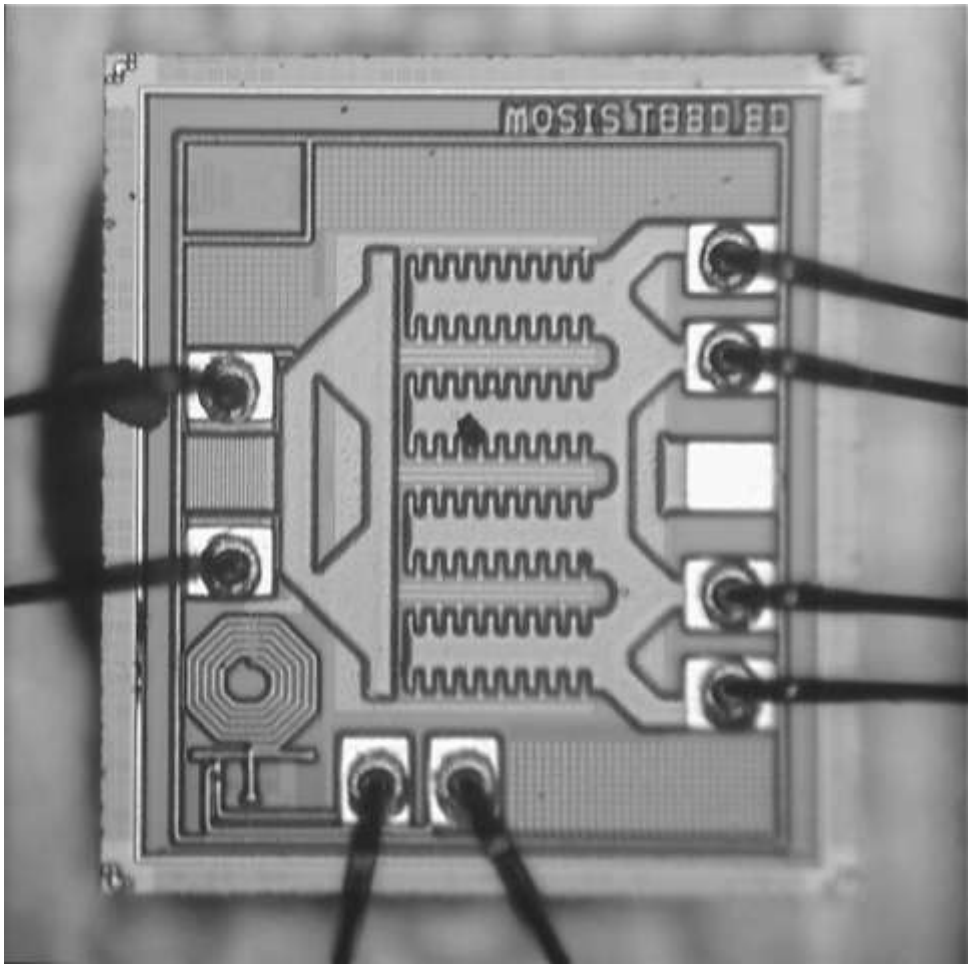


Figure 7

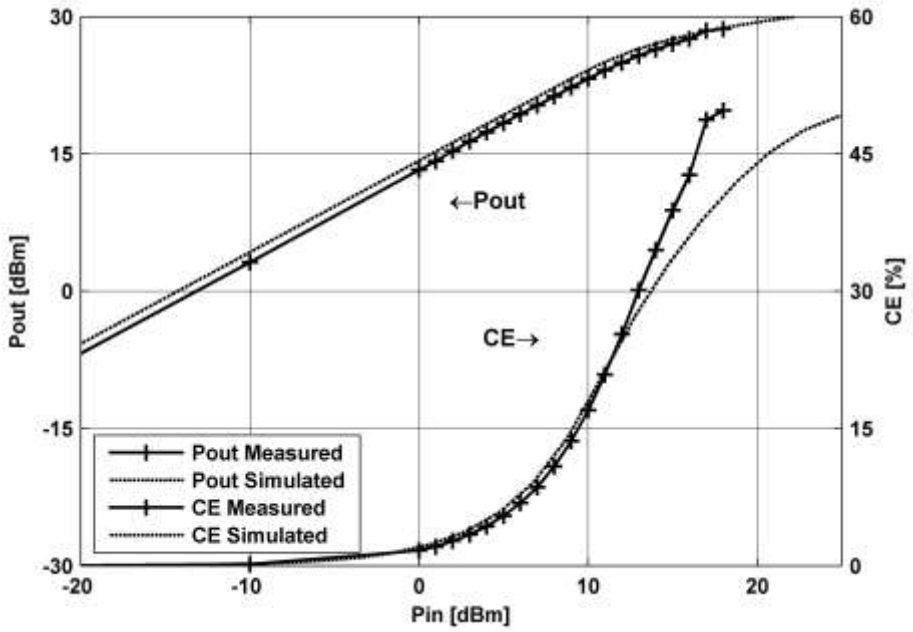
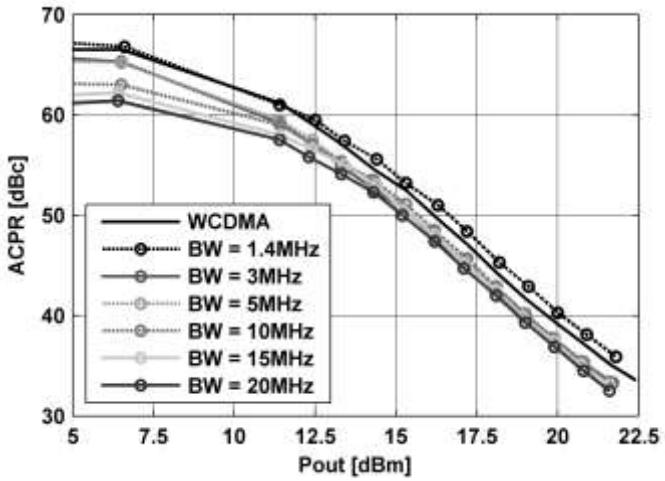

30
15
0
-15
-30
60
45
30
15
0
-20
-10
0
10
20
Pout [dBm]
CE [%]
Pin [dBm]
←Pout
CE→
Pout Measured
Pout Simulated
CE Measured
CE Simulated

Figure 8


70
60
50
40
30
ACPR [dBc]
5
7.5
10
12.5
15
17.5
20
22.5
Pout [dBm]
WCDMA
BW = 1.4MHz
BW = 3MHz
BW = 5MHz
BW = 10MHz
BW = 15MHz
BW = 20MHz