Analysis of a 5.5-V Class-D Stage Used in +30-dBm Outphasing RF PAs in 130- and 65-nm CMOS

Jonas Fritzin, Christer Svensson and Atila Alvandpour

Linköping University Post Print

N.B.: When citing this work, cite the original article.

©2012 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Jonas Fritzin, Christer Svensson and Atila Alvandpour, Analysis of a 5.5-V Class-D Stage Used in +30-dBm Outphasing RF PAs in 130- and 65-nm CMOS, 2012, IEEE Transactions on Circuits and Systems - II - Express Briefs, (59), 11, 726-730.

<http://dx.doi.org/10.1109/TCSII.2012.2228391>

Postprint available at: Linköping University Electronic Press

<http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-88467>

Analysis of a 5.5 V Class-D Stage Used in +30 dBm Outphasing RF PAs in 130nm and 65nm CMOS

Jonas Fritzin, *Member, IEEE*, Christer Svensson, *Fellow, IEEE*, and Atila Alvandpour, *Senior Member, IEEE*

Abstract—This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level, +32.0 dBm and +29.7 dBm, outphasing RF Power Amplifiers (PA) in standard 130 nm and 65 nm CMOS technologies. The Class-D stage utilizes a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V supply in the 1.2/2.5 V technologies without excessive device voltage stress. RMS electric fields (E) across the gate oxides and the optimal bias point, where the voltage stress is equally divided between the transistors, are computed. At the optimal bias point, the RMS E , the power dissipation of the parasitic drain capacitance of the common-source transistors, and the equivalent on-resistances are reduced by approximately 25 %, 50 %, and 25 %, compared to a conventional cascode (inverter) stage. To the authors' best knowledge, the Class-D PAs presented are among the first fully integrated CMOS outphasing PAs reaching +30 dBm and demonstrate state-of-the-art output power and bandwidth.

Index Terms—outphasing, CMOS, amplifier.

I. INTRODUCTION

WITH the scaling of CMOS transistors, the speed of the transistors has increased while being operated at lower supply voltages and it becomes more challenging to meet the requirement on output power (P_{out}), linearity, and efficiency in Power Amplifiers (PA). With the improved speed of CMOS transistors, highly efficient switched PAs, like Class-D/E, have gained increased interest in polar modulation [1], [2] and outphasing [3]–[10]. In the outphasing amplifier, an input signal, $s(t)$, containing both amplitude and phase modulation is divided into two constant envelope phase-modulated signals, $s_1(t)$ and $s_2(t)$, as in Fig. 1. The signals are amplified by efficient switched amplifiers, A_1 and A_2 , and connected to a combiner with strict requirements on gain/phase matching, whose output, $y(t)$, is an amplified replica of $s(t)$. With an isolating combiner, the linearity is high as the amplifiers do not interact and the seen load impedance for each amplifier is fixed. For a non-isolating combiner the amplifiers' seen load impedance varies with outphasing angle, making Class-E PAs less suitable and require predistortion [11], as the switching characteristic and constant envelope operation depend on the load impedance. A Class-D PA mitigates this as it can be considered as an ideal voltage source, independent of the load [12], thus maintaining linearity even when non-isolating combiners, e.g. transformers, are used. The output power of Class-D RF PAs has, until recently [8]–[10], been lower than

Fig. 1. (a) Outphasing concept and signal decomposition. (b) Ideal power combining of the two constant-envelope signals.

Fig. 2. (a) Cascode inverter stage used in several Class-D PAs [1], [2], [4]–[8]. In [1] and [4] non-overlapping driver signals were used. (b) The proposed Class-D stage. C_1 – C_4 are MIM capacitors. T_4 is biased for improved reliability and to be able to affect the on-resistance, r_{on} . The driver is a tapered buffer with tapering factor $\lambda = 2.5$ [9] ($\lambda = 2$ in [10]).

+30 dBm [1]–[7]. This can be explained as follows: for a given supply voltage and load resistance the P_{out} from a Class-D PA is -3.9 dB (1) lower compared to Class-A/B PAs.

$$10 \log_{10} \left(\frac{P_{out,A/B}}{P_{out,D}} \right) = 10 \log_{10} \left(\frac{V_{DD}^2 / 2R_L}{2V_{DD}^2 / \pi^2 R_L} \right) \approx -3.9 \text{ dB} \quad (1)$$

$$20 \log_{10} (5.5 / (1.2 + 2.5)) \approx 3.4 \text{ dB} \quad (2)$$

$$P_{sw,C_d} = f C_d V_{swing}^2 = f C_d V_{d,4}^2 \quad (3)$$

For higher P_{out} , either a high supply voltage or a small load impedance, i.e. a high impedance transformation ratio, is needed. A high impedance transformation ratio results in reduced bandwidth and low efficiency, especially for on-chip matching networks [13]. A high supply voltage (and swing) can be used in Class-D PAs by utilizing cascoding techniques to operate at two or three times the transistors' nominal supply voltage [1], [2], [4]–[8], [14]. In [1], [2], [4]–[8], the voltage stress on the devices is limited to the nominal supply voltage by using two supplies in the output stage and in the drivers, i.e. $2 \times V_{DD}$ and V_{DD} as shown in Fig. 2(a). However, during RF operation, the Time-Dependent Dielectric Breakdown (TDDb) is proportional to the RMS electric field (E) across the gate oxide [15], [16] and not the peak E . Thus, the capacity of the transistors may not be fully exploited.

This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level outphasing RF PAs with on-chip transformers in standard 130nm and

Manuscript received April 21, 2012;

J. Fritzin was with the Department of Electrical Engineering, Linköping University, SE-581 83 Linköping, Sweden. He is now with Radio Design at Ericsson AB, Stockholm, Sweden, phone: +46709605290, e-mail: jonas@jonasfritzin.com.

C. Svensson and A. Alvandpour are with the Department of Electrical Engineering, Linköping University, SE-581 83 Linköping, Sweden.

Fig. 3. (a) The implemented Class-D outphasing RF PA using four [9] (two [10]) transformers. (b) Operation of the Class-D stage. (c) The cascode of the NMOS transistors and associated voltages.

Fig. 4. Simulated gate, $V_{g,i}$, and drain, V_1 and V_2 , and output voltages, V_{out} , for the Class-D stage in [9], for $V_{DD2} = 5.5$ V and $V_{DD1} = 1.3$ V.

65nm CMOS technologies. The PAs, optimized for output power [9] and bandwidth [10], delivered +32.0 dBm and +29.7 dBm, respectively. The Class-D stage utilized a cascode configuration, driven by an AC-coupled low-voltage driver operating at 1.3 V, V_{DD1} , to allow a 5.5 V, V_{DD2} , supply without excessive device voltage stress. Compared to earlier works [9] and [10], expressions for RMS E across the gate oxides, the reduction in on-resistance, r_{on} , and the power dissipation of the parasitic drain capacitance of the common-source transistors in the proposed cascode stage are derived. The properties are compared with a conventional cascode (inverter) stage. The presented technique is also useful in wideband high voltage drivers for base stations [17] and to enable direct connection to the battery in more deeply scaled nanometer technologies like 45nm. The outline of the paper is as follows. Section II describes the operation of the proposed Class-D, and in Section III the properties are compared with a conventional cascode (inverter) stage. Section IV presents the design of the outphasing RF PAs, and in Section V, the measured RF performance is compared with other work. Section VI provides the conclusions.

II. OPERATION/RELIABILITY OF THE CLASS-D STAGE

A. Design and Operation of the Class-D stage

The proposed Class-D stage, denoted PA in Fig. 2(b) and Fig. 3(a), operate with a high supply voltage of 5.5 V, V_{DD2} , and utilize cascoded devices. The transistors used are 1.2 V thin-oxide devices, T_1 and T_4 , and 2.5 V thick-oxide devices, T_2 and T_3 , with t_{ox} of 2.0 nm [9] (1.8 nm [10]) and 5.0 nm, respectively. The gates of T_1 - T_4 are separated from the 1.3 V, V_{DD1} , driver stage by AC coupling capacitors, C_1 - C_4 , and biased via off-chip resistors (for flexibility of bias level). Fig. 3(b) shows the operation principle, where the gate voltages, $V_{g,1}$ - $V_{g,4}$, of the four transistors and the output voltage, V_{out} , are plotted. Fig. 3(c) shows the cascode of the NMOS transistors and associated voltages. The gate bias levels

Fig. 5. Simulated $V_{gd,i}$ and $V_{ds,i}$ voltages ($V_{DD2} = 5.5$ V, $V_{DD1} = 1.3$ V) for (a) the T_4 and (b) the T_3 device in [9].

Fig. 6. (a) The proposed Class-D stage (b) A conventional cascode (inverter) stage where the cascode device is biased at V_{bias} .

of T_1 - T_4 are assumed to be $V_{DD2}-V_{DD1}/2$, $V_{DD2}/2+V_{DD1}/2$, $V_{DD2}/2-V_{DD1}/2$, and $V_{DD1}/2$, respectively.

The simulated $V_{g,i}$ and drain, V_1 and V_2 , voltages are shown in Fig. 4(a). When the driver signal, V_x in Fig. 2(b), is high, $V_{g,3}$ is raised above the bias level and becomes $V_{DD2}/2$, reducing r_{on} of T_3 (Section III.C). When V_x is low, $V_{g,3}$ is lowered below the bias level and becomes $V_{DD2}/2-V_{DD1}$. This lowers $V_{gd,4}$ and $V_{ds,4}$ to $\approx V_{g,3}-V_{th,T3}$ if subthreshold conduction is neglected, but also increases $V_{gd,3}$ and $V_{ds,3}$. With the reduced voltage swing at $V_{d,4}$, the power consumption due to switching C_d (3) is reduced by $\approx 50\%$ similar to [18] (Section III.B). The operation of T_1 and T_2 is the same, but they are in their on-state (off-state) when T_3 and T_4 are in their off-state (on-state). Thus, by choosing suitable bias points and driving all transistors, the voltage stress can be distributed for the whole RF cycle, enabling a high supply voltage. As the PA stage does not use the sum of the transistors' nominal supply voltages, as in Fig. 6(b), a 3.4 dB larger P_{out} can be achieved (2).

B. Reliability Considerations

The reliability of CMOS transistors due to oxide degradation is especially important to consider in circuits with large voltage swings, like PAs, but the impact of RF stress is not as damaging as DC stress [19], [20]. Two major degradation mechanisms are Fowler-Nordheim tunneling, due to high E across the gate oxide, and Hot Carriers (HC), i.e. accelerated carriers in the channel [21]. During RF operation, the TDDb is proportional to the RMS E applied to the gate oxide [15], [16]. In [15], the devices had similar time to failure when RMS RF and DC stress was compared. Fig. 5 shows the simulated V_{gd} and V_{ds} for the Class-D stage in [9] (similar in [10]). The RMS E_{gd} , E_{gs} , and E_{gb} are ≈ 0.6 V/nm gate oxide, which is similar to the voltage stress in digital circuits, and is expected to result in a lifetime of more than 10 years [21].

HC stress typically occurs when V_{ds} is larger than maximum rated V_{ds} while V_{gs} is at least $V_{ds}/2$ [16]. Sign of HC stress is for example increased V_{th} . In the PAs, presented in this paper,

Fig. 7. Computed RMS E ($V_{DD2} = 5.5$ V, $V_{DD1} = 1.3$ V), for [9]: NMOS devices in (a) the proposed Class-D stage, (b) in a conventional cascode stage.

V_{ds} is high ($\approx 1.5 \times V_{DD,nom}$) when the transistors are in their off-state and V_{gs} is close to 0 V, minimizing the HC stress [14], [16]. Also, the simulated V_{ds} of the proposed Class-D stage is smaller compared to Class-AB PAs, where the cascode device is typically not driven by the driver and V_{ds} approaches $2 \times V_{DD,nom}$ [16]. The drain/well breakdown voltage of the processes used is 10 V, far from the drain voltage switching between V_{DD2} and GND . This was also seen in simulations for a wide range of impedances including open/short load.

III. ANALYSIS AND COMPARISON OF CLASS-D STAGES

A. Computed RMS Electric Fields

Assuming the drain voltage is square-wave and is pulled to either V_{DD2} or GND , the V_{gd} and V_{gs} voltages for the proposed (Fig. 6(a)) and conventional (Fig. 6(b)) Class-D stages can be expressed as in Table I. In Fig. 6(a), the gate of the cascode device is assumed to operate between $V_{bias} \pm V_{DD1}/2$. In Fig. 6(b), the gate voltage is held constant at its bias level, V_{bias} . The gate-drain, $E_{gd,T3,prop}$, and the gate-source, $E_{gs,T3,prop}$, and the gate-drain, $E_{gd,T4,prop}$, RMS E (4) in the proposed Class-D stage in Fig. 6(a) can be expressed as in (5) - (7) as a function of V_{bias} . The fields are plotted in Fig. 7(a) for [9], assuming $V_{DD2} = 5.5$ V and $V_{DD1} = 1.3$ V and $V_{th,T3} = 0$ since $V_{gs,3} = 0$ in Fig. 4(a). The corresponding fields for the conventional cascode (inverter) stage in Fig. 6(b) can be expressed as in (8) - (10). The fields are plotted in Fig. 7(b), where the supply is assumed to be the same as in the proposed Class-D stage, i.e. V_{DD2} .

$$E_{rms} = \sqrt{\frac{1}{T} \int_0^T \left| \frac{V(t)}{t_{ox}} \right|^2 dt} \quad (4)$$

$$E_{gd,T3,prop} = \frac{\sqrt{\left[\left(V_{bias} + \frac{V_{DD1}}{2} \right)^2 + \left(V_{bias} - \frac{V_{DD1}}{2} - V_{DD2} \right)^2 \right]}}{\sqrt{2} t_{ox,T3}} \quad (5)$$

$$E_{gs,T3,prop} = \frac{\sqrt{\left[\left(V_{bias} + \frac{V_{DD1}}{2} \right)^2 + V_{th,T3}^2 \right]}}{\sqrt{2} t_{ox,T3}} \quad (6)$$

$$E_{gd,T4,prop} = \frac{\sqrt{\left[\frac{V_{DD1}^2}{2} + \left(V_{bias} - \frac{V_{DD1}}{2} - V_{th,T3} \right)^2 \right]}}{\sqrt{2} t_{ox,T4}} \quad (7)$$

$$E_{gd,T3,conv} = \frac{\sqrt{\left[V_{bias}^2 + (V_{bias} - V_{DD2})^2 \right]}}{\sqrt{2} t_{ox,T3}} \quad (8)$$

$$E_{gs,T3,conv} = \frac{\sqrt{\left[V_{bias}^2 + V_{th,T3}^2 \right]}}{\sqrt{2} t_{ox,T3}} \quad (9)$$

Fig. 8. Simulated RMS E_{gd} over supply voltage, V_{DD2} , for the PA in [9] when: (a) all transistors, i.e. T_1 - T_4 , as in Fig. 6(a) and (b) only the thin-oxide devices, T_1 and T_4 , as in Fig. 6(b) are driven by the driver.

$$E_{gd,T4,conv} = \frac{\sqrt{\left[\frac{V_{DD1}^2}{2} + (V_{bias} - V_{th,T3})^2 \right]}}{\sqrt{2} t_{ox,T4}} \quad (10)$$

$$\frac{P_{sw,Cd,prop}(V_{bias})}{P_{sw,Cd,conv}(V_{bias})} = \frac{\left(V_{bias} - \frac{V_{DD1}}{2} - V_{th,T3} \right)^2}{(V_{bias} - V_{th,T3})^2} \quad (11)$$

$$r_{on} = \frac{1}{\left(\frac{\mu C_{ox} W (V_{gs} - V_{th})}{L} \right)} = \frac{1}{\left(\frac{\mu e_r e_r W (V_{gs} - V_{th})}{t_{ox} L} \right)} \quad (12)$$

$$\frac{r_{on,T3,prop}(V_{bias}) + r_{on,T4,prop}}{r_{on,T3,conv}(V_{bias}) + r_{on,T4,conv}} = \frac{\frac{t_{ox,T3} L T_3}{W T_3 (V_{bias} + \frac{V_{DD1}}{2})} + \frac{t_{ox,T4} L T_4}{W T_4 V_{DD1}}}{\frac{t_{ox,T3} L T_3}{W T_3 V_{bias}} + \frac{t_{ox,T4} L T_4}{W T_4 V_{DD1}}} \quad (13)$$

$$r_{on,ratio,T3} = \frac{r_{on,T3,prop}(V_{bias})}{r_{on,T3,conv}(V_{bias})} = \frac{V_{bias}}{V_{bias} + \frac{V_{DD1}}{2}} \quad (14)$$

The optimal bias points where the life-time of the devices is optimized (assuming thin and thick gate oxide devices have the same characteristics regarding voltage stress), are marked with a circle. The value of $V_{bias,opt}$ is 2.11 V for [9] (1.88 V for [10]) and corresponds well to the ideal bias point of 2.1 V ($V_{DD2}/2 - V_{DD1}/2$). The figure shows that in the proposed Class-D stage, a significantly higher bias level of the cascode device can be used while still having comparable RMS E between the gate-drain and gate-source, enabling the use of a high supply voltage. Thus, if only T_1 and T_4 are driven by the driver as in Fig. 6(b), either a lower V_{DD2} or bias levels $> V_{DD2}/2 + V_{DD1}/2$ for T_2 (or $< V_{DD2}/2 - V_{DD1}/2$ for T_3) must be used to reduce the oxide stress. Reducing the supply voltage or adjusting the bias voltages, i.e. reducing voltage swing and increasing r_{on} , lower the P_{out} . Increasing transistor widths would reduce r_{on} , but introduce more capacitive losses.

Fig. 8(a) shows simulated RMS E_{gd} over V_{DD2} for the PA in [9] and the proposed Class-D stage in Fig. 6(a) (0.6 V/nm is indicated with a dashed line). Fig. 8(b) shows the corresponding simulated E when only T_1 and T_4 are driven by the driver as in Fig. 6(b). Fig. 8(b) shows that RMS E are about 25 % higher reducing the predicted oxide lifetime by more than a factor of 10 [15]. For a V_{DD2} larger than 4 V, the difference in P_{out} is ≈ 0.5 dB. Lowering the bias level to 1.3 V, the reduction in P_{out} is ≈ 1 dB. The results demonstrate the benefits of the proposed Class-D stage in terms of reduced device voltage stress and higher P_{out} compared to a conventional cascode stage.

Fig. 9. Ratio of (a) the power dissipation of the drain capacitance and (b) the r_{on} in the proposed Class-D stage compared to the conventional cascode stage for [9]. ($V_{DD2} = 5.5$ V, $V_{DD1} = 1.3$ V).

B. Power consumption reduction of C_d in the CS stage

As shown in Fig. 6(a) and Fig. 6(b), $V_{d,4}$ is reduced in the proposed Class-D stage. With the reduced swing, the power consumption due to charging and discharging the parasitic drain capacitance, C_d , of T_4 is reduced as seen in (3). In (11), plotted in Fig. 9(a) using Table I and assuming $V_{th} = 0$, the ratio of the power consumption, due to switching C_d in the proposed Class-D stage and in the conventional cascode stage is mathematically expressed as a function of the bias level, V_{bias} . For bias levels above $V_{DD1}/2$, the power consumption due to the parasitic drain capacitance is reduced. At the optimal bias point, $V_{bias,opt}$, the ratio is ≈ 0.48 [9] (0.43 [10]), thus the power consumption is reduced by 52 % [9] (57 % [10]) compared to the conventional cascode stage. Taking into account that the drain capacitance of the thick-oxide devices are charged to 5.5 V each RF cycle, the overall power reduction is 5-10 %. Notice that the same bias level wouldn't be possible in the conventional cascode stage due to the higher level of voltage stress if the expected life-time should remain the same.

Even if the power consumption due to charging/discharging the drain cap of T_1 and T_4 is reduced, it does not include C_d of T_2 and T_3 . The technique presented in [22] lead to suppression of the third harmonic and higher drain efficiency, no short-circuit power dissipation, reduced impact of the drain capacitance, but the fundamental tone is reduced and therefore that approach was not used. The technique presented in this paper is not only applicable when using a 5.5 V supply, but also in deeply scaled CMOS technologies like 45nm [23]. Assuming thin and thick gate oxide devices with t_{ox} of 1.5 nm and 3.0 nm and a 1.0 V voltage driver, a 3.0 V supply (V_{DD2}) can be used to achieve RMS E of ≈ 0.6 -0.7 V/nm if $V_{bias} = V_{DD2}/2$. ~ 3.0 V is a reasonable battery voltage [23], enabling direct connection of the PA to the battery instead using voltage converters. However, if a supply voltage larger than 3.0 V is desirable, e.g. 5.5 V, a DC-DC converter is needed.

C. On-resistance reduction

With the proposed Class-D stage, r_{on} (12) is reduced compared to the conventional cascode stage as $V_{g,3}$ is raised above its bias level. The ratio of the equivalent r_{on} , i.e. the sum of r_{on} of T_3 and T_4 , for the proposed and conventional cascode stages are computed in (13) and plotted in Fig. 9(b) using Table II. The ratio of the r_{on} of T_3 is also plotted with a dashed line according to (14). The ratios are smaller for low bias levels, but at $V_{bias,opt}$, the equivalent r_{on} ratios for [9] are 0.81 and 0.76, respectively, i.e. a reduction of the equivalent

r_{on} by 19 % and the r_{on} of the cascode device by 24 %. The corresponding reductions in r_{on} for [10] are 23 % and 26 %. Thus, for the same r_{on} , the proposed Class-D stage requires smaller devices, reducing associated losses and area.

IV. DESIGN OF THE OUTPHASING RF PAS

For a high voltage swing and high P_{out} in the PAs in Fig. 3(a), the Class-D stage are combined using 1:1 on-chip transformers, TR . The PAs, optimized for P_{out} [9] and bandwidth [10], used four and two transformers. Under TR floating metal shields were placed in M_1 and M_2 to reduce the losses [24], but the optimal effect is obtained at maximum P_{out} , i.e. as the Class-D output operate on complementary signals. Simulations of [10] showed a 1.2 dB higher P_{out} and a ≈ 30 % relatively higher efficiency with the floating shields than without. Tuning capacitors were placed at the primary windings in [9] to reduce the losses. In [10], the inductance of the transformer and transistor sizes (and associated capacitances) were optimized at 1.95 GHz to omit the MIM tuning capacitors with a maximum allowed voltage of 5.5 V (10 V in [9]), potentially causing reliability issues with the 5.5 V supply, V_{DD2} . The top/bottom plates of the capacitors were connected to V_{DD2}/GND [9] (V_{DD2}/V_{DD1} [10]).

V. MEASUREMENT RESULTS

The measurement setup is shown in Fig. 10. 5.5 V comes from an off-chip power supply and was chosen by using the derived equations and by sweeping the bias level to achieve an E of ≈ 0.6 -0.7 V/nm gate oxide and provide reasonable life-time. P_{out} was +32.0 dBm [9] with a DE and PAE of 20.1 % and 15.3 %, including all drivers, at 1.85 GHz. P_{out} was +29.7 dBm [10] at 5.5 V (+30.5 dBm at 6.0 V) with a DE and PAE of 30.2 % and 26.6 % at 1.95 GHz. The PAs had a 3 dB bandwidth of 0.9 GHz (1.2-2.1 GHz) [9] and 1.6 GHz (1.2-2.8 GHz) [10], respectively. The measured P_{out} and efficiency are 10 % lower than the simulated performance at 65 °C, incl. S-parameters of EM-simulated transformers and layout parasitics. The PA performance over temperature has not been characterized in measurements, but in simulations the relative changes in P_{out} and efficiencies were < 15 % between 25 and 125 °C. Table III lists published state-of-the-art fully integrated CMOS Class-D PAs. The PAs present state-of-the-art P_{out} [9] and bandwidth [10], comparable with [8], but larger than other PAs with state-of-the-art bandwidths (1.3 GHz) [25]. Modulation/spectral requirements were met for uplink WCDMA/LTE [9], [10].

TABLE I
VGD AND VGS IN THE PROPOSED (PROP.) AND
THE CONVENTIONAL (CONV.) CLASS-D STAGE

Prop.	V_x high ($V_x = V_{DD1}$)	V_x low ($V_x = 0 = GND$)
T_3 : V_{gd}	$(V_{bias} + V_{DD1}/2) - (0)$	$(V_{bias} - V_{DD1}/2) - (V_{DD2})$
T_3 : V_{gs}	$(V_{bias} + V_{DD1}/2) - (0)$	$(V_{bias} - V_{DD1}/2) - (V_{bias} - V_{DD1}/2 - V_{th,T_3})$
T_4 : V_{gd}	$(V_{DD1}) - (0)$	$(0) - (V_{bias} - V_{DD1}/2 - V_{th,T_3})$
Conv.	V_x high ($V_x = V_{DD1}$)	V_x low ($V_x = 0 = GND$)
T_3 : V_{gd}	$(V_{bias}) + (0)$	$(V_{bias}) - (V_{DD2})$
T_3 : V_{gs}	$(V_{bias}) - (0)$	$(V_{bias}) - (V_{bias} - V_{th,T_3})$
T_4 : V_{gd}	$(V_{DD1}) - (0)$	$(0) - (V_{bias} - V_{th,T_3})$

Fig. 10. Measurement setup with two SMBV signal generators.

In an initial reliability assessment [10] two devices were continuously operated for 168 h without performance degradation in P_{out} or efficiency. Thus, the 5.5 V supply does not seem have to any direct impact on device reliability. The required life-time has to be put in relation to the employed standard (e.g. 2G GSM has a 12.5% duty cycle) and an expected user case. Presuming 4 h talk time a day for 1.5 years (estimated life-time of a handset) [23] corresponds to ≈ 275 h ($365 \cdot 1.5 \cdot 4 \cdot 0.125$) of continuous PA operation. WLAN products may experience similar effective operating times, where a test time of 168 h at elevated supply voltage is considered to cover more than five years of product reliability [16].

VI. CONCLUSIONS

This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level outphasing RF Power Amplifiers (PA) in standard 1.2/2.5 V 130nm and 65nm CMOS technologies. The Class-D stage utilizes a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V supply without excessive device voltage stress. The properties are compared with a conventional cascode (inverter) stage. To the authors' best knowledge, the Class-D PAs presented are among the first fully integrated CMOS outphasing PAs reaching +30 dBm of output power and demonstrate state-of-the-art output power and bandwidth.

REFERENCES

- [1] S. Yoo, J. Walling, E. Woo, and D. Allstot, "A Switched-Capacitor Power Amplifier for EER/Polar Transmitters," in *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 427–428.

TABLE II

TRANSISTOR WIDTHS AND LENGTHS

Transistor widths and lengths	+32 dBm PA	+30 dBm PA
T_1 : W (μm), L (nm), t_{ox} (nm)	5000, 130, 2	2850, 65, 1.8
T_2 : W (μm), L (nm), t_{ox} (nm)	5000, 280, 5	2600, 280, 5
T_3 : W (μm), L (nm), t_{ox} (nm)	2000, 280, 5	2550, 280, 5
T_4 : W (μm), L (nm), t_{ox} (nm)	2000, 130, 2	2230, 65, 1.8

TABLE III

COMPARISON OF CMOS CLASS-D AND OUTPHASING RF PAs

	P_{out} [dBm]	V_{DD} [V]	DE [%]	PAE [%]	f [GHz]	Tech. [nm]	BW [GHz]
2010 [6]	+25.1	2.0	-	40.6	2.40	32	> 1.0
2011 [1]	+25.2	2.5	-	55.2	2.25	90	1.0
2011 [2]	+25.2	3.0	-	45.0	2.25	90	> 1.2
2011 [5]	+25.3	2.0	-	40.6	2.40	32	> 1.0
2011 [4]	+27.0	2.0	-	26.0	2.40	90	> 0.7
2009 [7]	+28.1	2.4	-	19.7	2.25	45	0.6
2011 [10]	+29.7	5.5	30.2	26.6	1.95	65	1.6
	+30.5	6.0	29.7	26.5	1.95	65	1.6
2011 [8]	+31.5	2.4	-	27.0	2.40	45	1.7
2011 [9]	+32.0	5.5	20.1	15.3	1.85	130	0.9

- [2] S. Yoo, J. Walling, E. Woo, B. Jann, and D. Allstot, "A Switched-Capacitor Power Amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
- [3] J. Fritzin, Y. Jung, P. Landin, P. Händel, M. Enqvist, and A. Alvandpour, "Phase Predistortion of a Class-D Outphasing RF Amplifier in 90nm CMOS," *IEEE Trans. Circuits Syst.-II: Express Briefs*, vol. 58, no. 10, pp. 642–646, Oct. 2011.
- [4] S.-M. Yoo, J. Walling, E. Woo, and D. Allstot, "A Power-Combined Switched-Capacitor Power Amplifier in 90nm CMOS," in *IEEE Radio Freq. Integrated Circuits Symp. (RFIC)*, Jun. 2011.
- [5] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. El-Tanani, and K. Soumyanath, "A Flip-Chip-Packaged 25.3 dBm Class-D Outphasing Power Amplifier in 32 nm CMOS for WLAN Application," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.
- [6] H. Xu, Y. Palaskas, A. Ravi, and K. Soumyanath, "A Highly Linear 25dBm Outphasing Power Amplifier in 32nm CMOS for WLAN Application," in *IEEE Europ. Solid-State Circ. Conf.*, Sep. 2010, pp. 306–309.
- [7] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. Elmala, and K. Soumyanath, "A 28.1dBm class-D Outphasing Power Amplifier in 45nm LP Digital CMOS," in *VLSI Symp.*, Jun. 2009, pp. 206–207.
- [8] W. Tai, H. Xu, A. Ravi, H. Lakdawala, O. Degani, L. Carley, and Y. Palaskas, "A +31.5dBm Outphasing Class-D Power Amplifier in 45nm CMOS with Back-Off Efficiency Enhancement by Dynamic Power Control," in *IEEE ESSCIRC*, Sep. 2011, pp. 131–134.
- [9] J. Fritzin, C. Svensson, and A. Alvandpour, "A +32dBm 1.85GHz Class-D Outphasing RF PA in 130nm CMOS for WCDMA/LTE," in *IEEE Europ. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2011, pp. 127–130.
- [10] —, "A Wideband Fully Integrated +30dBm Class-D Outphasing RF PA in 65nm CMOS," in *IEEE Int. Symp. Integr. Circ. (ISIC)*, Dec. 2011.
- [11] R. Beltran, F. Raab, and A. Velazquez, "HF Outphasing Transmitter Using Class-E Power Amplifiers," in *IEEE Microw. Symp. (IMS)*, Jul. 2009, pp. 757–760.
- [12] J. Yao and S. Long, "Power Amplifier Selection for LINC Application," *IEEE Trans. Circuits Syst.-II: Express Briefs*, vol. 53, no. 8, pp. 763–766, Aug. 2006.
- [13] I. Aoki, S. Kee, D. Rutledge, and A. Hajimiri, "Distributed Active Transformer - New Power-Combining and Impedance-Transformation Technique," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 1, pp. 316–331, Jan. 2002.
- [14] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A High-Voltage Output Driver in a 2.5-V 0.25- μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576–583, Mar. 2005.
- [15] L. Larcher, D. Sanzogni, R. Brama, A. Mazzanti, and F. Svelto, "Oxide Breakdown After RF Stress: Experimental Analysis and Effects on Power Amplifier Operation," in *IEEE IRPS*, Mar. 2006, pp. 283–288.
- [16] M. Ruberto, O. Degani, S. Wail, A. Tendler, A. Fridman, and G. Goltzman, "A Reliability-Aware Power Amplifier Design for CMOS Radio Chip Integration," in *IEEE IRPS*, Jul. 2008, pp. 536–540.
- [17] D. Calvillo-Cortes, M. Acar, M. v.d. Heijden, M. Apostolidou, L. Vreede, D. Leenaerts, and J. Sonky, "A 65nm CMOS Pulse-Width-Controlled Driver with 8Vpp Output Voltage for Switch-Mode RF PAs up to 3.6 GHz," in *ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 58–59.
- [18] J. Lindstrand, C. Bryant, M. Törmänen, and H. Sjöland, "A 1.6-2.6GHz 29dBm Injection-Locked Power Amplifier with 64% peak PAE in 65nm CMOS," in *IEEE ESSCIRC*, Sep. 2011, pp. 299–302.
- [19] C. Yu and J. Yuan, "MOS RF Reliability Subject to Dynamic Voltage Stress - Modeling and Analysis," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1751–1758, Aug. 2005.
- [20] J. Yuan and J. Ma, "Evaluation of RF-stress Effect on Class-E MOS Power Amplifier Efficiency," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 430–434, Jan. 2008.
- [21] W. Chan and J. Long, "A 58-65 GHz Neutralized CMOS Power Amplifier With PAE Above 10% at 1-V Supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.
- [22] J. Fritzin, C. Svensson, and A. Alvandpour, "Design and Analysis of a Class-D Stage with Harmonic Suppression," *IEEE Trans. Circuits Syst.-I: Regular Papers*, vol. 59, no. 6, pp. 1178–1186, Jun. 2012.
- [23] Int. Tech. Roadmap for Semiconductors (ITRS) 2007: Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications.
- [24] T. Cheung and J. Long, "Shielded Passive Devices for Silicon-Based Monolithic Microwave and Millimeter-Wave Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1183–1200, Sep. 2006.
- [25] S. Kousai and A. Hajimiri, "An Octave-Range, Watt-Level, Fully-Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off-Efficiency Improvement," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3376–3392, Dec. 2009.