Analysis of a 5.5-V Class-D Stage Used in +30-dBm Outphasing RF PAs in 130- and 65-nm CMOS

Jonas Fritzin, Christer Svensson and Atila Alvandpour

Linköping University Post Print

N.B.: When citing this work, cite the original article.

©2012 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Jonas Fritzin, Christer Svensson and Atila Alvandpour, Analysis of a 5.5-V Class-D Stage Used in +30-dBm Outphasing RF PAs in 130- and 65-nm CMOS, 2012, IEEE Transactions on Circuits and Systems - II - Express Briefs, (59), 11, 726-730.
http://dx.doi.org/10.1109/TCSII.2012.2228391
Postprint available at: Linköping University Electronic Press
http://urn.kb.se/resolve?urn=urn:nbn:se:liu:diva-88467
Analysis of a 5.5 V Class-D Stage Used in +30 dBm Outphasing RF PAs in 130nm and 65nm CMOS

Jonas Fritzin, Member, IEEE, Christer Svensson, Fellow, IEEE, and Atila Alvandpour, Senior Member, IEEE

Abstract—This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level, +320.0 dBm and +297.7 dBm, outphasing RF Power Amplifiers (PA) in standard 130 nm and 65 nm CMOS technologies. The Class-D stage utilizes a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V supply in the 1.2/2.5 V technologies without excessive device voltage stress. RMS electric fields ($E$) across the gate oxides and the optimal bias point, where the voltage stress is equally divided between the transistors, are computed. At the optimal bias point, the RMS $E$, the power dissipation of the parasitic drain capacitance of the common-source transistors, and the equivalent on-resistances are reduced by approximately 25 %, 50 %, and 25 %, compared to a conventional cascade (inverter) stage. To the authors’ best knowledge, the Class-D PAs presented are among the first to a conventional cascode (inverter) stage. The output power of transistors, are computed. At the optimal bias point, the RMS $E$, the power dissipation of the parasitic drain capacitance of the common-source transistors, and the equivalent on-resistances are reduced by approximately 25 %, 50 %, and 25 %, compared to a conventional cascade (inverter) stage. To the authors’ best knowledge, the Class-D PAs presented are among the first to a conventional cascode (inverter) stage. The output power of transistors, are computed. At the optimal bias point, the RMS $E$, the power dissipation of the parasitic drain capacitance of the common-source transistors, and the equivalent on-resistances are reduced by approximately 25 %, 50 %, and 25 %, compared to a conventional cascade (inverter) stage. To the authors’ best knowledge, the Class-D PAs presented are among the first to a conventional cascode (inverter) stage.

Index Terms—outphasing, CMOS, amplifier.

I. INTRODUCTION

With the scaling of CMOS transistors, the speed of the transistors has increased while being operated at lower supply voltages and it becomes more challenging to meet the requirement on output power ($P_{out}$), linearity, and efficiency in Power Amplifiers (PA). With the improved speed of CMOS transistors, highly efficient switched PAs, like Class-D/E, have gained increased interest in polar modulation [1], [2] and outphasing [3]–[10]. In the outphasing amplifier, an input signal, $s(t)$, containing both amplitude and phase modulation is divided into two constant envelope phase-modulated signals, $s_1(t)$ and $s_2(t)$, as in Fig. 1. The signals are amplified by efficient switched amplifiers, $A_1$ and $A_2$, and connected to a combiner with strict requirements on gain/phase matching, whose output, $y(t)$, is an amplified replica of $s(t)$. With an isolating combiner, the linearity is high as the amplifiers do not interact and the seen load impedance for each amplifier is fixed. For a non-isolating combiner the amplifiers’ seen load impedance varies with outphasing angle, making Class-E PAs less suitable and require predistortion [11], as the switching characteristic and constant envelope operation depend on the load impedance. A Class-D PA mitigates this as it can be considered as an ideal voltage source, independent of the load [12], thus maintaining linearity even when non-isolating combiners, e.g. transformers, are used. The output power of Class-D RF PAs has, until recently [8]–[10], been lower than +30 dBm [1]–[7]. This can be explained as follows: for a given supply voltage and load resistance the $P_{out}$ from a Class-D PA is -3.9 dB (1) lower compared to Class-A/B PAs.

\[
10 \log_{10} \left( \frac{P_{out,A/B}}{P_{out,D}} \right) = 10 \log_{10} \left( \frac{V_{DD}^2}{2RL} \right) \approx -3.9 \text{ dB (1)}
\]

\[
20 \log_{10} (5.5/((1.2 + 2.5))) \approx 3.4 \text{ dB (2)}
\]

For higher $P_{out}$, either a high supply voltage or a small load impedance, i.e. a high impedance transformation ratio, is needed. A high impedance transformation ratio results in reduced bandwidth and low efficiency, especially for on-chip matching networks [13]. A high supply voltage (and swing) can be used in Class-D PAs by utilizing cascading techniques to operate at two or three times the transistors’ nominal supply voltage [1], [2], [4]–[8], [14]. In [1], [2], [4]–[8], the voltage stress on the devices is limited to the nominal supply voltage by using two supplies in the output stage and in the drivers, i.e. $2xV_{DD}$ and $V_{DD}$ as shown in Fig. 2(a). However, during RF operation, the Time-Dependent Dielectric Breakdown (TDDB) is proportional to the RMS electric field ($E$) across the gate oxide [15], [16] and not the peak $E$. Thus, the capacity of the transistors may not be fully exploited.

This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level outphasing RF PAs with on-chip transformers in standard 130nm and...
65nm CMOS technologies. The PAs, optimized for output power [9] and bandwidth [10], delivered +32.0 dBm and +29.7 dBm, respectively. The Class-D stage utilized a cascode configuration, driven by an AC-coupled low-voltage driver operating at 1.3 V, \( V_{DD1} \), to allow a 5.5 V, \( V_{DD2} \), supply without excessive device voltage stress. Compared to earlier works [9] and [10], expressions for RMS \( E \) across the gate oxides, the reduction in on-resistance, \( r_{on} \), and the power dissipation of the parasitic drain capacitance of the common-source transistors in the proposed cascode stage are derived. The properties are compared with a conventional cascode (inverter) stage. The presented technique is also useful in wideband high voltage drivers for base stations [17] and to enable direct connection to the battery in more deeply scaled nanometer technologies like 45nm. The outline of the paper is as follows. Section II describes the operation of the proposed Class-D, and in Section III the properties are compared with a conventional cascode (inverter) stage. Section IV presents the design of the outphasing RF PAs, and in Section V, the measured RF performance is compared with other work. Section VI provides the conclusions.

II. OPERATION/RELIABILITY OF THE CLASS-D STAGE

A. Design and Operation of the Class-D stage

The proposed Class-D stage, denoted PA in Fig. 2(b) and Fig. 3(a), operate with a high supply voltage of 5.5 V, \( V_{DD2} \), and utilize cascode devices. The transistors used are 1.2 V thin-oxide devices, \( T_1 \) and \( T_4 \), and 2.5 V thick-oxide devices, \( T_2 \) and \( T_3 \), with \( t_{ox} \) of 2.0 nm [9] (1.8 nm [10]) and 5.0 nm, respectively. The gates of \( T_1-T_4 \) are separated from the 1.3 V, \( V_{DD1} \), driver stage by AC coupling capacitors, \( C_1-C_4 \), and biased via off-chip resistors (for flexibility of bias level). Fig. 3(b) shows the operation principle, where the gate voltages, \( V_{g1}-V_{g4} \), of the four transistors and the output voltage, \( V_{out} \), are plotted. Fig. 3(c) shows the cascode of the NMOS transistors and associated voltages. The gate bias levels of \( T_1-T_4 \) are assumed to be \( V_{DD2}-V_{DD1}/2 \), \( V_{DD2}/2+V_{DD1}/2 \), \( V_{DD2}/2-V_{DD1}/2 \), and \( V_{DD1}/2 \), respectively.

The simulated \( V_{gd} \), and drain, \( V_1 \) and \( V_2 \), voltages are shown in Fig. 4(a). When the driver signal, \( V_x \) in Fig. 2(b), is high, \( V_{g3} \) is raised above the bias level and becomes \( V_{DD2}/2 \), reducing \( r_{on} \) of \( T_3 \) (Section III.C). When \( V_x \) is low, \( V_{g3} \) is lowered below the bias level and becomes \( V_{DD2}/2-V_{DD1}/2 \). This lowers \( V_{gd} \) and \( V_{ds} \) to \( \approx V_{g3}+V_{th} \) if subthreshold conduction is neglected, but also increases \( V_{gd,3} \) and \( V_{ds,3} \). With the reduced voltage swing at \( V_{d,4} \), the power consumption due to switching \( C_3 \) is reduced by \( \approx 50 \% \) similar to [18] (Section III.B). The operation of \( T_1 \) and \( T_2 \) is the same, but they are in their on-state (off-state) when \( T_3 \) and \( T_4 \) are in their off-state (on-state). Thus, by choosing suitable bias points and driving all transistors, the voltage stress can be distributed for the whole RF cycle, enabling a high supply voltage. As the PA stage does not use the sum of the transistors’ nominal supply voltages, as in Fig. 6(b), a 3.4 dB larger \( P_{out} \) can be achieved (2).

B. Reliability Considerations

The reliability of CMOS transistors due to oxide degradation is especially important to consider in circuits with large voltage swings, like PAs, but the impact of RF stress is not as damaging as DC stress [19], [20]. Two major degradation mechanisms are Fowler-Nordheim tunneling, due to high \( E \) across the gate oxide, and Hot Carriers (HC), i.e. accelerated carriers in the channel [21]. During RF operation, the TDDB is proportional to the RMS \( E \) applied to the gate oxide [15], [16]. In [15], the devices had similar time to failure when RMS RF and DC stress was compared. Fig. 5 shows the simulated \( V_{gd} \) and \( V_{ds} \) for the Class-D stage in [9] (similar in [10]). The RMS \( E_{gd}, E_{gs} \), and \( E_{gb} \) are \( \approx 0.6 \) V/nm gate oxide, which is similar to the voltage stress in digital circuits, and is expected to result in a lifetime of more than 10 years [21].

HC stress typically occurs when \( V_{ds} \) is larger than maximum rated \( V_{ds} \) while \( V_{gs} \) is at least \( V_{ds}/2 \) [16]. Sign of HC stress is for example increased \( V_{th} \). In the PAs, presented in this paper,
\(V_{ds}\) is high \((\approx 1.5 \times V_{DD,nom})\) when the transistors are in their off-state and \(V_{gs}\) is close to 0 V, minimizing the HC stress \([14], [16]\). Also, the simulated \(V_{ds}\) of the proposed Class-D stage is smaller compared to Class-AB PAs, where the cascode device is typically not driven by the driver and \(V_{ds}\) approaches \(2 \times V_{DD,nom}\) \([16]\). The drain/well breakdown voltage of the processes used is 10 V, far from the drain voltage switching between \(V_{DD2}\) and \(GND\). This was also seen in simulations for a wide range of impedances including open/short load.

III. ANALYSIS AND COMPARISON OF CLASS-D STAGES

A. Computed RMS Electric Fields

Assuming the drain voltage is square-wave and is pulled to either \(V_{DD2}\) or \(GND\), the \(V_{gd}\) and \(V_{gs}\) voltages for the proposed (Fig. 6(a)) and conventional (Fig. 6(b)) Class-D stages can be expressed as in Table I. In Fig. 6(a), the gate of the cascode device is assumed to operate between \(V_{DD2}\) \(\pm V_{DD1}/2\). In Fig. 6(b), the gate voltage is held constant at its bias level, \(V_{bias}\). The gate-drain, \(E_{gd,T3,prop}\), and the gate-source, \(E_{gs,T3,prop}\), and the gate-drain, \(E_{gd,T4,prop}\), RMS \(E\) (4) in the proposed Class-D stage in Fig. 6(a) can be expressed as in (5) - (7) as a function of \(V_{bias}\). The fields are plotted in Fig. 7(a) for [9], assuming \(V_{DD2} = 5.5\) V and \(V_{DD1} = 1.3\) V and \(V_{th,T3} = 0\) since \(V_{gs,3} = 0\) in Fig. 4(a). The corresponding fields for the conventional cascode (inverter) stage in Fig. 6(b) can be expressed as in (8) - (10). The fields are plotted in Fig. 7(b), where the supply is assumed to be the same as in the proposed Class-D stage, i.e. \(V_{DD2}\).

\[
E_{rms} = \sqrt{\frac{1}{T} \int_0^T |V(t)|^2 dt}
\]

\[
E_{gd,T3,prop} = \frac{\left(V_{bias} + \frac{V_{DD1}}{2}\right)^2 + \left(V_{bias} - \frac{V_{DD1}}{2} - V_{DD2}\right)^2}{2 \omega_{ox,T3}}
\]

\[
E_{gs,T3,prop} = \frac{\left(V_{bias} + \frac{V_{DD1}}{2}\right)^2 + V_{th,T3}^2}{2 \omega_{ox,T3}}
\]

\[
E_{gd,T4,prop} = \frac{\left(V_{bias} + \frac{V_{DD1}}{2}\right)^2 + \left(V_{bias} - \frac{V_{DD1}}{2} - V_{DD2}\right)^2}{2 \omega_{ox,T4}}
\]

\[
E_{gs,T4,prop} = \frac{\left(V_{bias}^2 + (V_{bias} - V_{DD2})^2\right)}{2 \omega_{ox,T4}}
\]

\[
E_{gd,T3,conv} = \frac{V_{bias}^2 + (V_{bias} - V_{DD2})^2}{2 \omega_{ox,T3}}
\]

\[
E_{gs,T3,conv} = \frac{V_{bias}^2 + V_{th,T3}^2}{2 \omega_{ox,T3}}
\]

The optimal bias points where the life-time of the devices is optimized (assuming thin and thick gate oxide devices have the same characteristics regarding voltage stress), are marked with a circle. The value of \(V_{bias, opt}\) is 2.11 V for [9] (1.88 V for [10]) and corresponds well to the ideal bias point of 2.1 V (\(V_{DD2}/2 - V_{DD1}/2\)). The figure shows that in the proposed Class-D stage, a significantly higher bias level of the cascode device can be used while still having comparable RMS \(E\) between the gate-drain and gate-source, enabling the use of a high supply voltage. Thus, if only \(T1\) and \(T4\) are driven by the driver as in Fig. 6(b), either a lower \(V_{DD2}\) or bias levels \(> V_{DD2}/2 + V_{DD1}/2\) for \(T2\) (or \(< V_{DD2}/2 - V_{DD1}/2\) for \(T3\)) must be used to reduce the oxide stress. Reducing the supply voltage or adjusting the bias voltages, i.e. reducing voltage swing and increasing \(r_{on}\), lower the \(I_{out}\). Increasing transistor widths would reduce \(r_{on}\), but introduce more capacitive losses.

\[
\frac{\mu_{Cox} W(V_{gs} - V_{th})}{2} = \frac{1}{L} \left(\frac{\mu_{Cox} W(V_{gs} - V_{th})}{2} \right) + \frac{\mu_{Cox} W(V_{gs} - V_{th})}{2}
\]

\[
\frac{r_{on,prop}}{r_{on,conv}} = \frac{r_{on,T3,prop}(V_{bias})}{r_{on,T3,conv}(V_{bias})} = \frac{W_{T3} + V_{DD1}/2}{W_{T3} + V_{DD1}/2} + \frac{W_{T3} + V_{DD1}/2}{W_{T3} + V_{DD1}/2}
\]

Fig. 8(a) shows simulated RMS \(E_{gd}\) over supply voltage, \(V_{DD2}\), for the PA in [9] when: (a) all transistors, i.e. \(T1\) and \(T4\), as in Fig. 6(a) and (b) only the thin-oxide devices, \(T1\) and \(T4\), as in Fig. 6(b) are driven by the driver.

\[
E_{gd,T4,conv} = \frac{\left(V_{bias} + \frac{V_{DD1}}{2}\right)^2 + \left(V_{bias} - \frac{V_{DD1}}{2} - V_{DD2}\right)^2}{2 \omega_{ox,T4}}
\]

\[
P_{out,prop}(V_{bias}) = \left(V_{bias} - V_{DD2}/2 - V_{DD1}/2\right)^2
\]

The results demonstrate the benefits of the proposed Class-D stage in terms of reduced device voltage stress and higher \(P_{out}\) compared to a conventional cascode stage.
C. On-resistance reduction

The ratio of the equivalent on-resistance, $r_{on}$, for the proposed Class-D stage compared to the conventional cascode stage is 0.81 and 0.76, respectively, i.e. a reduction of the equivalent on-resistance by 19% and the on-resistance of the cascode device by 24%. The corresponding reductions in $r_{on}$ for [10] are 23% and 26%. Thus, for the same $r_{on}$, the proposed Class-D stage requires smaller devices, reducing associated losses and area.

IV. DESIGN OF THE OUTPHASING RF PAs

For a high voltage swing and high $P_{out}$ in the PAs in Fig. 3(a), the Class-D stage are combined using 1:1 on-chip transformers, $TR$. The PAs, optimized for $P_{out}$ [9] and bandwidth [10], used four and two transformers. Under $TR$ floating metal shields were placed in $M_1$ and $M_2$ to reduce the losses [24], but the optimal effect is obtained at maximum $P_{out}$, i.e. as the Class-D output operate on complementary signals. Simulations of [10] showed a 1.2 dB higher $P_{out}$ and a $\approx 30\%$ relatively higher efficiency with the floating shields than without. Tuning capacitors were placed at the primary windings in [9] to reduce the losses. In [10], the inductance of the transformer and transistor sizes (and associated capacitances) were optimized at 1.95 GHz to omit the MIM tuning capacitors with a maximum allowed voltage of 5.5 V (10 V in [9]), potentially causing reliability issues with the 5.5 V supply, $V_{DD2}$. The top/bottom plates of the capacitors were connected to $V_{DD2}/GND$ [9] ($V_{DD2}/V_{DD1}$ [10]).

V. MEASUREMENT RESULTS

The measurement setup is shown in Fig. 10. 5.5 V comes from an off-chip power supply and was chosen by using the derived equations and by sweeping the bias level to achieve an $E$ of $0.6-0.7 \text{V/mm}$ gate oxide and provide reasonable life-time. $P_{out}$ was $+32.0$ dBm [9] with a DE and PAE of 20.1% and 15.3%, including all drivers, at 1.85 GHz. $P_{out}$ was $+29.7$ dBm [10] at 5.5 V ($+30.5$ dBm at 6.0 V) with a DE and PAE of 30.2% and 26.6% at 1.95 GHz. The PAs had a 3 dB bandwidth of 0.9 GHz (1.2-2.1 GHz) [9] and 1.6 GHz (1.2-2.8 GHz) [10], respectively. The measured $P_{out}$ and efficiency are $10\%$ lower than the simulated performance at $65^\circ \text{C}$, incl. S-parameters of EM-simulated transformers and layout parasitics. The PA performance over temperature has not been characterized in measurements, but in simulations the relative changes in $P_{out}$ and efficiencies were $< 15\%$ between 25 and $125^\circ \text{C}$. Table III lists published state-of-the-art fully integrated CMOS Class-D PAs. The PAs present state-of-the-art $P_{out}$ [9] and bandwidth [10], comparable with [8], but larger than other PAs with state-of-the-art bandwidths (1.3 GHz) [25]. Modulation/spectral requirements were met for uplink WCDMA/LTE [9], [10].

<table>
<thead>
<tr>
<th>TABLE I</th>
<th>VGD AND VGS IN THE PROPOSED (PROP.) AND THE CONVENTIONAL (CONV.) CLASS-D STAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prop.</td>
<td>$V_{GD}$ high ($V_{GD} = V_{DD1}$)</td>
</tr>
<tr>
<td>$T_{1}$</td>
<td>$V_{pd}$ ($V_{bias} + V_{DD1}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD2}/2$)</td>
</tr>
<tr>
<td>$T_{2}$</td>
<td>$V_{gs}$ ($V_{bias} + V_{DD2}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD2}/2$)</td>
</tr>
<tr>
<td>Conv.</td>
<td>$V_{GD}$ high ($V_{GD} = V_{DD1}$)</td>
</tr>
<tr>
<td>$T_{1}$</td>
<td>$V_{pd}$ ($V_{bias} + V_{DD1}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD2}/2$)</td>
</tr>
<tr>
<td>$T_{2}$</td>
<td>$V_{gs}$ ($V_{bias} + V_{DD2}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD1}/2$) ($V_{bias} - V_{DD2}/2$)</td>
</tr>
<tr>
<td>$M$</td>
<td>$V_{GD}$ ($V_{DD1}/2$) ($V_{DD1}/2$) ($V_{DD1}/2$) ($V_{DD1}/2$)</td>
</tr>
</tbody>
</table>

Fig. 9. Ratio of (a) the power dissipation of the drain capacitance and (b) the $r_{on}$ in the proposed Class-D stage compared to the conventional cascode stage for [9]. ($V_{DD2} = 5.5 \text{ V}, V_{DD1} = 1.3 \text{ V}$).
In an initial reliability assessment [10] two devices were continuously operated for 168 h without performance degradation in $P_{\text{out}}$ or efficiency. Thus, the 5.5 V supply does not seem have to any direct impact on device reliability. The required life-time has to be put in relation to the employed standard (e.g. 2G GSM has a 12.5 % duty cycle) and an expected user case. Presuming 4 h talk time a day for 1.5 years (estimated life-time of a handset) [23] corresponds to $\approx 275$ h (365 · 1.5 · 4 · 0.125) of continuous PA operation. WLAN products may experience similar effective operating times, where a test time of 168 h at elevated supply voltage is considered to cover more than five years of product reliability [16].

VI. CONCLUSIONS

This paper presents the design and analysis of a 5.5 V Class-D stage used in two fully integrated watt-level outphasing RF Power Amplifiers (PA) in standard 1.2/2.5 V 130nm and 65nm CMOS technologies. The Class-D stage utilizes a cascode configuration, driven by an AC-coupled low-voltage driver, to allow a 5.5 V supply without excessive device voltage stress. The properties are compared with a conventional cascode (inverter) stage. To the authors’ best knowledge, the Class-D PAs presented are among the first fully integrated CMOS outphasing PAs reaching +30 dBm of output power and demonstrate state-of-the-art output power and bandwidth.

REFERENCES


