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Bias stress effect in polyelectrolyte-gated organic field-effect transistors

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A main factor contributing to bias stress instability in organic transistors is charge trapping of mobile carriers near the gate insulator-semiconductor interface into localized electronic states. In this paper, we study the bias stress behavior in low-voltage (*p*-type) polyelectrolyte-gated organic field effect transistors (EGOFETs) at various temperatures. Stressing and recovery in these EGOFETs are found to occur six orders of magnitude faster than typical bias stress/recovery reported for dielectric-gated OFETs. The mechanism proposed for EGOFETs involves an electron transfer reaction between water and the charged semiconductor channel that promotes the creation of extra protons diffusing into the polyelectrolyte. © 2013 American Institute of Physics. [http://dx.doi.org/10.1063/1.4798512]

The performance of organic field effect transistors (OFETs) has improved tremendously during recent years.[1] These devices will be included in several future low-cost-applications, which makes device stability an important technological issue.[2,3] Many OFETs exhibit undesirable current instability and threshold voltage shifts upon prolonged application of the gate-source voltage; this phenomenon is known as bias stress.[4] The origin of bias stress in organic transistors has been heavily discussed and is not yet fully understood. There are various factors that can contribute to this observed instability where the main one is charge trapping[5] that could occur either in the insulator,[6] in the semiconductor,[7–9] or at the semiconductor/insulator interface.[10,11] Other suggested mechanisms include variation of contact resistance under gate bias,[5] a minor electrical leakage or ionic displacements in gate insulators,[12] and humidity effect on gate insulator properties.[13] The presence of active trapping sites due to intrinsic structural defects (gate insulator/organic semiconductor interface[14,15] and disordered gate insulator[6]) or impurities (water or oxygen)[16] has been identified as one of the main causes behind bias stress.

Bias stress behaviour in OFETs has been investigated and reported in several previous manuscripts but the mechanism has not been conclusively determined and may differ depending on materials used. For example, Park *et al.* suggest that bias-induced threshold voltage shift in pentacene-based FETs is due to charge trapping in the semiconductor/dielectric interface region, where the trapping mechanism is influenced by the molecular structural ordering at such an interface.[17] Mathijssen *et al.* repported bias stress in OFETs—prepared on heavily doped Si wafers acting as a common gate with 200 nm thermally grown SiO_2 gate dielectric—to be caused by charge trapping in the gate dielectric established by the fact that the threshold voltage shift is sustained upon depositing a pristine organic semiconductor on the exposed dielectric of a stressed and delaminated transistor.[18] Wang *et al.* correlate bias stress instability in pentacene thin film transistors (TFTs) to the time-dependent charge trapping in both the channel and the metal/

organic contact regions since they found that the shift in threshold voltage is accompanied by an increase in contact resistance.[19] Street *et al.* suggested that formation of hole bipolarons is responsible for the observed bias stress effect in polymer TFTs, given that the number of holes removed from the channel per time and area is proportional to the square of their concentration.[20] Sharma *et al.* proposed that the mechanism for bias stress in p-type OFETs is associated with the electrolysis of residual water at the semiconductor-dielectric interface where holes are converted to protons that consequently migrate into the gate dielectric.[21]

Electrolyte-gated organic field-effect transistors (EGOFETs) are promising candidates for low cost, robust, printed electronics, thanks to their low operating voltages. Upon gate biasing, the polarization of the polyelectrolyte gate insulator is accompanied with the formation of ionic electric double layers (EDLs) at the gate/electrolyte and at the electrolyte/semiconductor interfaces. This high capacitance of the EDL capacitor enables low operating voltages. P-channel, n-channel, and CMOS circuits based on EGOFETs have been already achieved[22–24] but there has not been a prior investigation on the bias stress characteristics for this type of transistors. Such an investigation is important since the interface in EGOFETs is completely different than other OFETs; the dielectric is replaced by a polyelectrolyte. Common to several of the previous bias stress studies is the importance of the semiconductor/insulator interface, which raises the question of how bias stress will be manifested in EGOFETs, where polyelectrolytes are utilized as gate insulators.

In this paper, we have, therefore, chosen to study the bias stress behaviour in *p*-type EGOFETs and identify specific mechanisms for the polyelectrolyte/semiconductor interface. Bias stress measurements in EGOFETs are performed at low voltages (<1 V). The structure of the EGOFET used in this paper is shown as an inset in Fig. 1(a).

The EGOFETs were manufactured according to the following process. Bottom electrode material (50 nm of gold on top of 5 nm of chromium) was thermally evaporated on a Si/SiO_2 wafer. Source and drain electrodes were patterned from this film by means of photolithography and wet-etching. The organic semiconductor layer was spincoated from a solution

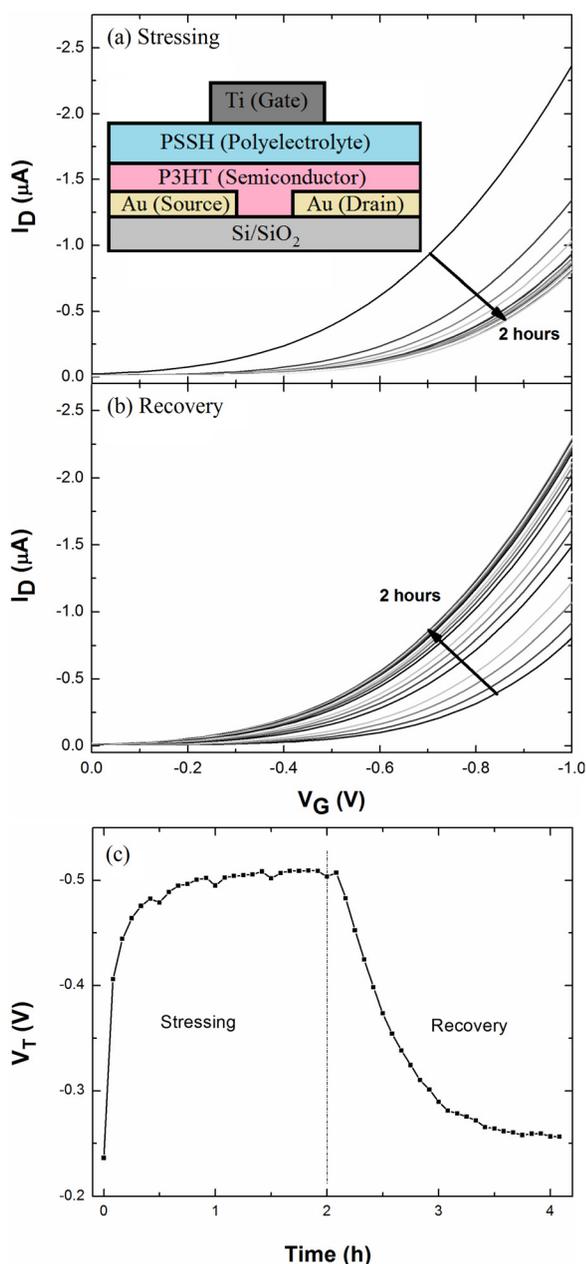a)Electronic mail: Isak.Engquist@liu.se

FIG. 1. Transfer curves as a function of (a) stressing and (b) recovery time were measured up to 2 h with a 5 min stressing and recovery cycles. The applied gate bias during stressing was -0.5 V along with a drain bias of -0.1 V. The gate and drain electrodes were grounded during recovery cycles. The inset in Figure 1(a) shows the transistor structure. (c) Threshold voltage vs. time. The measurement was done at 22 °C, 40% RH, and in darkness.

of 3 mg ml^{-1} regioregular poly(3-hexylthiophene) (rr-P3HT, Sigma-Aldrich with a regioregularity greater than 95% and a molecular weight of 15 000-45 000) in chloroform and afterwards annealed at 120 °C under nitrogen for 10 min, resulting in a 30 nm thick film. After that, a mixture of 1:14 vol:vol poly(styrene sulfonic acid) (PSSH, Sigma-Aldrich with a molecular weight of about 75 000 and a concentration of 18 wt. % in de-ionized water) to de-ionized water with 0.3% zonyl FS-300 as a surfactant was spin-coated on top of the organic semiconductor layer and annealed under vacuum at 110 °C for 90 s, resulting in a 100 nm film. Finally, a 100 nm titanium film was thermally evaporated under vacuum through a shadow mask forming the gate electrode. The channel length and width of the resulting transistor were

2 μm and 500 μm, respectively. The field effect mobility of the obtained EGOFET is around 0.13 cm^2 V^{-1} s^{-1} (calculated for $C_i = 3\ \mu$F. cm^{-2}, at $V_D = V_G = -1$ V), and the subthreshold swing is estimated around 0.37 V per decade.

The transistor characteristics reported here were measured with a Keithley 4200-SCS parameter analyzer. The threshold voltage V_T was determined from the linear fit to the square root of the drain current in the saturation region that intersects the gate voltage axis (V_G-axis).[1] Some of the measurements were carried out in nitrogen atmosphere; these were performed in a glove bag filled with an overpressure of dry nitrogen. The humidity inside the glove bag was kept at around 5% relative humidity (RH). Bias stressing was applied using continuous gate and drain biases of -0.5 V and -0.1 V respectively, while the source contact was grounded. To achieve recovery of the drain current, the gate, source, and drain contacts were all grounded. The continuous stressing and recovery were interrupted by very short intervals in which the transfer curves were recorded. Every 5 min, a transfer curve was recorded by sweeping the gate bias from 0 V to -1 V at a drain bias of -1 V. This measurement only lasts for 3 s and did not result in any significant disturbance of the stressing or recovery processes.

The initial characterization of the bias stress process in the EGOFET was carried out at room temperature (22 °C) and 40% RH. Stressing for 2 h was followed by recovery for another 2 h that resulted in a set of transfer curves shifting in a parallel manner (Figs. 1(a) and 1(b)). We note that during stressing, the transfer curves shift, with time, in the direction of the applied gate bias; i.e. towards more negative values, while they shift back in the opposite direction during recovery. The threshold voltage is extracted from the transfer curves and is plotted versus time in Fig. 1(c). Similar to the transfer curves, the threshold voltage shifts towards more negative values during stressing and shifts back in the opposite direction during recovery.

The threshold voltage of our EGOFETs shifts faster in comparison to other reported OFETs under both stressing and recovery. The maximum V_T shift is reached in approximately 30 min in our devices while for OFETs with dielectric gate insulators it takes much longer time; for example, in bottom-gate bottom-contact OFETs with PTAA semiconductor and SiO$_2$ gate dielectric, stressing times of 2 weeks has been observed to obtain a maximum shift.[8] This difference suggests that the mechanism of bias stress is different. The relative magnitude of the shift recorded here is comparable to what has been reported in other OFETs, since in each case, the threshold voltage is found to saturate at the applied gate stress bias at the end of stressing.[8,21]

Temperature dependent measurements are used to evaluate the activation energy for the mechanism involved in this bias stress phenomenon. The bias stress measurement was repeated for different temperatures (22 °C, 12 °C, 5 °C, and 0 °C) at 5% RH in nitrogen atmosphere using a scheme consisting of 3 h of stressing followed by 3 h of recovery. The resulting threshold voltage shift is plotted versus time in Fig. 2(a). It is noted that the 5% and 40% RT measurements in Figs. 1(c) and 2(a) are slightly different; however, the overall agreement is good and we consider the differences to be within the error range of the measurement and the
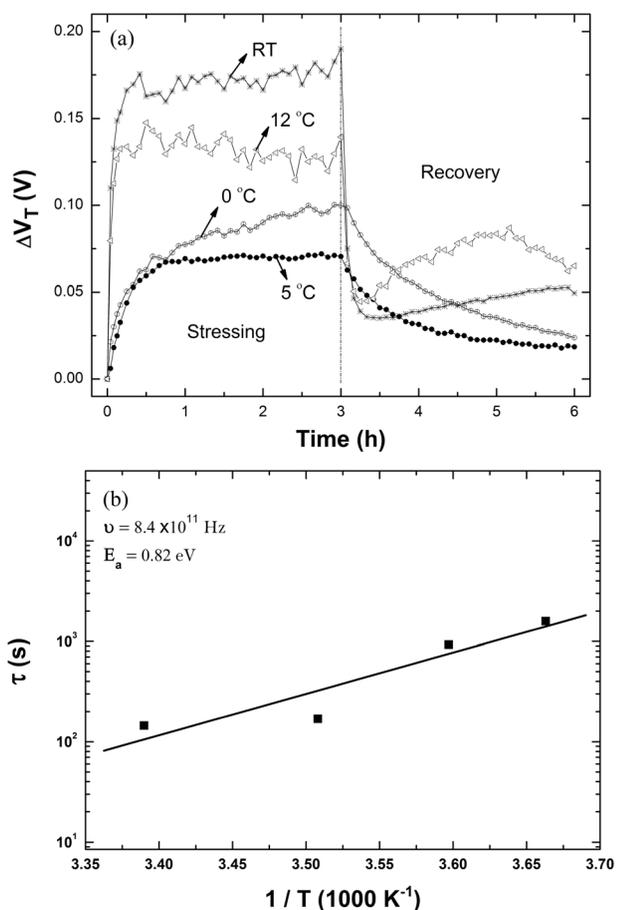
FIG. 2. (a) Absolute threshold voltage shift versus time at different temperatures, all data are under nitrogen atmosphere, 5% RH, and in darkness. (b) A linear fit of the relaxation time, τ, versus inverse of temperature. Activation energy for the transport of protons is extracted from this figure and is found to be 0.82 eV.

threshold voltage extraction method. Measurements were also made at temperatures above ambient (40 °C, 60 °C, and 80 °C) but those data are not included in the analysis or this report since materials and/or interfaces undergo degradation (see supplemental material).[35] The data analysis aiming to find the activation energy of the bias stress mechanism was restricted to the temperature interval in Fig. 2(a), where no irreversible temperature effects occur. As commonly seen in other organic transistors, the threshold-voltage shift shows a stretched-exponential time dependence under constant gate-source and drain-source voltages. The threshold voltage shift obeys the following equation:[13,25–27]

$$\Delta V_T(t) = [V_T(\infty) - V_T(0)][1 - \exp^{-(t/\tau)^\beta}], \quad (1)$$

where $V_T(0)$ is the initial threshold voltage, $V_T(\infty)$ is the threshold voltage when equilibrium has been reached (at $t \to \infty$), τ is the relaxation time, and β is the stretching or dispersion parameter ($0 < \beta \leq 1$). τ and β are given by

$$\tau = v^{-1} \times \exp^{(E_a/(k_B \times T))}, \quad (2)$$

$$\beta = T/T_0, \quad (3)$$

where v is the frequency prefactor, E_a is the mean activation energy for trapping, T is the temperature, and T_0 is the

characteristic temperature of the "trap states." Thus, from curve fitting using the least squares method, the relaxation time (τ) and the dispersion parameter (β) can be extracted from the stretched exponential fit of the threshold voltage shift versus time for the four different measurements (shown in the supplemental material).[35] We notice that the relaxation time increases considerably as the temperature decreases. By plotting the logarithm of the relaxation time versus the inverse of the temperature (see Fig. 2(b)), we see that there is a linear relationship, which supports the applicability of Eq. (1). The curve fit allows extraction of the activation energy and the frequency prefactor as follows: ($E_a = 0.82$ eV and $v = 8.4 \times 10^{11}$ Hz). Surprisingly, the frequency prefactor is much higher than what has been reported for other organic transistors with charge trapping as the bias stress mechanism (around 10^3 Hz in bottom-gate bottom-contact OFETs with PTAA semiconductor and SiO$_2$ gate dielectric)[8] and is comparable to a simple phonon-mediated escape-to-attempt frequency (10^{12} Hz).[28] Again, this indicates that the bias stress mechanism with polyelectrolytes might be different than electronic charge trapping in conventional dielectrics. Trapping of water molecules in P3HT grain boundaries, which sometimes is the cause of bias stress, is ruled out in our case since the sample is thoroughly annealed after spin coating the polyelectrolyte. Regarding the activation energy, it is comparable to that of other organic transistors, which is commonly found around 0.6 eV.[8,27]

We have also measured the drain current recovery under darkness and in light. We observe that the sample recovers in both cases (in light and in darkness) suggesting that visible light has no effect over the recovery process, which can be attributed to the fact that the bias stress scenario in EGOFETs does not involve charge trapping in the semiconductor.[9] Thus, quenching of excitons by trapped charges mechanism is not predominant here.

We propose to explain our measured data with a mechanism similar to what explains the bias stress in OFETs with SiO$_2$ dielectrics.[8,12,21,29] The mechanism proposed by several authors implies an electron transfer from adsorbed water present at the semiconductor/SiO$_2$ interface to positively charged semiconducting channel in the transistor (P3HT$^+$). The products of the water oxidation are a proton and a dioxygen

$$2H_2O \rightarrow 4H^+ + O_2 + 4e^-$$

$$P3HT^+ + e^- \rightarrow P3HT.$$
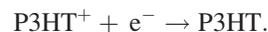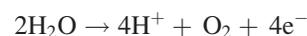
The produced protons slowly penetrate into the SiO$_2$ dielectric through the negative gate bias. This extra charge leads to the threshold potential shift and explains the bias stress phenomenon (Fig. 3). In our case, instead of SiO$_2$, we have a dry polyelectrolyte (5% RH). The local concentration of water at the interface is not known but is likely lower. A major difference between polyelectrolytes and SiO$_2$ is the large proton mobility in polyelectrolytes. A typical order of magnitude of proton mobility and conductivity in a fully hydrated sulfonic acid membrane is about 10^{-3} cm^2 V^{-1} s^{-1} and 0.1 S cm^{-1} respectively.[30] In our PSSH thin film, the
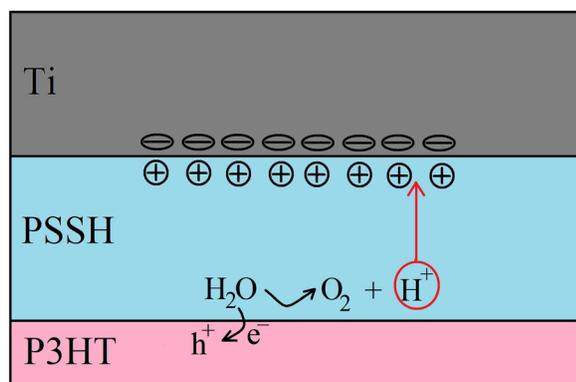
FIG. 3. A cross section of the transistor showing the bias stress mechanism where in the presence of water a hole is converted into a proton that subsequently migrates into the gate insulator towards the gate/electrolyte interface creating an additional proton that is not balanced, thus leading to a shift of the threshold. It is important to note that there is also another electric double layer present at the P3HT/PSSH interface consisting of the anions in the polyelectrolyte and the holes in the channel, but it is not shown in the figure for clarity reasons.

proton conductivity at about 5% RH is of the order of $10^{-6}\,\mathrm{S\,cm^{-1}}$.[31] Since the mobile proton concentration is quasi constant versus relative humidity in sulfonic acid based polyelectrolytes,[32] we can estimate an order of magnitude of the proton mobility in the PSS layer used in the bias stress experiment to be about $\mu = 10^{-8}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. The diffusion constant of a proton in PSS estimated from the Einstein relationship is about $D = \mu\ (kT/F) = 2.5 \times 10^{-7}\,\mathrm{m^2\,s^{-1}}$, which agrees with data achieved from theoretical models.[33]

The relaxation time $\tau = 10^8\,\mathrm{s}$ (40% RH and 295 K) for a SiO$_2$/P3HT device is six orders of magnitude longer ($\tau = 10^2\,\mathrm{s}$ and 295 K) than in our PSS/P3HT device. The fast saturation of the threshold voltage shift and the recovery time in EGOFETs is attributed to the large diffusion constant of protons in PSS as compared to SiO$_2$ ($D \sim 10^{-19}\,\mathrm{m^2\,s^{-1}}$).[12,34]

The migration of protons leads to the accumulation of protons in the gate insulator, which partially screens the applied gate voltage by creating an electric field that is compensated for by the gate voltage in order for an accumulation layer to be formed, and thus the threshold voltage of the OFET increases. Longer periods of time of the gate voltage application leads to larger number of holes converted into protons, and hence a larger increase or shift in the threshold voltage. However, threshold voltage shift reaches a saturation point when the shift is equal to the applied gate stressing voltage, and thus no further shift is observed. This is not expected with an electronic trapping phenomenon, since no trap filling level is observed. This is rather in strong agreement with an electrochemical reaction where there is a large amount of the reactant (water). Bias stress is reversible, with the most plausible mechanism being the back conversion of protons into holes after that the gate electrode is grounded.[21]

The presence of water is due to the nature of the polyelectrolyte that is hygroscopic. Thus, the concentration of water in the polyelectrolyte membrane might be crucial for the rate of the reaction and the reversibility of the phenomenon and will be the object of further investigations.

In summary, our measurements indicate that bias stress in EGOFETs occurs through the oxidation of water present at the polyelectrolyte/semiconductor interface and the subsequent migration of these protons into the gate insulator. A 6 order of magnitude faster relaxation time in the bias stress characteristics effect while comparing with other similar OFETs based on the same mechanism is attributed to the high proton diffusion coefficient in the polyelectrolyte. Hence, EGOFETs undergo a fast bias stress and recovery effect, which might be advantageous for circuits and sensors.

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[35]See supplementary material at http://dx.doi.org/10.1063/1.4798512 for above-ambient temperature dependent measurements and threshold voltage shift fitted with the stretched-exponential function.