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Fast-switching all-printed organic electrochemical transistors

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Abstract

Symmetric and fast (~ 5 ms) on-to-off and off-to-on drain current switching characteristics have been obtained in screen printed organic electrochemical transistors (OECT) including PEDOT:PSS (poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonic acid)) as the active transistor channel material. Improvement of the drain current switching characteristics is made possible by including a carbon conductor layer on top of PEDOT:PSS at the drain electrode that is in direct contact with both the channel and the electrolyte of the OECT. This carbon conductor layer suppresses the effects from a reduction front that is generated in these PEDOT:PSS-based OECTs. In the off-state of these devices this reduction front slowly migrate laterally into the PEDOT:PSS drain electrode, which make off-to-on switching slow. The OECT including carbon electrodes was manufactured using only standard printing process steps and may pave the way for fully integrated organic electronic

systems that operate at low voltages for applications such as logic circuits, sensors and active matrix addressed displays.

1. Introduction

Major efforts have been invested to create a reliable platform consisting of organic field-effect transistors (OFETs) [1]. Along with this device development activity an impressive number of different organic semiconductors have been synthesized, of which the material properties have been improved with respect to solubility, processability and field-effect mobility [2,3]. However, to make OFETs a successful technology in distributed electronic applications, it is important that the operation voltages are kept low, preferably around 1 V or so; the OFETs are typically operated at voltages on the order of tens of Volts. High permittivity materials and ultra-thin film insulator films for the gate insulator have extensively been explored to achieve low-voltage operation in OFETs [4]. Device operation below 1 V in easily printed and robust OFET architectures has therefore been difficult to achieve. However, thin film organic transistors gated via a solid or gelled electrolyte layer have proven to be a promising robust alternative to achieve low driving voltages. There are two kinds of electrolyte-gated organic thin film transistors; electrolyte-gated organic field-effect transistors (EGOFET) [5–7] and organic electrochemical transistors (OECT) [8–12]. These two transistor types are not only governed by different switching mechanisms but they also exhibit differences in device characteristics and opportunities regarding device manufacturing. EGOFTs are typically manufactured by traditional photo lithography processing since small feature sizes are required to obtain good or at least proper transistor characteristics, while low voltage operation in OECTs can be achieved without using any very narrow and critical dimensions. This gives that OECT device structures are typically more robust and thus also easier to include and integrate into printed electronic systems. To print electronics onto labels and foils

surface roughness, flexibility and non-planarity are obvious features that certainly is a challenge for thin film electronics. Hence, conventional printing techniques can be utilized in the manufacturing process of OECTs [13]. Another advantage of the OECT devices in comparison to OFETs is that this transistor type can deliver high on-current because an open transistor channel conducts charges through the entire bulk of the channel. Conversely, in the (EG)OFETs field-effect gating provide charge accumulation only along a thin sheet of the semiconducting layer. Printable or printed OECTs have been realized and reported previously for various applications, such as logic circuits [14], sensors [15,16] and active matrix addressed displays [17,18]. They typically suffer from non-symmetric switching characteristics, i.e. the on-to-off switching time is much shorter than the off-to-on switching time. Such switching characteristics are of course not desired since it would cause major problems related to slow updating, or even erroneous operation, in different printed electronic systems and applications. Here, novel architectures for printed OECTs are reported aiming at improving the switching time of OECTs and to achieve symmetric on-to-off and off-to-on switching.

2. Materials and methods

PEDOT:PSS, *Clevios SV3* purchased from Heraeus, which serves as the electrochemically active transistor channel, is patterned by screen printing on top of a flexible plastic substrate, for example the transparent polyethylene terephthalate (PET) foil *Polifoil Bias* purchased from Policrom Screen, and dried at 120 °C for 5 minutes. Carbon, *7102* conducting screen printing paste from DuPont, is typically patterned, for example by screen printing, as the source and drain electrodes on top of the PEDOT:PSS transistor channel. The carbon paste is dried at 120 °C for 5 minutes. An electrolyte is then deposited, by stencil printing, where the stencil is created by a screen printed lacquer layer in which an opening defines the area of the

electrolyte pattern. The lacquer material, *Tactile varnish* purchased from Sericol, is cured by exposure to UV light. The compounds of the electrolyte layer, containing sodium poly(styrene sulfonate) (PSSNa, M.W. $\sim 70,000$), D-sorbitol and glycerol that were purchased from Alfa Aesar, Sigma-Aldrich and Merck, respectively, were mixed into an aqueous solution according to the weight ratio of PSSNa/D-Sorbitol/glycerol/deionized water = 40/10/10/40 wt.%. The deposited electrolyte layer, which was solidified by careful evaporation of water at 50 °C for 45 s, ensures the ionic connection between the transistor channel and the gate electrode; the latter consists of PEDOT:PSS coated on PET, Orgacon EL-350 purchased from AGFA Gevaert, and is laminated on top of the electrolyte to complete the vertically stacked transistor device.

All measurements are performed in controlled environment at a temperature of ~ 20 °C and at a relative humidity of ~ 40 %RH. The transistor sweeps were performed by using a HP/Agilent 4155 B semiconductor parameter analyzer and the transistor switching time measurements were performed by using two Keithley 2400 sourcemeter units. Graphical interfaces programmed in LabView (National Instruments) were used to control the measurements and to simplify data storage.

3. Results and discussion

The OECT, here reported, includes the poly(3,4-ethylenedioxythiophene) (PEDOT) as the active material in the transistor channel. The polymeric anion poly(styrene sulfonic acid) (PSS) ensures charge neutrality of the chemically oxidized PEDOT, such that the electrically conducting polymer PEDOT:PSS system is formed, see Figure 1. An OECT device can be configured in either a lateral or vertical architecture; the main requirement though is that the transistor channel and the gate electrode are connected via an electrolyte that provides the ions required for the two electrochemical half-reactions necessary for the OECT device

operation. Figure 1 illustrates both a lateral and a vertical OECT structure, in which the source and drain electrodes, the transistor channel and the gate electrode all are based on PEDOT:PSS. A layer of electrolyte represents the ionic connection between the transistor channel and the gate electrode. The lateral transistor structure enables manufacturing using only two printing steps in which all the PEDOT:PSS layers are formed adjacent to each other in the same plane. The vertical structure is preferably realized simply by depositing or applying the gate electrode on top of an electrolyte, either by additive printing or by lamination. The vertical OECT design is typically advantageous in printed and relatively more densely integrated electronic systems since its structure is more compact. The lateral OECT architecture is more commonly studied as the transducer in electronic sensor applications due to that its channel is freely exposed to the electrolyte (analyte). The channel and gate electrodes are here configured in the same plane directly under the electrolyte. Upon applying a voltage difference between the gate electrode and the transistor channel, electrical double layers are formed at the interface between the electrolyte and the gate electrode as well as across the electrolyte and the transistor channel interface, respectively. Since the potential drop occurs mainly across these two interfaces, and not within the bulk of the electrolyte, low-voltage transistor operation is possible.

Figure 1. a) The chemical structures of poly(3,4ethylenedioxythiophene) and poly(styrene sulfonate), that together form the electrically conducting polymer PEDOT:PSS, is shown to the left. b) Sketch showing the architecture of a lateral OEET. c) Sketch showing the architecture of a vertical OEET.

PEDOT:PSS is a versatile material; electrochemical reduction of its pristine oxidized state, which is transparent and electronically conducting, transfers the PEDOT phase into its semiconducting (close to insulating) form accompanied with a change in its optical absorption characteristics. The control in conductivity can be utilized as the switch mechanism in transistor devices [9], while the change in color can be used as the color switch functionality in electrochromic displays, such as in printed matrix-addressed paper displays [17]. Electrochemical switching of PEDOT:PSS is governed by:

PEDOT^+ denotes the oxidized state and is compensated by the PSS^- counter ions. As PEDOT is oxidized cations and electrons are egressed from the polymer film into the electrolyte and to the connected electrode, respectively. PEDOT^0 denotes the neutral, semiconducting and deep-blue colored form and when switched to this state, electrons are injected into the polymer and PSS^- is now instead compensated by cations. For instance, in a matrix-addressed electrochromic display PEDOT:PSS can serve as the conducting addressing lines of the cross-point matrix, as the electrodes of the electrochromic display and also as the channel of the electrochemical transistor. The fact that few different materials are needed to realize a complete system considerably simplifies the manufacturing process since only a few process steps are needed.

A major disadvantage with both the lateral and vertical OECT architectures, described above, is that they suffer from non-symmetric on-to-off and off-to-on drain current switching characteristics. This switching non-symmetry is caused by that a reduction front propagates [19] within the PEDOT:PSS film when a positive voltage is applied to the gate electrode in combination with a negative voltage applied to the drain electrode. The negative drain voltage causes the reduction front to migrate and extend beyond the electrolyte edge of the channel, into the bulk of the drain electrode of the OECT. This is possible since slow ion migration

occurs inside the thin PEDOT:PSS film, preferably in the PSS phase. This results in a prolonged off-to-on switching time since it takes long time to re-oxidize the electrochemically reduced volume of the front in the drain electrode. Further, the OECT is operating in the so-called depletion-mode, which implies that the transistor channel is conducting when the gate voltage, V_G , equals 0 V, while the channel switches off upon applying $V_G > 0$ V. Hence, the combination of depletion mode operation and non-symmetric switching characteristics is disadvantageous while using the transistor as the addressing switch in active matrix addressed displays. The depletion-mode operation causes undesired strain on the transistors since V_G must be applied (the transistor is turned off) during the major part of each complete display update cycle. This establishes a reduction front outside the electrolyte edge which extends into the drain electrode, thus prolonging the off-to-on switching by hundreds of milliseconds, or even seconds. In order to achieve active matrix addressed displays or logic circuits with sufficient performance, the OECT therefore needs to show symmetric switching behavior. Various attempts to prevent the reduction front have been evaluated, e.g. using a lacquer layer that confines the electrolyte layer to the transistor channel. Such an attempt can help preventing lateral capillary spreading of the electrolyte above and along the PEDOT:PSS film but the non-desired reduction front will still propagate within the PEDOT:PSS material system outside the edge of the deposited electrolyte.

Figure 2. a) Sketch showing the architecture of the previously reported vertical OECT, also denoted P:P-design, in which the reduction front is propagating outside the electrolyte edge. b) Sketch showing the architecture of a vertical OECT, also denoted C:C-design, in which the reduction front is prevented by that the electrolyte partly covers the carbon-based source and drain electrodes. c) Sketch showing the architecture of a vertical OECT, also denoted P:C-design, in which the reduction front is prevented by that the electrolyte partly covers the carbon-based drain electrode.

Here, an approach is explored to obtain an OECT exhibiting symmetric and also fast switching characteristics, which take use of printed carbon paste as the source and drain electrodes such that migration of the reduction front into the drain electrode is prevented. As illustrated in Figures 2b and 2c, there are two alternative device architectures possible as

compared to the previously reported P:P-OECT (Figure 2a). In the C:C-OECT both the source and the drain are composed by carbon electrodes that both are covered by the electrolyte, and in the P:C-OECT only the negatively biased drain carbon electrode is covered by the electrolyte. The abbreviations P:P, C:C and P:C simply refers to the choice of materials for the source and drain electrodes; P for PEDOT:PSS and C for carbon. Figure 3 shows the drain-source current (I_{DS}) vs. drain-source voltage (V_{DS}) characteristics, at various gate voltages (V_G), for all three different OECT architectures; P:P-, C:C- and P:C-OECT. A clear difference in the pinch-off behavior is observed when comparing the three different OECT designs. The pinch-off in drain current occurs at a relatively lower voltage in the P:P-OECT as compared to the other two ones. The pinch-off is caused by the steep potential gradient along the channel due to the voltage applied between the drain and source electrodes [20], an effect that apparently is more pronounced in the P:P-OECT as compared to the two other designs where the electrolyte covers one or both carbon electrodes. This difference in pinch-off-behavior is, however, not crucial in applications targeting logic circuits and matrix-addressed displays. Instead, the off-current levels at elevated voltages are more critical in such applications. The P:P- and the P:C-OECT both show a low and stable off-current level upon elevating the V_{DS} , i.e. the on/off-ratio remains constant. The off-current level for the C:C-OECT increases when V_{DS} exceeds ~ 2 V (data not shown), i.e. the on/off-ratio probably decreases due to a parasitic non-faradaic current contribution established at elevated voltage levels. This parasitic current originates most likely from electrolysis of the water-based electrolyte at the two carbon electrodes. Despite the increased off-current level measured for the C:C-OECT, this transistor architecture could still be suitable in various applications wherein low voltage operation is ensured.

Figure 3. The I_{DS} vs. V_{DS} characteristics of the three different transistor architectures are shown; P:P-design to the left, C:C-design in the middle and P:C-design to the right.

Both the C:C- and P:C-OECT exhibit proper transistor functionality with respect to I_{DS} vs. V_{DS} and V_{GS} modulation, which motivates us to pursue evaluation of the switching characteristics of these devices. The results of this evaluation show not only the difference in switching characteristics among the three OECT architectures, but also how the off-to-on switching in the P:P-OECT strongly depends on the pulse length of the applied gate voltage. In Figure 4a, the on-to-off switching events are all comparable and occur within the 500 ms data pitch. The on-to-off switching events of the very same OECT components shown in Figure 4b are almost comparable; the C:C-design switches off in ~ 5 ms and the P:P- and the P:C-designs both switch off in about 10 ms. The major difference between the different transistor architectures are observed when comparing the off-to-on switching events; the P:C- and the C:C-design switches from off to on in ~ 10 ms and ~ 30 ms, respectively, while the off-to-on switching time of the P:P-design is typically much longer than 100 ms. In fact, the V_G pulse length, which in Figure 4b corresponds to ~ 0.17 s, is not sufficiently long to completely switch the channel back to its on-state, as evidenced in Figure 4b. Prolonging the V_G pulse length adds more strain on the transistors, and hence the effect of the reduction front becomes more pronounced in the P:P-OECT, which is shown in Figure 4a by that its switching time is exceeding 3 s at a V_G pulse length of ~ 17 s. The explanation to the results obtained is that the C:C- and the P:C-designs are not suffering from a reduction front

propagating into the drain electrode, which would prolong the off-to-on switching time. The voltage difference between the gate electrode and the negatively biased drain electrode was kept below 2 V in the measurements shown in Figure 4, i.e. $V_{DS} = -1$ V and V_G was switched between 0 and 1 V. The three different transistor architectures all showed comparable on/off-ratios of approximately 500-1000; the corresponding on/off current values were approximately 70 μ A/100 nA, 140 μ A/250 nA and 1.05 mA/1.4 μ A for the P:P, P:C and C:C OEET design, respectively. Hence, short switching time, symmetric switching behaviour and maintained high on/off-ratio are combined properties that especially make the P:C-design suitable in various printed electronics system applications. The C:C-design is also an interesting candidate as long as the operation voltages are kept at sufficiently low levels so that undesired parasitic currents between the source and drain electrodes do not appear.

Figure 4. A comparison of the dynamic switching characteristics of the OEET architectures is shown. All transistor devices show approximately the same behavior when their respective channel is switched from on to off. The major deviation is observed during the off-to-on switching event; the prevented reduction fronts in the P:C- and the C:C-designs clearly result in shorter switching time as compared to the P:P-design. The V_G pulse length corresponds to ~ 17 s and ~ 0.17 s in (a) and (b), respectively, and the time between two consecutive data points is 500 ms and 5 ms in (a) and (b), respectively.

Conclusions

Symmetric on-to-off and off-to-on switching and also fast switching, down to 5 ms, has been reported for all-printed electrochemical transistors based on PEDOT:PSS. The current through the transistor channel is modulated by electrochemical reduction and oxidation of the conducting polymer PEDOT:PSS. In the off-state a reduction front is generated that migrates towards and into the drain electrode, which then slows down the off-to-on switching. The major contribution, here reported, is the development of two different transistor architectures including electrochemically “inert” carbon electrodes that suppress this reduction front. This solution adds only one extra manufacturing step, thus keeping the simplicity of which electrochemical transistors are manufactured. The properties of the resulting electrochemical transistor devices, such as low-voltage operation and high on/off-ratio, make these transistors promising candidates in all-printed integrated electronic systems, such as logic circuits, active matrix addressed displays and sensor applications.

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