Linköping Studies in science and technology

Dissertation No. 1535

Polyelectrolyte-Gated Organic Field Effect Transistors – Printing and Electrical Stability

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Norrköping 2013

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Printed by LiU-Tryck, Linköping, Sweden, 2013

ISBN: 978-91-7519-549-0

ISSN: 0345-7524

Abstract

The progress in materials science during recent decades along with the steadily growing desire to accomplish novel functionalities in electronic devices and the continuous strive to achieve a more efficient manufacturing process such as low-cost robust high-volume printing techniques, has brought the organic electronics field to light. For example, organic field effect transistors (OFETs) are the fundamental building blocks of flexible electronics. OFETs present several potential advantages, such as solution processability of organic materials enabling their deposition by various printing methods at low processing temperatures, the possibility to coat large areas, and the mechanical flexibility of polymers that is compatible with plastic substrates. Employing polyelectrolytes as gate insulators in OFETs allows low-voltage operation in the range of 1 V, suppresses unintended electrochemical doping of the semiconductor bulk, and provides tolerance to thicker gate insulator layers and to the gate electrode alignment over the channel which eases the design and manufacturing requirements. These features place polyelectrolyte-gated OFETs (EGOFETs) as promising candidates to be realized in low-cost, large-area, light-weight, flexible electronic applications.

The work in this thesis focuses on EGOFETs and their manufacturing using the inkjet printing technology. EGOFETs have been previously demonstrated using conventional manufacturing techniques. Several challenges have to be overcome when attempting to achieve a fully printed EGOFET, with the incompatible wetting characteristics of the semiconductor/polyelectrolyte interface being one of the main problems. This issue is addressed in paper I and paper II. Paper I presents a surface modification treatment where an amphiphilic diblock copolymer is deposited on the surface to enable the printability of the semiconductor on top of the polyelectrolyte. Paper II introduces an amphiphilic semiconducting copolymer that can switch its surface from hydrophobic to hydrophilic, when spread as thin film, upon exposure to water. Moreover, characterization of the reliability and stability of EGOFETs in terms of bias stress is reported. Bias stress is an undesired operational instability, usually manifested as a decay in the drain current, triggered by the gradual shift of the threshold voltage of the transistor under prolonged operation. This effect has been extensively studied in different OFET structures, but a proper understanding of how it is manifested in EGOFETs is still lacking. Bias stress depends strongly on the material, how it is processed, and on the transistor operating conditions. Papers III

and IV report bias stress effects in EGOFET devices and inverters, respectively. The proposed mechanism involves an electron transfer reaction between adsorbed water and the charged semiconductor channel, which promotes the generation of extra protons that subsequently diffuse into the polyelectrolyte. Understanding and controlling the mechanism of bias stress in EGOFETs is crucial for further advancements and development towards commercially viable organic transistor circuits.

Sammanfattning

Organisk elektronik är ett forsknings- och utvecklingsområde som vuxit kraftigt under de senaste decennierna. Utvecklingen har möjliggjorts genom stora framsteg inom materialteknik, t.ex. ledande och halvledande plastmaterial, och drivits framåt av behovet av nya typer av elektroniska kretsar, såsom flexibel (böjbar) elektronik. De material som används medger att elektroniken tillverkas kostnadseffektivt, genom robusta tryckmetoder med hög kapacitet, till exempel screentryckning eller med bläckstråleskrivare (inkjet). Detta är möjligt på grund av att materialen kan hanteras i form av lösningar (elektroniskt bläck), kan appliceras enkelt över stora ytor, inte kräver höga processtemperaturer, och är mekaniskt flexibla och därför kompatibla med plast- eller papperssubstrat. En av de viktigaste organiska elektronikkomponenterna är den organiska fälteffekttransistorn (OFET), som är outhärlig i de flesta kretsar. Bland de material som används i uppbyggnaden av en OFET finns gateisolatorn, som är en elektrisk barriär mellan transistorns styrelektrod (gate) och själva transistorkanalen. Genom att använda en s.k. polyelektrolyt som gateisolator kan flera fördelar uppnås, såsom mycket låga drivspänningar (kring 1 V) och undvikande av elektrokemisk dopning av halvledaren. Man får också bättre tolerans för tjocka gateisolatorer och variationer i gate-elektrodens exakta position över transistorkanalen, vilket minskar kraven på precision vid tillverkningen. Detta gör sammantaget att OFETs med polyelektrolyt-gate (EGOFETs) är lovande kandidater för lätta, flexibla elektronikkretsar med stor yta till låg kostnad.

Denna avhandling fokuserar på tillverkning av EGOFETs, samt de elektriska egenskaperna hos desamma. Tidigare forskning kring EGOFETs har främst använt transistorer tillverkade med konventionella tekniker, liknande dem som används för vanlig (icke-organisk) elektronik. För att åstadkomma en fullt tryckbar EGOFET behöver man lösa flera utmanande problem, varav ett av de viktigaste är vätbarhetsegenskaperna i gränsytan mellan halvledare och polyelektrolyt. I korthet är det förenat med svårigheter att trycka en vattenälskande polyelektrolyt ovanpå en vattenfrånstötande halvledare. Lösningar på detta problem presenteras i avhandlingens artikel I och II. I den första artikeln används en speciellt framtagen polymer bestående av två olika segment som ett interfacelager mellan de båda materialen. I artikel II introduceras en polymer som fungerar både som halvledare och som interfacelager. Den elektriska karakteriseringen av EGOFETs har utförts med fokus på hur deras stabilitet påverkas av ett fenomen benämnt bias stress. Bias stress

är en oönskad instabilitet som manifesteras genom en minskad elektrisk ström (drain current) genom transistorn, vilket beror på att dess tröskelspänning ändras vid långvarig drift. Denna effekt har studerats noggrant för OFETs och det finns en stark koppling till materialval, tillverkningsmetoder och driftparametrar, men trots detta saknas en bra förståelse av hur den fungerar i EGOFETs. Artikel III och IV fokuserar på bias stress i EGOFETs och i enkla logiska kretsar (inverterare) baserade på dessa. Baserat på mätningarna föreslås en mekanism som inbegriper sönderdelning av vattenmolekyler, vilket ger fria protoner som kan diffundera in i polyelektrolyten. Förståelse av bias stress i EGOFETs och kontroll av hur den uppstår är avgörande för hur dessa organiska transistorer kan utvecklas vidare till kommersiellt gångbara komponenter.

Acknowledgements

There are several people that I would like to acknowledge for the help they provided, with big or small things, at work or in private, during my studies at LiU. Thus, I would like to express my sincerest gratitude to the following people:

Isak Engquist, my co-supervisor, for all the help, support, and guidance during all these years. This thesis would not have been a reality without your indispensable contribution and patience.

Magnus Berggren, my main supervisor, for your never-ending optimism, inspiring enthusiasm, and for giving me the chance to study and work in this group.

Xavier Crispin, for your invaluable input to my papers and for all the stimulating scientific discussions.

Sophie Lindesvik, for all the administrative and practical help.

I also like to thank all the people that I had the chance to work with, in particular the **co-authors** of the included papers, the personnel at **Acreo**, and the entire **Organic Electronics** group with past and present members. I would like to specially thank **Olga** for being a great friend both at work and in private; I hope you can make it to my dissertation. I would also like to thank **Jiang, Negar, Amanda, Henrik, Simone**, and **Loig** for creating a nice and friendly atmosphere at the office. Special thanks to **Anders Hågerström**, for your help in the first project.

My special gratitude goes to my friends and family in Lebanon, especially my **mom, dad**, and **sister**. To my **brother** in New Zealand, thank you for being there for me whenever I needed your help.

Last, but not least, I would like to thank my **fiancée** for his boundless love and support and for always believing in me.

List of included Papers

Paper I

Amphiphilic semiconducting copolymer as compatibility layer for printing polyelectrolyte-gated OFETs

Hiam Sinno, Ha Tran Nguyen, Anders Hägerström, Mats Fahlman, Linda Lindell, Olivier Coulembier, Philippe Dubois, Xavier Crispin, Isak Engquist, Magnus Berggren

Organic Electronics **2013**, 14, 790-796

Contribution: Most of the experimental work. Wrote the first draft and was involved in the final editing of the manuscript.

Paper II

Amphiphilic Poly(3-hexylthiophene)-Based Semiconducting Copolymers for Printing of Polyelectrolyte-Gated Organic Field-Effect Transistors

Ari Laiho, Ha Tran Nguyen, Hiam Sinno, Isak Engquist, Magnus Berggren, Philippe Dubois, Olivier Coulembier, Xavier Crispin

Macromolecules **2013**, 46, 4548-4557

Contribution: Part of the experimental work. Wrote a small part of the manuscript and was involved in the final editing of the manuscript.

Paper III

Bias stress effect in polyelectrolyte-gated Organic Field-Effect Transistors

Hiam Sinno, Simone Fabiano, Xavier Crispin, Magnus Berggren, Isak Engquist

Applied Physics Letters **2013**, 102, 113306-113310

Contribution: All the experimental work. Wrote the first draft and was involved in the final editing of the manuscript.

Paper IV

Bias stress effect in inverters based on polyelectrolyte-gated organic field effect transistors

Hiam Sinno, Loig Kergoat, Simone Fabiano, Xavier Crispin, Magnus Berggren, Isak Engquist

submitted

Contribution: Most of the experimental work. Wrote the first draft and was involved in the final editing of the manuscript.

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Part 1

Background

1 Introduction

1.1 Introduction to Organic Electronics

One of the most notable inventions of the 20th century was the world's first transistor that was fabricated by the Noble Prize laureates John Bardeen and Walter Brattain at Bell Laboratories in 1947.^[1] Later, this discovery led to the advent of the transistor era that replaced vacuum tubes, and paved the way for numerous other discoveries that shaped the field of electronics with its increasingly grand impact on our daily life. Currently, the transistor is the key active component in almost all daily-used electronic appliances, such as computers, mobile phones, and TVs. The idea of the field-effect transistor (FET) was first proposed by Julius Edgar Lilienfeld in 1930,^[2] while the first field-effect transistor was designed and made in 1959 by Kahng and Atalla; it was a silicon based metal-oxide-semiconductor field-effect transistor (MOSFET).^[3] The electronic industry has been dominated by transistors based on inorganic semiconductor materials, mainly silicon, up until the introduction of the first organic FET that was fabricated using polythiophene as the active semiconducting material in 1986.^[4] All of this was made possible after the astonishing discovery of Alan J. Heeger, Alan G. MacDiarmid, and Hideki Shirakawa at the University of Pennsylvania in 1976 who later were awarded the Noble Prize in chemistry in 2000 for their discovery and development of conductive polymers.^[5]

Traditionally, polymers (most commonly referred to as plastics) served exclusively as electrically insulating materials. However, this view was changed after the introduction of synthetic conductive polymers in 1976 which opened up the route for their use as the active material in electronic applications, hereby revolutionizing polymer science. Polymers are used in nearly every industry due to their exceptional properties. Both natural and synthetic polymers can

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be produced with wide-ranging stiffness, density, strength, heat resistance, and even price. With continued research in polymer science and applications, they are playing an ever growing role in modern society. Conductive polymers represent a new class of polymers offering a unique combination of properties since they exhibit the attractive mechanical properties and the advantages of processability of plastics while having the possibility to fine-tune their electrical and optical properties allowing them to act as insulators, semiconductors, or conductors.^[6] Thus, the development of conductive polymers has laid the foundation for organic electronics technology that today has evolved to become a well-established research field and technology.

Organic materials are carbon based materials as they contain the element of carbon in combination with other atoms. Since the discovery of conducting polymers more than three decades ago, a remarkable progress has been observed in the science and technology of semiconducting polymers.^[7] Semiconducting polymers are now utilized in a wide variety of innovative applications owing to their remarkable properties especially their ability to be dissolved in common solvents and to be formulated as inks with electronic functionality. Further, their electronics and opto-electronic functionality can be tailor-made via chemical synthesis in order to meet specific functional and performance requirements when included in devices.^[8] This opens a route towards the production of large-area, high throughput, and low cost organic electronic components on flexible substrates – such as paper and plastic foils – utilizing conventional additive printing methods, e.g. flexography, gravure, offset, inkjet, roll-to-roll, and screen printing.^[9, 10] Compared to the complex and expensive manufacturing techniques of inorganic semiconductor based components, organic semiconductor based components possess a promising future despite their inferior performance, owing to their low cost, low power consumption, robust, flexible, and ease of manufacture.

Thanks to these features, the scope of envisioned applications in the world of electronics has expanded dramatically to address a wide range of polymer based devices including photovoltaic cells,^[11-14] organic light emitting diodes (OLEDs),^[15, 16] organic field-effect transistors (OFETs),^[17-21] and sensors.^[22, 23] Hence, this research development area currently involves flexible, medical, wireless, sensing, and ultrathin applications. Preliminary applications comprised of lightweight batteries and antistatic coatings; however, nowadays new concepts have emerged such as lightweight rollable flexible matrix displays based on OLEDs that are already commercial, integrated sensor technologies, printed radio frequency identification (RFID). Thus,

polymer based applications are evolving beyond research and development towards the verge of commercialization since there is an ever driven interest in more robust, thinner, disposable, and cheaper electronics. It is noteworthy that the performance of organic based electronics might never match that of conventional electronics; nevertheless, they have the potential to reach farther places in the future beyond the scope of conventional electronics.

1.2 Motivation for this Thesis

The concept of printed electronics was first introduced in 1968 by Brody and Page at Westinghouse where a stenciling method was used as a deposition technique for inorganic thin-film transistors (TFTs) on flexible paper substrates inside a vacuum chamber.^[24, 25] However, due to the high cost, i.e. the required vacuum processing, and the brittleness of inorganic materials; there was a limited interest in this approach around that time. It was not until the past two decades that the interest in the development of printed electronics was renewed due to the technological potential that solution-processable conjugated polymers possess. Numerous advances have been recently reported in the field of printed organic electronics where novel applications and device approaches have emerged. Printed organic electronics combines the flexibility of organic materials with the low cost, robustness, and high throughput of printing technologies. However, there are many challenges within this field that need to be overcome when attempting to achieve reliable portable electronic devices with adequate performance that can be possibly realized using printing techniques. One important feature when targeting organic printed electronic circuits is related to power consumption. The powering of printed circuits is typically done via printed batteries,^[26] thermoelectric generators,^[27] or solar cells;^[12] which suggests that the circuit's organic components - e.g. transistors - have to be compatible with such power sources suggesting that low voltage operation - in the range of 1 V - is an essential feature of these components. Therefore, countless efforts are devoted to lowering the operating voltage of organic electronic components. Another key factor that needs to be addressed is related to the difficulties faced in the manufacturing process of printed organic electronic components such as the limitation in the thickness of the gate insulator layer within the transistor structure while retaining the required and desired low-voltage operation. In conventional organic field-effect transistors, low-voltage operation is achieved by the use of gate insulators with high capacitance implying the need for

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nanometer-thick gate insulator layers in order to attain operating voltages in the range of few volts.^[28, 29] Thin layers can be deposited by printing techniques, but targeting high-volume, low cost, robust roll-to-roll printing production implicates the use of thicker layers which necessitates exploring new materials and novel device concepts compatible with thicker films. Hence, the progress of printed electronics is hindered by the lack of transistors combining low voltage operation and tolerance to thicker gate insulator layers.

Polyelectrolyte-gated organic field effect transistors (EGOFETs) are suitable candidates to be realized by printing techniques. EGOFTs have previously been demonstrated and fabricated using conventional manufacturing techniques; they differ from ordinary OFETs by having a polyelectrolyte as the gate insulator material instead of a dielectric layer.^[30-32] Electrolytes are attractive materials for use in printing applications since a high capacitance that is independent of the electrolyte layer thickness can be achieved in electrolytic capacitors. Combining organic semiconductors with electrolytes in an OFET enables the formation of thin electric double-layers (EDLs) at the gate/electrolyte and electrolyte/semiconductor interfaces upon gate biasing that is induced by ion migration within the electrolyte. However, the ions can easily penetrate into the bulk of the organic semiconductor which leads to a bulk electrochemical doping preventing the transistor from operating in the desired field-effect mode, thus resulting in an electrochemical transistor with a low operation speed. Therefore, polyelectrolytes are used in EGOFTs instead since polyelectrolytes consist of mobile counter-ions with immobile charged polymer chains which prevents electrochemical doping of the semiconductor bulk (more details about this later) and ensures field-effect operation mode. EGOFTs possess high interfacial capacitances that make device operation at low voltages possible while being relatively tolerant to the polyelectrolyte thickness; such qualities make them suitable to manufacture using printing techniques.

A proper understanding of the different factors influencing the performance and reliability of EGOFTs and how these factors contribute to the operational instability known as the bias-stress effect is still lacking. Bias stress is usually manifested as a decay in the drain current caused by the progressive shift of the threshold voltage of the transistor under prolonged operation.^[33, 34] Bias stress depends strongly on the material, how it is processed, and on the transistor's operating conditions.^[35-38] Understanding and controlling the mechanism of bias stress in printed organic transistors have become increasingly important in light of the long term goal of developing the field of printed electronics. In this thesis, we report a fully printed EGOFT along with

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characterization of its operational stability with respect to bias stress and identifying the mechanism behind it.

The objective of the first part of this thesis is to provide the required background information that is imperative to understand the scientific results and findings in the papers presented in the second part of the thesis. In chapter two, a brief review of the physical and chemical properties of organic semiconductors and electrolytes is presented. In chapter three, a background on organic field-effect transistors is given. Chapter four discusses the history of bias stress and recovery along with the different proposed mechanism behind this phenomenon. Chapter five presents the manufacturing and characterization techniques of EGOFETs. Finally, conclusions and a future outlook are presented in chapter six.

2 Organic Electronic Materials

2.1 Organic Semiconductors

Organic semiconductors are divided into two categories, conjugated polymers and conjugated small molecules.^[39] Conjugated polymers are organic macromolecules consisting of at least one backbone chain of alternating double and single carbon–carbon bonds. They have high molecular weight and they can be processed from solution into thin flexible films by spin-coating, gravure, inkjet printing, and other coating and printing methods as well.^[40] An example of a widely used conjugated polymer is regioregular poly(3-hexylthiophene) (P3HT, Fig. 2.1a); the carrier mobility of P3HT is in the range of $0.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[41] As to small electronic molecules, they are typically not solution-processable and they are commonly deposited onto substrates by thermal vacuum sublimation or by organic vapor phase deposition. An optimized choice of substrate temperature can lead to a well-organized polycrystalline films.^[42] Therefore, they have high carrier mobility. Pentacene is a common example of a conjugated small molecule (Fig. 2.1b); the carrier mobility of pentacene is around $6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[43]

2.1.1 Molecular Structure

The atom is the basic building block of all matter; it consists of a dense central nucleus surrounded by a cloud of negatively charged electrons. When two or more atoms come close together, their valence electrons might interact leading to that their atomic orbitals combine

Figure 2.1: Chemical structures of selected common organic semiconductors. a) Head-to-Tail regioregular poly(3-hexylthiophene), P3HT. b) Pentacene.

linearly to form molecular orbitals (MO). The resulting MOs can be of two types, bonding and antibonding. Bonding MOs are formed due to constructive interference of atomic orbitals and are lower in energy than the original atomic orbitals since they stabilize the molecule. Conversely, antibonding MOs are the result of destructive interference of atomic orbitals and they destabilize the molecule and thus have higher energy. Consequently, there is splitting of the atomic single energy level into two molecular energy levels where the separation indicates the strength of the interaction of atomic orbitals. In the ground state, the electrons fill lower energy orbitals that give the lowest energy for the molecule. The highest energy orbital that is occupied with electrons is called Highest Occupied Molecular Orbital (HOMO) and the lowest energy orbital that is unoccupied by electrons is called Lowest Unoccupied Molecular Orbital (LUMO). The type of interaction between atomic orbitals can be further categorized by the molecular-orbital symmetry labels σ (sigma) and π (pi), where a σ bond is symmetrical with respect to rotation around the internuclear axis while a π bond is not. The π bond is weaker than the σ bond and thus has higher energy orbitals. The corresponding antibonding orbitals are called σ^* and π^* .

Polymers are macromolecules built-up from monomeric units covalently bonded to each other to form long chains upon polymerization.^[44] Polymer chains can have linear, branched, or a network structure. The backbone of organic polymers consists mainly of covalently bonded carbon atoms. An isolated carbon atom has $1s^2 2s^2 2p_x^1 2p_y^1$ electronic ground state configuration, and thus can only form two covalent bonds with other atoms. Close presence of other atoms around

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the carbon atom promotes one of the carbon 2s electrons to the empty 2p orbital, thus forming an excited state of the carbon atom ($1s^2 2s^1 2p_x^1 2p_y^1 2p_z^1$); thereby having four valence electrons available for bonding. Combining the 2s with one, two, or three of the 2p orbitals leads to the formation of two sp, three sp^2 , or four sp^3 hybridized orbitals, respectively. The electrical conductivity of a polymeric material ranges from insulating, via semiconducting, to conducting. This depends on the electronic states formed along the polymer chain from the electrons of the carbon atoms and how these interact with each other. Conventional insulating polymers are sp^3 hybridized where the four hybrid orbitals of the carbon atom form a tetrahedral-shaped structure with an angle of 109.5° between them, thus each of the hybrid orbitals is single-bonded to an adjacent atom through σ bonding. On the other hand, semiconducting polymers are sp^2 hybridized, where three of the four carbon valence electrons adopt sp^2 hybrid orbitals forming a planar structure separated by an angle of 120° while the remaining electron is described by one unperturbed p-orbital ($2p_z$) that is perpendicular to the rest of the orbitals. The hybrid orbitals form strongly localized σ bonds with other adjacent atoms, while the remaining $2p_z$ orbitals of two adjacent atoms overlap sideways to form delocalized π and π^* orbitals. Thus, the localized electrons in the σ bonds form the backbone in a polymer chain and dominate the mechanical properties, while the electrons in the π bonds are delocalized along the chain and are responsible for the electrical and optical properties of the conjugated polymer material. In the electronic ground state, the π bonding molecular orbitals will be filled with electrons and the higher energy π^* molecular orbitals will be empty. The number of discrete energy levels and the number of π and π^* orbitals is proportional to the number of carbon atoms in the conjugated polymer. For an infinitely long conjugated polymer, the discrete energy levels become so closely spaced that they form continuous bands. If the bonds between every two neighboring carbon atoms in the conjugated polymer are equally long, this would result in a half-filled band as in the case of a one dimensional metal. However, such configuration is not favored energetically according to Peierl's instability theorem which states that a one-dimensional metal is unstable against distortions of the lattice. Instead, the energetics of the conjugated system can be lowered by creating a π bond in addition to a σ bond, which is a double bond. This structure distortion will result in single (long) and double (short) bond alternation, hence opening up a band gap (E_g) in the range of 1 – 4 eV between the filled π band and the empty π^* band; thus rendering the polymer a semiconductor.^[45] The band gap of both semiconducting polymers and inorganic semiconductors is in the same range.

Figure 2.2: The splitting of molecular orbitals into bonding and antibonding levels and band formation in conjugated polymers.

It is quite common to designate the π and π^* bands as valence and conduction bands respectively. A series of alkenes is shown in Fig. 2.2 to illustrate how the energy level splitting and band formation occurs in conjugated polymers.

2.1.2 Charge Carriers and Charge Transport

A large range of electrical conductivity can be obtained upon introducing charges into polymers through doping; enabling polymers to behave as metals, semiconductors, or insulators. These charges are stored in different states called solitons, polarons, and bipolarons; depending on the material and the doping level.^[46] Various types of doping may be used such as electrochemical doping, electric field-effect doping, photo-induced doping, charge-injection doping, or chemical doping.^[47]

A few conjugated polymers have a degenerate ground state; i.e., two geometric structures corresponding to the same energy. An example of such material is trans-polyacetylene, where the

Figure 2.3: Energy levels of a neutral soliton, a positively charged soliton, and a negatively charged soliton.

single and double bond alteration can be arranged in two equivalent ways (degenerate ground states Fig. 2.3). Uneven number of carbon atoms in a polymer chain gives rise to a π -electron placed between two domains with opposite bond length alternations, with the boundary between the two domains extending over several carbon atoms. This unpaired electron along with the resulting bond distortion is called a soliton, and it is the relevant charge carrier in degenerate conjugated polymers.^[48] The energy level of a soliton is situated in the middle of the band gap. A neutral soliton consists of a single electron in a localized electronic state with spin $\frac{1}{2}$ whereas a charged soliton is spinless and consists of unoccupied or doubly occupied localized electronic state.

Most conjugated polymers have a non-degenerate ground state with a preferred bond order; i.e., the overall energy of the system changes upon reversing the bond length alternation. Upon introducing a charge (electron or hole) into the polymer chain, a local reorganization of the bond length alternation takes place in the vicinity of the charge. The combination of the charge and the associated lattice distortion is termed a polaron,^[49] and it is delocalized over a few monomeric units in the polymer chain. When two polarons get close together, they can lower their energy by sharing the same distortion, leading to the formation of a bipolaron which is more energetically stable. The polaron and bipolaron energy levels are localized inside the forbidden band with the bipolaron energy levels being located further away from the band edges as compared to those of a

Figure 2.4: The energy levels for a neutral molecule, a positively and negatively charged polaron, a positively and negatively charged bipolaron.

polaron. Polarons carry a spin while bipolarons are spinless. The energy levels of polarons and bipolarons are illustrated in Fig. 2.4.

Conjugated polymers are generally composed of microcrystallites connected by disordered amorphous regions, thus charge carriers tend to be delocalized on individual polymer chains due to the weak π -orbitals-overlap between neighbouring polymer chains.^[50] Since polymer chains are of a finite length and typically contain defects, charge transport through the entire polymer systems is achieved via thermally activated variable range hopping and tunneling between localized states across different polymer chains.^[51-54]

2.2 Electrolytes

An electrolyte is any substance that can dissociate into free ions (anions and cations). Applying an electric field across an electrolyte causes the anions and cations to move in opposite directions, thereby conducting electrical current while gradually separating the ions. Depending on their degree of dissociation, electrolytes are considered as either strong (completely or mostly dissociated into free ions) or weak (partially dissociated into free ions). The ionic conductivity level depends on the concentration of mobile ions. Electrolytes can be found in liquid, solid, and gelled state. Solid or gelled electrolytes are often preferred for use in solid-state devices. Various

Figure 2.5: Schematic representation of different types of electrolytes. See text for further explanation.

types of electrolytes that are commonly used in organic electronics include: electrolyte solutions, ionic liquids, ion gels, polyelectrolytes, and polymer electrolytes (Fig. 2.5).

2.2.1 Electrolyte Solutions

Electrolyte solutions are the most common type of electrolytes, as they basically consist of a salt dissolved in a liquid. Electrolyte solutions are usually suitable for electrochemical experiments. Water is a common solvent, but various organic solvents are sometimes favored due to their electrochemical stability. It is noteworthy to mention that pure water by itself is a weak electrolyte where it dissociates into hydroxide (OH^-) and hydronium (H_3O^+) ions, with a concentration of $0.1 \mu\text{M}$ under normal conditions.

2.2.2 Ionic Liquids

An ionic liquid is a room temperature molten salt consisting of ions and ion pairs with relatively large anions and cations. At least one ion has a delocalized charge and one component is organic, which prevents the formation of a stable crystal lattice. Ionic liquids have many interesting properties such as non-volatility, high ionic conductivity (ca. 0.1 S cm^{-1}),^[55] and chemical and thermal stability.^[56] They are highly viscous, frequently exhibit low vapor pressure, and have a melting point that is below 100°C . Such salts that are liquid at near-ambient temperature are important for electric battery applications, and have been used as sealants due to their very low vapor pressure.

2.2.3 Ionic Gels

An ion gel consists of an ionic liquid that is immobilized inside a polymer matrix,^[57] e.g. a polyelectrolyte^[58] or a block copolymer^[59]. Ion gels exhibit easy handling film forming properties of the solid-state combined with the high ionic conductivity of ionic liquids (in the range of $10^{-4} - 10^{-2} \text{ S cm}^{-1}$)^[60]. Ion gels are used as gate insulators for field effect transistors.^[60]

2.2.4 Polyelectrolytes

Polyelectrolytes are polymers with ionisable groups whose molecular backbone bears electrolytic repeat groups.^[61] When in contact with a polar solvent such as water, these groups dissociate leaving behind charged polymers chains and oppositely charged counter-ions that are released in the solution. Positively and negatively charged polyelectrolytes are termed polycations and polyanions respectively. In solid dry polyelectrolyte films, charged polymer chains are effectively immobile due to their large size while counter-ions are mobile, which gives rise to ion transport of counter ions. Examples of polyelectrolytes include poly(styrene sulphonic acid) or PSSH and poly(vinyl phosphonic acid-co-acrylic acid) or P(VPA-AA) which are shown in Fig. 2.6. PSSH and P(VPA-AA) are both anionic polyelectrolytes with typical room temperature ionic conductivity in the range of $10^{-8} \text{ S cm}^{-1}$ and $10^{-6} \text{ S cm}^{-1}$, respectively.^[31, 62] One of the applications of polyelectrolytes is their use as gate insulators in polyelectrolyte-gated organic field effect transistors due to their remarkable ability to suppressing electrochemical doping of the semiconductor bulk.^[30, 32]

Figure 2.6: Molecular structures of a) poly(styrene sulphonic acid) and b) poly(vinyl phosphonic acid-co-acrylic acid) with protons as the mobile counter-ions.

2.2.5 Polymer Electrolytes

Polymer electrolytes are solvent-free solid electrolytes consisting of a salt dispersed in a polar polymer matrix. Both the cations and the anions can be mobile in polymer electrolytes. Typical ionic conductivity is in the range of 10^{-8} to 10^{-4} S cm⁻¹.^[63] Polymer electrolytes are used in electrochemical device applications, namely, high energy density rechargeable batteries, fuel cells, supercapacitors, and electrochromic displays.

2.2.6 Ionic Conductivity and Transport

Ionic conduction behavior in electrolytes depends on the concentration and the mobility of the ions present in the electrolyte, where the concentration of ions is determined by the solubility and the degree of dissociation. The ionic motion is governed by two different processes: diffusion caused by a concentration gradient of ions and drift or migration caused by the presence of an external electric field. As to ionic transport, the mechanism is strongly dependent on the electrolyte nature.

In electrolytes with low molecular weight solvents, such as polyelectrolytes, the ions are surrounded by solvation shells formed by the solvent molecules. Hence, the ions along with the solvent molecules belonging to the solvation shells are transported as a package through the electrolyte. These ions experience a frictional force proportional to the viscosity of the solvent and the size of the solvated ion, which is the rate limiting factor for ionic mobility at low concentrations. On the other hand, transport of protons in aqueous solutions is done by hydrogen bonds rearrangement according to the Grotthuss mechanism: In aqueous solutions, a proton is immediately hydrated to form a hydronium ion, which subsequently transfers one of its protons to a neighboring water molecule that also transfers the proton to another molecule, and so on. This gives protons the high ionic conductivity in aqueous systems.

In electrolytes with high molecular weight solvents such as polymer electrolytes, the polymer matrix which is considered as the solvent is immobile. The ionic motion is strongly coupled to the mobility of the polymer chain segments, where the ions travel across the material by hopping from one site to another. Thus, the ionic conductivity in polymer electrolytes is owed to the flexibility of the polymer chains in disordered regions of their structure. This explains why

the ionic conductivity is low in polymers with much crystalline regions where the material is densely packed and does not have sufficient open space to allow for fast ionic transport.

2.2.7 Electric Double Layers

Electrolytes are ion conductors and electron insulators. Upon contact with a charged ion-blocking electrode, the electric potential difference between the electrode and the electrolyte gives rise to the formation of a region consisting of two parallel layers of positive and negative charges called the electric double layer (EDL). This is due to the interactions between the ions in the electrolyte and the electrode surface, where the outermost electrode surface holds an excess of electronic charges that are balanced by the redistribution of oppositely charged ions located in the electrolyte close to the electrolyte/electrode interface. The EDL charge distribution is divided into two distinct layers that are described by the Gouy-Chapman-Stern (GCS) model. It consists of a compact Helmholtz layer of ions located close to the electrode surface followed by a diffuse layer extending into the electrolyte bulk (Fig. 2.7). The Helmholtz layer comprises adsorbed dipole-oriented solvent molecules and solvated ions, which are assumed to approach the electrode at a

Figure 2.7: Schematic illustration of the Gouy-Chapman-Stern model of the ionic distribution in an electric double layer. The empty circles represent solvent molecules and the circles with the '+' and '-' signs represent solvated cations and anions respectively.

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distance limited to the radius of the ion itself and a single shell of solvated ions around each ion. Thus, the Helmholtz layer and the electrode are analogous to a parallel plate capacitor separated by a distance of few Ångströms^[64], with the potential drop occurring in a steep manner between the two plates. As to the diffusion layer, it consists of both positively and negatively charged ions with an excess of ions that are oppositely charged compared to the metal electrode. The potential profile in this layer has an exponential decay towards the bulk of the electrolyte. The thickness of the diffuse layer is dependent on the electrode potential and ionic concentration of the electrolyte. The capacitance of the entire double layer is typically in the order of tens of $\mu\text{F cm}^{-2}$.^[30]

3 Organic Field-Effect Transistors

Transistors are the fundamental building blocks in modern electronic circuitry. They are mainly used as either signal amplifiers or electronic gates and switches. The most common type of transistors is the field-effect transistor (FET). The field effect is a phenomenon in which an electric field, oriented in the normal direction with respect to the surface plane, controls the conductivity of a channel of one type of charge carriers in a semiconductor material. The electric field is generated from the voltage applied to the gate electrode in the device. The charge carriers in the transistor channel can be dominated by holes (positive charges) or electrons (negative charges), which defines whether the semiconductor is a p-type or n-type FET, respectively. An organic FET (OFET) is a kind of a FET where the semiconducting layer is an organic material. The first OFET was demonstrated and reported in 1986 by Tsumura et al.^[4]. Since then, OFETs have developed and evolved enormously and rapidly to attract widespread interest due to their low-cost fabrication methods and acceptable performances along large areas and on flexible substrates. Nowadays, they serve as the main component in cheap and flexible electronics demonstrators and they offer a promising platform for numerous novel applications by circumventing some of the limitations of inorganic materials while providing comparable device performance at a considerably reduced cost. Major applications include radio frequency identification (RFID) tags^[65, 66] and flexible displays^[67-69].

3.1 Device Operation

An organic field-effect transistor (OFET) is a three-terminal device comprising gate,

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source, and drain electrodes. The semiconductor layer, which is an organic material, acts as a conducting channel between the source and drain electrodes, and is separated from the gate electrode by an insulating layer referred to as the gate dielectric or gate insulator. The source and drain electrodes are separated by a region known as the channel, of length and width L and W , respectively. A schematic illustration of an OFET is shown in Fig. 3.1. The gate/insulator/semiconductor stack can be seen as a capacitor-like structure, with a capacitance per unit area, C_i , given by

$$C_i = \frac{\epsilon_0 \kappa}{d} \quad (3.1)$$

where ϵ_0 is the vacuum permittivity, κ is the relative permittivity, and d is the gate insulator thickness. Drain and gate voltages, V_D and V_G , are applied relative to the source electrode which is normally grounded and kept as a reference electrode ($V_S = 0$). Applying a negative (positive) potential to the gate electrode leads to the accumulation of positive (negative) charge carriers that are injected from the source electrode into the organic semiconductor (OSC), thereby increasing the semiconductor surface conductivity and thus modulating the source-to-drain conductance. These induced charges that form the transistor channel, are located within the first monolayer of the semiconductor layer near the insulator/semiconductor interface.^[70] Depending on whether positive (holes) or negative (electrons) charges are accumulated, the channel is called p-channel or n-channel, respectively. OFETs commonly operate in the accumulation mode, where an increase in the gate-source voltage enhances the channel conductivity.^[71] Thus, the transistor is normally in the OFF-state at zero gate voltage. However, examples of depletion-mode behavior in OFETs

Figure 3.1: Schematic illustration of an organic field-effect transistor.

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have also been reported, where the transistor is in the ON-state at zero applied gate voltage.^[72, 73]

The number of accumulated charges in the channel is proportional to the gate voltage and the capacitance of the insulator; however, some of these charges are trapped and will consequently not contribute to the current in the transistor. Thus, the applied gate voltage has to be higher than a certain voltage called the threshold voltage, V_T , before the channel becomes conducting and the transistor is turned “ON”, and hence the effective gate voltage is $V_G - V_T$. The threshold voltage depends strongly on the semiconductor and insulator materials used. It originates from several effects, such as the presence of traps at the insulator/semiconductor interface and the differences in the gate material and semiconductor work functions.^[74] Thus, the charge density or the accumulated mobile charges per unit area in the transistor channel, Q , at a specific gate voltage ($V_G > V_T$) with the absence of drain voltage, is given by

$$Q = C_i(V_G - V_T) \quad (3.2)$$

Hence, applying a gate voltage that exceeds the threshold voltage would induce a uniform distribution of the charge carriers in the transistor channel as shown in Fig. 3.2a. When a small drain voltage is applied ($V_D \ll V_G - V_T$), a linear gradient of charge density is formed from the source electrode towards the drain electrode. The potential within the channel is a function of the position x , where it increases linearly from the source ($x = 0$, $V(x) = 0$) to the drain electrode ($x = L$, $V(x) = V_D$). Thus, the induced channel charge density depends on the position x along the channel, and is given by

$$Q(x) = C_i(V_G - V_T - V(x)) \quad (3.3)$$

The drain current induced by the channel charge carriers at some position x in the channel, after neglecting diffusion, is given by

$$I_D(x) = W\mu Q(x)E_x(x) \quad (3.4)$$

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Figure 3.2: Illustrations of the different operating regimes of an OFET and the corresponding current-voltage characteristics. a) The linear regime, b) the start of the saturation regime at pinch-off point, and c) the saturation regime.

where μ is the field-effect carrier mobility of the semiconductor, and E_x is the lateral electric field at a position x along the channel. Substituting $Q(x)$ and $E_x = dV/dx$ into Eq. (3.4), and integrating both sides of the equation from $x = 0$ to L and $V(x) = 0$ to V_D while assuming that the mobility is independent of the charge carrier density; we find

$$I_D = \frac{W}{L} \mu C_i \left[(V_G - V_T) V_D - \frac{1}{2} V_D^2 \right] \quad (3.5)$$

However, the channel conductance remains constant at a very small V_D , and thus the drain current (I_D) is directly proportional to the drain voltage (V_D) (since $V_D \ll V_G - V_T$); which defines the linear regime of an OFET (Fig. 3.2a). In the linear regime, the drain current expression can be simplified to

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$$I_{D,lin} = \frac{W}{L} \mu_{lin} C_i (V_G - V_T) V_D \quad (3.6)$$

where the field-effect mobility in the linear regime (μ_{lin}) can be extracted by differentiating Eq. (3.6) with respect to the gate voltage at a constant drain voltage, and is given by

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G} \frac{L}{WC_i V_D} \quad (3.7)$$

As the drain voltage is further increased, the number of accumulated charge carriers in the channel close to the drain electrode decreases. When $V_D = V_G - V_T$ is reached ($V_D = V_{D,sat}$), the channel is pinched-off; i.e. a charge-depleted region is formed next to the drain electrode which results in the saturation of the drain current (Fig. 3.2b). Thus, a space-charge-limited saturation current ($I_{D,sat}$) flows through this depleted region and the potential at the pinch-off point is the effective gate voltage ($V_G - V_T$). This point denotes the start of the saturation regime. A further increase in the drain voltage ($V_D > V_G - V_T$) results in the broadening of the charge-depleted region without any substantial increase in the drain current. Therefore, the pinch-off point moves away from the drain electrode towards the source electrode, which leads to the reduction of the channel length to an effective value L' (Fig. 3.2c). The potential at the pinch-off point remains constant ($V(x) = V_G - V_T$) resulting in a constant potential drop between the pinch-off point and the source electrode, and hence the drain current remains constant and is said to saturate ($I_{D,sat}$). This is known as the saturation regime. Neglecting channel shortening to L' , the saturation drain current is obtained by substituting $V_D = V_G - V_T$ into Eq. (3.5) as follows

$$I_{D,sat} = \frac{W}{2L} \mu_{sat} C_i (V_G - V_T)^2 \quad (3.8)$$

where the field-effect mobility in the saturation regime can be extracted from Eq. (3.8) as follows

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_{D,sat}}}{\partial V_G} \right)^2 \frac{2L}{WC_i} \quad (3.9)$$

Note that the above equations are only valid if the gradual channel approximation holds. This implies that the transverse electric field generated by the applied gate voltage that is perpendicular to the drain current flow is much larger than the lateral electric field parallel to the current flow induced by the applied drain voltage. This holds for long channel transistors where the channel length is much larger than the gate-insulator thickness ($L > 10 d$).^[75] If the constraints of the gradual channel approximation do not hold, a space-charge-limited bulk current will prevent saturation and the gate voltage will not determine the “on” or “off” state of the transistor.^[76, 77]

3.2 Transfer and Output Characteristics

The current-voltage characteristics of an OFET are generally classified as transfer characteristics (I_D versus V_G) and output characteristics (I_D versus V_D) depending on whether V_G is varied while V_D is fixed, or vice versa. Fig. 3.3 shows typical transfer (Fig. 3.3a) and output (Fig. 3.3b) characteristics of a p-channel OFET with a channel length and width of 2.5 μm and 1 mm, respectively. In the transfer characteristics, it is quite common to have a semi-log plot since the drain current variation range is usually over several decades. The transfer characteristics show how effectively the gate voltage can switch the transistor “ON” or “OFF”. Several important parameters can be extracted from the transfer characteristics such as the on/off current ratio, the subthreshold swing, the field effect mobility in the linear and saturation regimes, and the threshold voltage. The on/off current ratio, I_{on}/I_{off} , is the ratio of the drain current in the on-state at a certain gate voltage to the drain current in the off-state. It is desirable to have this ratio as large as possible. The off-current is determined by gate leakage, the conduction pathways at the substrate interface, and the bulk conductivity of the semiconductor. As to the subthreshold swing, it is the inverse of the slope of the transfer curve in the subthreshold region; the region where the gate voltage is lower than the threshold voltage, and is given by

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)} \quad (3.10)$$

The subthreshold swing depends on the gate insulator capacitance and the trap states at the

Figure 3.3: Representative current-voltage characteristics of a p-channel OFET with a channel length and width of 2.5 μm and 1mm, respectively. a) Transfer characteristics indicating the threshold voltage extraction from the intersection of the linear fit to the square root of the drain current with the V_G -axis. b) Output characteristics. This data is related to the paper “Bias stress effect in inverters based on polyelectrolyte-gated organic field effect transistors”

interface. The field-effect mobility in the linear regime, μ_{lin} , is directly proportional to the gradient of the drain current increase in the linear regime according to Eq. (3.7). Fig. 3.3a also shows the plot of the square root of the drain current versus the gate voltage. From this plot, the field-effect mobility in the saturation regime can be estimated by calculating the slope of the curve in the saturation region according to Eq. (3.9). Also, the threshold voltage can be extracted from this plot by extrapolating the linear fit of the square root of the drain current in the saturation region to the gate voltage axis.

The output characteristics are displayed by a plot of the drain current versus the drain voltage, at various fixed gate voltages. For a given gate voltage, the drain current initially increases linearly with the drain voltage and then levels-off as V_D becomes larger than the effective gate voltage ($V_G - V_T$). In this plot, we can clearly distinguish the linear and saturation regimes.

3.3 OFET Structure

There are four different possible OFET configurations (Fig. 3.4). In all these configurations, the source and the drain electrodes are always in contact with the organic semiconductor film and the gate is isolated from the rest by the insulating layer. The different

Figure 3.4: Typical OFET configurations with the corresponding position of the channel associated with each configuration.

configurations are: top-gate/bottom-contact, bottom-gate/top-contact, top-gate/top-contact, and bottom-gate/bottom-contact. The choice of which configuration to be used usually depends on the availability of suitable substrates and the available fabrication technique. The main difference between these configurations is in the sequence of deposition of the different layers which affects the choice of the material of the different layers since the solvents used to deposit the upper layers should not dissolve or damage the layers beneath. In addition, OFETs' charge transport occurs within 1–2 nanometers of the semiconductor/insulator interface. Thus, optimizing the properties of this buried interface, such as its roughness, trap density, and orientation and interchain packing of molecules, will provide the key to future advances in the performance of OFETs. Moreover, the position of the transistor channel in terms of the source and drain contacts is altered depending on the configuration used. Thus, top-gate/bottom-contact and bottom-gate/top-contact configurations mainly exhibit lower contact resistance owing to the possibility to inject and extract charge carriers over a broad front of the source and drain electrodes.

3.4 Electrolyte-Gated Organic Field Effect Transistor (EGOFET)

Over the past two decades, OFETs have gained considerable attention owing to their potential as alternatives to conventional inorganic counterparts in low-cost large-area flexible electronic applications. A majority of the OFETs reported to date can only operate well at voltages beyond 20 V.^[78] However, implementing low-cost flexible-electronic-applications enforces several requirements that OFETs must comply with including low-operating voltages (in the range of few volts), low-temperature processing, mechanical flexibility and compatibility with flexible substrates, and low-cost robust processing techniques such as printing. Tremendous efforts have been devoted to achieve low-voltage OFETs while maintaining high output current levels which can be accomplished by using a high capacitance gate insulator. The approaches proposed to achieve this include using a high-permittivity (κ) insulator,^[79] using a nanometer-thick self-assembled monolayer of organic compound as the gate insulator,^[78, 80, 81] or using an electrolyte as gate insulator.^[82-86] However, organic materials normally have low permittivity values and depositing very thin insulator layers is not possible with the low-cost printing techniques. Therefore, we will focus here on the third approach which is using an electrolyte as the gate insulator material. The idea of using electrolyte-gating in transistors is far from new. Plenty of work on electrolyte-gated organic field-effect transistors (EGOFETs) have been previously reported with various electrolyte systems explored such as ionic liquids,^[87, 88] ion gels,^[60, 89, 90] polymer electrolytes,^[91-94] and polyelectrolytes.^[30, 32, 95]

3.4.1 EGOFET Principle of Operation

An EGOFET differs from a conventional OFET by having an electrolyte as a gate insulator instead of a dielectric layer. The layout of a p-channel EGOFET is shown in Fig. 3.5a. The operation of an EGOFET is quite similar to that of an ordinary OFET with the difference being in terms of the charge polarization characteristics of the gate insulator. Applying a negative potential to the gate electrode will lead to the redistribution of the ions inside the electrolyte where the cations migrate towards the negatively charged gate electrode and the anions towards the semiconductor which induces the accumulation of positive charge carriers (holes) in the semiconductor channel. This results in the formation of two electric double layers (EDLs) at the

Figure 3.5: a) Schematic illustration of a p-channel electrolyte-gated organic field-effect transistor (EGOFET). b) Schematic illustration of a p-channel EGFET operating in the electrochemical mode.

semiconductor/electrolyte interface (lower EDL) and the electrolyte/gate interface (upper EDL) leaving a charge-neutral bulk in the middle of the electrolyte. After the EDLs are established and steady-state is reached, the driving force for ion migration in the electrolyte bulk is eliminated and the entire applied gate voltage is nearly dropped across the two EDLs with the electric field being very high at the interfaces and negligible in the charge-neutral electrolyte bulk.^[96] The EDLs act as nanometer-thick capacitors, hence they provide the transistor with high interfacial capacitances that enables these devices to operate at low voltages (< 2 V).^[97] The total capacitance of the electrolyte is the series equivalent of the two EDLs' capacitances which is dominated by the capacitance of the semiconductor/electrolyte interface which is typically smaller. Thus, the electrolyte capacitance is independent of the gate insulator thickness which enables the use of thicker electrolyte layers while maintaining low-voltage operation.^[98] The typical capacitances of electrolyte-gates in thin-film transistors are on the order of ($C_i \sim 1\text{-}10 \mu\text{F cm}^{-2}$)^[97] which exceeds the capacitances of conventional high-permittivity dielectrics^[99] and that of ultra-thin dielectrics.^[100] It is worthwhile noting that it is possible for the ions in the electrolyte to penetrate into the organic semiconductor layer, resulting in the intentional or unintentional electrochemical doping of the semiconductor bulk, which causes the transistor to operate in the electrochemical mode (Fig. 3.5b) that will slow the switching speed.^[92, 101] An EGFET that undergoes electrochemical doping is no longer an OFET and is referred to as an organic electrochemical transistor instead.

3.4.2 Polyelectrolyte-Gated OFET Characteristics

Electrolyte-gated organic field effect transistors can be classified according to the permeability of the organic semiconductor to the ions in the electrolyte. Transistors that employ permeable semiconductors tend to exhibit electrochemical behavior upon increasing the gate bias which switches their operation mode from field-effect to electrochemical, thus they are termed electrochemical transistors. This potential drawback has been reported in several ion gel-gated and polymer electrolyte-gated transistors.^[101, 102] One way to mitigate this problem is by the use of a polyelectrolyte as the gate insulator material which has been previously demonstrated in several papers.^[30, 32, 95] This is attributed to the fact that charged polymer chains in polyelectrolytes are effectively immobile and only the small counter-ions are mobile which prevents the ion penetration into the organic semiconductor bulk. For instance, applying a negative gate bias to a polyanion-gated OFET causes the mobile cations to move towards the gate leaving bulky polyanions at the semiconductor/electrolyte interface which are less likely to diffuse into the semiconductor. Other advantages of employing polyelectrolyte-gated OFETs include large capacitance value of the EDLs regardless of the gate insulator thickness, low voltage operation ($< 1\text{ V}$),^[30, 32] compatibility with printed batteries, delivery of large drive currents, and fast switching times ($< 100\text{ }\mu\text{s}$).^[95] Since the EDLs spontaneously form at the insulator/semiconductor interface upon applying a gate bias, the transistor performance is insensitive to the gate electrode misalignment or to the variations in thickness and roughness of the gate insulator layer which eases the manufacturing requirements and enables robust manufacturing. These features make polyelectrolyte-gated OFETs promising candidates for flexible electronic applications.

3.5 Inverters

An essential route for the field of organic electronics is to move beyond discrete devices fabrication towards integrated circuits manufacturing to allow the demonstration of real functions. Signal processing circuits is one of many applications of OFETs. The basic circuit element for digital circuit design is the logic inverter or the NOT gate which is used to build logic gates and more complicated digital circuits. The inverter functions as a complementary switch where a high input signal results in a low output signal and vice versa. To date there are two demonstrated

Figure 3.6: Equivalent electric circuit layout of a p-type unipolar inverter with a) saturated load and b) depleted load. V_{in} is the input voltage, V_{out} is the output voltage, and V_{DD} is the supply voltage. The driver and load transistors are denoted in each configuration.

technologies for the fabrication of organic integrated circuits: the unipolar and the complementary technology. Unipolar inverter circuits are inverters built with a pair of the same type of transistors, i.e., either p-channel or n-channel transistors only. Using p-channel OFETs is more common due to the fact that p-type organic semiconductors with promising hole transporting mobilities are more abundant than n-type organic semiconductors. While complementary inverter circuits composed of both n-type and p-type transistors are more desirable owing to high signal integrity and low power consumption, most of the best developed organic semiconductors for use in circuits are p-type materials. Most n-type organic semiconductors suffer from very low electron mobility and are easily degraded in the atmosphere. However, recently several air-stable n-type organic semiconductors with promising electron mobility levels have been developed, and organic complementary inverter circuits have been reported.^[103] The common layouts of a unipolar inverter circuit with saturated load and depleted load configurations are shown in Fig. 3.6a and Fig. 3.6b, respectively. The unipolar inverter circuit consists of a driver transistor and a load transistor connected in series. The supply voltage (V_{DD}) is connected to the drain electrode of the load transistor and the input and output signals (V_{out} and V_{in}) are connected to the gate and drain electrodes of the driver transistor, respectively. When the gate and drain electrodes of the load transistor are connected together, the load transistor operates in the saturation regime and hence the inverter is termed a saturated load inverter. On the other hand, when the gate and source

Figure 3.7: The voltage transfer characteristic of an inverter.

electrodes of the load transistor are connected together, the load transistor is constantly turned off and thus the inverter is designated as a depleted load inverter. For circuits made from a single organic semiconductor for both driver and load OFETs, they are based on all enhancement-mode,^[104] ambipolar,^[105] or depletion-mode transistors.^[106] In such circuits, the swing is limited and tuning the threshold voltage of the driver transistor or using different device dimensions between the driver and load transistors is required in order to make the inverter characteristics more symmetrical. The typical inverter transfer characteristic curve, V_{out} versus V_{in} , is shown in Fig. 3.7. Inverter noise margins and gain can be estimated from the transfer characteristics. The inverter gain is given by

$$gain = \frac{\partial V_{out}}{\partial V_{in}} \quad (3.11)$$

The output and input voltages are equal to each other at an input voltage V_M , which is denoted as the switching threshold voltage. V_{OH} and V_{OL} correspond to high and low output voltage values, respectively. V_{IL} and V_{IH} correspond to the input voltage at which the slope of the curve, or the gain, is equal to -1. We can observe from the transfer characteristic curve that there is a range of input voltages (from V_{OL} to V_{IL}) that produces a high output voltage, and a range of input voltages

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(from V_{IH} to V_{OH}) that produces a low output voltage. These ranges of input voltages are known as noise margins. In particular, the noise margin for high input voltages, NM_H , is defined as

$$NM_H = V_{OH} - V_{IH} \quad (3.12)$$

Similarly, the noise margin for low input voltages, NM_L , is defined as

$$NM_L = V_{IL} - V_{OL} \quad (3.13)$$

The higher the gain and the larger the noise margins are, the better the inverter is. In ideal cases:

$$V_M = \frac{V_{DD}}{2} \quad , \quad V_{OL} = 0 \quad , \quad V_{OH} = V_{DD} \quad , \quad NM_L = NM_H$$

4 Bias Stress

Reliability of transistors is one of the main issues that has been extensively addressed over the past years. Device stability, particularly with respect to electrical stress, has been studied for more than 20 years. The basic observation found in most transistors is manifested in a gradual shift in the transistor threshold voltage upon a prolonged gate voltage application, which results in the degradation of the transistor drain current. This undesirable operational instability is referred to as the “bias stress effect”. In most systems, trapping of the channel mobile charge carriers is the main cause behind bias stress. Bias stress is a longstanding problem in both organic and inorganic semiconductor field-effect transistors and it is usually reversible. Investigation of this phenomenon is of paramount importance for practical reasons and for understanding the fundamentals of the energetic structure of the semiconductor-insulator interface. The origin of this effect has been heavily debated and there are several proposed mechanisms related to extrinsic and intrinsic phenomena.

4.1 Bias Stress and Recovery in OFETs

OFETs are emerging as the basic building blocks of low-cost contactless identification transponders, pixel drivers of flexible active matrix displays, and electronic barcodes.^[20, 107, 108] However, further development towards commercially viable OFETs is impeded by their lack of long-term operational stability. Operational instability, such as the bias stress effect, manifests itself as a decrease of the drain current with time triggered by the gradual threshold voltage shift towards the applied gate bias voltage.^[34, 109] The threshold voltage defines the applied gate voltage

Figure 4.1: Transfer curves of a polyelectrolyte-gated OFET during a) stressing and b) recovery as a function of time. The interval of stressing and recovery is indicated in hours (hr). The stressing and recovery were measured up to 3 hours with a 5 minutes stressing and recovery cycles after which a transfer sweep was recorded. The applied gate bias during stressing was -0.5 V along with a drain bias of -0.1V. The gate and drain electrodes were grounded during recovery cycles. The measurement was done at 22 °C, 40% RH, and in darkness. The inset in (a) shows the schematic cross section of the transistor. The transistor has a channel length and width of 2 μm and 500 μm , respectively. The thickness of the organic semiconductor (P3HT) and the polyelectrolyte (PSSH) is 30 nm and 100 nm, respectively. This work is related to the “Bias stress effect in polyelectrolyte-gated OFETs” paper.

at which a transistor switches to the ON-state. As an example, an undesired outcome in an active matrix display would be the unintended switching-off of an OFET driving a pixel in the course of time as a consequence of the threshold voltage shift. Since the total amount of accumulated charges in the OFET channel close to the semiconductor/insulator interface is determined by the applied gate voltage, this implies that the channel mobile charges undergo a certain process in which they are transformed into immobile charges. However, the form and precise location of these immobile charges and identification of the origin behind this effect have remained elusive.

Bias stress has been studied and reported for a wide variety of organic semiconducting materials and different device structures. A common way to investigate bias stress effect is by applying a continuous fixed voltage to the gate electrode for a certain period of time, referred to as the stressing interval, which can extend from few hours to days. After the stressing interval, the transistor electrodes are all grounded for a certain period of time, known as the recovery interval. The stress and recovery behavior is monitored by interrupting the stressing interval with periodic swift sweeps (in the range of few seconds) of the gate voltage at a fixed drain voltage, during which the drain current is measured at a small applied drain voltage and the transfer characteristics

Figure 4.2: a) Normalized drain current of the transistor as a function of time during stressing and recovery measured at $V_G = -0.5$ V and $V_D = -0.1$ V. b) Threshold voltage of the transistor versus time during stressing and recovery. The interval of stressing and recovery is indicated in hours (hr). The stressing and recovery were measured up to 3 hours with a 5 minutes stressing and recovery cycles. The applied gate bias during stressing was -0.5 V along with a drain bias of -0.1V. The gate and drain electrodes were grounded during recovery cycles. The measurement was done at 22 °C, 40% RH, and in darkness. This work is related to the “Bias stress effect in polyelectrolyte-gated OFETs” paper.

of the transistor are recorded. A set of such measurements is illustrated in Fig. 4.1a and Fig. 4.1b. In this measurement, the bias stress is recorded for a p-type top-gate/bottom-contact polyelectrolyte-gated organic field effect transistor. The main effect of the prolonged applied gate bias is a shift of the transfer curves in the direction of the applied gate bias during stressing (Fig. 4.1a) and a shift back to the initial state (prior to stressing) during recovery (Fig. 4.1b) which demonstrates that bias stress is a reversible process. The normalized drain current during stressing and recovery is shown in Fig. 4.2a. It is clear that the current decreases during stressing and increases during recovery until its initial value is approximately reached. Using the transfer curves data, the threshold voltage can be extracted from the intersection of the extrapolation of the linear fit to the square root of the drain current in the saturation region with the gate voltage axis, as shown in Fig. 3.3a. Fig. 4.2b shows the threshold voltage as a function of time during stressing and recovery. As commonly seen, the shift in the threshold voltage during stressing ends when it is equivalent to a value close to the applied gate bias. The decay in the drain current during stressing starts as a fast decay and then slows down until it saturates at a certain level where no more decay is observed. Similarly, the threshold voltage increases rapidly at the beginning of the

stress interval and then slows down and saturates with time at a value close to that of the applied gate stress voltage.

4.2 Proposed Mechanisms

There have been many different theories proposed to explain the mechanism responsible for the bias stress effect in OFETs. One of the most commonly suggested mechanisms involves the gradual trapping of the channel mobile charge carriers in pre-existing or stress-generated deep localized states located either in the organic semiconductor,^[35, 110] the gate insulator,^[111] or at the semiconductor/insulator active interface.^[112, 113] Once trapped, they no longer contribute to the current, thus giving rise to the observed decay in the ON drain current level. However, the trapped charge carriers still contribute to the electrostatic charge on the gate insulator induced by the applied gate voltage. Hence, a higher gate voltage is required in order to maintain the same mobile charge carrier concentration and current level, thus causing the observed threshold voltage shift over time.

It has been also suggested that the mechanism of bias stress effect in OFETs involves pairing of the semiconductor mobile carriers to form a tightly bound state called a bipolaron, given that the number of holes (in a p-type OTFT) removed from the channel per time and area is proportional to the square of their concentration.^[114] The mechanism is based on the idea that immobile bipolarons are formed when two holes collide with each other in the transistor channel. The formation of bipolarons is equivalent to trapping in the notion that the tightly bound state is immobile.

Moreover, it has been proposed that the mechanism responsible for bias stress in OFETs is based on the hole-assisted generation of protons from water in the accumulation layer, and their subsequent migration into the gate insulator.^[115, 116] This mechanism is associated with the electrolysis of residual water present at the semiconductor/insulator interface, where holes are converted to protons that consequently migrate into the gate insulator leading to a shielding of the gate electric field, henceforth triggering the threshold voltage shift. The mechanism for bias stress that is proposed in our p-type top-gate/bottom-contact polyelectrolyte-gated OFETs is similar to

Figure 4.3: A cross section of a p-type top-gate/bottom-contact polyelectrolyte-gated OFET showing the bias stress mechanism where in the presence of water a hole is converted into a proton that subsequently migrates into the gate insulator towards the gate/polyelectrolyte interface creating an additional proton that is not balanced, thus leading to a shift of the threshold.

this one. It involves an electron transfer from adsorbed water present at the semiconductor/polyelectrolyte interface to the positively charged semiconducting channel in the transistor (P3HT^+ in our case). The products of the water oxidation are a proton and a dioxygen:

The produced protons slowly penetrate into the polyelectrolyte through the negative gate bias which leads to the threshold potential shift and explains the bias stress phenomenon as shown in Fig. 4.3.

The effect of illumination on the recovery process has been heavily debated, where exposure to light with an energy above the band gap of the semiconductor has been found to accelerate the de-trapping process significantly.^[35, 117] The basic claimed mechanism involves quenching of excitons by trapped charges. The idea here is that the absorbed photons leads to the formation of electron-hole pairs (excitons) in the organic semiconductor. When a photo-generated exciton collides with a trapped hole, it is possible that this leads to the recombination of the electron (from the exciton) with the trapped hole leaving behind a mobile hole capable of escaping from the channel.

4.3 Characterization and Analysis of Bias Stress

For a quantitative assessment of bias stress in an OFET, it has become customary to fit the threshold voltage shift ($\Delta V_T(t)$) to a stretched-exponential function^{[110, 118] [119]} as follows:

$$\Delta V_T(t) = (V_T(\infty) - V_T(0)) \left[1 - \exp \left(- \left(\frac{t}{\tau} \right)^\beta \right) \right] \quad (4.1)$$

where $V_T(\infty)$ is the threshold voltage when equilibrium has been reached and is typically equal to the applied gate bias, $V_T(0)$ is the threshold voltage prior to stressing, τ is the relaxation time, and β is the stretching or dispersion parameter ($0 < \beta \leq 1$). The relaxation time (τ) and the dispersion parameter (β) are given by:

$$\tau = \nu^{-1} \exp \left(\frac{E_a}{k_B T} \right) \quad (4.2)$$

$$\beta = \frac{T}{T_o} \quad (4.3)$$

where ν is the frequency prefactor, E_a is the mean activation energy for trapping, k_B is the Boltzmann constant, T is the temperature, and T_o is the characteristic temperature of trap states. This fitting model has been developed and used extensively for analyzing the threshold voltage shift in amorphous silicon based field effect transistors.^[120] The stretched exponential function has a faster than exponential response early in the process (for times up to τ) and a slower than exponential response later in the process (for times beyond τ). The stretching parameter, β , acts as an indicator of the degree of diversion from the exponential behavior, with $\beta = 1$ being the exponential function and $\beta \ll 1$ giving a broader distribution of the function. Fig. 4.4a shows the stretched exponential fit of the threshold voltage shift in a p-type top-gate/bottom-contact polyelectrolyte-gated organic field effect transistor. While curve fitting the threshold voltage shift using the least square method, β and τ are treated as fitting parameters. This fitting procedure is useful when comparing the stability of different OFETs. Further analysis of the trapping dynamics and determination of the activation energy is done by performing temperature-dependent bias stress measurements. After curve fitting the threshold voltage shift with the stretched exponential

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Figure 4.4: a) Stretched exponential fit of the threshold voltage shift during stressing at 22 °C showing the extracted values for the dispersion parameter (β) and the relaxation time (τ). b) A linear fit of the relaxation time (τ) versus the reciprocal of the temperature. Activation energy for the transport of protons and the frequency prefactor are extracted from this figure. All measurements are under nitrogen atmosphere, 5% RH, and in darkness. These data are presented in the “Bias stress effect in polyelectrolyte-gated OFETs” paper.

function for the various temperatures, β and τ are extracted for each measurement. As shown in Fig. 4.4b, by plotting the logarithm of the relaxation time, τ , against the reciprocal of the temperature, the activation energy and the frequency prefactor can be estimated. A straight line is obtained in Fig. 4.4b which indicates that the relaxation time is thermally activated.

5 Experimental and Fabrication Methods

5.1 Device Fabrication

Organic transistor fabrication includes different production stages, since OFETs are built-up from multilayered structures and electrode patterns. Printing of the different elements of an OFET is a promising route towards low cost fabrication of circuits based on organic materials, but has many challenges which stem from the inherent incompatibility and wettability issues of the materials used in the different transistor layers. Common conventional techniques used to deposit the various building blocks of a transistor include thermal evaporation, photolithography, and spin-coating. Throughout all papers included in this thesis, deposition of transistor electrodes was done by thermal evaporation through a shadow mask or by thermal evaporation combined with photolithography and wet etching to achieve the required pattern. Deposition of the organic semiconductor and the polyelectrolyte films was done by either spin-coating or inkjet printing. Inkjet printing was selected as the deposition technique owing to its flexibility, short lead-time for small sample series, low cost, non-contact, and additive approach where material waste is minimized while delivering a wide range of functional materials.

5.1.1 Inkjet Printing

The process of inkjet printing consists of the ejection of fluid-ink, in the form of droplets, from a chamber through a nozzle to form a pattern on a substrate. Then the pattern is dried out through evaporation or post thermal annealing treatment. In piezoelectric drop on demand systems, a droplet is ejected from a reservoir through a nozzle by means of an electromechanical pressure

Figure 5.1: Schematic illustration of a piezoelectric DOD inkjet printer.

generated upon applying a voltage pulse to the piezoelectric transducer, as shown in Fig. 5.1. Thus, the droplet is issued due to the mechanical deformation of the piezoelectric material under the application of an electric field. The drop formation cycle consists of four phases, illustrated in Fig. 5.2, which are the start or standby phase, the relaxed phase, the drop ejection phase, and the recovery phase. During the start phase, the fluid chamber is slightly depressed to prevent the ink from falling down of the nozzle. Then, during the relaxed phase the piezoelectric material is brought to a neutral straight where a zero piezo-voltage is applied, leading to a maximum volume of the fluid chamber and to the fluid being drawn from the reservoir into the chamber and also pulled back from the nozzle. After that, the chamber is strongly compressed which generates a

Figure 5.2: Schematic illustration of the drop formation mechanism in a piezoelectric DOD inkjet printer.

pressure that causes drop ejection from the nozzle. In the final phase, the chamber is brought back to its initial slightly decompressed position to partially refill the fluid chamber in preparation for the next cycle, where there is also a pull-back on the nozzle meniscus.

The inkjet printer used for the fabrication of devices reported in this thesis is the Dimatix material printer DMP-2800, shown in Fig. 5.3a and Fig. 5.3b, which is a piezoelectric drop-on-demand (DOD) inkjet printer provided by Fujifilm Dimatix. The printer is based on the electromechanical coupling achieved via the piezo-electric actuator using MEMS technology, and the acoustic-fluid dynamics coupling done through the drop formation mechanism accomplished by tuning the input voltage waveform that deforms the fluid chamber. As voltage pulses are applied, ink droplets are ejected by a pressure wave created by the mechanical deformation motion of the piezo-ceramic material causing the ink volume change in the pressure chamber. This generates a pressure wave that propagates towards the nozzle. DMP-2800 allows the deposition of fluid materials on an A4-sized substrate with a maximum thickness of 25 mm using a disposable piezo-driven inkjet cartridge of a reservoir capacity of 1.5 ml, placed in the print carriage. The cartridge has 16 nozzles linearly spaced at 254 μm with nominal drop sizes of 1 pl (9 μm diameter nozzle) or 10 pl (21 μm diameter nozzle), depending on the cartridge type used. Using 1 pl cartridges is more challenging due to easier nozzle clogging. Normally, ink-jetting a 10 pl drop produces a 40 μm spot size on a polymeric substrate. Cartridges are available in two grades of chemical inertness, where the DMCLCP cartridges are more resistant to organic solvents. The

Figure 5.3: a) A digital photo of DMP-2800. b) An illustration of the printer's main components. ©2007 FUJIFILM Dimatix, Inc. Reprinted with the permission of FUJIFILM Dimatix, Inc.

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cartridge has a built-in heater capable of heating the fluid from ambient to a maximum temperature of 70 °C. However, heating the ink can result in faster nozzle clogging due to solvent evaporation, especially in the case of volatile solvents, and thus it is favorable to keep the cartridge fluid at room temperature (RT). The print carriage also contains a fiducial camera that assists in alignment procedures, in measuring the size of printed lines and droplets, and in quality inspection and evaluation of the printed pattern. The fiducial camera has three different light operation modes which are the bright field, dark field, and a combination of both dark and bright field.

As to the platen, it is a perforated metal surface that acts as the substrate holder which secures the substrate in place through a vacuum system. The temperature of the platen can be adjusted from ambient up to 60 °C, which is useful in controlling the drying behavior and the spreading of the ink-jetted droplets on the substrate.

The system is also provided with a stroboscopic camera at the drop watcher station which allows direct monitoring of the drop formation and the actual jetting of the nozzles which is critical for adjusting the jetting performance prior to printing. The jetting performance is said to be optimal if single spherical drops are ejected from the nozzles in a direction perpendicular to the nozzle plate and parallel to one another with matched velocities, which in turn gives higher precision in terms of droplets deposition and allows minimal spreading on the substrate. To reach optimal jetting performance, several parameters have to be modified in the cartridge settings with the help of the drop watcher camera system such as the firing voltage, jetting frequency, the number of jetting nozzles used, the cartridge maintenance operations during printing, and the voltage waveform selected. The firing voltage corresponds to the voltage applied to deform the piezoelectric crystal required for a droplet ejection, and it can be adjusted for each nozzle independently. The drop velocity is adjusted through the firing voltage where a higher firing voltage results in a higher drop velocity, and vice versa. The maximum firing voltage supported by the system is 40 V. It is noteworthy to mention that varying the firing voltage can affect the droplet shape and direction as well where a high firing voltage produces more compact droplets but with a long tail while a low firing voltage can reduce the tail and the droplets-scattering but can lead to misdirected drops and higher probability of nozzle clogging during printing, which has to be taken into consideration when setting the firing voltages. As to the jetting frequency, it is defined as the frequency at which the droplets are ejected from the nozzles, basically affecting the

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printing speed and precision. Thus, a higher jetting frequency gives a higher throughput and faster printing at the cost of precision and accuracy in droplet deposition, and vice versa. The maximum jetting frequency is 80 kHz. The choice of the number of nozzles to be used in the printing procedure depends on the pattern and precision required, and on the obtained jetting performance of adjacent nozzles. Thus, using few jets is more suitable in the case where finely-defined patterns and high accuracy and resolution are required, while using many nozzles leads to faster printing at the cost of resolution and is more suited for printing rough layers. Maintaining the cartridge during, prior, and after printing is also essential for good jetting performance. This is done by the aid of the cleaning station, or blotting station, where a disposable cleaning pad soaks up the ink from the nozzle plate. There are three different cleaning functions that can be run individually or combined as a cleaning cycle which are purging, blotting, and spitting. Purging is the most efficient solution for clearing clogged nozzles and consists of pushing the fluid out of the nozzles by applying pressure to the outside of the fluid bag, thereby also ensuring that all nozzles are free from air-bubbles. Blotting function removes excess fluids present in proximity of the nozzles by keeping the nozzle plate in contact with the cleaning pad. As to the spitting function, it is useful for fluids prone to clogging where it clears the nozzles from any clogging formed at the nozzle orifice by jetting a predetermined number of drops at a predetermined frequency to keep the fluid path surface wet. It is recommended to run the desired cleaning cycle prior to printing, and during printing as well if necessary to avoid nozzle clogging especially in the case of a long lasting printing process. When fine structures are printed, running cleaning cycles during printing is avoided since the nozzle plate can be slightly moved during the cleaning procedure which might result in misaligned printed stripes. Using the waveform editor, the shape of the input voltage waveform cycle that deforms the fluid chamber, consisting of a jetting waveform and a non-jetting waveform, can be manipulated which allows the user to adjust the whole jetting process and to control the droplets formation and break-off as they are ejected from the nozzles. Depending on the jetted fluid, the waveform has to be adjusted to achieve the most optimal jetting performance.

The printing action proceeds in a raster-style where the print carriage moves horizontally (x -direction) above the substrate while the platen shifts vertically (y -direction). Depending on the desired printing resolution, the drop spacing, i.e. the distance between the centers of two adjacent drops, is set accordingly. As shown in Fig. 5.4, the horizontal printing resolution (x -direction) is managed by the an encoder signal while the vertical printing resolution (y -direction) is determined

Figure 5.4: Printed pattern resolution in x- direction and y-direction. The resolution in x-direction is managed by an encoder. The resolution in y-direction depends on the cartridge saber angle and the native print head resolution (or nozzles separation). ©2007 FUJIFILM Dimatix, Inc. Reprinted with the permission of FUJIFILM Dimatix, Inc.

by the native print-head resolution (the distance between two adjacent nozzles, 254 μm) and the cartridge saber angle, i.e. the angle between the print carriage scan direction and the nozzles plate, which is set manually by the user through a rotating system. The maximum achievable resolution is 5080 dpi corresponding to a drop spacing of 5 μm and a saber angle of 1.1°, while the minimum resolution is 100 dpi corresponding to a drop spacing of 254 μm and a saber angle of 90°. The drop spacing is related to the resolution as shown in the following equation:

$$Drop\ spacing(\mu m) = \frac{25400}{resolution(dpi)} \quad (5.1)$$

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The most critical factor of inkjet printing is the ink chemistry and choosing the appropriate ink formulation that is most suited for this technique, as this would determine the drop ejection characteristics and the quality of the printed pattern. For optimal printing performance at the corresponding jetting temperature, the fluid ink should have a viscosity in the range of 10 – 12 cps, a surface tension value between 28 and 33 dynes / cm, a low volatile solvent with a boiling point higher than 100 °C, and an acidity with a pH in the range 4 – 9 so as not to cause corrosion and damage to the print-head. Prior to printing, it is recommended to put the fluid ink in an ultrasonic bath to ensure that the solute is properly dissolved in the solvent and then to filter it, with a 0.2 µm filter for 10 pl cartridges or 0.09 µm filter for 1 pl cartridges, to get rid of big particles and aggregates which lowers the risk of having clogged nozzles. One of the main challenges in inkjet printing is the wettability and compatibility problem of adjacent layers where a suitable combination of materials and solvents having matched wettability characteristics is required. This issue is of special concern when attempting to print OFETs, and it is addressed in paper I and II where a block copolymer is used as a solution for this problem.

5.2 Characterization

5.2.1 Contact Angle Measurements

When a liquid drop settles on a solid surface, three different interfaces are formed as shown in Fig. 5.3. This gives rise to surface tension or surface free energy (SFE) at the solid/liquid (γ_{sl}), solid/gas ($\gamma_{sg} \sim \gamma_s$), and liquid/gas interfaces ($\gamma_{lg} \sim \gamma_l$). These interfacial surface tensions are related by Young's equation, which defines the balances of forces caused by a wet drop on a dry surface, as follows:

$$\gamma_s = \gamma_{sl} + \gamma_l \cos \theta_c \quad (5.2)$$

where θ_c is the contact angle. The contact angle is the angle formed between the liquid/solid interface and the liquid/gas interface. It quantifies the wettability of a solid surface by a liquid and reflects the relative strength of the liquid, solid, and gas molecular interaction. A surface is said to be hydrophobic if its water contact angle is larger than 90°, whereas it is considered hydrophilic if its water contact angle is less than 90°. Hydrophilic surfaces have higher surface energy than

Figure 5.3: Schematic of a liquid droplet resting on a solid surface and surrounded by gas. Interfacial force vectors due to surface tensions at the solid/liquid, liquid/gas, and solid/gas interfaces are shown. The angle, denoted by θ_c , is the contact angle.

hydrophobic ones. The contact angle is typically measured by a goniometer that uses an optical system to capture the profile of a pure liquid on a solid substrate. One of the most common methods for estimating the SFE of a solid is by the utilization of the results of contact angle measurements. This is done by using the Owens-Wendt theoretical model,^[121] which estimates the long-range dispersion (Lifshitz-van der Waals, γ^d) and the short-range polar (hydrogen bonding, γ^p) components of SFE according to the following equation:

$$(1 + \cos \theta_c) \gamma_l = 2\sqrt{\gamma_l^d \gamma_s^d} + 2\sqrt{\gamma_l^p \gamma_s^p} \quad (5.3)$$

For this purpose, contact angle measurements of two different liquids has to be conducted. A liquid with a dominant polar component (such as deionized water) should be chosen as one of the measuring liquids and a dispersion liquid (such as hexadecane) as the other one. The overall surface tension, γ , is given by the sum of the dispersive γ^d and polar γ^p components.

5.2.2 Current-Voltage Measurement

The current-voltage characteristics of the devices reported in the included papers were measured by means of a Keithley 4200-SCS semiconductor parameter analyzer. All electrical measurements were made in ambient air unless otherwise specified. For a description of typical transistor performance data (transfer and output curves), see section 3.2.

6 Conclusions and Future Outlook

This thesis focuses on p-type EGOFETs, their manufacturing process using inkjet printing technology, and their electrical characterization in terms of bias stress instability. EGOFETs employ polyelectrolytes as the gate insulator, and thus have low operating voltages on the order of 1 V due to their high interfacial capacitances, which are virtually independent of the thickness of the electrolyte layer. The use of polyelectrolytes also suppresses electrochemical doping of the semiconductor bulk since polyelectrolytes consist of virtually immobile charged polymer chains with mobile counter ions, and hence transport ions of only one polarity. These features along with solution processability and mechanical flexibility of organic materials make EGOFETs ideally suited for realization via printing techniques in low cost, large-area, flexible electronic circuitry. EGOFETs have already been demonstrated using conventional techniques. However, there are several hurdles to overcome before fully printed EGOFETs can become reality. One of the main challenges is the wettability issue faced when attempting to print the hydrophobic semiconductor layer on top of the hydrophilic polyelectrolyte surface, or vice versa. This problem is addressed in paper I and II where dedicated synthesized block copolymers are used to solve this issue. In paper I, an amphiphilic diblock copolymer is deposited at the polyelectrolyte / semiconductor interface which acts as an adhesion promoting layer that enables the printability of the semiconductor film on top of the polyelectrolyte layer. As to paper II, an amphiphilic semiconducting copolymer that acts as a semiconductor is used. Upon spreading this block copolymer as a thin film, its surface is switched from hydrophobic to hydrophilic due to water exposure. Inkjet printing is used as the manufacturing technique due to its low cost, non-contact and additive approach, which makes it surely a promising technique of printed electronics.

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Since device stability is an important technological issue, characterizing the reliability and performance of EGOFETs is crucial for their realization in future low-cost applications. EGOFETs, as the case is for other OFETs, exhibit undesirable current instability and threshold voltage shifts upon prolonged gate bias application. This operational instability is known as the bias stress effect. The origin of bias stress in OFETs has been heavily debated and studied in several different OFET structures, but is not yet fully understood. Bias stress depends strongly on the materials included, how they are processed, and on the transistor operating conditions. Since a proper understanding of how this effect is manifested in EGOFETs is still lacking, this issue is investigated and reported in paper III and IV. Paper III suggests a mechanism responsible for this undesired drain current instability in EGOFETs. The proposed mechanism involves an electron transfer reaction between water, present at the polyelectrolyte / semiconductor interface, and the charged semiconductor channel which promotes the creation of extra protons subsequently diffusing into the polyelectrolyte and leading to the observed threshold potential shift. Paper IV reports how bias stress is manifested in inverters based on EGOFETs. The inverter is the most basic logic element and it is one of the basic building blocks in digital electronics. Investigating the stability of inverters and the transistors comprised in the inverter under bias stress is a significant reliability concern for digital circuit design.

Substantial research efforts have been devoted to achieve organic transistors that combine printability and low-voltage operation. EGOFETs are built-up from robust device architectures (printability) and operate below 1 V. These devices are therefore suitable for further development towards printed circuits that can be incorporated into future low-cost flexible printed electronic applications. In the results presented in this thesis and the included papers, the most critical few layers were printed in the EGOFET structure; however, without taking the step to a fully printed EGOFET. For this to become a reality, several obstacles have to be overcome, such as finding a suitable combination of materials and solvents for the remaining unprinted layers with matched wettability characteristics that do not as well dissolve each other. Another challenge is to print the source and drain electrodes while achieving short channel lengths. Also, it is essential to improve the obtained EGOFET electrical performance by achieving higher current modulation, lower off-leakage-currents, and faster transistor switch operation. This can be achieved by employing organic semiconductors with relatively higher mobility, polyelectrolytes with high ionic conductivity, and by minimizing the gate-electrode overlap over the channel. Moreover, a good

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understanding of the effect of illumination over the bias stress recovery phenomenon when different polyelectrolytes are employed is still lacking. It is important to address this issue in future research in order to have a better control over the bias stress behavior in EGOFETs.

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