Programmable voltage reference generator for a SAR-ADC
Programmable voltage reference generator for a SAR-ADC
Programmable voltage reference generator for a SAR-ADC

SAR-ADCs are very popular and suitable for conversions up to few tens of MHz with 8 to 12 bits of resolution. A very popular type is the Charge Redistribution SAR-ADC which is based on a capacitive array. Higher speeds can be achieved by using the interleaving technique where a number of SAR-ADCs are working in parallel. These speeds, however, can only be achieved if the reference voltage can cope with the switching of the capacitive array.

In this thesis the design of a programmable voltage reference generator for a Charge Redistribution SAR-ADC was studied. A number of architectures were studied and one based on a Current Steering DAC was chosen because of the settling time that could offer to the Charge Redistribution SAR-ADC switching operation. This architecture was further investigated in order to spot the weak points of the design and try to minimize the settling time.

In the end, the final design was evaluated and possible trimming techniques were proposed that could further speed up the design.
Abstract

SAR-ADCs are very popular and suitable for conversions up to few tens of MHz with 8 to 12 bits of resolution. A very popular type is the Charge Redistribution SAR-ADC which is based on a capacitive array. Higher speeds can be achieved by using the interleaving technique where a number of SAR-ADCs are working in parallel. These speeds, however, can only be achieved if the reference voltage can cope with the switching of the capacitive array.

In this thesis the design of a programmable voltage reference generator for a Charge Redistribution SAR-ADC was studied. A number of architectures were studied and one based on a Current Steering DAC was chosen because of the settling time that could offer to the Charge Redistribution SAR-ADC switching operation. This architecture was further investigated in order to spot the weak points of the design and try to minimize the settling time.

In the end, the final design was evaluated and possible trimming techniques were proposed that could further speed up the design.
Acknowledgments

First of all, I would like express my special thanks of gratitude to Dr. Jacob Wikner for his support and guidance throughout this project. His comments and his help were educating and inspiring.

I would also like to thank Dr. Robert Hägglund from AnaCatum AB who trusted me with this project and Mr. Pavel Angelov for his help and suggestions.

I would like to thank my fiancée Chara for her support and her patience during my studies.

Finally, I would like to thank my parents and my sister for their support and their unconditional love.

Linköping, September 2013
## Contents

List of Figures viii  
List of Tables x  

### 1 Introduction  
1.1 Aim and goals ................................................. 1  
1.2 Desired specifications ....................................... 2  
1.3 Core library cells ........................................... 3  
1.4 Contribution of this work .................................... 3  
1.5 Outline of the thesis ......................................... 4  

### 2 Successive Approximation Register ADC  
2.1 Introduction .................................................. 5  
2.2 Analog to Digital Converter principle .......................... 5  
2.3 Operation principle of a SAR-ADC ............................ 7  
2.4 Voltage Reference in a SAR-ADC .............................. 9  
2.5 Model of the SAR-ADC from the Reference Input ............. 10  
2.6 Error correction using voltage reference calibration ......... 11  
2.7 Conclusion ................................................... 12  

### 3 Architecture study  
3.1 Introduction .................................................. 15  
3.2 Architecture 1: PWM/PDM technique .......................... 15  
3.3 Architecture 2: Operational Amplifier with Resistive Divider 16  
3.4 Architecture 3: Current source controlled by variable duty ratio signal .................................................. 18  
3.5 Architecture 4: Architecture based on a Current Steering DAC 19  
3.6 Conclusion ................................................... 20  

### 4 Design phase of the chosen architecture  
4.1 Introduction .................................................. 21  
4.1.1 Architecture overview .................................... 22  
4.1.2 Estimation of main parameters ............................ 22
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1.3</td>
<td>Output and reference resistor</td>
<td>25</td>
</tr>
<tr>
<td>4.2</td>
<td>Unit current cell topologies</td>
<td>25</td>
</tr>
<tr>
<td>4.2.1</td>
<td>Single current source with switch in series</td>
<td>25</td>
</tr>
<tr>
<td>4.2.2</td>
<td>Cascoded current source with switch in series</td>
<td>27</td>
</tr>
<tr>
<td>4.2.3</td>
<td>Switched cascoded current source</td>
<td>29</td>
</tr>
<tr>
<td>4.2.4</td>
<td>Other topologies</td>
<td>31</td>
</tr>
<tr>
<td>4.3</td>
<td>Current divider design</td>
<td>31</td>
</tr>
<tr>
<td>4.3.1</td>
<td>Simple version</td>
<td>32</td>
</tr>
<tr>
<td>4.3.2</td>
<td>Cascoded PMOS version</td>
<td>34</td>
</tr>
<tr>
<td>4.3.3</td>
<td>Cascoded PMOS and NMOS version</td>
<td>35</td>
</tr>
<tr>
<td>4.4</td>
<td>Reference current generator design</td>
<td>36</td>
</tr>
<tr>
<td>4.4.1</td>
<td>Single bias version</td>
<td>37</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Splitted bias version</td>
<td>38</td>
</tr>
<tr>
<td>4.4.3</td>
<td>Self-biased version</td>
<td>40</td>
</tr>
<tr>
<td>4.5</td>
<td>Possible trimming techniques</td>
<td>40</td>
</tr>
<tr>
<td>4.6</td>
<td>Conclusion</td>
<td>41</td>
</tr>
<tr>
<td>5</td>
<td>Simulation results</td>
<td>43</td>
</tr>
<tr>
<td>5.1</td>
<td>Introduction</td>
<td>43</td>
</tr>
<tr>
<td>5.2</td>
<td>Simulation Results</td>
<td>45</td>
</tr>
<tr>
<td>5.2.1</td>
<td>Reference Set</td>
<td>45</td>
</tr>
<tr>
<td>5.2.2</td>
<td>Main Set</td>
<td>45</td>
</tr>
<tr>
<td>5.3</td>
<td>Conclusion</td>
<td>54</td>
</tr>
<tr>
<td>6</td>
<td>Conclusion and Future Work</td>
<td>55</td>
</tr>
<tr>
<td>A</td>
<td>Impedance derivation for the splitted bias current reference generator</td>
<td>57</td>
</tr>
<tr>
<td>B</td>
<td>Verilog model of the counter</td>
<td>59</td>
</tr>
<tr>
<td>Bibliography</td>
<td></td>
<td>63</td>
</tr>
</tbody>
</table>

**List of Figures**

1.1 Overview of the programmable voltage reference generator | 2   
1.2 Desired settling behavior of the voltage reference | 3   
2.1 Overview of a basic Analog to Digital Converter | 6   
2.2 Illustration of sampling and digitizing of a signal | 6   
LIST OF FIGURES

2.3 Ideal transfer characteristic for an A/D converter ............... 7
2.4 Overview of the SAR-ADC architecture ....................... 8
2.5 Overview of the Charge Redistribution SAR-ADC architecture .. 8
2.6 Model of the SAR-ADC provided by AnaCatum AB .......... 11
2.7 Pipeline ADC basic architecture ........................... 12
2.8 Impact of incomplete settling of the amplifier on residue plot ... 12

3.1 Architecture with PWM/PDM technique ....................... 16
3.2 Architecture with Operation Amplifier and Resistive Divider .. 16
3.3 Possible implementation of a programmable resistor .......... 17
3.4 Variable duty ratio controlled current source architecture ... 18
3.5 Architecture overview based on a Current Steering DAC ...... 20

4.1 Top overview of the architecture based on a Current Steering DAC 22
4.2 Architecture overview of the segmented Current Steering DAC .. 22
4.3 Simplified model of the Current Steering DAC along with the SAR-ADC ............................................. 23
4.4 Single current source with switch in series topology .......... 26
4.5 Single current source with switch in series model .......... 26
4.6 Cascoded current source with switch in series topology with parasitics and simplified output load ................. 27
4.7 Cascoded current source with switch in series model with parasitics and simplified output load ................. 27
4.8 Switched cascoded current source topology with parasitics and simplified output load .......................... 29
4.9 Switched cascoded current source model with parasitics and simplified output load ................................ 30
4.10 Other current source topologies that have been tested ...... 31
4.11 Simple current mirror topology ............................ 32
4.12 Simple current mirror model ................................ 32
4.13 Ratio deviation of the simple current divider ............... 33
4.14 Cascoded PMOS current mirror topology ................... 34
4.15 Ratio deviation of the cascoded PMOS current divider .... 35
4.16 Cascoded PMOS and NMOS current mirror topology ....... 35
4.17 Ratio deviation of the cascoded PMOS and NMOS current divider 36
4.18 Single bias current reference generator topology .......... 37
4.19 Kickback path of the simple current reference generator .... 37
4.20 Splitted bias current reference generator topology .......... 38
4.21 Current reference generator topology proposed by [20] .... 38
4.22 Parasitics at the output of the splitted bias current reference generator ........................................ 39
4.23 Self biased current reference generator topology .......... 40
4.24 Trimmable resistor using a multiplexer .................... 41

5.1 Testbench overview for the simulations ....................... 44
5.2 Current reference generator and current source for the reference set 45
List of Tables

1.1 Summary of the desired specifications for the programmable voltage reference generator ........................................... 2

5.1 Typical simulation results from the reference set .................................. 45
5.2 Excerpt from corners simulation for untrimmed reference resistance ................................................................. 49
5.3 Excerpt from corners simulation for trimmed reference resistance ............................................................ 49
5.4 Monte Carlo summary of the main set ................................................. 51
5.5 Integrated output RMS noise at reference voltage ........................................ 53
5.6 Achieved specifications summary for a single SAR-ADC .......................... 54
List of Abbreviations

ADC  Analog to Digital Converter
DAC  Digital to Analog Converter
DLL  Delay Locked Loop
MSB  Most Significant Bit
MSPS Mixed Signal Processing Systems
OA   Operational Amplifier
PDM  Pulse Density Modulation
PSRR Power Supply Rejection Ratio
PVT  Process Voltage Temperature variations
PWM  Pulse Width Modulation
RMS  Root Mean Square
SAR  Successive Approximation Register
1

Introduction

1.1 Aim and goals

The aim of this thesis is the design of a programmable voltage reference generator for a Charge Redistribution Successive Approximation Register (SAR) Analog to Digital Converter (ADC). Because of the nature of the converter, a very high settling time of the reference generator is demanded while having a very high accuracy in order to eliminate possible errors at the output of the ADC caused by the reference voltage. The combination of the settling time and the accuracy will proved to be very challenging and will be our main goal during the design phase.

After a study of different possible architectures, one architecture was chosen and implemented in STM 65nm technology. The implementation will be consider to be a reference design and for that reason only cells from the core library of the technology will be used.

The thesis was co-supervised by AnaCatum AB. The company defined the desired specifications and provided the model of the SAR-ADC while the choice of the architectures to be studied was under the free choice of the student.
1.2 Desired specifications

In this section we will present the specifications for the voltage reference generator. Figure 1.1 depicts the general overview of the system in its generic form with a differential output. A well defined and independent to temperature bandgap reference voltage is fed to the reference voltage generator which then generates a reference voltage determined by the input control word. The specifications of the system are summarized in table 1.1.

According to the specifications the output voltage of the generator should be vary between 0.4 and 0.8V. The specific value of the reference voltage will be dictated by the application for which the SAR-ADC is meant to be used. Different applications might require different reference voltage and the programmable voltage reference generator provides us with the flexibility to alter the reference voltage on-line without the need to modify the whole design.

The second important requirement of the system is the settling time which should be below 1ns. The settling time is the time window in each successive approximation phase of the SAR-ADC operation which has been assigned for the stabilization of the voltage reference generation. In each phase of the successive approximation a voltage drop at the output will be caused due to the connections and disconnections in the capacitor array of the SAR-ADC. A more detailed presentation of the operation of the ADC will be made in section 2.3. This voltage drop should be compensated within this time window.

The settling of the voltage reference is illustrated in figure 1.2 for the case we wish to output 0.8V at the output. After 1ns the output voltage must not deviate

Table 1.1: Summary of the desired specifications for the programmable voltage reference generator

<table>
<thead>
<tr>
<th>Specification</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>0.4 – 0.8 V</td>
</tr>
<tr>
<td>Settle time</td>
<td>1 ns</td>
</tr>
<tr>
<td>Accuracy</td>
<td>16 bits</td>
</tr>
<tr>
<td>Output Load</td>
<td>400 fF</td>
</tr>
</tbody>
</table>
more than $V_{LSB}/2$ with respect to 16 bits.

![Figure 1.2: Desired settling behavior of the voltage reference](image)

After the reference voltage has settled the ADC can proceed with the rest of its internal operation.

The final requirement is the driving capability of the system. The effective capacitive load of the SAR-ADC as seen from the voltage reference input has a maximum of 400 $fF$ capacitance. The voltage reference generator should have the ability to drive this load and pull the reference voltage to the desired value within the time window and accuracy. Further details on the SAR-ADC model from the voltage reference point of interest are presented in section 2.5.

### 1.3 Core library cells

An extra requirement for the design was the use of cells from the core library of the process kit. In this library transistors with different features are available but for our application we will restrict to thin oxide which, in contrast to thick oxide transistors, provides lower threshold voltage. More specifically we will focus on the transistors for general purpose with standard threshold voltage. The above combination allows the design to be more generic since it does not utilize very process-specific cells.

### 1.4 Contribution of this work

The contribution of this work is the study and the design of a programmable voltage reference generator which can be used in a variety of applications where a charge redistribution SAR-ADC consists the heart of the system.

The main attribute of this study is the focus on high precision and low settling time of the reference voltage. This will allow the designer to relax the require-
ments of the SAR-ADC since there is less error induced by the voltage reference generator and more time for the conversion to finish.

1.5 Outline of the thesis

The thesis is divided in six chapters in total.

The first two chapters are an introduction to the subject of the thesis and the operation of a Charge Redistribution SAR-ADC. Here the operation of the SAR-ADC is described in detail and the model of the SAR-ADC from the reference input is presented. Moreover, it is explained how the Voltage Reference Generator can be used for error corrections.

The third chapter presents the study of four different potential architectures. Each architecture is evaluated in order to justify if it can be used within the requirements of the generator.

The design of the chosen architecture, namely, the one based on a Current Steer-DAC is then presented in chapter 4. Each block consisting this architecture is presented and analyzed and their relation to the settling time is examined.

The final chapters of the thesis are devoted on the simulation results of the design and the conclusion of this work.
2.1 Introduction

In modern electronics the Mixed Signal Processing Systems (MSPS) is a field of great interest both in the academia and the industry. A main part of MSPS is the Analog to Digital Converter (ADC) which interconnects the analog with the digital world. It allows engineers to transfer an analog signal, related to a natural source, to the digital domain, where processing and computations are feasible, cheaper and faster.

In this chapter we will go through the basic principles of Analog to Digital conversion and then focus on the Charge Redistribution Successive Approximation Register (SAR) ADC. Then we will see how we can model the SAR-ADC from the voltage reference input and finally discuss some error correction techniques which can be achieved by calibrating the reference voltage.

2.2 Analog to Digital Converter principle

The ADC is a system with an analog signal at the input and a digital representation of it at the output. The analog signal is sampled with a given frequency and each sample is quantized based on the resolution of the converter.
The relation between the amplitude of the analog signal and the digital word is described by the equation 2.1 where $A_{\text{sig}}$ is the amplitude of the analog signal at the current instant, $V_{FS}$ is the analog full scale level and $b_n$ is either 0 or 1 representing the value of the corresponding bit.

$$A_{\text{sig}} = V_{FS}(b_{n-1} \cdot 2^{-1} + b_{n-2} \cdot 2^{-2} + \ldots + b_0 \cdot 2^{-n}) \quad (2.1)$$

In figure 2.3 the ideal transfer function of an ADC is depicted and we can see that the whole range of the analog signal is divided in quantized levels where each level belongs to a unique digital word.
The width of the quantized levels is a critical parameter of the ADC and is also known as the resolution of the converter. In a N-bit ADC the width of the levels is given by $V_{LSB} = \frac{V_{FS}}{2^N}$. The resolution of the converter should not be confused with the accuracy of it since the first one is an ideal parameter while the later one is a performance metric measured in units of $V_{LSB}$ [11].

2.3 Operation principle of a SAR-ADC

Among different types of ADCs the SAR-ADC is a suitable type for resolutions between 8 and 12 bits and speeds of up to few tens of MHz [2].

The SAR-ADC is an Analog to Digital Converter which utilizes the binary search algorithm in order to estimate the digital representation of the input. This algorithm result in a conversion speed which is a fraction of the input clock frequency. From the SAR-ADC family, we will focus on the Charge Redistribution SAR-ADC. This type is a good candidate for a low power and small size converter due to the use mainly of passive components rather than active ones.

Figure 2.4 shows the basic architecture of a SAR-ADC. During the first phase the input is sampled from the Sample and Hold component. Then the binary search algorithm takes place. At the first iteration the Most Significant Bit (MSB) of the register is set to high and the rest of the bits to low resulting in the mid value of the register. This value will force the DAC to output a voltage of $\frac{v_{Ref}}{2}$ which will be compared to the sampled input voltage. After the comparison the MSB either
remains at high state or it is reset to low in case the input voltage is lower than $v_{\text{Ref}}/2$. In the next iteration the 2nd MSB is set to high and a new comparison is made between the input voltage and the $b_{N-1} \cdot v_{\text{Ref}}/2 + v_{\text{Ref}}/4$. After $N$ iterations the input voltage has been fully converted and a new conversion can begin. As we see from the aforementioned one conversion needs at least $N + 1$ iterations which means that the conversion speed is $N + 1$ times the clock period.

![Figure 2.4: Overview of the SAR-ADC architecture](image)

The same conversion can be made by the Charge Redistribution ADC shown at 2.5.

![Figure 2.5: Overview of the Charge Redistribution SAR-ADC architecture](image)

In the Charge Redistribution SAR-ADC the sampling phase is done by connecting the common terminal of the capacitors to ground and the other plate of the capacitors to the input voltage ($v_{\text{In}}$).

In the next phase the common voltage is disconnected from the ground and the switches of the capacitors are connected to the ground except the MSB which is
connected to \( vRef \). In that way, the common terminal is driven at \( \frac{vRef}{2} - vIn \) and the comparator makes a comparison between that voltage and the ground. If the comparison is positive (\( \frac{vRef}{2} - vIn > 0 \)) then the MSB remains connected to \( vRef \) otherwise returns back to the ground.

In the next iteration the 2nd MSB is connected to \( vRef \), the common terminal is forced to \( b_{N-1} \cdot \frac{vRef}{2} + \frac{vRef}{4} - vIn \) and the comparator decides the state of the 2nd switch.

In each iteration the common node voltage is \( \sum_{n=0}^{N-1} b_n \cdot \frac{vRef}{2^n} - vIn \). The conversion is finished after \( N \) comparisons and a new comparison may begin. [1]

### 2.4 Voltage Reference in a SAR-ADC

As we have seen in section 2.3 a number of capacitors are connected and disconnected from the voltage reference input at every phase of the SAR cycle. This forces the voltage reference generator to charge the capacitor array at the beginning of every phase. The total power provided by the voltage reference for a N-bit CR SAR-ADC due to the switching of the capacitor array was analyzed in [15] and is given by equation 2.2 where \( T_s \) is the conversion time and \( Q_i \) is the charge drawn by the \( vRef \) during the \( i \)-th phase.

\[
P_{vRef} = \frac{vRef}{T_s} \sum_{i=1}^{N} Q_i
\]  

(2.2)

According to [15] the charges of the first three phases are calculated in the equations 2.3 to 2.5 where \( D_n \) is the value of the respective bit and \( V_{DAC_i} \) is the \( i \)-th approximation of the input voltage i.e. \( \sum_{j=1}^{i} D_j \cdot \frac{vRef}{2^j} \) with \( D_1 \) being the MSB.

\[
Q_1 = C_1[(vRef - V_{DAC_1}) - (0 - 0)] \tag{2.3}
\]

\[
Q_2 = C_2[(vRef - V_{DAC_2}) - (0 - V_{DAC_1})] + C_1D_1[(vRef - V_{DAC_2}) - (vRef - V_{DAC_1})] \tag{2.4}
\]

\[
Q_3 = C_3[(vRef - V_{DAC_3}) - (0 - V_{DAC_2})] + (C_1D_1 + C_2D_2) \cdot [(vRef - V_{DAC_3}) - (vRef - V_{DAC_2})] \tag{2.5}
\]

In total, the charge provided by \( vRef \) is given by the general expression 2.6 where \( C_i = 2^{N-i} C_u \).
\[
\sum_{i=1}^{N} Q_i = Q_1 + \sum_{i=2}^{N} Q_i \\
= 2^N \cdot C_u \cdot vRef \cdot \left( \frac{1}{2} \right) + 2^N \cdot C_u \cdot vRef \\
\cdot \left( \sum_{i=2}^{N} \frac{1}{2^i} + \sum_{i=2}^{N} \frac{1}{2^{2i}} + \sum_{i=2}^{N} \left( \frac{1}{2^i} \sum_{j=1}^{i-1} D_j \right) \right) \\
- \sum_{i=2}^{N} \left( \frac{D_{i-1}}{2^{i-1}} \sum_{j=1}^{i-1} \frac{D_j}{2^j} \right) - \sum_{i=2}^{N} \left( \frac{1}{2^i} \frac{D_{i-1}}{2^{i-1}} \right) 
\]

Based on the aforementioned, the total power of the \(vRef\) towards the capacitor array is given in 2.7 where \(V_{DAC}\) is the corresponding analog voltage of the final digital word.

\[
P_{vRef} \simeq \frac{2^N f_{clk} C_u}{N + 1} \\
\cdot \left( \frac{5}{6} - \left( \frac{1}{2} \right)^N - \frac{1}{3} \left( \frac{1}{2} \right)^{2N} \right) vRef^2 \\
- \frac{1}{2} V_{DAC}^2 - \left( \frac{1}{2} \right)^N V_{DAC} vRef 
\]

Finally, we should denote that in order to have a correct comparison in each phase, the voltage reference generator should be capable to provide the charge \(Q_i\) within the given maximum settling time \(t_s\).

### 2.5 Model of the SAR-ADC from the Reference Input

In order to be able to test our design, a model was provided by AnaCatum AB which is shown in figure 2.6.
This model depicts the worst possible case for the settling behavior of the voltage reference generator. The left branch of the model is composed by a constantly connected capacitor of 7\(C_u\) capacitance and a resistor in series representing the connected switches. The right branch is composed by 9 in parallel switches with a capacitor of 9\(C_u\) in series and a discharging switch.

During the simulation there will be two consecutive cycles. The first cycle is represented by the model as it is in figure 2.5 and in the second cycle, the most crucial one, the switches S1 and S2 will be triggered. We will study the settling of the \(v_{\text{Ref}}\) from the time when the switches are triggered until the settling of \(v_{\text{Ref}}\) within the desired accuracy. Further details on the simulation will be given in chapter 5.

2.6 Error correction using voltage reference calibration

A programmable voltage reference generator can also be used to correct linear errors such as gain errors and capacitor mismatches. In [19] digital calibration of the reference voltage was used in order to correct linear errors as well as to cope with the slow settling of the amplifier of a Pipeline ADC.
The overview of a Pipeline ADC is shown in figure 2.7. Each stage is composed by a sample and hold, a sub-ADC and a sub-DAC with a resolution of X-bits and an amplifier which amplifies the residue voltage by $2^X$. The amplifier is characterized by its bandwidth which determines the settling time of the output voltage. If the operation frequency of the ADC is faster than the settling time then the amplifier might not be able to reach its final value resulting in an error ($\epsilon$). Such case is depicted in figure 2.8. If we know the error $\epsilon$ as a percentage of the final value then we can reduce the reference voltage by the same percentage and compensate for the incomplete settling.

In [19] a calibration technique has been proposed where a well defined sinusoid external signal is fed to the ADC and the reference voltages of each stage are being adjusted until the SNDR is maximized.

2.7 Conclusion

In this chapter we discussed about the Charge Redistribution SAR-ADC and its functionality. The model of the ADC was then presented which will be used in order to simulate the worst case settling of the reference voltage. Finally, the abil-
ity to correct errors introduced by the ADC by calibrating the reference voltage was presented. Now, we can move on to the discussion regarding the different architectures that were studied for the programmable voltage reference generator implementation.
3.1 Introduction

During this thesis a number of architectures were studied and evaluated in order to justify which one should be used for the current design given the desired specifications. During this pre-study calculations and simulations were conducted for each architecture and some of them were excluded based on the results. Finally, one architecture, namely the one based on the current steering DAC, was chosen which seemed to be realistically viable from a design point of view.

3.2 Architecture 1: PWM/PDM technique

In this architecture a bit stream is generated using either the Pulse Width Modulation (PWM) or the Pulse Density Modulation (PDM) technique. A low pass filter is used in order to extract the DC voltage of the stream. By using an inverter a complementary stream can also be generated which will give us the complementary reference voltage with respect to $V_{DD}/2$ in case of using a supply of $0V$ and $V_{DD}$.

The DC voltage will be determined by the ratio between the number of ones and the total number of bits $N_b$ while the fundamental frequency of the spectrum of the bit stream will be determined by the clock frequency $F_s$ and the total number of bits. However, by utilizing a first order $\Sigma - \Delta$ modulator for the PDM technique we can get a higher fundamental frequency [8],[12].
This architecture requires an extremely high frequency clock, with a period of a very small fraction of 1\text{ns}, in order to meet the requirements. This is both unviable and not realistic, so, the current architecture was excluded from further design.

### 3.3 Architecture 2: Operational Amplifier with Resistive Divider

The concept of this simple architecture as proposed by [17] is shown in figure 3.2. The voltage divider is composed by one constant resistor and one programmable which is controlled by the control word. A programmable resistor can be implemented in its simplest form as in figure 3.3 [16],[17].
The value of the $v_{Ref}$ can be expressed as: $v_{Ref} = v_{BG}(1 + \frac{R_c}{R_1})$ where $v_{BG}$ is the bandgap reference voltage, $R_c$ is the value of the controllable resistance and $R_1$ is the constant value resistor.

Moreover, the unity-gain frequency of the amplifier based on the desired settling time and without taking into account the slew-rate is given by 3.1 where $\epsilon$ is the relative error (half LSB with respect to 16 bits) and $t_s$ is the settling time [7].

$$f_u = \frac{\ln(\epsilon)}{2\pi t_s}$$

$$= \frac{11.78}{2\pi \text{ns}}$$

$$= 1.87 \text{GHz}$$

This requirement is unrealistic and not achievable and is the reason that this architecture has been also excluded from further study.
3.4 Architecture 3: Current source controlled by variable duty ratio signal

In this architecture two current sources charge a discharged capacitor up to the desired voltage. The reset switch discharge the capacitor to $0V$ at the beginning of the cycle. Then, currents flow through the two switches $S_C$ and $S_F$ for a period of time defined by the duty ratio of the control signal of the switches. The control signals are generated by a Delay Locked Loop (DLL) along with some extra control logic.

The two current sources ($I_C$ and $I_F$) correspond to the coarse and the fine tuning. For a capacitive load of $400\, fF$ and a maximum settling time of $1\, ns$ we would need a coarse current of:

\[
I_C = C_{out} \frac{\Delta V}{\Delta t} = 400\, f \cdot \frac{0.8\, V}{1\, ns} = 320\, \mu A
\]  

and a fine current for a $25\, mV$ of fine tuning:

\[
I_F = C_{out} \frac{\Delta V}{\Delta t} = 400\, f \cdot \frac{25\, mV}{1\, ns} = 10\, \mu A
\]
The reason for which we cannot use this architecture becomes clear when we derive the jitter requirements for each current source. The jitter requirements are derived in equations 3.4 and 3.5 in order to maintain $\frac{1}{2}V_{\text{LSB}}$ accuracy with respect to 16 bits.

\[
\Delta t_{\text{jitter}} = C_{\text{out}} \frac{\Delta V}{I_C}
\]

\[
= 400 f \cdot \frac{3.05 \mu V}{320 \mu A}
\]

\[
= 3.8 f s
\] (3.4)

\[
\Delta t_{\text{jitter}} = C_{\text{out}} \frac{\Delta V}{I_C}
\]

\[
= 400 f \cdot \frac{3.05 \mu V}{10 \mu A}
\]

\[
= 122 f s
\] (3.5)

In literature peak-to-peak jitter results have reported to be of few tens of picoseconds [18], [3], [4]. Based on this the required jitter for our design is very unrealistic and this architecture is proved to be inadequate for high accuracy.

According to the reported jitter values, this architecture could be used for accuracies of around 4 bits using the same settling requirement. Doubling the settling requirement can increase the accuracy by 1 bit.

### 3.5 Architecture 4: Architecture based on a Current Steering DAC

The last architecture that is being studied in this thesis was based on a Current Steering Digital to Analog Converter (DAC). Such architecture is frequently used in literature [21], [9], [14], [10]. The overview of the architecture can be seen in figure 3.5.
In this architecture a segmented Current Steering DAC is used in order to generate the output current which will generate the reference voltage. In the fine tuning portion of the DAC a larger current is generated and then is mirrored with a scale factor of $B$. This is useful when the fine tuning is very small and a very small current is demanded which might be troublesome from a design perspective. The current from the fine portion is summed with the coarse current and generate a voltage through a resistor $R_{out}$. In section 4.1.2 the values of the maximum currents, current scaling factor and the resistor $R_{out}$ are calculated based on the specifications.

This architecture has been chosen to be designed as it is the most viable choice for the desired specifications.

### 3.6 Conclusion

In this chapter the different potential architectures were presented and the most viable one was chosen to be designed. The design requirements proved to be very demanding and they were the key factor to choose the proper architecture. The fourth architecture, the one based on a Current Steering DAC, was chosen to be implemented and further investigated for its potential performance. In the next chapter we will focus on the design of that architecture followed by the simulation results.
4.1 Introduction

The architecture based on current steering DAC was eventually chosen as the most viable solution for the voltage reference generator. In this chapter we will go through the design phase of the system. We will start with the estimation of the main parameters of the design and then we will proceed with the study of different topologies for the main components of the design. These components are namely the Current Source, the Current Divider, and the Reference Current Generator which will bias the Current Sources. Finally, we will discuss some possible trimming techniques which can increase the robustness of the design without the expense of extra power and area.
4.1.1 Architecture overview

![Diagram of architecture overview](image)

Figure 4.1: Top overview of the architecture based on a Current Steering DAC

![Diagram of segmented Current Steering DAC](image)

Figure 4.2: Architecture overview of the segmented Current Steering DAC

Figure 4.1 depicts the general overview of the architecture. A current reference generator generates a reference current based on the bandgap reference voltage and one or more bias voltages are fed to the current sources. The topology of the reference current generator and the current sources are discussed in the later sections.

As we have already mentioned in section 3.5 a segmented Current Steering DAC is used to generate the reference voltage across the resistor $R_{out}$. The coarse portion of the DAC will generate the current responsible for the coarse tuning and the fine portion will generate the current for the fine tuning. The parameters that will characterize the system are estimated in the following section 4.1.2.

4.1.2 Estimation of main parameters

The first step of the design is to estimate the basic parameters of our system in order to meet the specifications. These parameters are the output resistance ($R_{out}$), current scaling factor ($B$), coarse and fine tuning currents. The estimations are
made under ideal conditions and in the later stages they will be altered according to the simulation results.

**Output resistance** $(R_{\text{out}})$

We will first estimate the output resistance. According to section 2.5 the total capacitance at the output will be $400\,fF$. We will use a more simplified model of the Current Steering DAC along with the SAR-ADC as in figure 4.3 assuming a single pole response of the output.

![Simplified model of the Current Steering DAC along with the SAR-ADC](image)

**Figure 4.3: Simplified model of the Current Steering DAC along with the SAR-ADC**

The current $I_{\text{total}}$ is the total current generated by the DAC. The worst case scenario is when we wish to generate the maximum voltage at the output i.e. $0.8\,V$. Moreover, we should take into account that the output capacitance is composed by two capacitors. One capacitor has a capacitance of $7\,C_u$ and the other one a capacitance of $9\,C_u$ according to the SAR-ADC model. The first capacitor has been already charged at $0.8\,V$ and its charge is given by equation 4.1.

$$Q_1 = C \cdot V = 7C_u \cdot 0.8 \quad (4.1)$$

When the discharged second capacitor will be connected at the output the total charge will remain the same but the voltage will drop. By equalizing the charges before and after the connection we get the initial voltage $(V_i)$ in equation 4.2.

$$\begin{align*}
Q_{\text{before}} &= Q_{\text{after}} \\
7C_u \cdot 0.8 &= 16C_u \cdot V_i \\
V_i &= \frac{7}{16} \cdot 0.8 \\&= 0.35 \, V \quad (4.2)
\end{align*}$$

The voltage $V_i$ will be the initial voltage of the capacitor in the model of figure 4.3.

Now that we know the initial voltage of the capacitor in our model we can estimate the necessary resistance which will give us the proper settling. With the help of Mathematica we can derive the equation 4.3 using the following code.
\[ \text{deq1} = i == v[t]/r + c*v'[t]; \]
\[ \text{dsol} = \text{DSolve}[\{ \text{deq1, } v[0] == vi \}, v, t] \]
\[ v[t_] = v[t] / . \text{Part}[\text{dsol}, 1, 1] \]
\[ \text{Solve}[v[t] == vf - \epsilon, t] \]
\[ t = R_{out} \cdot C_{out} \cdot \ln(\frac{V_f - V_i}{\epsilon}) \iff \]
\[ R_{out} = \frac{1}{C_{out} \cdot \ln(\frac{V_f - V_i}{\epsilon})} \]

Where \( R_{out} \) and \( C_{out} \) are the resistance and the capacitance of the model, \( V_f \) and \( V_i \) are the final and the initial value of the capacitor-output and \( \epsilon \) is the error at the given time instance \( t \) and in our case is equal to 3.05\( \mu \)V. Substituting the right values to the equation 4.3 we end up to the value:

\[ R_{out} = \frac{1\text{ns}}{400f \cdot \ln(\frac{0.8 - 0.35}{3.05\mu})} \]
\[ = 210\Omega \]

This is approximately the value of the resistor that we need in order to meet the specifications. Actually, a smaller resistance will be used since the output capacitance does not include parasitics and other effects.

**Output Currents**

The resistance that we estimated in the previous section will be used to generate the output voltage according to the current which will be generated by the DAC. The output current is composed by two components. The coarse and the fine tuning components.

For the given implementation we will choose to cover the whole range from 0.4\( V \) up to 0.8\( V \) with 4 bits of coarse tuning and 5 bits of fine tuning which seems to be generic enough as suggested by the supervision side. However, in some applications we might need different settings based on the needs of each application. In order to cover 0.4\( V \) of range we need a maximum coarse current of:

\[ I_{coarse} = \frac{0.4V}{210\Omega} \]
\[ = 1.9mA \]

and given that each step of the coarse tuning will be \( \frac{0.4}{25} = 25mV \) wide, the maximum fine current after the division should be:
\[ \frac{I_{fine}}{B} = \frac{25mV}{210\Omega} = 199\mu A \]

Although this current could be generated by the fine tuning part without the need of any current division, we choose the parameter \( B \) to be equal to 4. This is an arbitrarily choice and the reason behind this is to illustrate the generic case. There might be some applications where a finer control is need and thus a smaller current needs to be generated which is more tricky from design perspective.

### 4.1.3 Output and reference resistor

As we will see in the later sections the amount of output current will be defined by a reference resistor in the current reference generator block.

From a layout perspective the choice of the material for the output resistor and the resistor which will be used to generate the reference current is very crucial.

It is known that after the tape out different chips exhibit different characteristics because of the process variations. That means that parameters which affect the value of the resistance will differ from chip to chip. In our design a polysilicon silicided resistor was used with a sheet resistance of around 15\( \Omega \) and a variation of approximately 30% between the worst cases. However, by cleverly design the layout and by placing the two resistors in the same vicinity we can ensure that the resistors will vary the same way and eventually the will have approximately the same value.

### 4.2 Unit current cell topologies

In this section we will present some of the available and most popular unit current cell topologies. Each cell will differ from the others on the number of the in series transistors that will compose the current source and the position of the switch.

#### 4.2.1 Single current source with switch in series

This is the simplest approach for the design of the current source cell. One transistor biased properly by the current reference generator will generate the current and a second transistor connected in series will act as a switch biased either at 0\( V \) in the ON state or at \( V_{DD} \) in the OFF state. This bias will make the switch transistor to operate in the linear region when it will be ON.
This topology can be modeled as in figure 4.5.

\[ Z_{\text{out}} = r_{o1} + r_{o2} \]  \hspace{1cm} (4.4)

This topology, with the switch operating in linear mode, although it is fast, lacks of high output impedance which is essential for high Power Supply Rejection Ratio (PSRR). The only way to increase \( r_o \) is by using longer transistor lengths which is inefficient. By doubling the length the area of the transistor quadruples for a constant shape factor \( \frac{W}{L} \). A more efficient way to increase the output impedance is by using a cascoded version.
4.2.2 Cascoded current source with switch in series

In this topology a cascoded current source is used in order to increase the output impedance. The two transistors that compose the current source are biased by the current reference generator. The switch is turned on and off by applying either $0\, V$ or $V_{DD}$ which forces it to operate in linear mode while it is ON. In figure 4.6 and figure 4.7 we see the topology overview and its model including the parasitic capacitances and the output load.

![Figure 4.6: Cascoded current source with switch in series topology with parasitics and simplified output load](image1)

![Figure 4.7: Cascoded current source with switch in series model with parasitics and simplified output load](image2)
In order to estimate the output impedance the following equations are extracted and the output impedance is estimated in equation 4.8.

\[ i_T - \frac{V_T - V_2}{r_{o3}} = 0 \] (4.5)

\[ i_T + g_{m2} V_1 - \frac{V_2 - V_1}{r_{o2}} = 0 \] (4.6)

\[ g_{m2} V_1 + \frac{V_1}{r_{o1}} - \frac{V_2 - V_1}{r_{o2}} = 0 \] (4.7)

\[ Z_{out} = r_{o3} + \left( g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) r_{o1} r_{o2} \] \[ \approx g_{m2} r_{o1} r_{o2} \] (4.8)

This topology has a higher output impedance but simulations have shown that it is slower than the topology described in section 4.2.1. However, we can come up with an efficient way to size this topology for minimum delay by estimating the time constant of the topology. For that we need to derive the time constant for each parasitic capacitance shown in the model.

\[ \tau_1 = C_{p1} \cdot (r_{o1} || \frac{1 + g_{ds2}(r_{o3} + R_L)}{g_{m2}}) \] (4.9)

\[ \tau_2 = C_{p2} \cdot (g_{m2} r_{o1} r_{o2} || (r_{o3} + R_L)) \] (4.10)

\[ \tau_3 = C_{p3} \cdot (R_L || (r_{o3} + g_{m2} r_{o1} r_{o2})) \] (4.11)

\[ \tau_L = C_{out} \cdot (R_{SW} + R_{out} || (r_{o3} + g_{m2} r_{o1} r_{o2})) \] (4.12)

where \( \tau \) denotes the time constant, \( R_L \) the in parallel combination of \( R_{out} \) and \( R_{SW}, R_{SW} \) the on resistance of the switch in the SAR-ADC model, \( r_o = \frac{1}{g_{ds}} \), the output impedance of the transistor, \( g_m \) the dynamic transconductance of the transistor and the symbol || denotes the in parallel connection of the impedances. Each equation from 4.9 to 4.12 approximate the time constant of each parasitic capacitance shown in the model and we expect a total time constant of:

\[ \tau_{total} = \tau_1 + \tau_2 + \tau_3 + \tau_L \] (4.13)

Although the aforementioned might be a very rough approximation, it shows us the dependence of the time response upon the different parameters such us the \( g_m \) and \( g_{ds} \) which are defined by the size and the bias point of each transistor.

Finally, we can assume that by increasing \( g_{m2} \) while keeping the size of that transistor as small as possible we can achieve a faster response. This is due to the fact that by increasing the \( g_{m2} \) we are reducing \( \tau_1 \) while the resistive factor of \( \tau_2 \)
becomes dominated by $r_{o3} + R_L$. At the same time the resistive factors of $\tau_3$ and $\tau_L$ are dominated by $R_L$ and $R_{SW} + R_{out}$ respectively. Moreover, by reducing the size of transistor 2 (the cascode transistor) we are reducing the parasitics $C_1$ and $C_2$. Taking these into account we can rewrite equations 4.9 to 4.12 as below:

$$\tau_1 = C_{p,1} \cdot \left( \frac{1 + g_{ds2}(r_{o3} + R_L)}{g_{m2}} \right)$$  \hspace{1cm} (4.14)$$

$$\tau_2 = C_{p,2} \cdot (r_{o3} + R_L)$$  \hspace{1cm} (4.15)$$

$$\tau_3 = C_{p,3} \cdot R_L$$  \hspace{1cm} (4.16)$$

$$\tau_L = C_{out} \cdot (R_{SW} + R_{out})$$  \hspace{1cm} (4.17)$$

To conclude, this topology, although it has a high output impedance, it has a slow response while another disadvantage is the difficulty to bias the transistors properly given that the available voltage headroom is very small. We are trying to overcome these problems in the next section 4.2.3 where the number of transistors in series are reduced by one by placing the switch at the input of the cascode transistor.

### 4.2.3 Switched cascoded current source

A faster response and a better use of the voltage headroom can be achieved by removing the switch from its previous position and placing it at the input of the cascode transistor as shown in figure 4.8. The model of this topology is depicted in figure 4.9.

![Figure 4.8: Switched cascoded current source topology with parasitics and simplified output load](image)
For the estimation of the output impedance we derive the following equations from the model ignoring the parasitic capacitances and the SAR-ADC part:

\[
\begin{align*}
    i_T + g_{m2} V_1 - \frac{V_T - V_1}{r_{o2}} &= 0 \\
    g_{m2} V_1 + \frac{V_1}{r_{o1}} - \frac{V_T - V_1}{r_{o2}} &= 0
\end{align*}
\] (4.18) (4.19)

The output impedance is then given by the following equation:

\[
Z_{out} = \left( g_{m2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} \right) r_{o1} r_{o2}
\]

\[\approx g_{m2} r_{o1} r_{o2}\] (4.20)

The comparison of the equations 4.8 and 4.20 shows that the two topologies offer the same high output impedance. However, in the current topology we can spend more headroom on the cascode transistor and thus increase \(g_{m2}\) which will increase the output impedance.

With the same reasoning as in section 4.2.2 we can derive the equivalent time constant to study the time response of the topology. The following equations are extracted from the model in figure 4.9.

\[
\begin{align*}
    \tau_1 &= C_{p,1} \cdot \left( r_{o1} \parallel \frac{1 + g_{ds2} R_L}{g_{m2}} \right) \\
    \tau_2 &= C_{p,2} \cdot \left( g_{m2} r_{o1} r_{o2} || R_L \right) \\
    \tau_L &= C_{out} \cdot \left( R_{SW} + R_{out} || g_{m2} r_{o1} r_{o2} \right)
\end{align*}
\] (4.21) (4.22) (4.23)

and the total time equivalent time constant is approximated by:
\[ \tau_{total} = \tau_1 + \tau_2 + \tau_L \] (4.24)

We can still see that by increasing \( g_{m2} \) while keeping the size of the cascode transistor as small as possible we can minimize the time settling. Equations 4.21 to 4.23 are then simplified as below:

\[ \tau_1 = C_{p,1} \cdot \left( r_{o1} \parallel \frac{1 + g_{ds2}R_L}{g_{m2}} \right) \] (4.25)

\[ \tau_2 = C_{p,2} \cdot R_L \] (4.26)

\[ \tau_L = C_{out} \cdot (R_{SW} + R_{out}) \] (4.27)

With the aforementioned taken into account we can conclude that the current topology shows better behavior regarding the time settling and the output impedance which affects the PSRR.

### 4.2.4 Other topologies

The topologies depicted in figure 4.10 have also been tested. The first one positions the switch at the input of the current source transistor. The second one uses a global cascode transistor and the switch is placed between the power supply and the current source. The last one is the same as the first one but uses a global cascode transistor for all the unit current sources.

The results have shown that they do not present better characteristics neither in the time settling nor in the PSRR and these topologies have been excluded from the final simulations.

### 4.3 Current divider design

In the following sections we will study the different topologies that have been investigated for the implementation of the current divider. We will start with
the simplest topology which is composed by two non-cascoded mirrors. Then we will see how the use of a cascoded pmos mirror affects the mirroring ratio with respect to the input current. Finally, we will see if the use of cascoded mirrors for both the pmos and the nmos side is worthwhile.

4.3.1 Simple version

![Simple current mirror topology](image1)

**Figure 4.11: Simple current mirror topology**

In figure 4.11 we see the simple version of the current divider which is based on the combination of two simple current mirrors. The first NMOS current mirror divides the input current by $B/2$ and the subsequent PMOS mirror makes the rest of the total division by $B$. In figure 4.12 the model of the NMOS current mirror is depicted.

![Simple current mirror model](image2)

**Figure 4.12: Simple current mirror model**

The minimum voltage that can be available at the output is given by the equation 4.28:

$$V_{out_{min}} = V_{DS(sat)} = V_{GS} - V_T$$

where $V_{DS(sat)}$ is the drain-source saturation voltage and $V_T$ is the threshold voltage of the NMOS transistor while the output to input current ratio can be derived by the equations 4.29 and 4.30 for $V_{GS_1} = V_{GS_2}$. 
$$I_{in} = I_{D_1} = \frac{1}{2\mu C_{ox}} \frac{W_1}{L_1} (V_{GS_1} - V_T)^2 (1 + \lambda V_{DS_1})$$  \hspace{1cm} (4.29)$$

$$I_{out} = I_{D_2} = \frac{1}{2\mu C_{ox}} \frac{W_2}{L_2} (V_{GS_2} - V_T)^2 (1 + \lambda V_{DS_2})$$  \hspace{1cm} (4.30)$$

$$\Rightarrow \frac{I_{out}}{I_{in}} = \frac{W_2/L_2}{W_1/L_1} \cdot \frac{1 + \lambda V_{DS_2}}{1 + \lambda V_{DS_1}}$$  \hspace{1cm} (4.31)$$

where $W$ and $L$ are the width and length of the respective transistor, $\mu$ is the charge-carrier effective mobility, $C_{ox}$ is the gate oxide capacitance per unit area and $\lambda$ is the channel length modulation parameter [13].

As can be seen from equation 4.31 the output to input current ratio is not constant and it is strongly depended on the bias of the transistors which is expressed here in terms of the voltage $V_{DS}$. For a wide range of input current the bias is changed significantly and the ratio varies considerably.

### Simulation results

![Graph showing current ratio deviation](image)

**Figure 4.13: Ratio deviation of the simple current divider**

The simulation of this version is depicted in figure 4.13. The total ratio of the current mirror shows an absolute difference of 2 between 100 $\mu$A and 900 $\mu$A. Although we have mentioned that the minimum current is 20 $\mu$A in the real design a smaller output resistance will be used in order to reduce the settling time, so, it is more wise to evaluate the current divider using a higher current.
4.3.2 Cascoded PMOS version

![Cascoded PMOS current mirror topology](image)

*Figure 4.14: Cascoded PMOS current mirror topology*

The next approach of the design of the current divider is to replace one of the mirrors with a wide swing cascoded version which exhibits a more constant mirroring ratio and reduce the total variability of the division ratio.

This mirror, when is placed at the PMOS side, can afford a maximum voltage at the input of:

\[ V_{in_{\text{max}}} = V_{DD} - V_{ds(sat)} - V_T \] (4.32)

and provides a maximum voltage at the output of:

\[ V_{out_{\text{max}}} = V_{DD} - 2 \cdot V_{ds(sat)} \] (4.33)

At this point we should state the problem that arises with the wide range input current. Based on the initial calculations the input current has a minimum value of 20\(\mu\)A and a maximum of 660\(\mu\)A. This causes the DC voltages to vary significantly shifting the transistors between different operating modes. Because of that the sizing of the transistors is not so trivial and extra care should be taken to ensure that all the transistors operate in the proper region.
4.3 Current divider design

Simulation results

![Graph showing current ratio against input current for different ratios: PMOS Ratio, NMOS Ratio, Total Ratio.](image)

**Figure 4.15:** Ratio deviation of the cascoded PMOS current divider

In this version the ratio seems considerably more constant. From 100\(\mu\text{A}\) up to 900\(\mu\text{A}\) a variation of 0.77 is experienced which gives the best results so far.

4.3.3 Cascoded PMOS and NMOS version

![Cascoded PMOS and NMOS current mirror topology](image)

**Figure 4.16:** Cascoded PMOS and NMOS current mirror topology

The last option regarding the current divider is the use of wide swing cascoded current mirrors in both NMOS and PMOS sides. This option promises a constant
current division ratio but having a cascoded current mirror at the output of the fine tuning part will increase the settling time.

Simulation results

![Graph showing current ratio deviation](image)

**Figure 4.17:** Ratio deviation of the cascoded PMOS and NMOS current divider

This final version exhibits a more constant ratio with 0.18 variation. However, this kind of current divider increases prohibitively the settling time due to the parasitic capacitive load at the output of the fine tuning part. So, this version will not be used in the final design.

### 4.4 Reference current generator design

A very critical part of the design is the reference current generator. This block will be responsible for the generation of the biasing of the unit current cells. The choice of the topology of this cell will be proved to be very important for keeping the settling time and the power as low as possible. We will start from the simple single bias reference current generator which will be a quite ideal approach and then we will proceed with the more realistic splitted-bias and self-biased topologies.
4.4 Reference current generator design

4.4.1 Single bias version

This simple reference current generator is composed by an OA, a reference resistor and a PMOS transistor. The properties of the OA will force the upper node of the reference resistor to be equal to $v_{BG}$ which is the available Bandgap Reference voltage. The loop that is formed between this elements will keep the gate voltage of the transistor at such a value where the current of the transistor will be equal to $0.8/R_{ref}$. This relation is described by equation 4.34.

$$\frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 = \frac{0.8}{R_{ref}}$$  \hspace{1cm} (4.34)

The voltage $V_{gs}$ will be the bias voltage of a unit current source like the one described in section 4.2.1. The reference transistor of figure 4.18 and the current source transistor of the unit current source (as can be seen both in figure 4.19) will form a current mirror and the unit current will be depended on the ratio of the shape factors ($W/L$) of these two transistors.

The results from this topology should be carefully evaluated because they are compromised by the model of the OA. A very ideal model will give better results but it can still be used as a reference point of view.
An important negative feature of this topology is the impact of the output switching on the bandgap reference block. A switching activity of the SAR-ADC will cause a disturbance at the output of the voltage reference generator which will propagate through the different parasitics towards the bandgap reference input. In order to reduce the impact of the kickback a small switch in the unit current cells and a properly designed OA should be used.

### 4.4.2 Splitted bias version

![Figure 4.20: Splitted bias current reference generator topology](image)

The next option for the design of the reference current generator is the topology shown in figure 4.20 which was inspired from [20]. A reference current is generated in the OA loop as described in section 4.4.1. This current is then mirrored at the transistors B3, T6 and T7 which generate the bias voltages for the unit current cells.

The topology of figure 4.21 proposed in [20] was initially tested but proved to be slow. The reason behind this is the kickback effect on the node A between B4 and T4. A switching activity at the output of the voltage reference generator disturbs the node A and the transistors T4 and T5 are not capable to settle this node fast enough because of their high output dynamic impedance. Figure 4.22 shows the parasitics of the output part of the topology.

![Figure 4.21: Current reference generator topology proposed by [20]](image)
Parasitic capacitances $C_{p,1}$ and $C_{p,2}$ are consisted by the capacitive loads of the gates of the unit current cells. $C_{p,3}$ is formed by the parasitic capacitance of the diffusions of $T_4$ and $B_4$. In this case the time constant of node $A$ is given by equation 4.35.

$$
\tau_A = (C_{p,1} + C_{p,3}) \cdot R_{p,3}
$$

$$
= (C_{p,1} + C_{p,3}) \cdot \frac{g_{m_{T_4}} \cdot r_{o_{T_4}} \cdot r_{o_{T_5}}}{\frac{g_{m_{M_{bias}}} + \frac{1}{r_{o_{M_{bias}}}}}{g_{m_{B_4}}} + \frac{g_{m_{M_{bias}}} + \frac{1}{r_{o_{B_4}}}}{g_{m_{B_4}}} + \frac{1}{r_{o_{B_4}} \cdot r_{o_{M_{bias}}}}}.
$$

In order to speed up the settling of this node we should decrease either $R_{p,3}$, $C_{p,3}$ or both at the same time. Sizing up the transistors $T_4$ and $T_5$ result in a faster decrease of $R_{p,3}$ with respect to $C_{p,3}$ but this also consumes more area and power since we increase the current of this branch. A more power efficient approach is to replace the cascade NMOS current mirror (formed by transistors $T_2$, $T_3$, $T_4$ and $T_5$) with a simple one in order to effectively decrease both $R_{p,3}$ and $C_{p,3}$ while keeping the area and power consumption as low as possible. This choice sacrifices the accuracy of the circuit but it is more affordable.

Simulations have shown that by increasing the current 2.2 times result in a reduction of settling time by 14.4% while the use of simple current mirror result in a reduction of 30% with the same current.
4.4.3 Self-biased version

The topology shown in figure 4.23 is the last topology studied for the current reference generator. A self-biased cascoded current mirror is formed between $T_6$, $T_7$ and the transistors of the unit current cells. In this version we have eliminate a complete branch which was used for the generation of bias $V_{bias2}$ in order to study if we can reduce the area and the power consumed by this circuit. Simulation results have shown that the extra parasitics in the branch consisted of $T_5$, $T_6$ and $T_7$ in combination with the kickback effect produce longer settling times which can only be compensated by increasing the current of this branch resulting in disproportional increase of the area and the power consumption.

4.5 Possible trimming techniques

In order to achieve higher performance a post layout trimming technique must be used. Although the fine tuning of the current steering DAC will serve as a trimming method, an extra trimming will be needed to overcome the PVT (Process, Voltage and Temperature) variations, in a first level, while maintaining sufficient speed and accuracy.

The reference resistor can be chosen as the trimmable part of the design. Trimmmable resistors are very common and are used by different systems from low offset amplifiers and oscillators to ADCs.

There are two ways to implement a trimmable resistor. One way is to use a number of resistances connected in series and then using a sort of multiplexer made by switches extract a part of the total resistance. Figure 4.24 shows the principle structure of such method. Of course other structures of interconnected resistances can be used. The right structure should be chosen based on the impact of the switches and their parasitics to the total accuracy and speed of the system.
Another way of trimming is by using a post layout pulse current trimmable resistor. In [6] such technique is described for a polysilicon resistor. In this technique a pulse current is applied to the resistor for few milliseconds and the resistance value is reduced based on the amplitude of the pulse. The resistance value can be increased back again by applying a lower amplitude. However, one should consider the long term impact of the DC current on the value of the resistance.

A critical parameter for choosing between these two types of trimming resistors is the cost of the implementation with respect to the accuracy of the resulted resistance value. The first trimming technique is very cheap but has a low accuracy which in our case is affordable. On the other hand the later trimming technique due to its extra cost, since it requires a pulse current generator, should be only used only when accuracy is of high importance.

4.6 Conclusion

In this chapter the available topologies for each block of the system were presented and their main characteristics were described. A study has been made on the impact of the parasitics of the topologies to the settling time and a "rule of thumb" was deduced based on this study for the design of the current sources. In the next chapter we will proceed with the simulation results of the final design.
In this chapter we will present the simulation results of the design. At first, we will very briefly present the settling time and PSRR results of the reference design and in the next section a thorough presentation of the results of the main design will follow covering all the necessary simulations.

Although both sets use the cascoded PMOS current mirror, the first set is composed by the simple version of the current reference generator and the simple current source. The main design on the other hand is composed by the self-biased current reference and the switched cascoded current source.

### 5.1 Introduction

The figure 5.1 depicts the testbench that was used to conduct all the necessary simulations. In the figure the programmable voltage reference generator is shown in the center and is connected to the SAR-ADC model. At the left side we see the voltage sources responsible for the generation of the necessary signals and supply and below them the block which generates the control word. In appendix B the verilog model of this block is presented.
Figure 5.1: Testbench overview for the simulations
5.2 Simulation Results

For the reference set we will briefly present the maximum settling and the minimum PSRR in order to have a reference point for comparison against the results of the main set. For the main set we will first present the voltage reference and the PSRR throughout the control word range for the nominal corner. Then, focusing on the maximum output voltage we will present the corners and the monte carlo simulations and discuss their results. Finally, we will summarize the achievable specifications in the final section.

5.2.1 Reference Set

![Figure 5.2: Current reference generator and current source for the reference set](image)

<table>
<thead>
<tr>
<th>Settling 16bits (ns)</th>
<th>1.147</th>
</tr>
</thead>
<tbody>
<tr>
<td>Settling 13bits (ns)</td>
<td>0.96</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>17.47</td>
</tr>
</tbody>
</table>

*Table 5.1: Typical simulation results from the reference set*

The reference set is the one which promises the minimum settling time due to its low parasitics. In table 5.1 two settling times are given. One is for 16bits accuracy as per the desired specifications and one for 13bits which gives results close to the desired specifications. The PSRR is also given which is quite small but can be partially compensated depending on the configuration of the ADC.

5.2.2 Main Set

The key blocks of the main set are shown in figure 5.3. We will come back to this figure later on to study the transient responses of some key nodes of the design.
Transmit response

We will begin with the transient response of the reference voltage. Up to 3\textit{ns} the initialization phase takes place and the switch of the SAR-ADC model remains open while the reference voltage reaches the desired voltage. Then we trigger the switches of the SAR-ADC and a voltage drop occurs, as expected, of 149.5\textit{mV}. We should denote that the voltage drop does not match the calculations since the current limitations does not allow that much drop in such short time.

This voltage drop propagates towards the bandgap reference block through the kickback paths which can be seen in figure 5.5. In figure 5.6 we see the drops that occur in the bias nodes as well as the node V5 between transistors B2 and T3. These drops will dictate the amount of current through the transistors T3, T4 and T5 which will define the necessary time constants of this nodes.
Figure 5.5: Kickback paths of the current reference generator
**Typical corner results**

In the figure 5.7 the output voltage reference is shown with respect to the control word. The control word which is composed by 9 bits has been converted to integer format with values from 0 to 511 for better readability.

**Figure 5.7: Output voltage reference of the main set for the typical case**

The PSRR can be seen in figure 5.8 where we can see that around the control word 418 (1101-00000) a cancellation effect takes place and the output exhibits higher PSRR.
5.2 Simulation Results

![PSRR Graph]

**Figure 5.8:** PSRR of the main set for the typical case

### Corners and Monte Carlo Results

By simulating the design for different Process, Voltage and Temperature corners (PVT) we realize that the output voltage varies greatly resulting in a failing system in many cases. Table 5.2 shows an excerpt from the PVT corners simulation results for the maximum control word case.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal</th>
<th>Min</th>
<th>Max</th>
<th>FFA</th>
<th>SSA</th>
<th>SS</th>
<th>SFA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>1.08</td>
<td>1.08</td>
<td>1.32</td>
<td>1.08</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Temperature</td>
<td>70</td>
<td>-10</td>
<td>920.2</td>
<td>755.7</td>
<td>790.6</td>
<td>834.5</td>
<td></td>
</tr>
<tr>
<td>vRef (mV)</td>
<td>809.1</td>
<td>755.7</td>
<td>920.2</td>
<td>790.6</td>
<td>834.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>17.74</td>
<td>10.35</td>
<td>33.31</td>
<td>11.94</td>
<td>12.36</td>
<td>12.76</td>
<td></td>
</tr>
<tr>
<td>Settling 16bits (ns)</td>
<td>1.36</td>
<td>1.248</td>
<td>2.003</td>
<td>1.786</td>
<td>1.554</td>
<td>1.648</td>
<td></td>
</tr>
<tr>
<td>Settling 13bits (ns)</td>
<td>1.006</td>
<td>0.930</td>
<td>1.556</td>
<td>1.497</td>
<td>1.315</td>
<td>1.394</td>
<td></td>
</tr>
</tbody>
</table>

**Table 5.2:** Excerpt from corners simulation for untrimmed reference resistance

To overcome this problem a trimmable reference resistor was introduced. Simulations have shown that a resistor value spanned from 900Ω to 1.2kΩ with 8 steps in total is sufficient to compensate for the variations. In a real implementation the right value of the reference resistor could be picked by a Process Voltage and Temperature (PVT) monitor. In [5] a PVT sensor is proposed which outputs a digital code which determines in which corner the chip operates in at the moment. However, the trimmable resistor solution was tested on a simulation level and by that we mean that there was not any real implementation of the trimmable resistor. For each corner one of the 8 values of the resistance was used and then a corner simulation was conducted giving us the results in table 5.3 for the maximum output voltage.
Simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal</th>
<th>Min</th>
<th>Max</th>
<th>FFA</th>
<th>SSA</th>
<th>SS</th>
<th>SFA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td></td>
<td></td>
<td></td>
<td>1.32</td>
<td>1.08</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Temperature</td>
<td></td>
<td>115</td>
<td>-10</td>
<td>-10</td>
<td>70</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vRef (mV)</td>
<td></td>
<td>809.1</td>
<td>801.2</td>
<td>826.9</td>
<td>806.9</td>
<td>809.7</td>
<td>823.4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>826.9</td>
<td>809.7</td>
<td>823.4</td>
<td></td>
<td></td>
<td>817.3</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td></td>
<td>17.74</td>
<td>11.61</td>
<td>21.94</td>
<td>14.23</td>
<td>15.82</td>
<td>11.66</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14.23</td>
<td>15.82</td>
<td>11.66</td>
<td></td>
<td></td>
<td>13.27</td>
</tr>
<tr>
<td>Settling 16bits (ns)</td>
<td></td>
<td>1.36</td>
<td>1.36</td>
<td>2.021</td>
<td>1.818</td>
<td>1.619</td>
<td>1.54</td>
</tr>
<tr>
<td>Settling 13bits (ns)</td>
<td></td>
<td>1.006</td>
<td>1.006</td>
<td>1.603</td>
<td>1.576</td>
<td>1.297</td>
<td>1.288</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.54</td>
<td>1.66</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5.3: Excerpt from corners simulation for trimmed reference resistance

As we can see the reference voltage has now less variation which can be corrected by the fine tuning. Figures 5.9 and 5.10 show how the trimming technique compensates for the variations for the two worst case corners.

Figure 5.9: Trimmed and untrimmed FFA8 corner compared to the typical

Figure 5.10: Trimmed and untrimmed SSA0 corner compared to the typical
Finally, in table 5.4 the summary from 200 runs Monte Carlo simulation is presented. We can expect that the fine tuning along with the trimmable reference resistance will compensate the deviation of the reference voltage.

<table>
<thead>
<tr>
<th>Name</th>
<th>Min</th>
<th>Max</th>
<th>Mean</th>
<th>Sigma</th>
</tr>
</thead>
<tbody>
<tr>
<td>vRef (mV)</td>
<td>792.1</td>
<td>827.3</td>
<td>809.1</td>
<td>6.5</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>13.66</td>
<td>22.67</td>
<td>17.85</td>
<td>1.636</td>
</tr>
<tr>
<td>Settling 16bits (ns)</td>
<td>1.115</td>
<td>1.598</td>
<td>1.37</td>
<td>0.13</td>
</tr>
<tr>
<td>Settling 13bits (ns)</td>
<td>0.94</td>
<td>1.27</td>
<td>1.038</td>
<td>0.742</td>
</tr>
</tbody>
</table>

*Table 5.4: Monte Carlo summary of the main set*

**Impact of the unity-gain frequency of the OP-amp**

The above simulations were conducted with a very high unity-gain frequency OP-amp in the reference current generator. The simulation in figure 5.11 shows how the unity-gain frequency affects the settling time of the reference voltage. Moreover, we can see that an OP-amp of 145 MHz unity-gain frequency is enough to support the design operation. This frequency indicates that the role of the OP-amp is very crucial and its design is of great importance both for the speed and the power consumption.

*Figure 5.11: Settling time with respect to unity-gain frequency of the OP-amp*
Impact of the number of SAR-ADC slices on the settling time

So far we were investigating the performance of the system assuming that only one SAR-ADC was operating. In reality, the interleaving technique will be used in order to achieve faster conversion time. That means that the ADC will be composed by K number of parallel SAR-ADC slices. Each slice will handle the conversion of every K-th sample of the input and the total conversion speed will be K times lower than the conversion time of each slice.

Figure 5.12: Multi SAR-ADC slices configuration with global bias

Figure 5.13: Settling time and power consumption with respect to the number of SAR-ADC slices

Figure 5.12 shows the configuration of the interleaving method where a global
current reference generator feeds all the current DACs. The settling time can be seen in figure 5.13 where the lower graph shows the minimum settling time for the specified number of slices and the top graph shows the power that needs to be consumed by the current reference generator in order to minimize the settling time.

**Noise Simulation**

The final results are the noise simulation of the reference voltage. Noise from the voltage reference generator will be fed into the SAR-ADC and compromise the accuracy of the ADC. This is why the estimation of the noise is an important performance metric.

![Output noise graph](image)

**Figure 5.14: Output noise**

The following table 5.5 summarizes the Root Mean Square (RMS) noise over some frequencies of interest.

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>100</th>
<th>333M</th>
<th>500M</th>
<th>1G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output noise (µV)</td>
<td>101.2</td>
<td>331.6</td>
<td>369.4</td>
<td>427.7</td>
</tr>
</tbody>
</table>

*Table 5.5: Integrated output RMS noise at reference voltage*

Based on the noise summary transistors T3, B2 and B1 contribute the 78.14% of the total noise. A guideline for the reduction of noise could be the sizing up of this transistors in order to increase their $g_m$ and thus the noise contribution.
5.3 Conclusion

After presenting the results of different simulations the achieved specifications are summarized in table 5.6. The results correspond to a single SAR-ADC operation and the area has been estimated based on the summation of the sizes of the transistors without taking into account the routing overhead.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Goal</th>
<th>Units</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning range</td>
<td>1.26</td>
<td>1.36</td>
<td>2.02</td>
<td>1</td>
<td>mV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Settling Time</td>
<td>1.36</td>
<td>1.36</td>
<td>2.02</td>
<td>1</td>
<td>ns</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>PSRR</td>
<td>11.61</td>
<td>17.74</td>
<td>21.94</td>
<td>-</td>
<td>dB</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Noise (rms)</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>µV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Noise @100Hz</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>µV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Noise @333MHz</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>µV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Noise @500MHz</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>µV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Noise @1GHz</td>
<td>-</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>µV</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Operating supply</td>
<td>1.08</td>
<td>1.2</td>
<td>1.32</td>
<td>-</td>
<td>V</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>-10</td>
<td>70</td>
<td>113</td>
<td>-</td>
<td>°C</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Current DAC</td>
<td>-</td>
<td>-</td>
<td>9.7</td>
<td>-</td>
<td>mW</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Power</td>
<td>-</td>
<td>-</td>
<td>6.9</td>
<td>-</td>
<td>W</td>
<td>Achieved results under trimming</td>
</tr>
<tr>
<td>Area</td>
<td>513</td>
<td>-</td>
<td>553.7</td>
<td>-</td>
<td>µm²</td>
<td>Achieved results under trimming</td>
</tr>
</tbody>
</table>

Table 5.6: Achieved specifications summary for a single SAR-ADC
Conclusion and Future Work

Four different architectures were studied and evaluated for the design of a programmable voltage reference generator. The architecture based on a current steering DAC was chosen according to its potential to fulfill the desired specifications. Then, different aspects of the chosen architecture were investigated and the results of the final design were presented.

The desired specifications proved to be very challenging for the STM 65nm technology. The proposed trimming technique managed to increase the speed considerably but the speed goal is yet to be reached. Moreover the PSRR is quite low which might be problematic in some applications. The main barricade to fulfill the desired specifications was the limited voltage headroom.

A possible way to increase both the speed and the PSRR is by redesigning the voltage reference generator around a NMOS based current steering DAC. The charge carriers of the NMOS transistors are the electrons which exhibit higher mobility than the holes making them faster by default. The output current could then be mirrored to the output resistance through a PMOS current mirror. The power consumption of this solution, however, must be evaluated since the generated current from the DAC will be mirror doubling the power consumption assuming that the current mirror has a 1:1 ratio.

The proposed trimming technique was tested at a simulation level but it also needs to be implemented and retested to ensure its effectiveness and its drawbacks when real transistors will form the multiplexer.

Finally, like in every integrated circuit, the final phase is the design of the layout. During this phase some back and forth iterations between schematic and layout will be made in order to fine tune the design for an efficient layout. Then, post-
layout simulations need to be conducted in order to take into account the effect of the floor-planing, routing and parasitics.
In section 4.4.2 the impedance $R_{p,3}$ of figure A.1 was used for the derivation of the time constant.

\[ \text{Figure A.1: Parasitics at the output of the splitted bias current reference generator} \]

In this appendix we will show how the output impedance of the transistors $M_{bias}$ and $B_4$ is extracted. In figure A.2 the model of the $M_{bias}$ and $B_4$ transistors is shown.
From this model we can derive the following equations A.1 and A.2 which result in an output impedance expressed by equation A.3.

\[ \begin{align*}
  i_T + g_{mB4} V_1 - \frac{V_T - V_1}{r_{oB4}} &= 0 \quad (A.1) \\
  g_{mB4} V_1 + \frac{V_1}{r_{oMbias}} + g_{mMbias} V_T - \frac{V_T - V_1}{r_{oB4}} &= 0 \quad (A.2) \\
  R_{p3, TOP} &= \frac{g_{mB4} + \frac{1}{r_{oMbias}} + \frac{1}{r_{oB4}}}{g_{mMbias} g_{mB4} + \frac{g_{mMbias}}{r_{oB4}} + \frac{1}{r_{oB4} r_{oMbias}}} \quad (A.3)
\end{align*} \]
The block that generated the control word of the voltage reference generator was essentially a counter which could either operate in a running mode, i.e. increment its output in every cycle or in a freeze mode where the output had the same value throughout the simulation.

A not so common feature of this counter is the way it computes the current state of the output. Instead of saving the previous output in a variable and then increment it in the next cycle, another approach was used based on the time that has passed since the beginning of the simulation and the period of the counter. This allows the counter to be independent to previous stages which was a requirement for some specialized simulations such as the pnoise simulation in spectre tool.

```verilog
'include "constants.vams"
'include "disciplines.vams"

module videoAdc_Misc_OutStreams(outStr, clk);
    input clk; // Clock input
    electrical clk;
    output [15:0] outStr; // 16bits bus output
    electrical [15:0] outStr;

    parameter real trise = 2f; // Rise time
    parameter real tfall = 2f; // Fall time
    parameter real tdel = 2f; // Delay time
    // Voltage corresponding to logic 1
    parameter real vlogic_high = 1.2;
    // Voltage corresponding to logic 0
    parameter real vlogic_low = 0;
    // Transit voltage from 0 to 1 or from 1 to 0
```
parameter real vtrans_clk = 0.6;
\Period of the clock input for estimation of the \current period
parameter real clk_per = 1n;
\Initial clock delay
parameter real clk_del = 0;
\Choose between running mode or freeze mode
parameter integer option = 1;
\Increment step size
parameter integer value = 1;
\Initial value of the counter
parameter integer icvalue = 0;

integer incounter, n;
real invOut[15:0];
integer i, j;
integer unconv;

analog begin
  @ (cross(V(clk) - vtrans_clk, 1)) begin
    if (option==2) begin
      incounter=icvalue;
    end else begin
      //Estimate the current clock period
      n=($abstime-clk_del)/clk_per;
      //Derive the output value
      incounter=(icvalue+n*value)%pow(2,16);
    end
  end

  //Derive the state of each bit
  for (i=0; i<=15; i=i+1) begin
    if ((incounter % 2) == 1) begin
      invOut[i]=vlogic_high;
      incounter=(incounter - (incounter % 2))/2;
    end else begin
      invOut[i]=vlogic_low;
      incounter=incounter/2;
    end
  end
  // @ (cross(V(clk) - vtrans_clk, 1))

  \Assign the voltage to each bit
  V(outStr[15]) <+ transition( invOut[15], tdel, trise, tfall );
  V(outStr[14]) <+ transition( invOut[14], tdel, trise, tfall );
  V(outStr[13]) <+ transition( invOut[13], tdel, trise, tfall );
  V(outStr[12]) <+ transition( invOut[12], tdel, trise, tfall );
  V(outStr[11]) <+ transition( invOut[11], tdel, trise, tfall );
  V(outStr[10]) <+ transition( invOut[10], tdel, trise, tfall );
  V(outStr[9]) <+ transition( invOut[9], tdel, trise, tfall );
V(outStr[8]) <+ transition( invOut[8], tdel, trise, tfall );
V(outStr[7]) <+ transition( invOut[7], tdel, trise, tfall );
V(outStr[6]) <+ transition( invOut[6], tdel, trise, tfall );
V(outStr[5]) <+ transition( invOut[5], tdel, trise, tfall );
V(outStr[4]) <+ transition( invOut[4], tdel, trise, tfall );
V(outStr[3]) <+ transition( invOut[3], tdel, trise, tfall );
V(outStr[2]) <+ transition( invOut[2], tdel, trise, tfall );
V(outStr[1]) <+ transition( invOut[1], tdel, trise, tfall );
V(outStr[0]) <+ transition( invOut[0], tdel, trise, tfall );
B Verilog model of the counter
Bibliography


Upphovsrätt

Detta dokument hålls tillgängligt på Internet — eller dess framtida ersättare — under 25 år från publiceringsdatum under förutsättning att inga extraordinära omständigheter uppstår.

Tillgång till dokumentet innebär tillstånd för var och en att läsa, ladda ner, skriva ut enstaka kopior för enskilt bruk och att använda det oförändrat för icke-kommersiell forskning och för undervisning. Överföring av upphovsrätten vid en senare tidpunkt kan inte upphäva detta tillstånd. All annan användning av dokumentet kräver upphovsmannens medgivande. För att garantera äktheten, säkerheten och tillgängligheten finns det lösningar av teknisk och administrativ art.

Upphovsmannens ideella rätt innefattar rätt att bli nämnt som upphovsman i den omfattning som god sed kräver vid användning av dokumentet på ovan beskrivna sätt samt skydd mot att dokumentet ändras eller presenteras i sådan form eller i sådant sammanhang som är kränkande för upphovsmannens litterära eller konstnärliga anseende eller egenart.

För ytterligare information om Linköping University Electronic Press se förlagsets hemsida http://www.ep.liu.se/

Copyright

The publishers will keep this document online on the Internet — or its possible replacement — for a period of 25 years from the date of publication barring exceptional circumstances.

The online availability of the document implies a permanent permission for anyone to read, to download, to print out single copies for his/her own use and to use it unchanged for any non-commercial research and educational purpose. Subsequent transfers of copyright cannot revoke this permission. All other uses of the document are conditional on the consent of the copyright owner. The publisher has taken technical and administrative measures to assure authenticity, security and accessibility.

According to intellectual property law the author has the right to be mentioned when his/her work is accessed as described above and to be protected against infringement.

For additional information about the Linköping University Electronic Press and its procedures for publication and for assurance of document integrity, please refer to its www home page: http://www.ep.liu.se/

© Georgios Mylonas