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Organic Reprogrammable Circuits Based on Electrochemically-Formed Diodes

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ABSTRACT: We report a method to construct reprogrammable circuits based on organic electrochemical (EC) p-n junction diodes. The diodes are built up from the combination of the organic conjugated polymer poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene] and a polymer electrolyte. The p-n diodes are defined by EC doping performed at 70 °C, and then stabilized at -30 °C. The reversible EC reaction allows for in-situ reprogramming of the polarity of the organic p-n junction, thus enabling us to reconfigure diode circuits. By combining diodes of specific polarities dedicated circuits have been created, such as various logic gates, a voltage limiter and an AC/DC converter. Reversing the EC reaction allows in-situ reprogramming of the p-n junction polarity, thus enabling reconfiguration of diode circuits, for example, from an AND gate to an OR gate. The reprogrammable circuits are based on p-n diodes defined from only two layers, the electrodes and then the active semiconductor:electrolyte composite material. Such simple device structures are promising for large-area and fully-printed reconfigurable circuits manufactured using common printing tools. The structure of the reported p-n diodes mimics the architecture of, and is based on identical materials used to construct light emitting

electrochemical cells (LEC). Our findings thus provide a robust signal routing technology that is easily integrated with traditional LECs.

KEYWORDS: organic reprogrammable circuit, light-emitting electrochemical cell, electrochemistry, organic diode, MEH-PPV, polymer electrolyte.

1. Introduction

Si-based integrated circuits for modern electronics is a story of tremendous success. Organic electronics, although falling behind in speed and efficiency, offers several complementary benefits and is promising for solution-processable, inexpensive and flexible applications. Si-based programmable circuits, such as the early Programmable Array Logic (PAL) to the state-of-the-art Field Programmable Gate Arrays¹ (FPGAs), have played an important role in modern computing, but the organic counterpart is still lacking. In this paper, we utilize the combined electronic and ionic charge transport and electrochemical (EC) switching characteristics²⁻⁴ of organic materials to construct reprogrammable diode circuits. Taking advantage of these combined features, we developed solution-processed reconfigurable circuits constructed from programmable organic diode arrays (PODA). The actual programming is based on reversible EC doping of diodes identical to the structure of the light-emitting electrochemical cell (LEC)⁵⁻⁷.

LECs, consisting of a semiconducting polymer and an electrolyte, have emerged as promising components for solid state lighting, thanks to a simple fabrication process⁸⁻⁹, robust architecture as well as efficient luminescence properties¹⁰. In LECs, associated cations and anions dissociate as an electric field is applied. Injection of charges into the semiconducting polymers and the charge compensation provided by the ions results in the formation of p- and n-doped regions of the polymer. The resulting p-n junction can be stabilized chemically¹¹⁻¹⁵ or physically¹⁶⁻²² and

displays an electronic current rectification property together with a built-in potential^{6, 23}. The fixed p-n junction stabilized by the physical method, often termed “frozen junction”, takes advantage of the temperature-dependent ion mobility in the LECs, i.e., after the desired ion distribution is reached in the device, the temperature is decreased to a point where the ions are effectively immobile. This frozen p-n junction can be dissipated by yet another time increasing the temperature, after which the polarity of the p-n junction can be reversed using an inverted external potential^{6, 24}. This reversibility and the aforementioned rectification feature provides the foundation for the PODA concept. Based on this concept, examples of reconfigurable circuits will be demonstrated such as a logic AND gate, a logic OR gate, a voltage limiter and also an AC/DC convertor.

2. Materials and methods

The PODA system are built up from the semiconducting Poly[2-methoxy-5-(2-ethylhexyloxy)-1,4-phenylenevinylene] (MEH-PPV, Aldrich), the ion conducting polyethylene oxide (PEO, $M_v=100k$, Aldrich) and the potassium trifluoromethanesulfonate salt (KCF_3SO_3 , Aldrich). PEO (13.5 mg/mL) and KCF_3SO_3 (2.5 mg/mL) were dissolved in cyclohexanone and MEH-PPV (10 mg/mL) in chloroform. A mixture of the two solutions resulted in a mass ratio of MEH-PPV(1):PEO(1.35): KCF_3SO_3 (0.25). The solution was sequentially spin-coated onto the patterned gold electrodes (spacing 60 μm) on a SiO_2/Si substrate and dried in vacuum at 70 °C for 12 hours. The resulting polymer film is around 350 nm, as measured by ellipsometry. All fabrication was performed in ambient conditions with the exception of vacuum drying. The formation of the frozen p-n junctions and the electrical characterization of the PODA system was performed in a cryostat under vacuum using a Keithley 4200s parameter analyzer.

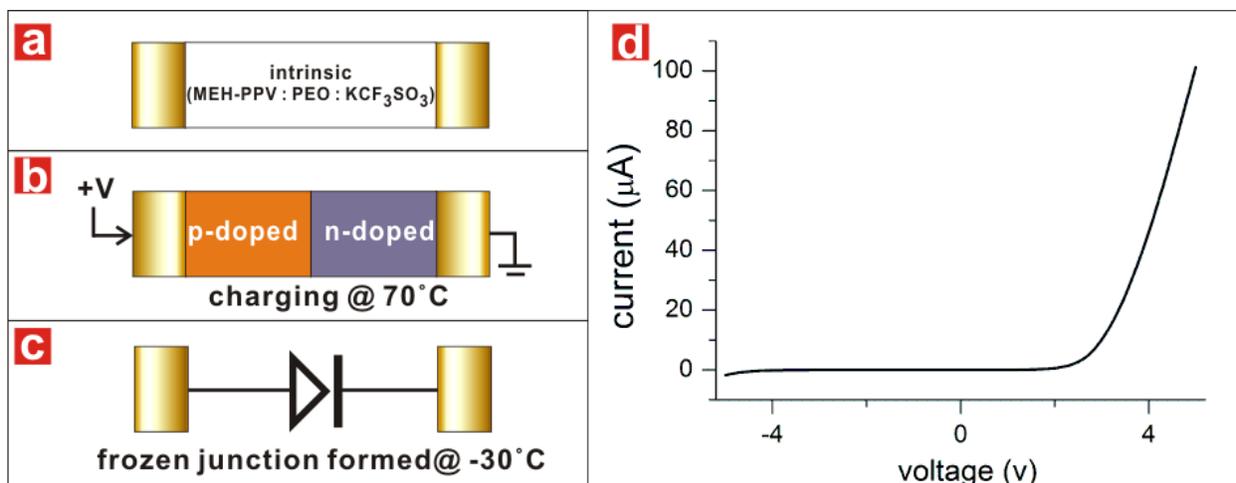


Figure 1. Formation and characterization of the frozen junction. a) global coating of active materials onto electrode pattern. b) EC doping leads to p- and n-doped regions of the polymer. c) diode is stabilized at low temperature. d) typical I-V characteristics of the frozen diode.

The frozen junction is defined as illustrated in figure 1, using the following steps: 1) after the deposition of active materials onto the electrodes (figure 1a), a doping potential of 4 Volt is applied at 70 °C (figure 1b) for a duration of 300 s. Since this temperature is above the melting point of the PEO material, ion transport will thus easily occur and results in p-doping and n-doping of the MEH-PPV adjacent to anode and cathode, respectively. Thus, an organic p-n junction is created. Light emission can be observed after 4-5 minutes, confirming the formation of the p-n junction. 2) With the voltage still applied, the temperature was decreased during 1200 s to -30 °C to freeze the as-formed p-n junction (current-time response shown in figure S1 in Supporting Information). At this temperature the ions are effectively immobile, meaning that a frozen p-n junction is established (figure 1c) and will remain irrespectively of the applied voltage. Different diode arrays can be created using different patterns of interconnected electrodes in combination with different programming voltage configurations.

3. Results

3.1 Characterization of the frozen diodes

Electrical current-voltage (I-V) characteristics of the frozen diode is given in figure 1d. The I-V characteristics displays a 2.2 V threshold voltage (V_{th}) and a current rectification of 80-100 between at -5 V/+5 V, which agrees with previously published value of frozen LEC p-n junctions²² ($V_{th} = 2.3$ V, rectification=80). Regarding the operational temperature, we have characterized frozen diodes at different temperatures and observed an increasing rectification ratio with temperature, as shown in figure S2 in Supporting Information. However, a too high temperature may mobilize the ions and neutralize the as-formed circuit. PODA displayed a stable signal output below -30 °C (see figure S3 in Supporting Information), but an unstable output at -20 °C. Therefore, we choose to operate PODA at -30 °C.

3.2 Two-diode array

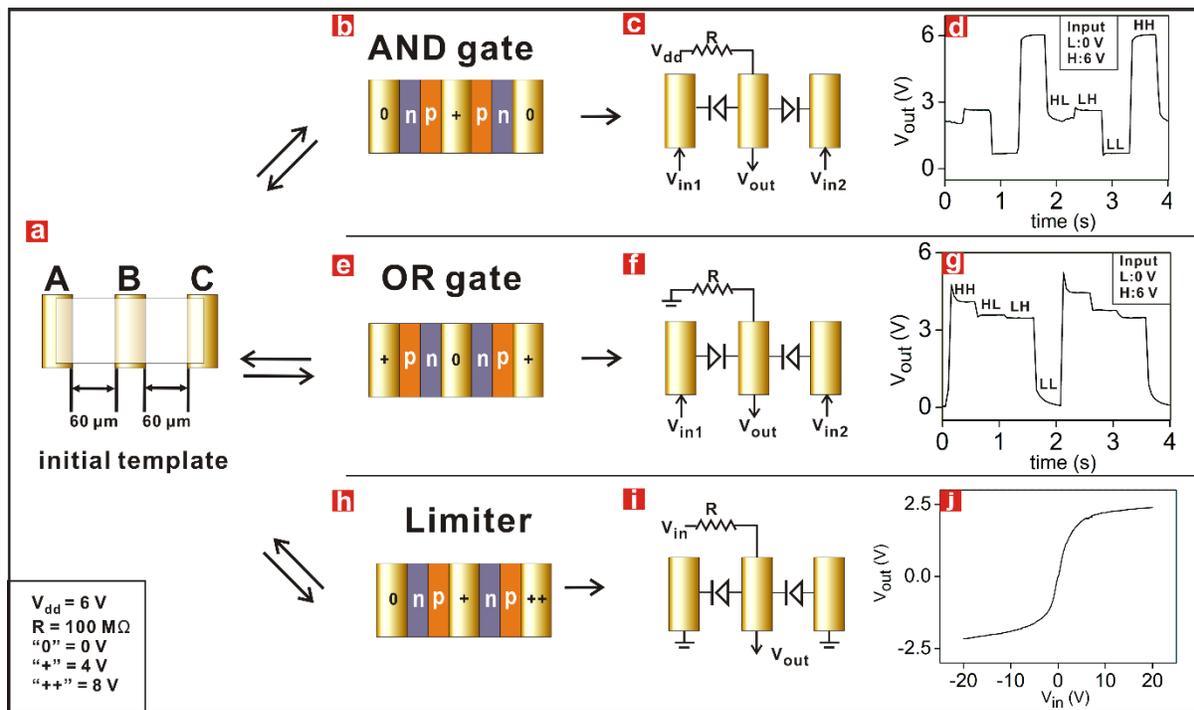


Figure 2. The electrode template (a) is used to create a logic AND gate (b,c), a logic OR gate (e,f) and a voltage limiter (h,i). The characterization is shown in (d), (g) and (j), respectively.

A two-diode array was created on an electrode template with three electrode pads in parallel as displayed in figure 2a, the pads are termed “A”, “B” and “C”. With external potentials applied between the A-B pads (V_{A-B}) and the B-C pads (V_{B-C}), two frozen p-n junctions can be formed simultaneously. Different applied voltage patterns can be used in order to set any desired pattern of polarities of the as-formed diodes. This is exemplified below by the sequential formation of three different circuits on the same two-diode electrode template.

Logic AND gate ($V_{A-B} = -4$ V, $V_{B-C} = +4$ V)

The logic AND gate can be formed using two diodes and one resistor, see figure 2c. To achieve this, we created two frozen diodes using the programming voltage configuration given in figure 2b and they were connected to external resistance and voltage sources (figure 2c). A series of digital voltage combinations with the frequency of 1 Hz were applied between terminal A and C, with digital LOW defined as 0 V and digital HIGH being 6 V. The resulting output signal levels are given in figure 2d. When both inputs are HIGH (6 V), a HIGH output (6 V) is delivered. Other input combinations result in a LOW output (0.5 V-2.5 V), where the voltage variation is due to the high V_{th} (2.2 V) of the p-n junction diode. During the transient between two input signals, a fluctuation of the output signal is observed which we ascribe to a charging effect in the p-n junction capacitor. After the measurement, the diode array was heated to a temperature of 100 °C for two hours, to neutralize the doped region through ion diffusion that erases the circuit.

Logic OR gate ($V_{A-B} = 4 \text{ V}$, $V_{B-C} = -4 \text{ V}$)

The erased template, presented above, was then used to create another circuit. The OR gate was created with a process similar to that used for the AND gate, see figure 2e and 2f. The characterization in figure 2g shows that when both inputs are LOW (0 V), a LOW output (0 V) is measured. Other input combinations result in HIGH output (4.7 V-3.5 V), again the output signal suffers from a voltage loss due to the high V_{th} of the diodes.

Voltage limiter ($V_{A-B} = -4 \text{ V}$, $V_{B-C} = -4 \text{ V}$)

Finally, the OR circuit was erased and a voltage limiter was formed on the very same template, as shown in figure 2h and 2i. An input voltage sweep from -20 V to 20 V was applied which results in an output voltage between 2.2 V and -2.2 V, as displayed in figure 2j. The output voltage (when $V_{in} > 2.2 \text{ V}$) was not ideally constant, because of the modest rectification ratio of the diodes.

3.3 Four-diode array

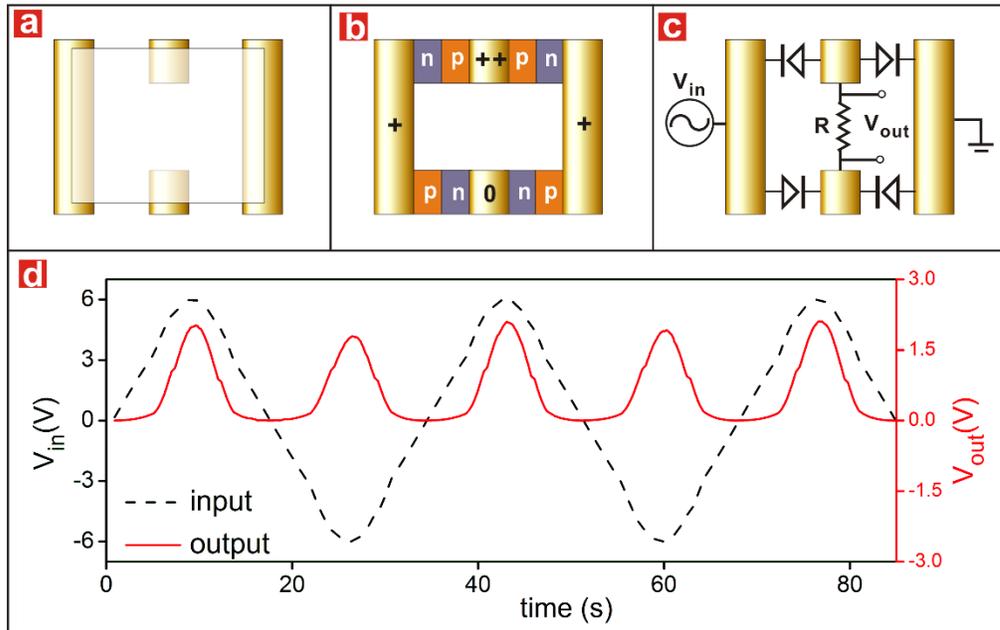


Figure 3. a) The four-diode template. b) Formation of diodes. c) Formation of the full-wave voltage rectifier. d) Characterization with an AC input signal of $\pm 6V$. The denotation used in figure 3 is the same as in figure 2.

Using a four-diode array, a full-wave voltage rectifier can be formed. With the electrode pattern shown in figure 3a and applied voltages as given in figure 3b, four diodes are simultaneously established. The connection of an external resistor, as illustrated in figure 3c, enables the circuit to function as a full-wave voltage rectifier, converting an 30 mHz AC input signal of $\pm 6V$ to a rectified voltage signal of double frequency, see figure 3d. The output signal exhibits a constant positive polarity and a synchronized phase as compared to the input, confirming the functionality of the rectifier. However, the output signal also has a relatively long empty cycle, which again is attributed to the large V_{th} . The peak amplitudes of the output signal are not totally even, due to slightly uneven EC doping profiles achieved in the four diodes.

4. Discussion

Considering that the PODA uses merely two material layers, i.e. the electrodes and the active material, that both are uncritical in terms of thickness, our suggested technology is a promising candidate for fully-printed, robust and large-area reconfigurable circuits requiring only two fabrication steps⁸. Starting from the working principle demonstrated here, there are several areas where the un-optimized process could be further improved. First of all, diode-based logics in general consumes more power than CMOS logics, due to the persistent V_{th} of diodes as well as the resistive component in the circuits. The high V_{th} in our PODA diodes are believed to relate to the bandgap of MEH-PPV²³. Therefore, a polymer with a relatively lower bandgap would be favorable in order to reduce the power consumption in the circuits. Furthermore, PODA requires a low temperature to immobilize the ions due to the low glass transition temperature (-67 °C) of PEO. Utilizing an ion conductor with a high glass transition temperature would allow for the formation of the frozen junction to occur already at room temperature (RT)^{16, 20}, indicating the possibility of a PODA operational at RT. Higher operating temperature leads to higher conductivity in conjugated polymers, thus PODA can potentially transform higher electrical power at RT. LECs frozen at RT also display a higher current rectification ratio ($\sim 10^5$)²⁰, which is crucial for minimizing the leakage current in PODA. Moreover, the circuits in this work display a relatively low operational speed. To combat this problem, the interelectrode distance should be reduced, which would decrease the time for charging and formation of the p-n junction capacitor. Gao et al. have shown that a vertically structured frozen junction can be turned on within 40 μs ²¹, which would enable a PODA circuit to operate at 25 kHz. Additionally, a reduced interelectrode distance would lead to a reduced device resistance thus increasing the current level

of the diode. A combination of the improvements listed above would certainly lead to PODAs that are practically useful in low-end printed applications.

5. Conclusion

In summary, we have demonstrated a working principle for a reprogrammable diode array based on reversible EC doping. Being a lateral structure, the fabrication of the device requires only two deposition steps, making it an interesting candidate for printed systems, in particular as the register and driver for LEC displays and lighting. In addition, the versatility of the LEC promises for more advanced circuit designs. An LEC can function as an insulator or as a conductor depending on the doping state, as a light-emitting device when a p- and n-doped region is formed, and also as a transistor when a gating electrode is added²⁵⁻²⁸. Combined with the logic and analog circuits demonstrated in this paper, more complex circuits/systems (such as a universal NAND gate) can be achieved with facile integration, and with the important advantage of using the same materials system for many different components.²⁹

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ASSOCIATED CONTENT

Supporting Information.

Temporal current response during diode formation, rectification of diodes under different temperatures, data retention of an AND gate. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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