Radiation Induced Effects in Electronic Devices
and
Radiation Hardening By Design Techniques

Examensarbete utfört i Elektroniska Komponenter
vid Tekniska högskolan vid Linköpings universitet
av
Johan Walldén
LiTH-ISY-EX--14/4771--SE
Linköping 2014
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Linköping, 13 juni 2014
Radiation Induced Effects in Electronic Devices and Radiation Hardening By Design Techniques

The aim with this thesis has been to make a survey of radiation hardened electronics, explaining why and how radiation affects electronics and what can be done to harden it.

The effects radiation have on electronics in general and in specific commonly used devices are explained qualitatively. The effects are divided into Displacement Damage (DD), Total Ionizing Dose (TID) and Single Event Effects (SEEs). The devices explained are MOSFETs, Silicon On Insulator (SOI) transistors, 3D-transistors, Power transistors, Optocouplers, Field Programmable Gate Arrays (FPGAs), three dimensional circuits (3D-ICs) and Flash memories.

Different radiation hardening by design (RHBD) techniques used to reduce or to remove the negative effects radiation induces in electronics are also explained. The techniques are Annular transistors, Enclosed source/drain transistors, Guard rings, Triple Modular Redundancy (TMR), Dual Interlocked Storage Cells (DICE), Guard gates, Temporal filtering, Multiple drive, Charge dissipation, Differential Charge Cancellation (DCC), Scrubbing, Lockstep, EDAC codes and Watchdog timers.

Keywords: Radiation, Radiation Hardening By Design, RHBD, Displacement Damage, DDD, Total Ionizing Dose, TID, Single Event Effect, SEE, Annular Transistor, Enclosed Transistor, Guard Ring, TMR, Guard Gate, Temporal Filtering, Charge Dissipation, Differential Charge Cancellation, Scrubbing, Lockstep, Lockahead, EDAC, Watchdog
Abstract

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The effects radiation have on electronics in general and in specific commonly used devices are explained qualitatively. The effects are divided into Displacement Damage (DD), Total Ionizing Dose (TID) and Single Event Effects (SEEs). The devices explained are MOSFETs, Silicon On Insulator (SOI) transistors, 3D-transistors, Power transistors, Optocouplers, Field Programmable Gate Arrays (FPGAs), three dimensional circuits (3D-ICs) and Flash memories.

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Chapter 1

Introduction

The purpose of this thesis has been to review the effects and damages caused by radiation in electronic systems and how they can be protected. The goal has been to qualitatively describe the effects and hardening techniques in a concise manner, providing the reader a good general knowledge within the area. The content of the thesis is divided into four chapters, including this introduction. The second chapter describes the radiation induced effects in materials and electronics in general. The third chapter further describes the radiation induced effects in important devices and technologies, emphasizing how their structure decides their susceptibility to the effects of radiation. The fourth chapter explains techniques that can be used to reduce or completely remove a systems susceptibility to radiation induced effects.

When designing spaceflight systems many sources and effects of radiation must be taken into account. The following citation from NASA [1] gives a good introduction into the different types of radiation effects and damage.

'The effects from the natural space radiation environment may be divided into two categories: long-term and short-term. The long-term effects have two separate concerns: ionizing and non-ionizing damage. Short-term effects are concerned primarily with single particle ionization and/or secondary particle formation. One should note that even short-term effects may be permanent.

Alternatively, one may view ionizing radiation effects in space electronics in two parts: total ionizing dose (TID) and single event effects (SEE). The two effects are distinct, as are their requirements and mitigation techniques. Though these effects are often a prime driver when discussing mission requirements, the non-ionizing radiation effects such as displacement damage dose (DDD) must also be considered.'
1.1 Environments

The sources of radiation affecting an electronic system naturally depends on its environment. Traditionally radiation has only been a problem in areas with elevated levels of radiation, such as space and particle accelerators. Nowadays device scaling has lead to that electronics are susceptible to radiation damage on a terrestrial level as well. This subchapter briefly discusses some environments where electronics are used and might require radiation hardening.

1.1.1 Space

Radiation levels in space depends on the proximity of extraterrestrial bodies. Always present are the galactic cosmic rays consisting of ions from other parts of the galaxy or deep space. Added to this are the constant flux of particles from stars if ‘within’ a solar system. These include x-rays, protons and electrons with protons being the dominant particle type. Close to stars and planets there can also be areas with higher particle density due to the magnetic field surrounding these bodies. Close to the earth there are two such belts, one at approximately 35768 km above the surface near the geosynchronous orbit consisting mostly of electrons, and one at approximately 500 km (varies rather much) near the low earth orbit consisting mostly of protons [2]. Both these fields are illustrated in figure figure 1.1.

![Figure 1.1: Near earth particle belts [2].](image)

1.1.2 Terrestrial

As device scaling continues the critical charge required to create single event effects (SEEs) gets smaller, 2.3. The main two contributors of particles capable of producing a SEE on a terrestrial level are radioactive components in the device package and neutrons created when cosmic rays interact with the earth’s atmosphere [3].

1.1.3 Particle accelerators

Particle accelerators usually produce particles with a wide range of energies. Depending on where in the accelerator the electronics are located different levels of radiation hardness must be met. Sensory equipment close to the area where the experiment take place must usually be able to sustain large amounts of radiation while most of the electronics used for processing data are placed further away and might not require any radiation hardness at all. One example would be a detector in the large hadron collider (LHC) in which the lifetime total ionizing dose (TID) is expected to be 250 Mrad (SiO2) and the displacement damage dose (DDD) \(2.5 \cdot 10^{15}\) n/cm\(^2\) (1 MeV neutron equivalent) [4].
1.2 List of Abbreviations

Abbreviations used throughout the thesis.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Definition</th>
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<td>TID</td>
<td>Total Ionizing Dose</td>
</tr>
<tr>
<td>SEE</td>
<td>Single Event Effect</td>
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<td>DD</td>
<td>Displacement Damage</td>
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<tr>
<td>DDD</td>
<td>Displacement Damage Dose</td>
</tr>
<tr>
<td>LHC</td>
<td>Large Hadron Collider</td>
</tr>
<tr>
<td>PKA</td>
<td>Primary Knock-on-Atom</td>
</tr>
<tr>
<td>SKA</td>
<td>Secondary Knock-on-Atom</td>
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<tr>
<td>SEU</td>
<td>Single Event Upset</td>
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<tr>
<td>MBU</td>
<td>Multiple Bit Upset</td>
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<td>SET</td>
<td>Single Event Transient</td>
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<td>ASET</td>
<td>Analog Single Event Transient</td>
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<td>DSET</td>
<td>Digital Single Event Transient</td>
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<td>SEFI</td>
<td>Single Event Functional Interrupt</td>
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<td>FPGA</td>
<td>Field Programmable Gate Array</td>
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<td>SEL</td>
<td>Single Event Latch-up</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
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<td>SCR</td>
<td>Semiconductor Controlled Rectifier</td>
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<td>SEB</td>
<td>Single Event Burnout</td>
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<tr>
<td>SEGR</td>
<td>Single Event Gate Rupture</td>
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<td>STI</td>
<td>Shallow Trench Isolation</td>
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<tr>
<td>SOI</td>
<td>Semiconductor On Insulator</td>
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<tr>
<td>BOX</td>
<td>Buried OXide</td>
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<tr>
<td>FinFET</td>
<td>Fin Field Effect Transistor</td>
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<tr>
<td>FDSOI</td>
<td>Fully Depleted Semiconductor On Insulator</td>
</tr>
<tr>
<td>PDSOI</td>
<td>Partially Depleted Semiconductor On Insulator</td>
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<tr>
<td>VDMOS</td>
<td>Vertically Depleted Metal Oxide Semiconductor</td>
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<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
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<tr>
<td>CTR</td>
<td>Current Transfer Ratio</td>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
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<tr>
<td>COTS</td>
<td>Consumer Off The Shelf</td>
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<tr>
<td>3D-IC</td>
<td>Three Dimensional Integrated Circuit</td>
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<td>RHBD</td>
<td>Radiation Hardening By Design</td>
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<td>TMR</td>
<td>Triple Modular Redundancy</td>
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<td>DICE</td>
<td>Dual Interlocked storage CEll</td>
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<td>DCC</td>
<td>Differential Charge Cancellation</td>
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<td>EDAC</td>
<td>Error Detecting And Correcting</td>
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<td>SEC-DED</td>
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<td>DWC</td>
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Table 1.1: Definition of terms.
Chapter 2

Radiation Induced Damage

Energetic particles incident on a solid material lose their energy through ionizing and non-ionizing processes as they travel through the material. Depending on what type of particle it is and its kinetic energy it will participate in one or more of these processes.

Charged heavy particles like protons and ions lose their energy through both ionizing and non-ionizing processes while lighter charged particles like electrons lose their energy mostly through ionizing processes. Heavy non-charged particles like neutrons lose their energy through non-ionizing processes.

The effects on electronics these processes have are usually divided into three categories: displacement damage, total ionizing dose and single event effects. The physics of these effects will be explained qualitatively in this chapter and their effects on different electronic devices in the next chapter.

2.1 Displacement Damage

Displacement damage occurs when an incident particle striking a material loses its energy through non-ionizing processes. The primary types of displacement damage are called vacancies and interstitials. A vacancy is the absence of an atom from its normal lattice position. An interstitial is when an atom resides in a non-lattice position. When a vacancy and an interstitial are close to each other they are called a Frenkel pair. Two adjacent vacancies are called a divacancy. Additional more complex defects occur when vacancies and interstitial are close to impurity atoms in the material, forming defect-impurity complexes [5].

The displacement defects can either be far apart, called point-defects or isolated defects, or close to each other and form a local region called a defect cluster, figure 2.1.

![Defect Cluster](image)

Figure 2.1: Conceptual illustration of the damage produced in Silicon [6].
When an incident particle strikes a material it will collide with the material’s atoms causing them to move. It is through these processes, non-ionizing, that the incident particle loses its kinetic energy and give rise to displacement damage. The first atom that the incident particle hits is called the primary-knock-on-atom (PKA). The PKA can, if its kinetic energy is high enough, produce secondary-knock-on-atoms (SKAs) which in turn can produce tertiary-knock-on-atoms and so on [7].

According to molecular dynamics simulations, many of the atoms in the PKAs path have kinetic energies higher than the average kinetic energy of atoms in the material at its melting point [7]. The PKA, and SKAs if they have high enough energy, therefore creates a track of molten material. When the molten material once again solidifies it is likely that various forms of defects remain. Depending on the momentum of the incident particle different types of defects are more or less likely to form. In general, incident particles can cause either isolated defects and clusters or only isolated defects. PKAs with a ‘small’ kinetic energy, relative to the energy required to displace atoms in the material, mostly leads to the formation of isolated defects while PKAs with a ‘high’ kinetic energy can cause both local defects along its track and SKAs capable of causing additional local defects and sometimes defect clusters if many local defects are caused within a small volume of material [7].

Once defects have been introduced in a material they will give rise to new energy levels in the band gap. Depending on where the new energy levels appear they will alter the materials electrical and optical properties differently [6].

![Figure 2.2: Radiation induced energy levels in the band gap [6].](image)

The following are fundamental effects on electrical properties [5]:

1. Increased thermal generation of electron-hole pairs through an energy level introduced near the middle of the band gap, figure 2.2 (a). This process can be viewed as the thermal excitation of a bound valence band electron to the defect center and the subsequent excitation of that electron to the conduction band. These defects will increase the leakage current in silicon devices that have a depletion region. The thermal generation is further increased if the irradiated material is near an electric field.

2. Increased recombination rate of electron-hole pairs. A carrier (electron or hole) is ‘captured’ at a newly introduced energy level and when a carrier of the opposite sign appears, recombination occurs, figure 2.2 (b). This reduces the carrier recombination lifetime and therefore harms bipolar devices that depend on it.

3. Carrier trapping at a shallow energy level (close to the conduction band), the carrier is later released, figure 2.2 (c). This defect therefore decreases the carrier transfer efficiency.

4. Compensation of donors or acceptors by radiation induced centers. For example, in n-type material free electrons from the donor level might be compensated for by radiation induced acceptors. This will alter the carrier mobility and thus the carrier concentration figure 2.2 (d). At length this might lead to type conversion in n- and p-type materials, making bulk silicon intrinsic.

5. A set of new energy levels can allow a carrier to tunnel through a potential barrier. For example, new energy levels in dielectrics might allow carriers to tunnel through them.

6. Radiation induced defects act as scattering centers which will reduce the carrier mobility.

The defects introduced in a material are however not permanent. Different types of annealing, forwards or reversed, takes place in most situations. Short-term annealing takes place immediately after the defect has been created and typically takes between a few minutes to some hours. After the short-term annealing, long-term
annealing takes place which can take many years, figure 2.3. The amount of annealing that happens depends on the material, the defect and the temperature. Higher temperature increases the defect mobility and thus its ability to move to a different position. The defects can be given higher mobility if carriers are injected into the material, increasing the annealing speed. This method is called injection annealing [5].

2.2 Total Ionizing Dose

When incident charged particles lose their kinetic energy through ionizing processes the long-term damages that occur are collected under the name total ionizing dose (TID). TID refers to the total amount of energy that is deposited by incident particles into a material, and is usually measured in rads. The main process by which TID affects a device is charge buildup in its dielectrics. One of the most commonly used dielectrics in transistors today are silicon dioxide, the effects described in this chapter will refer to that. Alternate dielectrics are being investigated more and more because of current leakage in the gate due to thin layers of dielectric in modern manufacturing processes, the end of this subchapter will contain a brief discussion about them.

The processes by which charge gets trapped in silicon dioxide when a charged particle strikes it are illustrated in figure 2.4 and are:

1. High-energy electrons and protons ionize atoms, generating electron-hole pairs. The generated electron-hole pairs can generate secondary electron-hole pairs if their energy are high enough. In this way, one incident electron or proton can generate thousands of electron-hole pairs.

2. The immediate recombination of a fraction of the generated electron-hole pairs. Most electron-hole pairs are not recombined since the electron mobility is much higher than the hole mobility, the electrons will leave the oxide in a matter of picoseconds [8]. The electric field applied across the oxide also affects how many electron-hole-pairs that will recombine since it will force the electrons and holes apart.

3. The generated holes that have not recombined will move through the silicon dioxide through a process called polaron hopping. A hole will move by hopping between localized states in the oxide. The direction decided by the electric field in the oxide. Due to its charge, as a hole moves through the oxide it causes a distortion of the local potential field of the oxide lattice. This local distortion increases the trap depth at the localized site, which tends to confine the hole to its immediate vicinity. This distortion follows the hole as it moves through the oxide, the charge of the hole combined with its strain on the oxide is called a polaron, this is why the process is called polaron hopping [8].

4. The holes that have not become trapped deep in the oxide will either leave the oxide, get trapped close to the surface of the oxide as a border trap or participate in the formation of an interface trap at the surface of the oxide, figure 2.5 [8].
Oxide traps

Two types of defect centers are participating in the formation of charge buildup in silicon dioxide, these defects are called E’ centers. $E_\delta$ is a relatively shallow trap responsible for the transportation of holes within the oxide, the polaron hopping. $E_\gamma$ is a significantly deeper trap [9]. Most of the $E_\gamma$ traps are located along the border of the oxide, close to the neighbouring silicon. These defects have the ability to communicate with the neighbouring silicon by transferring charges, and thereby switch state. The charges are transferred either by simple capture and re emission or tunneling [9]. Since these defects are close to the border and are able to exchange charge they are called border traps or switching states. The $E_\gamma$ located deeper in the oxide will act more like permanent traps. Once a hole has been trapped at a $E_\gamma$ trap deep in the silicon dioxide it will act as a permanent charge. Oxide traps have a net positive charge in both n- and p-channel devices. Both of these defects can be seen in figure 2.5.

Interface traps

As the name indicates, interface traps are located at the surface between an oxide and neighbouring silicon. Interface traps act very much like border traps in that they can switch state but since they are situated immediately on the surface of the oxide there is essentially no barrier for trapping and detrapping carriers. This will reduce the carrier mobility and recombination rates in the silicon adjacent to the oxide and thus affect devices that rely on those. In general, threshold interface traps are usually net positive in p-channel transistors and net negative in n-channel transistors. The formation of interface traps differ from the formation of oxide traps. It is believed that hydrogen ions (protons) are released as holes “hop” through the oxide or as they are trapped near the oxide interface. At the interface, hydrogen atoms can participate in a reaction leading to the formation of interface traps [8].

The amount of charge that can be trapped in an oxide depends on its thickness, the thicker the oxide is the more charge can be trapped. As technologies have continued to shrink, so has the thickness of the oxides. This has been beneficial in terms of TID damage since less charge can get trapped, charge buildup in the gate oxide
in modern technology nodes is therefore nearly non-existing. However the thinness of the dielectrics have caused problems as electrons can tunnel through them, increasing leakage currents. In order to prevent this leakage dielectrics with higher dielectric constants are being explored as they would allow the usage of thicker dielectrics with decreased tunneling leakage as a consequence. How these alternative dielectrics react to radiation seems to differ from material to material. Materials like Nitrified and Reoxidized Nitrified Oxides seems to be resistant to TID damage despite being much thicker than their silicon dioxide counterparts. Some materials like Hafnium Dielectrics have, at least in initial studies, been more susceptible to oxide traps than silicon dioxide [9]. Further testing of the materials and devices built from them is still required.

2.3 Single Event Effects

Single event effects are a collective name for scenarios where one incident particle causes an effect on a device or circuit level that propagates to system level. SEEs can be divided into soft-errors, that can be solved while the device is still working (such as a transient current), hard-errors that requires a power cycling or reconfiguration (such as a flipped memory bit or latch-up) and permanent-errors such as a broken transistor.

The most sensitive place, the place where a SSE is most likely to originate, is in a reverse biased pn-junction. When an incident particle strikes the reverse biased pn-junction a track of generated electron-hole-pairs forms a cylindrical volume with very high carrier concentration. A funnel shaped extension of the depletion region will form deep into the substrate while the generated electrons will start to drift towards the n-type material effectively creating a short across the pn-junction. The remaining carriers will proceed to diffuse towards the critical node where they get collected. This process is described in figure 2.6.

![Figure 2.6: Conceptual description of a pn-junction struck by a particle.](image)

With each new device scaling the charge used to store one bit of information gets smaller. The charge deposited by one incident particle is however constant. This leads to that the number of SEEs increases as device scaling continues. Depending on where in the device/circuit the particle strike, different SEEs occur. The most common SEEs are described in the following subchapters.
2.3.1 Single Event Upsets

A change in state or similar that may, or may not, cause the device to behave improperly. Flipped memory bits belong to this category. An example would be an SRAM cell whose nodes storing the information are struck by a particle and thereby makes them change state, figure 2.7.

![Figure 2.7: A particle strike in one node of an SRAM cell can cause a change in the node’s stored voltage state which can propagate to the other node, upsetting the cell [10].](image)

2.3.2 Multiple Bit Upsets

One single incident particle that causes multiple SEUs. This effect is becoming more probable as device scaling continues, allowing single particles to strike multiple devices, figure 2.8. The probability of an MBU increases when incident particles strike circuits at an angle, figure 2.9.

![Figure 2.8: Multiple sensitive volumes struck by an incident particle perpendicular to the surface [10].](image)

![Figure 2.9: Multiple sensitive volumes struck by an angled incident particle [10].](image)
2.3.3 Single Event Transients

SETs occur when a particle strike creates enough free charge to create a pulse that propagates through a part of combinatorial logic. This can happen in both analog and digital circuits but the events that decides if they cause damage differs.

A SET is created when a particle strikes the drain of a transistor. If the particle deposits enough charge the pn-junction will be upset and a short between the bulk and drain will form, giving the drain the same voltage as the bulk. The duration of this short depends on how fast the transistor can deliver enough charge to restore the reverse biasing of the pn-junction. The transistors current drive and the capacitive load on the drain therefore decides how wide the initial SET will be.

![Illustration of a pn-junction struck by an incident particle.](image)

**Figure 2.10: Illustration of a pn-junction struck by an incident particle.**

Analog Single Event Transients

ASETs appear as spikes and glitches in the output voltage of an analog circuit. Depending on the circuits function and what follows it the ASET may or may not cause damage.

Digital Single Event Transients

In order for a DSET to cause damage a certain sequence of events must happen.

1. A SET is generated in a sensitive logic node.
2. It propagates down a logic path to a memory element, like a flip-flop.
3. It arrives at the memory element with sufficient amplitude and duration to change the memory state.
4. It arrives during the setup and hold time of the memory element, i.e. the 'window of vulnerability'.

Depending on where in the digital logic the SET latches, masked, latent and unmasked errors can occur.

- A masked error is an error that is present in a memory element but does not affect the output nor the functionality of the system.
- A latent error is an error that does affect the output but not in a critical way, for example one faulty pixel in an image.
- An unmasked error is an error that affects the output in a critical way, making it unusable.

Digital Single Event Transient Pulse Broadening/Narrowing

DSET broadening, or more specifically 'propagation-induced-pulse-broadening' (PIPB), is an increasingly observed phenomenon in scaled technologies (<90 nm). The effect is that narrow SETs widen when propagating through combinatorial logic, increasing the risk of getting latched in a memory element. While DSET narrowing also occurs most effort is put into understanding DSET broadening since it makes the DSETs more dangerous. Whether DSET broadening or narrowing happens seems to depend on the input of a logic chain, a logical '1' leads to narrowing while a logical '0' leads to broadening [11].

The broadening/narrowing is caused by imbalance between the pull-up and pull-down networks switching point due to their transistors recent bias history, i.e. charge remaining in the transistors slightly shift the threshold voltage and thereby the switching point. This is especially troublesome in technologies with a floating body node, as an SOI technology without a body contact 3.2, since it takes some time before the charge in the body are neutralised but these effects can be observed in normal bulk technologies as well [12].

In figure 2.11 a chain of inverters have been used to illustrate PIPB experimentally.
DSET broadening/narrowing also depends on the system’s supply voltage and clock frequency. A decreased supply voltage generally results in increased PIPB while a higher clock frequency results in reduced PIPB, figure 2.12.
Digital Single Event Transient Pulse Quenching

In modern technology nodes, < 90 nm, the transistors are packed so densely together that the charge cloud from a single incident particle can affect multiple transistors. DSET pulse quenching involves two transistors as illustrated in figure 2.13 and proceeds as following:

![Figure 2.13: Depiction of SET pulse quenching. Normal SET generation and propagation through a 2-inverter chain (top). Pulse quenching appears since the charge sharing among PMOS P1 and P2 is coincident with the electrical propagation of the SET waveform from PMOS P1 to P2 (bottom) [12].](image)

1. A SET is created when the drain of the PMOS in the first inverter is struck by an incident particle.
2. The drain of the PMOS is driven high and the SET propagates to the next inverter.
3. The SET drives the PMOS in the second inverter to its off state and since this PMOS also is in the charge cloud, charge will diffuse towards it, helping it to return to its conducting state. The resulting SET that propagates past the second inverter is narrower than if no charge sharing had occurred since the PMOS was restored faster.

A requirement for pulse quenching is that charge sharing can occur in the technology. A second is that the charge collection time constant associated with charge sharing must be on the same order as the gate-to-gate electrical propagation delay of the logic, i.e. the propagating SET must arrive at the same time as the charge sharing ‘signal’ [13].

2.3.4 Single Event Latch-ups

SEL can occur in CMOS logic when the parasitic p-n-p-n structure between the source contacts are activated, figure 2.14. The p-n-p-n path resembles a semiconductor controlled-rectifier (SCR) that is stable in either its off- or on-state.

![Figure 2.14: Illustration of the p-n-p-n SCR between the source contacts in a CMOS technology [14].](image)

Normally the n-well is maintained at the same potential as the PMOS source, and the p-substrate at the same potential as the NMOS source. This prevents the SCR from latching, keeping it in its off-state. However, a
particle strike may cause the voltage in either the n-well or the p-substrate to drop and thereby make the SCR latch in its conductive state, effectively creating a short between the supply rails. In order to return the SCR to its off-state a power cycling is usually required.

Latch-up can also be caused by voltage transients in the supply rails which is why shallow trench isolation 3.1.2 or guard bands are used in modern CMOS technology nodes.

2.3.5 Single Event Functional Interrupts

SEFIs occur when radiation affects the control logic in a device such as a memory, an FPGA or a microprocessor. This may lead to multiple bit errors, page and block corruption, and loss of response in memories [15]. FPGAs can be placed in test modes, undefined states and experience halts. Devices experiencing a SEFI usually require a power cycling to restore its functionality [16].

2.3.6 Single Event Burnouts

An SEB occurs when the charge deposited by an incident particle creates a shunt between the drain and source whose current is large enough to burn a permanent short between the drain and source, rendering the device useless. The mechanism behind the thermal runaway is different in different transistor designs but it most commonly occurs in power transistors 3.4.

2.3.7 Single Event Gate Ruptures

An SEGR is caused when an energetic particle generates enough charge in the gate oxide to cause a local dielectric breakdown. The currents generated during the dielectric breakdown may result in a thermal runaway, melting a permanent short between the gate and source, rendering the device useless. SEGRs commonly occurs in power transistors 3.4.
Chapter 3

The Effects of Radiation on Different Technologies and Devices

Radiation induced damage affects different devices, circuits and systems differently depending on their structure and usage. This chapter explains the effects in some technologies currently used and some which might be of interest in the future. Having an understanding of how these technologies are affected is vital to understanding how they can be protected.

3.1 Bulk MOSFET and CMOS

The MOSFET has been the main transistor used during the latest three decades [9]. Continuous shrinking has allowed increased performance and system complexity as more and more devices can be placed on a chip. Not only the size of the devices themselves have decreased but also the amount of charge used to store and represent information. In modern technology nodes this charge is sufficiently small that single incident particles striking the transistor drain can result in transient currents in wires and multiple bit flips in memory elements.

3.1.1 Displacement damage

Not much information has been found on this topic while writing the thesis. The topic is usually ignored in most articles, sometimes with the comment ‘does not cause any relevant damage in this technology’. It is however clear that MOSFETs do get affected by displacement damage but not unless they are exposed to extreme amounts, such as in the LHC. In the remainder of this subchapter I give some reasoning as to why this is the case.

Being unipole transistors, MOSFETs do not suffer severely from displacement damage unless exposed to extreme amounts of radiation. This is because, as explained in 2.1, displacement damage mainly causes changes in the thermal generation, carrier concentration and electron-hole-pair recombination rates and the MOSFET only depends on its majority carrier. This means that the changes in carrier concentration and electron-hole-pair concentration will have little to no effect on a MOSFET. The increased thermal generation will increase the dark-currents (leakage currents) but this increase in leakage does not cause as many problems in modern technology nodes as it did in older technology nodes since significant leakage is already present due to tunneling through the thin dielectrics used in the transistors. The extra leakage from displacement damage is just a fraction of the total leakage, which is taken into account when designing circuits.

3.1.2 Total ionizing dose

Since the mechanism behind TID damage is charge trapped in isolation oxides, commonly silicon dioxide, the volume and location of isolation oxides both inside and close by a MOSFET determines its susceptibility to TID damage. Traditionally the gate oxide has been the major contributor to TID damage in a MOSFET. The charge trapped in the gate oxide would alter the MOSFET’s threshold voltage, figure 3.1, increasing the drain-to-source leakage in n-channel transistors since they would not be turned off properly and reducing the current drive in p-channel transistors since they would not be turned on properly. However, due to transistor
scaling the gate oxide in modern technology nodes is so thin that the charge buildup is either not present or very small [9]. It is also likely that any charge trapped in the gate oxide will be compensated for, or annihilated, by electrons tunneling through the gate oxide.

Figure 3.1: Shift in threshold voltage due to charge trapped in the gate oxide [9].

The use of shallow trench isolation (STI) to prevent latch-up in modern CMOS technology nodes is currently the main contributor for charge buildup and thus TID damage [17]. In general STI is implemented as shown in figure 3.2.

Figure 3.2: Shallow trench isolation in a CMOS technology.

As the charge trapped in oxides are predominately positive, NMOS and PMOS transistors are affected differently. The basic mechanism for leakage is that positive charge trapped in an oxide adjacent to a p-type silicon layer enables currents to flow from one isolated region to another. Places where this can occur are:

1. Drain-to-source leakage in one NMOS as shown in figure 3.3. Leakage parasitic NMOSs will form along the edges of the drain and source where the gate overlaps the STI. This will contribute to the off state drain-to-source leakage and a reduction of the threshold voltage.

Figure 3.3: (a) Parasitic NMOSFETs associated with the n-channel MOSFET, and (b) the effects of increased TID exposure on the threshold voltage and drive current of a parasitic NMOSFET [9].

2. Device-to-device leakage between two different NMOSs as shown in figure 3.4.

3. NMOS drain/source-to-n-well leakage as shown in figure 3.5.
Figure 3.4: Illustration of NMOSFET device-to-device leakage [9].

Figure 3.5: Illustration of NMOSFET drain/source-to-n-well leakage [9].

3.1.3 Single event effects

A MOSFET contain two reverse biased pn-junctions, one at the source and one at the drain. As described in 2.3 SEEs are originating from these junctions, most commonly the drain. When incident particles travel through the large volume of doped substrate material beneath the pn-junctions electron-hole-pairs are generated which give rise to SEEs. Separating the pn-junctions from the substrate material is thus one way to reduce the susceptibility of SEEs which is why SOI transistors, 3.2, are interesting when designing radiation hard circuits, figure 3.6.

Figure 3.6: Comparison of available substrate volume that can generate electron-hole-pairs near pn-junctions in bulk MOSFETs and SOI transistors [18].
3.2 Silicon on Insulator

Silicon on insulator (SOI) technologies have long been regarded as a contender for the regular bulk transistor in applications where radiation hardness is important. This is because the small volume of the bulk limits the collected charge and therefore SOI transistors are inherently resistant to SEEs, figure 3.6.

That which makes SOI transistors different from bulk transistors is the buried oxide (BOX) which isolates the drain, source and channel from the substrate. The BOX give SOI transistors complete immunity against classical latch-up but it also introduces two new parasitic structures, a parasitic bipolar transistor between the source, body and drain and a parasitic back-gate transistor, figure 3.7 (c). As an SOI transistors active areas are built on top of the BOX it has considerably less pn-junction area and capacitance than a bulk transistor which makes it ideal for low-power/high-performance applications.

There are two main types of SOI transistors, fully and partially depleted. The main difference between them is the thickness of the silicon layer above the BOX. In a fully depleted SOI transistor, figure 3.7 (a), the silicon layer is thin and totally depleted. In a partially depleted SOI transistor, figure 3.7 (b), the silicon layer is thicker and partially depleted with a neutral body zone beneath the gate.

Figure 3.7: Conceptual illustrations of a fully depleted SOI transistor (a), a partially depleted SOI transistor (b) and an equivalent electrical structure activated by radiation [19].

3.2.1 Total Ionizing Dose

In SOI MOSFETs the structures most susceptible to charge buildup from radiation are the BOX and, in CMOS configurations, the STI. The effects from charge buildup in the STI are similar to those in bulk MOSFETs, described in 3.1.2. The effects from charge buildup in the BOX differs between fully and partially depleted transistors.

**Partially depleted SOI transistors**

The primary effect of charge buildup in the BOX of partially depleted devices is increased drain-to-source
leakage currents in the top gate transistor. This will prevent the top-gate transistor from being completely turned off. If this leakage current gets too large the device might experience catastrophic failure.

**Fully depleted SOI transistors**

Fully depleted SOI transistors are more susceptible to the effects of oxide charge buildup and interface-traps as the top-gate transistor is electrically coupled to the back-gate transistor. Charge buildup in the BOX will, in addition to increased leakage currents, cause changes in the characteristics of the top-gate transistor such as decreased threshold voltage in n-channel transistors.

### 3.2.2 Single Event Effects

As mentioned above, SOI transistors are resistant to SEEs compared to bulk transistors because of their small bulk volume. The floating body does however make them susceptible to parasitic bipolar amplification. While minority carriers generated in a particle strike are quickly recombined, some majority carriers have a considerably longer lifetime. These majority carriers can drift towards the source and lower the source to body potential, making the pn-junction narrower, allowing injection of minority carriers into the body. The injected minority carriers will drift towards the drain where they are collected. These radiation induced effects resemble those of a bipolar transistor and they can negate any SEE advantage a SOI transistor has over a bulk transistor. The parasitic bipolar amplification can be reduced by adding a body contact, keeping the body at a fixed potential, figure 3.8. The non-recombined electrons will then drift to the body contact instead of the source and no bipolar amplification will occur.

![Figure 3.8: Conceptual illustrations of body contacts in SOI transistors [19].](image)

Parasitic bipolar amplification can also lead to a hard error, single event snapback. In an n-channel device, holes generated in the body region by a particle strike (that do not recombine immediately) will drift to the source and lower the source-to-body potential barrier allowing electrons to be injected into the body. These electrons will drift towards the drain and if the electric field in the body is strong enough they will generate new electron-hole-pairs by impact ionization. The holes generated in this way can drift towards the source allowing more electrons into the body that will generate even more electron-hole-pairs. This runaway condition is called snapback and can be caused either by radiation or electrically, if the potential difference between the drain and source is too large.

### 3.2.3 High Dose Rate

Due to their immunity to p-n-p-n latch-up, SOI circuits have long been used in applications where the radiation dose rate is very high. In addition to latch-up immunity the small sensitive body volume combined with the smaller pn-junction area reduces the dose received compared to bulk transistors. A prompt photocurrent generated in an off-state SOI transistor at high dose rate is shown in figure 3.9. As can be seen the photocurrent activate the parasitic bipolar transistor which increases the time it takes before the transistor is returned to its normal state (off in this case). If the parasitic bipolar transistor is prevented from activating, by adding multiple body contacts, an SOI transistor is very highly resistant to high dose rates.
3.3 FinFETs and Multigate 3D-transistors

Increased control of transistors electrical properties are required to enable devices to scale below 20 nm. Transistor designs with multiple gates and channels are being explored which allows tighter control of the electrostatics in the channels. The first breakthrough for these types of transistors was the FinFET, figure 3.10, in which the channel has been changed from its normal planar structure to a fin with the gate surrounding it from three sides.

As the idea behind 3D-transistors is to increase the control of the electrostatics in the channel, differences in how the gate surrounds the channel leads to different transistor designs with different properties. In figure 3.11 three examples of non-planar 3D-transistors are shown.

3.3.1 Total ionizing dose

The TID damage in a transistor is decided by where charge buildup in isolation oxides occur and how this charge affects the active areas. The differences in geometry between 3D-transistors and planar transistors thus account for their different TID behaviour. The gate surrounding the fin in a 3D-transistor can be divided into three smaller gates, two lateral gates on each side of the fin and one gate on top of the fin, figure 3.12.

Silicon on Insulator

In an SOI transistor an additional back-gate also exists on the surface between the fin and the BOX. The additional control of the electrostatic potential given by the lateral gates, and their vicinity to each other compared to the gate on top of the fin and the back-gate, will screen the vertical coupling effect between
the top gate and radiation induced charge in the BOX. The SOI FinFET will thus be intrinsically resistant to charge buildup in the BOX.

The geometry of the transistors also decide what the electrostatic potential in the BOX looks like. As shown in figure 3.13 the electric field lines in narrow fin transistors are pointing into the BOX while they bend and point towards the active silicon in wide fin transistors (planar transistors). This means that the radiation induced carriers will travel to the active silicon in wide transistors where they create trapped charges and interface traps while the radiation induced carriers in narrow transistors will travel into the BOX away from the active areas. This intrinsic ability makes the SOI FinFETs even more resistant to TID damage.

Figure 3.12: *The three 'different' gates in a FinFET.*

**Bulk FinFET**

In a bulk FinFET the fin is defined by the STI, figure 3.14, and its TID response will therefore be defined by the charges trapped in the STI. In figure 3.15 the electrical field inside the fin is plotted. As can be seen the electrical field inside the fin is affected by the electrical field originating from the charges trapped in the STI sidewalls. When the fin is made narrower the trapped charges are situated closer to the center of the fin and therefore affect the electrical field in the channel in a stronger way. This will appear as a degradation of the drain current in PMOS devices, preventing it from turning on properly [21]. In addition to this, STI sidewall leakage (parasitic lateral transistors) observed in planar devices might get activated in bulk FinFET devices as well since there are places where the STI sidewalls are adjacent to the channel 3.1.2 [20].

Figure 3.13: *The three 'different' gates in a FinFET* [20].

**Figure 3.14:** *A bulk FinFET.*

**Figure 3.15:** *The electrical field inside the fin in a bulk FinFET.*
3.3.2 Single Event Effects

The creation of SEEs depends on the critical charge required to upset a device and the charge collection capabilities of the device. These two parameters depend on device geometry, operating voltage and the circuit topology which makes the behaviour of FinFETs different from planar transistors [22].

Compared to planar SOI transistors, narrow SOI FinFET transistors experience increased parasitic bipolar amplification. When carriers are generated in the silicon fin the minority carriers recombine quickly while the majority carriers remain for a longer duration and forward bias the parasitic bipolar transistor. When the parasitic bipolar transistor is forward biased a current between the drain and source increases the amount of charge collected at the drain node. This results in that a FinFET requires more time before the effects from the radiation induced carriers are removed [21] [19]. An example of this is shown in figure 3.16 where the drain node collects more than twice the amount of charge in the $\Omega$ – FET as the planar FDSOI.

As shown in figure 3.17 the charge collection in bulk FinFETs are greater than the charge collection in SOI FinFETs. This is because of the larger sensitive volume available for charge deposition. The duration of the transients created by radiation may be reduced by using dual- or triple-well technologies which reduces the amount of collected charges [21].
Figure 3.16: Current transients induced by a pulsed laser irradiation in a planar FDSOI single-gate and in a non-planar Ω–FET [20].

Figure 3.17: Drain current transients generated by a pulsed laser in both p-type SOI and bulk FinFETs [20].

In scaled technologies the size of device features have reached the same dimensions as the track of generated charge from incident particles. This makes it possible for the charge track from an incident particle to create a shunt between the drain and source. The transient shunt effect is present in both SOI and bulk technologies as shown in figure 3.18. In the bulk FinFET (top) the transients at drain and source are different, the drain transient have higher amplitude and tail. The amplitude is higher since the electrons generated in the well are also collected in the reverse biased junction. The longer tail is due to electrons generated deeper in the well that takes more time to diffuse to the drain contact. In the SOI FinFET (bottom) the transients in the drain and source are equally large, the buried oxide isolates the well from the fin and thus the electrons generated deeper in the well cannot diffuse to the fin.
3.3.3 Permanent Heavy Ion Damage and Microdose Effects

As stated above, the size of transistors in scaled technologies are on the same level as the track of charge generated by incident particles. For narrow structures this means that single heavy ions can cause extensive damage to the crystal lattice in isolation oxides and active silicon areas as well as generating enough carriers to cause large amounts of trapped charges and interface traps. Damage to the gate crystal lattice changes the electrical properties of the gate oxide which increases the gate leakage current [21]. Interface traps are formed by ions along the lateral gates as shown in figure 3.19 (b) as well as in the BOX along with trapped charges figure 3.20.

These effects refer to SOI transistors as no experiments with bulk FinFETs have been found during the writing of this thesis.
3.4 Power Transistors

In situations where voltages need to be converted, such as in a power distribution system, special transistors capable of working with higher voltages are needed. Power MOSFETs are transistors designed to be able to handle higher current density, higher power dissipation and higher reverse breakdown voltages.

Traditionally the vertically diffused MOSFETs, figure 3.21 (a), are the most used power MOSFETs as their good switching behaviour makes them suitable to use in power supplies and DC-DC converters [23].

Transistors that are being used more and more in commercial technologies are trench power MOSFETs, figure 3.21 (b), superjunction MOSFETs, figure 3.21 (c), and laterally diffused power MOSFETs, figure 3.21 (d). Experimental radiation results from these technologies are still rare and inconclusive but with additional research they might be good contenders for applications in radiation environments [24] [25].

Figure 3.21: Illustration of four different types of power MOSFETs. (a) vertically diffused, (b) trench, (c) superjunction and (d) laterally diffused [26].

As power transistors are often used in power distribution systems it is important that they operate reliably because if they experience catastrophic failure the entire system could malfunction or stop working permanently. To be able to operate reliably power transistors are usually built from technology nodes two or more generations old so that their performance and liabilities are well known [23].
3.4.1 Total ionizing dose

Power MOSFETs contain, as they should be able to sustain higher voltages, thicker layers of isolation oxides than regular MOSFETs. This, includes thicker gate oxide which makes the power MOSFETs susceptibility for TID damage high.

As described in 3.1 MOSFETs get their threshold voltage and voltage swing shifted from charge buildup which causes problems as it will affect a power MOSFET’s switching behaviour and thus directly its performance in a power converter. In addition, in NMOSFETs the threshold voltage shift means that the transistor will not shut off properly which will increase the static power consumption (drain-to-source leakage) and potentially damage the device [23].

3.4.2 Single event effects

Power MOSFETs are particularly susceptible to SEB and SEGR due to the large voltages present in the transistors.

Single Event Burnout

SEBs occurs in VDMOSs when a high energy particle, like a heavy ion, passes through the n-p-n area of the transistor while it is biased in the off state. Carriers generated by the heavy ion turn on the parasitic bipolar transistor in the VDMOS and due to a regenerative feedback mechanism, collector currents in the parasitic BJT increases to the point where a thermal failure creates a permanent short between the source and drain [23]. This process can be seen in figure 3.22. The localized melting will often damage the gate, resulting in a leakage path between the gate and source and/or drain. Not all energetic particles that strike the correct place (the n-p-n area) will cause a SEB though, how close the drain is to its breakdown voltage, operating temperatures and the incident angle of the particle affects the likelihood of an SEB [24].

![Figure 3.22: Basic structure of a vertical power MOSFET with illustrations of the single event burnout and single event gate rupture events.](image)

Single Event Gate Rupture

The exact mechanism behind a SEGR in a VDMOS is not completely understood, it is therefore divided into two different mechanisms. A substrate response could be added to those two mechanisms but according to [24] the substrate’s role in SEGR is very limited since it does not contain any depletion field. Most reports declaring the substrate’s response in SEGR might be because is is difficult to differentiate between the substrate response and the epitaxial response.

Capacitor Response

The capacitor response can be understood as dielectric breakdown in a MOS capacitor figure 3.23. When a heavy particle strikes the capacitor the dielectric breakdown voltage is decreased. If the breakdown voltage is decreased below a critical value breakdown occurs which might result in a SEGR.
Epitaxial Response
In a VDMOS the role of the epitaxial layer is to support a high electric field within the device. The thickness and doping of the epitaxial layer decides the blocking voltage and the on-resistance. When a heavy particle generates a track of charge in the epitaxial layer it will couple a portion of the drain voltage to the surface between the epitaxial layer and the dielectric figure 3.24. This coupled charge will increase the electric field between the gate and source which might result in dielectric breakdown leading to a SEGR.

3.5 Optocouplers
Despite their simplicity optocouplers have been and are still used, especially in spaceflight electronics [27], to connect electronic subsystems without a direct electrical connection. A basic optocoupler consist of a LED, transmitting a signal optically, and a photo transistor that receives the optical signal, figure 3.25. Both the LED and the photo transistor depend on minority carrier lifetimes and carrier recombination rates making them highly susceptible to displacement damage. The main effect from displacement damage in optocouplers is changes in the current transfer ratio (CTR) which directly affects the optocoupler’s functionality [27].

As basic optocouplers have long response times and very low power transfer efficiency they are usually connected to a high-speed amplifier to compensate. The high-speed amplifier integrated together with a photo-diode to detect the signal from a LED with shallow junctions, figure 3.26, allow higher radiation hardness. However, optocouplers with high-speed amplifiers can experience catastrophic failure if the LED output is reduced below the minimum value required by the amplifier. In addition to this, the large active area of the photo-diode is susceptible to create SETs, especially for angled incident particles. The generated SETs will then be amplified by the amplifier, possibly creating errors in following circuits. These SETs can however be filtered away inside the optocoupler before entering the amplifier using temporal filtering, 4.2.4, at the cost of increased delay.
3.6 Field Programmable Gate Arrays

As the integration level continues to increase, enabling more functionality, providing higher performance and consuming less power, in applications that are not mass produced or requires extreme performance, FPGAs are a tempting alternative to designing an ASIC. While there are a few radiation hardened FPGAs on the market these are usually expensive and have less performance than the latest consumer-of-the-shelf (COTS) products.

FPGAs can be conceptually split in two layers, an application layer that includes the user logic and the memory elements managed by the user logic, and one configuration layer including the logic and memory required to configure the user logic and routing resources, figure 3.27. What type of memory the configuration memory is built with defines the main FPGA categories, SRAM, antifuse and flash. Due to their high susceptibility to TID damage flash based FPGAs are usually not deemed usable in radiation environments [28]. SRAM based FPGAs are susceptible to SEUs which is especially troublesome since upsets in the configuration memory might cause the user logic to change. Antifuse based FPGAs are immune to SEUs in the configuration memory, making them naturally radiation hardened.

What sets SRAM based FPGAs apart from ASICs and antifuse based FPGAs are their ability to be reconfigured and thus adapt to new mission parameters, allow patching and unique radiation mitigation techniques. That makes the use of SRAM based FPGAs in radiation environments desired if possible.

In order to make an SRAM based FPGA suitable for a radiation environment its configuration memory must be hardened. The most common technique to do this is called scrubbing, 4.3.2, in which parts of, or the entire configuration memory is reconfigured. Depending on the environment different levels of scrubbing can be used. In environments with low radiation levels and for non-critical systems, a reconfiguration at certain intervals might be enough. In environments with higher radiation levels and for mission critical systems a complete reconfiguration at certain intervals might be possible, but a partial reconfiguration of the configuration memory that does not interrupt the system’s operation is preferable.

Partial reconfiguration can be done in some newer FPGA technologies like Xilinx Virtex-4QV/5QV FPGAs [29]. In these FPGAs the configuration memory is organised into frames that can be reconfigured individually. Partial reconfiguration also makes it possible to handle permanently damaged areas of the configuration memory. If a frame is found to be upset after successive reconfiguration attempts it can be regarded as broken and forbidden to use. In a following reconfiguration the functionality of the broken frame is moved to another frame so that the system can regain functionality. This of course requires that there are some unused frames available in the configuration memory.
3.6.1 Total ionizing dose

The degree to which FPGAs are vulnerable to TID depends on the transistor type used and the use of STI. Most COTS FPGAs use bulk MOSFETs and STI in their CMOS parts and are thus susceptible to TID damage. Testing this during development is important to determine if the FPGA is usable or not. Radiation hardened FPGAs built in a radiation hardened process can be used if the amount of TID damage is large. Many FPGAs have their radiation hardness tested and collections of these tests, such as [30] and [31], can be used to decide which FPGA is suitable for a specific mission.

3.6.2 Single event effects

The SEEs that affect FPGAs, in addition to SEUs in the configuration memory as discussed above, are SETs, SEUs in the application layer’s user logic and SEFIs. SETs and SEUs can be hardened against using TMR. In some radiation hardened FPGAs, techniques such as temporal filtering, guard gates and TMR have been used in the design of the FPGA, but they have been made invisible to the user. SEFIs usually require a complete reconfiguration or power cycling to restore functionality to the FPGA.

3.7 Three Dimensional Circuits

In a 3D-IC dies have been stacked vertically to achieve higher transistor density and interconnect density. In figure 3.28 and figure 3.29 an example of a 3D-SOI circuit using three tiers (layers) are shown. The higher transistor density in 3D-ICs makes it possible to continue improving system performance beyond the end of Moore’s Law [32]. The increased interconnection density allows for using shorter interconnection wires with less wire capacitance which reduces the capacitive load and therefore the power consumption [33].

![Figure 3.28: Illustration of a three tier SOI 3D-IC [34].](image)

![Figure 3.29: Scanning Electron Micrograph of a 3D-IC wafer with three FDSOI CMOS tiers [34].](image)
The drawbacks with 3D-ICs are difficulties in manufacturing and heat dissipation. 3D-ICs are assembled on a wafer scale, each tier is manufactured as a die which is then assembled with the other dies. This means that if just one die is faulty the entire 3D-IC will malfunction which might reduce yield beyond acceptable limits [33]. As the tiers are stacked on top of each other the heat from all tiers except the top tier must dissipate through the tiers above. If this heat is not removed in some way the performance gained by using a 3D-IC is lost because of increased signal propagation delay.

### 3.7.1 Total Ionizing Dose

Results from TID experiments so far show that 3D-SOI circuits are equally sensitive to TID damage as single tier circuits. The cross section for different tiers are similar and angular effects from protons and neutrons can be directly attributed to the particle path length within the sensitive volume [32].

### 3.7.2 Single Event Effects

Results from SET experiments with heavy ions show that all tiers in a 3D-IC are vulnerable to SETs and they behave the same as single tier circuits. All tiers except the bottom one show similar SET distributions, the bottom tier have a larger cross section and narrower pulse width. This is likely because of the tungsten vias between the tiers. When incident particles collide with the high-Z tungsten, secondary particles are generated and since the bottom tier has more tungsten above it, it is exposed to a larger number of secondary particles, figure 3.30 [34].

In [35] it is also shown that using body ties reduces the duration of SETs in 3D-ICs with the same amount as in single tier circuits.

![Figure 3.30: Secondary particles created by a nuclear reaction between an incident particle and a tungsten via](34).

Figure 3.30: Secondary particles created by a nuclear reaction between an incident particle and a tungsten via [34].
3.8 Flash Memories

Flash memories are widely used as non-volatile storage in the commercial market but they have seen limited use in space and other radiation environments. It is however desirable to use flash memories since current radiation hard non-volatile memories have very limited capacities, usually below 64 MBit.

Flash memories comes with a number of advantages and disadvantages compared to normal SDRAMs which is why SRAMs are still used extensively in some applications. Important advantages include:

- Higher storage density -> Savings in mass and size.
- Can be kept unbiased -> Substantial energy savings.
- Non-volatile -> Can be power cycled without data loss -> SEFIs can quickly be restored with a power cycling.

Important disadvantages include:

- Lower data rate than SDRAMs -> Not as good as SDRAMs when used as workspace random-access-memories.
- Data cannot be modified in place, entire pages must be rewritten at the same time -> Unsuitable as workspace random-access-memories.
- Limited endurance, each memory cell only survives $10^4 - 10^5$ erase/program cycles -> Flash memories are only suitable as long term storage memories.

In conclusion flash memories’s qualities makes them suitable as long term storage memories. Their non-volatility also makes them easy to recover from a SEFI. However, flash memories are quite susceptible to radiation which is explained in the following subsections.

3.8.1 Effects on Storage Cells

A flash memory storage cell is designed to store charge in a floating gate as shown in figure 3.31. The floating gate (FG) is placed between two layers of insulating oxides trapping charge in the floating gate. The charges in the floating gate can tunnel through the bottom oxide under certain bias conditions which is how the memory cell is programmed/erased. When the memory cell is to be read a predetermined gate voltage is applied and the drain current measured. The charges trapped in the floating gate affects how large the drain current is and from this the memory content of the cell can be determined figure 3.32.

![Figure 3.31](image)

Figure 3.31: Cartoon explaining the functionality of a flash memory cell [28].
Figure 3.32: *By measuring the drain current when a predetermined gate voltage is applied the content of the memory cell can be determined [28].*

**Total Ionizing Dose**

The isolating oxides on both sides of the floating gate makes flash memory cells vulnerable to TID damage. The basic mechanisms are summarized in figure 3.33.

![Figure 3.33: Basic TID damage mechanisms in a flash memory cell [28].](image)

1. Carriers generated by radiation in the isolation oxides (ONO and tunnel) are injected into the floating gate, decreasing the amount of charge stored there.
2. Charge trapped in the channel isolation oxide, this charge is added to the charge in the floating gate and affects the gate threshold voltage.
3. The radiation transfers enough energy to the charges in the floating gate that they escape the potential well.

**Single Event Effects**

SEEs in flash memories are not yet completely understood. There are two models available, the ‘transient conductive path’ model and the ‘transient carrier flux’ model.

The ‘transient conductive path’ model assumes that a leakage path discharging the floating gate is created along the charge track from an incident particle. The path exists until the generated carriers recombine but the physical mechanism of the conductive path is still under discussion. One idea is that the radiation induced carriers make the band structure collapse. Another idea is that the particle strike creates temporary defects in the isolation oxides, allowing the stored charges to escape via tunneling.

The ‘transient carrier flux’ model assumes that carriers generated in a particle strike tunnel in and out of the floating gate. Unbalance between the tunneling currents is what discharges the floating gate.
A third, older model attributes the shift in the gate threshold voltage to oxide border traps and interface traps. While this effect likely exists, it is likely to be minor compared to the other mechanisms since the oxide thickness surrounding the floating gate is very thin. Any traps present are likely to be annealed by carriers tunneling through the oxide. This is more or less verified by experiments.

3.8.2 Effects on Peripheral Circuitry

Since flash memories require complex erase and program procedures peripheral circuits such as decoders, encoders and a microcontroller are involved in operating the flash memories and they are usually included on chip. Radiation affecting these peripheral circuits can cause SEFIs and catastrophic failures from TID damage and SEGRs.

Total Ionizing Dose

The most sensitive part of a flash memory is the charge pump producing the high voltages needed when erasing/programming a memory cell. The charge pump has to be very precise to enable correct functionality and since it is built with transistors with thicker oxide layers to cope with the higher voltages it is sensitive to TID damage. When the output from the charge pump drops below a certain value the flash memory will experience catastrophic failure since the memory cells cannot be read, programmed or erased. This effects can be seen in figure 3.34.

![Figure 3.34: The charge pump output voltage decreases as the TID increases [28].](image)

Single Event Effects

When data is to be read, programmed or erased in a flash memory an entire page needs to be modified. To do this the page is loaded into a page buffer where individual bytes can be modified. A number of SEFIs can occur when a page is read, programmed or erased such as partial reads/programmings/erases and endless loops. These errors appear when SETs and SEUs affect the peripheral circuitry.

Heavy ions striking the charge pump might also cause SEGRs. These events appear as an initial current spike followed by a significant drop of the charge pump’s output voltage, rendering the flash memory useless.
Chapter 4

Radiation Hardening by Design

Radiation hardening by design techniques are used to improve the radiation hardness of a device, circuit or system without changing the manufacturing process. RHBD is used because it is usually cheaper than a special manufacturing process and it allows the use of COTS products. In general it involves redesigning devices and circuits, adding redundancy and temporal filtering to mitigate the effects induced by radiation.

4.1 Device level

4.1.1 Transistor Layouts

In order to protect from the effects of charge buildup in isolation oxides, such as drain-source leakage 3.1.2, transistor layouts such as annular transistors and enclosed source/drain transistors can be used. In figure 4.1 a comparison between a standard two-edged, annular and enclosed source/drain transistor is made.

![Figure 4.1: Schematic top-views of a conventional two-edged, an octagonal annular gate and an enclosed ringed-source transistor [36].](image)

Annular Transistors

The idea behind an annular transistor is that it has no active diffusion areas that are adjacent to any isolation oxides that is overlapped by polysilicon (gate), figure 4.2. This means that it cannot be any source-to-drain leakage along an isolation oxide sidewall due to radiation induced parasitic transistors. This makes the annular transistor much less sensitive to the effects of charge buildup in isolation oxides, i.e. TID damage.

There are some drawbacks though, the first is increased area. An annular transistor requires approximately three times the area of a two-edged transistor at minimum size, the difference in size gets smaller when minimum transistor sizes are not used. The second drawback is drain/source capacitance. Depending on if the source or drain is placed in the middle, the device will behave differently as the node in the middle will have less capacitance to the bulk. Placing the drain in the middle thus yields higher performance while placing the source in the middle results in higher reliability. The third drawback is asymmetry in the output characteristic. The output conductance is higher for a device with the drain in the middle than for a device with the drain on the outside, at the same bias. This is because the distance between the pinch-off point and the drain will be smaller with the drain on the outside due to the conversion of space charge region.
Enclosed Source/Drain Transistors

In an enclosed source/drain transistor either the drain or source is completely enclosed by polysilicon (gate), figure 4.3. Just as with the annular transistor, this transistor layout has no places where the channel is adjacent to an STI sidewall that is overlapped by gate polysilicon. This prevents any leakage paths to connect between the drain and source and therefore the effects due to charge buildup in isolation oxides are reduced.

While an enclosed source/drain transistor can be made smaller than an annular transistor it is still larger than a two-edged transistor. The extra polysilicon used to enclose the drain/source also increases the enclosed drain/source-to-gate capacitance.

Just as with an annular transistor, enclosing either the drain or the source gives the transistor different characteristics compared to a normal two-edged device. When the drain is enclosed, the parasitic gate-to-drain capacitance appears as a Miller capacitance when referred to the input, making the device slower. This in combination with the added resistance from the larger gate can introduce an additional RC-delay to the circuit where the enclosed transistor is used. Because of this it is usually the source that is enclosed.
4.1.2 Guard Rings

Diffusion Rings

In order to prevent interdevice leakage, figure 4.4, a p\textsuperscript+ - diffusion or n\textsuperscript− - diffusion ring can be used to surround adjacent NMOS and PMOS devices respectively. The highly doped diffusion ring will introduce a very high voltage threshold in the bulk between two devices and thus prevent leakage between them, figure 4.5.

Figure 4.4: Radiation induced hole trapping in thick isolation field oxides can drive the parasitic field oxide transistor into inversion, resulting in leakage between adjacent devices [10].

Figure 4.5: A p\textsuperscript+ channel stop in the field-oxide isolation to reduce interdevice leakage [10].
Guard Bands with Contacts and n-well separation

Decreasing the charge sharing between adjacent devices can decrease the susceptibility of MBUs. Two ways to decrease charge sharing are:

1. Placing guard bands with additional bulk contacts between adjacent devices figure 4.6 (b).
2. Use separate n-wells for each PMOS device figure 4.6 (c).

If the drain of one device is struck by an incident particle the guard contact or separated n-wells will reduce the amount of induced charge that diffuses to the drain of an adjacent device and thus prevent a MBU.

Figure 4.6: Illustration of a) a baseline structure without guard bands, b) improved structure with guard contact isolation and c) improved structure with separate N-wells and guard contact isolation [37].
4.2 Circuit level

4.2.1 Triple Modular Redundancy

Triple modular redundancy (TMR) is a common way to mitigate the effects of SEUs and SETs. Duplication of a circuit/system allows the hardware to detect errors by comparing the outputs. Triplication of a circuit/system allows a voter to choose the output as the majority of three and also to point out the circuit/system that had the incorrect output, figure 4.7. TMR will thus provide a correct output as long as only one of the three circuits/systems outputs are incorrect. If more than one output are incorrect the voter can either pick any of the outputs or signal for a recomputation. On circuit level the voter usually picks any output if more than one output are incorrect but the probability of this event is very small (if not, these events must be taken care of). On system level recomputation may or may not be required depending on the consequences of one incorrect output. In sensitive situations the voting logic itself can be triplicated to prevent upsets in the voter to be propagated.

![Figure 4.7: Triple modular redundancy fault masking [38].](image)

The drawback with TMR is that the area and power consumption of the system/circuit increases with more than 200%. Therefore careful consideration must be taken when deciding which parts of the circuit/system TMR is to be applied on. The voting logic also takes some additional time which means that the circuit/system will get slightly longer latency that might require a lower clock speed.

4.2.2 Dual Interlocked Storage Cells

The DICE uses a four node redundant structure to reduce the probability of SEUs in memory elements such as flip-flops and SRAMs. It consists of two cross-coupled inverter latch structures, $N_0 - P_1$ and $N_2 - P_3$, connected by bidirectional feedback inverters, $N_1 - P_2$ and $N_3 - P_0$. The four nodes, $X_0 - X_3$, store data complementary, $X_0$ and $X_2$ store one value while $X_1$ and $X_3$ store the complementary value, figure 4.8. Since these nodes are feedback connected to each other, two nodes must be struck simultaneously if the DICE is to experience a SEU. In older technology nodes the probability of MBUs occurring in DICE was very small. DICE implemented in modern technology nodes might require a larger area to keep the nodes (that store the value) separated.

![Figure 4.8: Schematic of a dual interlocked storage cell [10].](image)
The DICE uses twelve transistors, twice as many as a normal SRAM cell, making it roughly twice as big in terms of area. The additional transistors also makes the DICE require additional drive current to read and write. While the DICE is hard against SEUs it is vulnerable to SETs while transparent, just as a normal SRAM cell.

4.2.3 Guard Gates

A guard gate is an approach to prevent SETs from reaching a latch. The guard gate is preceded by a temporal delay as shown in figure 4.9. When both inputs, A and B, are the same the guard gate acts like an inverter. When A and b are not the same the output node of the guard gate will float in a high impedance state, maintaining its last value until it is degraded by leakage or once again rewritten when A and B match once more.

SETs as wide as the temporal delay will be filtered away. The main drawback with guard gates is that the clock period needs to be extended to include the temporal delay, and thereby introduce penalties to the entire system.

![Figure 4.9: Block diagram and schematic of a guard gate [10].](image)

4.2.4 Temporal Filtering

Temporal filtering can be used to mitigate SETs. The principle is to create multiple versions of a signal, separate them from each other with delay elements and use a majority voter to select the correct output [10] [12].

In figure 4.10 a latch using temporal filtering has been achieved by temporal sampling. The signal arrive at the D-flip-flops at the same time but two of the flip-flops are clocked with delayed clocks and therefore the flip-flops will latch the signal at different times. As long as the SET is narrower than the delay, (time between the clocks), only one flip-flop will be able to latch the SET, allowing the majority voter to select the correct output. This design is, however, vulnerable to SETs in the clock distribution.

![Figure 4.10: A SET hardened latch using temporal filtering achieved through temporal sampling [10].](image)

Another latch using temporal filtering involves using a multiplexer, figure 4.11. This design follows the same principle as the previous, create delayed versions of the signal and majority vote the output. The benefit is that less hardware is used and it is insensitive to SETs in the clock distribution.
The main drawback with these approaches is that, as with the guard gate, the clock period need to be extended to include the temporal delay, and thereby introduce penalties to the entire system.

### 4.2.5 Multiple Drive

To mitigate SETs in the output node from a buffer, multiple buffers can be used figure 4.12. If a SET occurs in one buffer it will be subdued by the other buffers [39].

![Figure 4.12: Triple drive block diagram.](image)

### 4.2.6 Charge Dissipation

With each new technology scaling the drive currents of the transistors are reduced [40]. The charge deposited by incident particles are, however, constant. This causes the charge diffusion, 2.3, to take more time which in turn leads to more severe SEEs. To mitigate this, increasing the transistors drive current by making the wider is one option.

Charge dissipation was evaluated in [41] and while this, somewhat crude, method is easy to implement and gives a generally good result against many SEEs the circuit area and power consumption are greatly increased. These penalties may not be crucial to every design though, if area and power consumption are not a concern charge dissipation might be a good option.

In addition to increasing the size of the transistors adding extra capacitance to the node immediately after an up sized transistor increases the critical charge needed to upset the node. By increasing the size and capacitance proportionally the extra capacitance will not slow the circuit down [42].

### 4.2.7 Differential Charge Cancellation

In single ended analog circuits and digital circuits charge sharing is usually a problem that forces the designers to use countermeasures like interleaving devices, use extra spacing between devices and guard rings to avoid MBUs, multiple SETs and pulse broadening. In fully differential circuits charge sharing can instead be exploited to reduce the effects of ASETs.

By minimizing the distance between the drains of sister devices, figure 4.13, in the differential signal path, the likelihood that an incident particle strikes both sides of a differential pair and thereby cancelling some, or all, of the resulting transients can be maximized. Using common-centroid layouts to match devices where it is possible also beneficial since it enhances charge sharing [43].
Figure 4.13: The S/H amplifier is a commonly used differential switched-capacitor circuit that has several examples of differential sister transistors [43].

A concept of how differential transistor pairs should be placed to achieve DCC is shown in figure 4.14. In figure 4.15 the result of a two-photon-absorption laser experiment is shown, [41]. In the upper image charge collection for a single input-transistor of a differential amplifier is plotted, in the lower image charge collection is plotted for two sister transistors with adjacent drains.

Figure 4.14: Examples for baseline, common-centroid and DCC transistor layouts [44].

In [45], DCC with a common-centroid was tested and compared to a design without DCC. The result was a SET rejection improvement of at least 39 %. In [41] a design with DCC was compared to a design with
charge dissipation with mixed results. While charge dissipation was easy to implement and gave a good general protection against SETs it required significantly larger area (4x) and had higher power consumption (7x). The results from DCC was generally good, the impact on area and power consumption were minimal but the SET protection was dependent on the incident angle of incident particles. The resulting mitigation of SETs were up to 80% compared to an unhardened circuit. In their conclusion the authors emphasise the importance of choosing hardening technique with consideration of the specific environment and design.

4.3 System level

4.3.1 Triple modular redundancy

As described in 4.2.1, TMR can be applied on system level by triplicating the system that needs to be protected, i.e. memory, FPGA or microprocessor.

4.3.2 Scrubbing

Scrubbing is a technique used to prevent the accumulation of SEUs in memories, especially FPGA configuration memories. Scrubbing techniques are divided into two steps, the first being a scrubbing algorithm that decides if a scrub is to be done, the second is the reconfiguration to restore the correct memory content.

Scrubbing algorithms are divided into two main types, preventive (blind) or corrective. In a preventive scrubbing algorithm scrubbing is performed cyclically without checking if an upset has occurred or not. In a corrective scrubbing algorithm scrubbing is performed only when the algorithm has detected an upset. In figure 4.16 basic preventive and corrective scrubbing flowcharts can be seen.

![Figure 4.16: Basic flowcharts of preventive and corrective scrubbing algorithms.](image)

In order for a corrective scrubber to detect if a SEU has occurred either checksums, EDAC codes or comparison with a stored reference value can be used. Which one is to be used depends on performance and area requirements. Checksums and EDAC codes requires extra bits in the memory to be able to detect if an error has occurred while comparing values with a ‘golden memory’ requires more data to be read back and forth.

Depending on the mission, different levels of scrubbing frequency might be required at different times in different environments, i.e. a satellite passing through a particle belt close to a planet might need a higher scrubbing frequency since radiation levels are higher there than during other parts of the mission. Instead of having a constant scrubbing frequency designed after the worst scenario an adaptive scrubbing frequency can be used to reduce the power usage.

Depending on the application different reconfiguration techniques can also be used. Either the entire memory can be reconfigured in one step or only parts of it, i.e. complete or partial reconfiguration. Which one is to be used is decided by the the type of error, the environment and if the memory is in a part of a system that is mission critical and therefore cannot be interrupted.

In environments with low radiation levels and for parts of the system that can be interrupted, complete reconfiguration can be used. For some upsets, like a SEFI in an FPGA, the only way to restore the system is a complete
reconfiguration. If the system cannot be allowed to be interrupted if the radiation levels in the environment are sufficiently high to make complete reconfiguration impractical, it simply needs to be done to often, partial reconfiguration can be used. When partial reconfiguration is used only parts of the memory is reconfigured at one time, allowing mission critical systems, like the altitude control of a satellite, to remain functional.

The design and placement of the scrubber can be done in different ways depending on performance, area and adaptability requirements. For external memories and for FPGAs an external scrubber, figure 4.17, can be used. Depending on the performance and adaptability an external scrubber can either be implemented in hardware, as an ASIC or radiation hard antifuse based FPGA or as software in a microprocessor dedicated as a scrubber, figure 4.18. The benefit of using a hardware scrubber is increased performance (i.e. scrubbing rates) while the benefit of a software scrubber is adaptability and the possibility for more complex scrubbing schemes. In FPGAs the scrubber can also be placed internally. This reduces the area and power consumption but makes the scrubber vulnerable to SEUs in the configuration memory, internal scrubbers are thus qualitatively less reliable than external scrubbers [29].

**Figure 4.17: Illustration of an external and an internal scrubber [29].**

**Figure 4.18: A microprocessor based external scrubber including the microprocessor memory [29].**

**Usage of reconfiguration to restore a system with permanently damaged transistors**

In FPGAs, reconfiguration can be used to restore functionality to a system with permanently damaged transistors/circuits. If a scrubbing scheme cannot correct a SEU or there is a piece of logic that consistently miscalculates despite reconfiguration, a transistor in the configuration memory or the logic itself might be permanently damaged. In this case the part, frame, of the configuration memory that contains the damaged transistor can be marked as forbidden and in a subsequent reconfiguration the functionality of that frame is moved to another frame. This naturally requires that there are unused frames available.

**4.3.3 Lockstep**

A lockstep scheme is an extended version of a duplication with comparison (DWC) redundancy technique. Duplication with comparison allows the system to detect an error but not to correct it. In a lockstep scheme two processors are run in parallel executing the same data. A block diagram showing DWC hardware redundancy can be seen in figure 4.19.

In a basic lockstep scheme the processors contexts, the information required to restore the processors to a specific state, are saved at certain checkpoints. When the processors reach a new consistency check their results are compared and if the results match, a new context is saved and calculations proceed, if the results differ a
rollback to the previous context is done and the calculations proceed from there again. The general procedure including rollback is explained in figure 4.20.

While the lockstep scheme is simple its complexity lies in its implementation and impact on performance [46]. Deciding when a consistency check is to be done and how often contexts are to be saved decides how much impact the lockstep scheme will have on performance, especially since every rollback means throwing results and restart from an earlier point. Depending on hardware and performance requirements the lockstep scheme can be implemented in either hardware, software or both.

To avoid the performance loss from throwing results when making a rollback a more complex lockahead scheme with roll-forward can be implemented. If it is possible to decide which of the processors that is faulty at a consistency check the context of the correct processor can be loaded into the faulty processor. This removes the time needed for context saving at checkpoints and the time needed for recalculation at a rollback. More complex hardware and software are however required in order to decide which processor is faulty.

4.3.4 Error detecting and correcting codes

Error detecting and correcting (EDAC) codes can be used to detect and correct upset bits in a memory. Two common applications where EDAC codes are used are when data is read from a memory and as a part of a scrubbing algorithm. Depending on the code used different amounts of errors can be detected and corrected. Two commonly used EDAC codes are:

**Hamming Code**

The Hamming code was invented by Richard Hamming in 1950 and it is capable of detecting and correcting one error when a hamming distance of three is used. Most commonly used in electronic systems is a Hamming code with a hamming distance of four which is capable of correcting one error and detecting two, SEC-DED [47].

**Reed-Solomon Code**

The Reed-Solomon (RS) codes were developed by Irving S. Reed and Gustave Solomon in 1960 and they
are capable of detecting and correcting multiple errors. By adding check symbols to the data, an RS code can detect any combination of up to \( t \) erroneous symbols and correct up to \( t/2 \) symbols [47].

In order to achieve higher error correction and more effective codes concatenated codes, i.e. combinations of Hamming and RS codes, can be used [48]. In concatenated codes different codes are used to complement each other, figure 4.21.

In order to achieve higher error correction and more effective codes concatenated codes, i.e. combinations of Hamming and RS codes, can be used [48]. In concatenated codes different codes are used to complement each other, figure 4.21.

Figure 4.21: Hamming and RS codes used to complement each other [48].

EDAC codes can be implemented in either hardware or software depending on performance and area requirements. Since software EDAC codes introduce a performance penalty if applied on every read from a memory hardware EDAC codes are preferable in these instances. Software EDAC codes might be the better choice in scrubbing schemes though [49].

How much area overhead is introduced when using an EDAC code naturally depends on how many extra bits are needed by the code. In general, compared to applying TMR to an entire memory, with an overhead of more than 200 \%, applying a Hamming code introduces less area overhead.

### 4.3.5 Watchdog timer

Though not really a RHBD technique, a watchdog timer can be used to detect if a system malfunction has occurred. A watchdog timer is a counter that the system has to reset before it reaches a certain value. If the counter is not reset in time a fault is assumed to have happened and a signal for some corrective action is set. A simple watchdog timer consists of only one timer that allows one corrective action, usually a system reset, as shown in figure 4.22. If multiple corrective actions are to be used, a series of timers can be used as shown in figure 4.23.

Figure 4.22: A watchdog timer that is capable of resetting the protected system if it fails to reset the timer.

Figure 4.23: A watchdog timer system with three timers that is capable of trying two corrective actions before the protected system is reset.

In order to provide good fault coverage without having a large impact on system performance, the time allowed between one reset and the next has to be adapted to the application.
Chapter 5

Conclusion

This survey of radiation hardened electronics has explained the processes by which radiation affect electronics, both in principle and in commonly used devices, as well as general techniques used to harden electronics from these effects. The radiation induced effects have been divided into three different categories, displacement damage, total ionizing dose and single event effects. Depending on the device and technology used, some effects are more or less likely to occur. Displacement damage is mostly a concern in devices depending on minority carriers since it affects the energy levels in the semiconductor bandgap which in turn affects the recombination rates. The total ionizing dose affects devices by creating trapped charge in dielectrics which in turn changes the electric potential within different parts the device. Single event effects occur in devices where the functionality of the device is affected by a single particle, most often because the critical charge required to upset the device is generated by one particle.

The physical structure of a device is important as it decides its sensitivity to radiation. The substrate’s doping profile and the placement of metal layers and dielectrics decide which parasitic structures that are present within the device. The purity of the materials, especially the amount of imperfections along the surfaces between adjacent materials are important as they affect the susceptibility of defect buildup.

Traditionally, radiation tolerant manufacturing processes have existed alongside the commercial ones. In current technology nodes however, the cost of maintaining a specialized foundry with a small production volume is too high. This is why most radiation hardened electronics systems today are built from commercial foundries along with COTS products with relevant redundancy techniques. It is however more and more common that commercial foundries sell some radiation hardened transistors as long as they can be manufactured without adding additional processing steps. In general though, radiation hardening of electronics today is done with RHBD techniques. Most RHBD techniques rely on either redundancy or temporal filtering and therefore trades performance against radiation hardness.

In the end, the hardening technique used should reflect the specific requirements of the application environment. The most important part when designing a radiation hard system is the requirement specification, radiation testing is many times expensive and time consuming and it might not reflect the radiation response from the application environment. Since it is probable that it is also difficult to change any part of a system in a radiation environment, careful planning of both the development and system usage is crucial.
Bibliography


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